Digital PAL/NTSC Video Encoder with 10-Bit SSAF™ and Advanced Power Management

ADV7170/ADV7171[1]

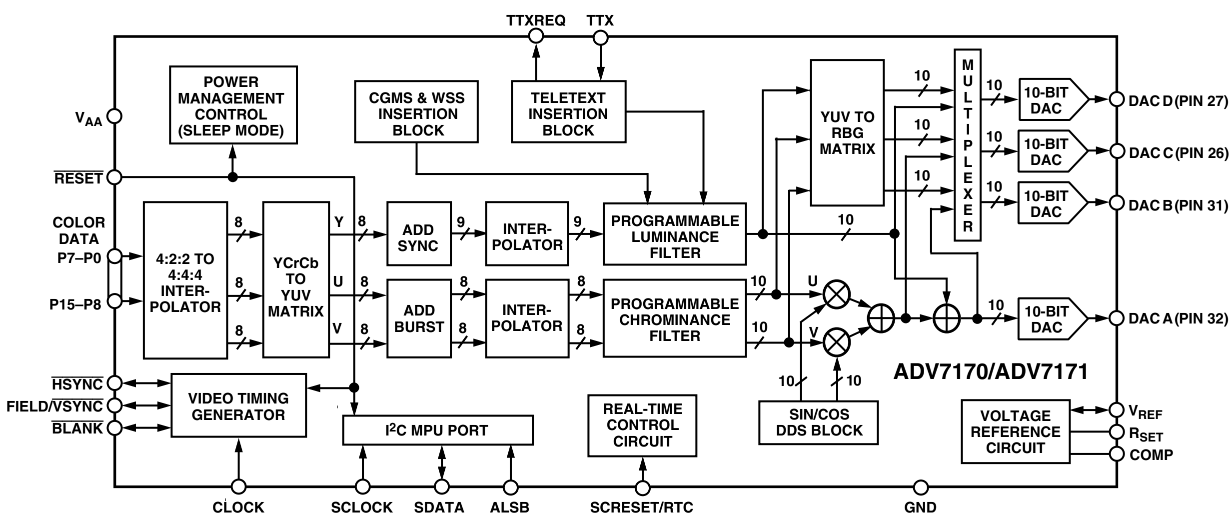
FEATURES

- ITU-R[2] BT601/656 YCrCb to PAL/NTSC Video Encoder
- High Quality 10-Bit Video DACs
- SSAF (Super Sub-Alias Filter)
- Advanced Power Management Features
- CGMS (Copy Generation Management System)
- WSS (Wide Screen Signalling)
- Simultaneous Y, U, V, C Output Format
- NTSC-M, PAL-M/N[3], PAL-B/D/G/H/I, PAL-60
- Single 27 MHz Clock Required (×2 Oversampling)
- 80 dB Video SNR
- 32-Bit Direct Digital Synthesizer for Color Subcarrier
- Multistandard Video Output Support:
  - Composite (CVBS)
  - Component S-Video (Y/C)
  - Component YUV and RGB
  - EuroSCART Output (RGB + CVBS/LUMA)
  - Component YUV + CHROMA
- Video Input Data Port Supports:
  - CCIR-656 4:2:2 8-Bit Parallel Input Format
  - 4:2:2 16-Bit Parallel Input Format
- Programmable Simultaneous Composite and S-Video or RGB (SCART)/YUV Video Outputs
- Programmable Luma Filters (Low-Pass [PAL/NTSC]) Notch, Extended (SSAF, CIF, and QCIF)
- Programmable Chroma Filters (Low-Pass [0.65 MHz, 1.0 MHz, 1.2 MHz and 2.0 MHz], CIF and QCIF)
- Programmable VBI (Vertical Blanking Interval)
- Programmable Subcarrier Frequency and Phase
- Programmable LUMA Delay
- Individual ON/OFF Control of Each DAC
- CCIR and Square Pixel Operation
- Integrated Subcarrier Locking to External Video Source
- Color Signal Control/Burst Signal Control
- Interlaced/Noninterlaced Operation
- Complete On-Chip Video Timing Generator
- Programmable Multimode Master/Slave Operation
- Macrovision AntiTaping Rev 7.1 (ADV7170 Only)[4]
- Closed Captioning Support
- Teletext Insertion Port (PAL-WST)
- On-Board Color Bar Generation
- On-Board Voltage Reference
- 2-Wire Serial MPU Interface (I^{2}C®-Compatible and Fast I^{2}C)
- Single Supply 5 V or 3.3 V Operation
- Small 44-Lead MQFP/TQFP Packages

APPLICATIONS

High-Performance DVD Playback Systems, Portable Video Equipment Including Digital Still Cameras and Laptop PCs, Video Games, PC Video/Multimedia and Digital Satellite/Cable Systems (Set-Top Boxes/IRD)

FUNCTIONAL BLOCK DIAGRAM



NOTES

[1]Protected by U.S. Patent Numbers 5,343,196 and 5,442,355 and other intellectual property rights.

[2]ITU-R and CCIR are used interchangeably in this document (ITU-R has replaced CCIR recommendations).

[3]Throughout the document N is referenced to PAL- Combination -N.

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5 V SPECIFICATIONS (V_{AA} = 5 V ± 5%[1], V_{REF} = 1.235 V, R_{SET} = 150 Ω. All specifications T_{MIN} to T_{MAX}[2] unless otherwise noted.)

Parameter	Conditions[1]	Min	Typ	Max	Unit
STATIC PERFORMANCE					
Resolution (Each DAC)				10	Bits
Accuracy (Each DAC)					
Integral Nonlinearity	R_{SET} = 300 Ω		±0.6		LSB
Differential Nonlinearity	Guaranteed Monotonic			±1	LSB
DIGITAL INPUTS					
Input High Voltage, V_{INH}		2			V
Input Low Voltage, V_{INL}				0.8	V
Input Current, I_{IN}	V_{IN} = 0.4 V or 2.4 V			±1	μA
Input Capacitance, C_{IN}			10		pF
DIGITAL OUTPUTS					
Output High Voltage, V_{OH}	I_{SOURCE} = 400 μA	2.4			V
Output Low Voltage, V_{OL}	I_{SINK} = 3.2 mA			0.4	V
Three-State Leakage Current				10	μA
Three-State Output Capacitance			10		pF
ANALOG OUTPUTS					
Output Current[3]	R_{SET} = 150 Ω, R_L = 37.5 Ω	33	34.7	37	mA
Output Current[4]	R_{SET} = 1041 Ω, R_L = 262.5 Ω		5		mA
DAC-to-DAC Matching			1.5		%
Output Compliance, V_{OC}		0		+1.4	V
Output Impedance, R_{OUT}			30		kΩ
Output Capacitance, C_{OUT}	I_{OUT} = 0 mA			30	pF
VOLTAGE REFERENCE					
Reference Range, V_{REF}	$I_{VREFOUT}$ = 20 μA	1.142	1.235	1.327	V
POWER REQUIREMENTS[5]					
V_{AA}		4.75	5.0	5.25	V
Normal Power Mode					
I_{DAC} (max)[6]	R_{SET} = 150 Ω, R_L = 37.5 Ω		150	155	mA
I_{DAC} (min)[6]	R_{SET} = 1041 Ω, R_L = 262.5 Ω		20		mA
I_{CCT}[7]			75	90	mA
Low Power Mode					
I_{DAC} (max)[6]			80		mA
I_{DAC} (min)[6]			20		mA
I_{CCT}[7]			75	90	mA
Sleep Mode					
I_{DAC}[8]			0.1		μA
I_{CCT}[9]			0.001		μA
Power Supply Rejection Ratio	COMP = 0.1 μF		0.01	0.5	%/%

NOTES

[1]The max/min specifications are guaranteed over this range. The max/min values are typical over 4.75 V to 5.25 V.

[2]Temperature range T_{MIN} to T_{MAX}: 0°C to 70°C.

[3]Full drive into 37.5 Ω doubly terminated load.

[4]Minimum drive current (used with buffered/scaled output load).

[5]Power measurements are taken with Clock Frequency = 27 MHz. Max T_J = 110°C.

[6]I_{DAC} is the total current (min corresponds to 5 mA output per DAC, max corresponds to 37 mA output per DAC) to drive all four DACs. Turning off individual DACs reduces I_{DAC} correspondingly.

[7]I_{CCT} (Circuit Current) is the continuous current required to drive the device.

[8]Total DAC current in Sleep Mode.

[9]Total continuous current during Sleep Mode.

Specifications subject to change without notice.

3.3 V SPECIFICATIONS (V_{AA} = 3.0 V – 3.6 V[1], V_{REF} = 1.235 V, R_{SET} = 150 Ω. All specifications T_{MIN} to T_{MAX}[2] unless otherwise noted.)

Parameter	Conditions[1]	Min	Typ	Max	Unit
STATIC PERFORMANCE[3]					
Resolution (Each DAC)				10	Bits
Accuracy (Each DAC)					
Integral Nonlinearity	R_{SET} = 300 Ω		±0.6		LSB
Differential Nonlinearity	Guaranteed Monotonic			±1	LSB
DIGITAL INPUTS[3]					
Input High Voltage, V_{INH}		2			V
Input Low Voltage, V_{INL}				0.8	V
Input Current, I_{IN}[3, 4]	V_{IN} = 0.4 V or 2.4 V			±1	µA
Input Capacitance, C_{IN}			10		pF
DIGITAL OUTPUTS[3]					
Output High Voltage, V_{OH}	I_{SOURCE} = 400 µA	2.4			V
Output Low Voltage, V_{OL}	I_{SINK} = 3.2 mA			0.4	V
Three-State Leakage Current				10	µA
Three-State Output Capacitance			10		pF
ANALOG OUTPUTS[3]					
Output Current[4, 5]	R_{SET} = 150 Ω, R_L = 37.5 Ω	33	34.7	37	mA
Output Current[6]	R_{SET} = 1041 Ω, R_L = 262.5 Ω		5		mA
DAC-to-DAC Matching			2.0		%
Output Compliance, V_{OC}		0		1.4	V
Output Impedance, R_{OUT}			30		kΩ
Output Capacitance, C_{OUT}	I_{OUT} = 0 mA			30	pF
POWER REQUIREMENTS[3, 7]					
V_{AA}		3.0	3.3	3.6	V
Normal Power Mode					
I_{DAC} (max)[8]	R_{SET} = 150 Ω, R_L = 37.5 Ω		150	155	mA
I_{DAC} (min)[8]	R_{SET} = 1041 Ω, R_L = 262.5 Ω		20		mA
I_{CCT}[9]			35		mA
Low Power Mode					
I_{DAC} (max)[8]			80		mA
I_{DAC} (min)[8]			20		mA
I_{CCT}[9]			35		mA
Sleep Mode					
I_{DAC}[10]			0.1		µA
I_{CCT}[11]			0.001		µA
Power Supply Rejection Ratio	COMP = 0.1 µF		0.01	0.5	%/%

NOTES

[1]The max/min specifications are guaranteed over this range. The max/min values are typical over 3.0 V to 3.6 V.

[2]Temperature range T_{MIN} to T_{MAX}: 0°C to 70°C.

[3]Guaranteed by characterization.

[4]Full drive into 37.5 Ω load.

[5]DACs can output 35 mA typically at 3.3 V (R_{SET} = 150 Ω and R_L = 37.5 Ω), optimum performance obtained at 18 mA DAC current (R_{SET} = 300 Ω and R_L = 75 Ω).

[6]Minimum drive current (used with buffered/scaled output load).

[7]Power measurements are taken with Clock Frequency = 27 MHz. Max T_J = 110°C.

[8]I_{DAC} is the total current (min corresponds to 5 mA output per DAC, max corresponds to 38 mA output per DAC) to drive all four DACs. Turning off individual DACs reduces I_{DAC} correspondingly.

[9]I_{CCT} (Circuit Current) is the continuous current required to drive the device.

[10]Total DAC current in Sleep Mode.

[11]Total continuous current during Sleep Mode.

Specifications subject to change without notice.

ADV7170/ADV7171–SPECIFICATIONS

5 V DYNAMIC SPECIFICATIONS

(V_{AA} = 5 V ± 5%[1], V_{REF} = 1.235 V, R_{SET} = 150 Ω. All specifications T_{MIN} to T_{MAX}[2] unless otherwise noted.)

Parameter	Conditions[1]	Min	Typ	Max	Unit
Differential Gain[3, 4]	Normal Power Mode		0.3	0.7	%
Differential Phase[3, 4]	Normal Power Mode		0.4	0.7	Degrees
Differential Gain[3, 4]	Lower Power Mode		1.0	2.0	%
Differential Phase[3, 4]	Lower Power Mode		1.0	2.0	Degrees
SNR[3, 4] (Pedestal)	RMS		80		dB rms
SNR[3, 4] (Pedestal)	Peak Periodic		70		dB p-p
SNR[3, 4] (Ramp)	RMS		60		dB rms
SNR[3, 4] (Ramp)	Peak Periodic		58		dB p-p
Hue Accuracy[3, 4]			0.7	1.2	Degrees
Color Saturation Accuracy[3, 4]			0.9	1.4	%
Chroma Nonlinear Gain[3, 4]	Referenced to 40 IRE		0.6		±%
Chroma Nonlinear Phase[3, 4]			0.3	0.5	±Degrees
Chroma/Luma Intermod[3, 4]			0.2	0.4	±%
Chroma/Luma Gain Inequality[3, 4]			1.0	1.4	±%
Chroma/Luma Delay Inequality[3, 4]			0.5	2.0	ns
Luminance Nonlinearity[3, 4]			0.8	1.4	±%
Chroma AM Noise[3, 4]		82	85		dB
Chroma PM Noise[3, 4]		79	81		dB

NOTES

[1]The max/min specifications are guaranteed over this range. The max/min values are typical over 4.75 V to 5.25 V.

[2]Temperature range T_{MIN} to T_{MAX}: 0°C to 70°C.

[3]Guaranteed by characterization.

[4]The low pass filter only and guaranteed by design.

Specifications subject to change without notice.

3.3 V DYNAMIC SPECIFICATIONS

(V_{AA} = 3.0 V – 3.6 V[1], V_{REF} = 1.235 V, R_{SET} = 150 Ω. All specifications T_{MIN} to T_{MAX}[2] unless otherwise noted.)

Parameter	Conditions[1]	Min	Typ	Max	Unit
Differential Gain[3]	Normal Power Mode		1.0		%
Differential Phase[3]	Normal Power Mode		0.5		Degrees
Differential Gain[3]	Lower Power Mode		0.6		%
Differential Phase[3]	Lower Power Mode		0.5		Degrees
SNR[3] (Pedestal)	RMS		78		dB rms
SNR[3] (Pedestal)	Peak Periodic		70		dB p-p
SNR[3] (Ramp)	RMS		60		dB rms
SNR[3] (Ramp)	Peak Periodic		58		dB p-p
Hue Accuracy[3]			1.0		Degrees
Color Saturation Accuracy[3]			1.0		%
Luminance Nonlinearity[3, 4]			1.4		±%
Chroma AM Noise[3, 4]			80		dB
Chroma PM Noise[3, 4]			79		dB
Chroma Nonlinear Gain[3, 4]	Referenced to 40 IRE		0.6		±%
Chroma Nonlinear Phase[3, 4]			0.3	0.5	±Degrees
Chroma/Luma Intermod[3, 4]			0.2	0.4	±%

NOTES

[1]The max/min specifications are guaranteed over this range. The max/min values are typical over 4.75 V to 5.25 V.

[2]Temperature range T_{MIN} to T_{MAX}: 0°C to 70°C.

[3]Guaranteed by characterization.

[4]These specifications are for the low-pass filter only and guaranteed by design. For other internal filters, see Figure 4.

Specifications subject to change without notice.

5 V TIMING SPECIFICATIONS (V_{AA} = 4.75 V – 5.25 V[1], V_{REF} = 1.235 V, R_{SET} = 150 Ω. All specifications T_{MIN} to T_{MAX}[2] unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Unit
MPU PORT[3, 4]					
SCLOCK Frequency		0		400	kHz
SCLOCK High Pulsewidth, t_1		0.6			μs
SCLOCK Low Pulsewidth, t_2		1.3			μs
Hold Time (Start Condition), t_3	After This Period the First Clock Is Generated	0.6			μs
Setup Time (Start Condition), t_4	Relevant for Repeated Start Condition	0.6			μs
Data Setup Time, t_5		100			ns
SDATA, SCLOCK Rise Time, t_6				300	ns
SDATA, SCLOCK Fall Time, t_7				300	ns
Setup Time (Stop Condition), t_8		0.6			μs
ANALOG OUTPUTS[3, 5]					
Analog Output Delay			7		ns
DAC Analog Output Skew			0		ns
CLOCK CONTROL AND PIXEL PORT[5, 6]					
f_{CLOCK}			27		MHz
Clock High Time, t_9		8			ns
Clock Low Time, t_{10}		8			ns
Data Setup Time, t_{11}		3.5			ns
Data Hold Time, t_{12}		4			ns
Control Setup Time, t_{11}		4			ns
Control Hold Time, t_{12}		3			ns
Digital Output Access Time, t_{13}			11	16	ns
Digital Output Hold Time, t_{14}[4]			8		ns
Pipeline Delay, t_{15}[4]			48		Clock Cycles
TELETEXT[3, 4, 7]					
Digital Output Access Time, t_{16}			20		ns
Data Setup Time, t_{17}			2		ns
Data Hold Time, t_{18}			6		ns
RESET CONTROL[3, 4]					
$\overline{\text{RESET}}$ Low Time		6			ns

NOTES

[1]The max/min specifications are guaranteed over this range. The max/min values are typical over 4.75 V to 5.25 V range.

[2]Temperature range T_{MIN} to T_{MAX}: 0°C to 70°C.

[3]TTL input values are 0 to 3 volts, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF.

[4]Guaranteed by characterization.

[5]Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full-scale transition.

[6]Pixel Port consists of the following:

Pixel Inputs:	P15–P0
Pixel Controls:	$\overline{\text{HSYNC}}$, FIELD/$\overline{\text{VSYNC}}$, $\overline{\text{BLANK}}$
Clock Input:	CLOCK

[7]Teletext Port consists of the following:

Teletext Output:	TTXREQ
Teletext Input:	TTX

Specifications subject to change without notice.

3.3 V TIMING SPECIFICATIONS

(V_{AA} = 3.0 V – 3.6 V[1], V_{REF} = 1.235 V, R_{SET} = 150 Ω. All specifications T_{MIN} to T_{MAX}[2] unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Unit
MPU PORT[3, 4]					
SCLOCK Frequency		0		400	kHz
SCLOCK High Pulsewidth, t_1		0.6			μs
SCLOCK Low Pulsewidth, t_2		1.3			μs
Hold Time (Start Condition), t_3	After This Period the First Clock Is Generated	0.6			μs
Setup Time (Start Condition), t_4	Relevant for Repeated Start Condition	0.6			μs
Data Setup Time, t_5		100			ns
SDATA, SCLOCK Rise Time, t_6				300	ns
SDATA, SCLOCK Fall Time, t_7				300	ns
Setup Time (Stop Condition), t_8		0.6			μs
ANALOG OUTPUTS[3, 5]					
Analog Output Delay			7		ns
DAC Analog Output Skew			0		ns
CLOCK CONTROL AND PIXEL PORT[4, 5, 6]					
f_{CLOCK}			27		MHz
Clock High Time, t_9		8			ns
Clock Low Time, t_{10}		8			ns
Data Setup Time, t_{11}		3.5			ns
Data Hold Time, t_{12}		4			ns
Control Setup Time, t_{11}		4			ns
Control Hold Time, t_{12}		3			ns
Digital Output Access Time, t_{13}			12		ns
Digital Output Hold Time, t_{14}			8		ns
Pipeline Delay, t_{15}			48		Clock Cycles
TELETEXT[3, 4, 7]					
Digital Output Access Time, t_{16}			23		ns
Data Setup Time, t_{17}			2		ns
Data Hold Time, t_{18}			6		ns
RESET CONTROL[3, 4]					
$\overline{\text{RESET}}$ Low Time		6			ns

NOTES

[1]The max/min specifications are guaranteed over this range. The max/min values are typical over 3.0 V to 3.6 V range.

[2]Temperature range T_{MIN} to T_{MAX}: 0°C to 70°C.

[3]TTL input values are 0 to 3 volts, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF.

[4]Guaranteed by characterization.

[5]Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full-scale transition.

[6]Pixel Port consists of the following:

Pixel Inputs:	P15–P0
Pixel Controls:	$\overline{\text{HSYNC}}$, FIELD/$\overline{\text{VSYNC}}$, $\overline{\text{BLANK}}$
Clock Input:	CLOCK

[7]Teletext Port consists of the following:

Teletext Output:	TTXREQ
Teletext Input:	TTX

Specifications subject to change without notice.

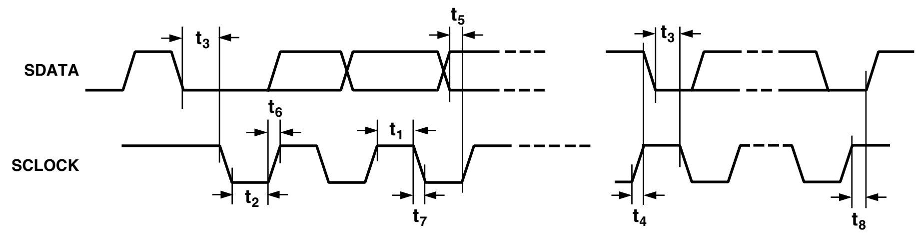


Figure 1. MPU Port Timing Diagram

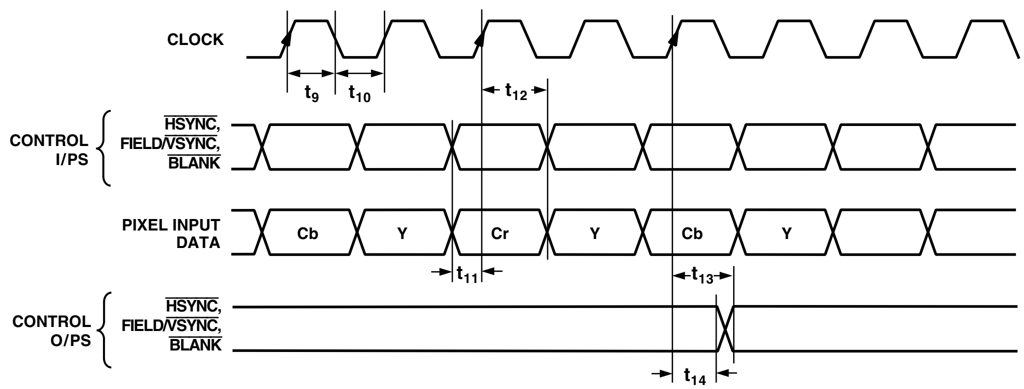


Figure 2. Pixel and Control Data Timing Diagram

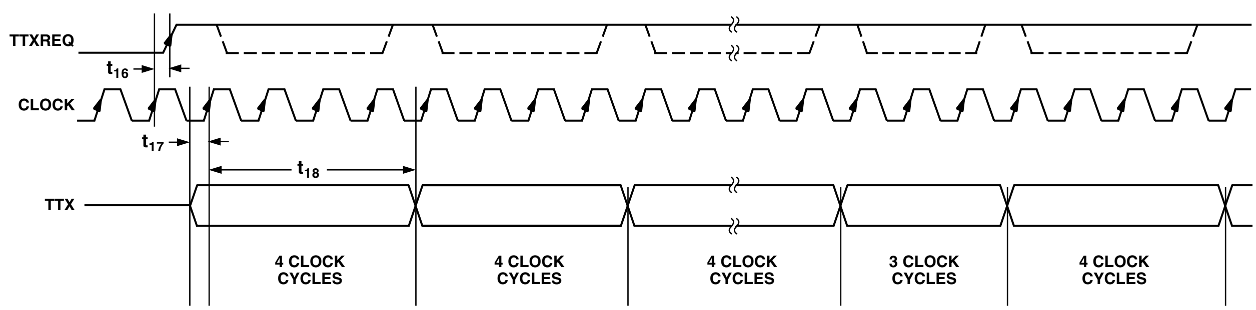


Figure 3. Teletext Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1]

V_{AA} to GND . . . . 7 V
Voltage on Any Digital Input Pin . GND – 0.5 V to V_{AA} + 0.5 V
Storage Temperature (T_S) . . . . –65°C to +150°C
Junction Temperature (T_J) . . . . 150°C
Lead Temperature (Soldering, 10 sec) . . . . 260°C
Analog Outputs to GND[2] . . . . GND – 0.5 V to V_{AA}

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Analog output short circuit to any power supply or common can be of an indefinite duration.

PACKAGE THERMAL PERFORMANCE

The 44-MQFP package used for this device takes advantage of an ADI patented thermal coastline lead frame construction. This maximizes heat transfer into the leads and reduces the package thermal resistance.

For the MQFP package the junction-to-ambient (θ_{JA}) thermal resistance in still air on a four-layer PCB is 35.5°C/W. The junction-to-case thermal resistance (θ_{JC}) is 13.75°C/W. For the TQFP package θ_{JA} in still air on a four-layer PCB is 53.2°C/W. θ_{JC} is 11.1°C/W.

Table I. Allowable Operating Conditions for KS and KSU Package Options

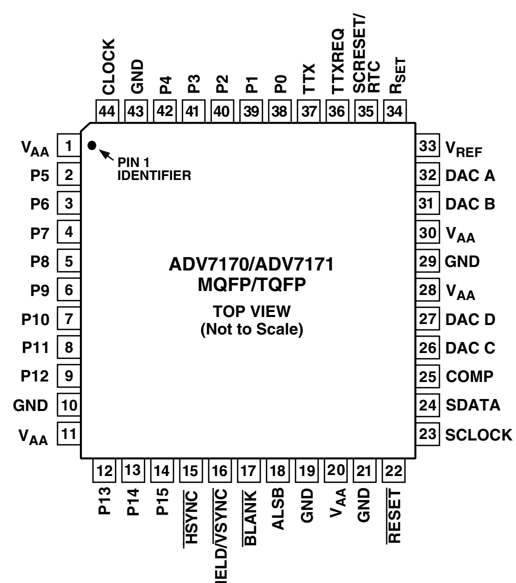
Conditions	KS 3 V	KS 5 V	KSU 3 V	KSU 5 V
4 DAC ON Double 75R[1]	Yes	Yes	Yes	No
4 DAC ON Low Power[2]	Yes	Yes	Yes	No
4 DAC ON Buffering[3]	Yes	Yes	Yes	Yes
3 DAC ON Double 75R	Yes	Yes	Yes	No
3 DAC ON Low Power	Yes	Yes	Yes	Yes
3 DAC ON Buffering	Yes	Yes	Yes	Yes
2 DAC ON Double 75R	Yes	Yes	Yes	Yes
2 DAC ON Low Power	Yes	Yes	Yes	Yes
4 DAC ON Buffering	Yes	Yes	Yes	Yes

NOTES
[1]DAC ON Double 75R refers to a condition where the DACs are terminated in a double 75R load and low power mode is disabled.
[2]DAC ON Low Power refers to a condition where the DACs are terminated in a double 75R load and low power mode is enabled.
[3]DAC ON Buffering refers to a condition where the DAC current is reduced to 5 mA and external buffers are used to drive the video load.

ORDERING GUIDE

Model	Temperature Range	Package Descriptions	Package Options
ADV7170KS	0°C to 70°C	Plastic Quad Flatpack	S-44
ADV7170KSU	0°C to 70°C	Thin Plastic Quad Flatpack	SU-44
ADV7171KS	0°C to 70°C	Plastic Quad Flatpack	S-44
ADV7171KSU	0°C to 70°C	Thin Plastic Quad Flatpack	SU-44

PIN CONFIGURATIONS



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADV7170/ADV7171 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTIONS

Mnemonic	Input/ Output	Function
P15–P0	I	8-Bit 4:2:2 Multiplexed YCrCb Pixel Port (P7–P0) or 16-Bit YCrCb Pixel Port (P15–P0). P0 represents the LSB.
CLOCK	I	TTL Clock Input. Requires a stable 27 MHz reference Clock for standard operation. Alternatively, a 24.5454 MHz (NTSC) or 29.5 MHz (PAL) can be used for square pixel operation.
$\overline{\text{HSYNC}}$	I/O	$\overline{\text{HSYNC}}$ (Modes 1 and 2) Control Signal. This pin may be configured to output (Master Mode) or accept (Slave Mode) Sync signals.
FIELD/$\overline{\text{VSYNC}}$	I/O	Dual Function FIELD (Mode 1) and $\overline{\text{VSYNC}}$ (Mode 2) Control Signal. This pin may be configured to output (Master Mode) or accept (Slave Mode) these control signals.
$\overline{\text{BLANK}}$	I/O	Video Blanking Control Signal. The pixel inputs are ignored when this is Logic Level "0." This signal is optional.
SCRESET/RTC	I	This pin can be configured as an input by setting MR22 and MR21 of Mode Register 2. It can be configured as a subcarrier reset pin, in which case a low-to-high transition on this pin will reset the subcarrier to Field 0. Alternatively, it may be configured as a Real-Time Control (RTC) input.
V_{REF}	I/O	Voltage Reference Input for DACs or Voltage Reference Output (1.235 V).
R_{SET}	I	A 150 Ω resistor connected from this pin to GND is used to control full-scale amplitudes of the video signals.
COMP	O	Compensation Pin. Connect a 0.1 µF Capacitor from COMP to V_{AA}. For Optimum Dynamic Performance in low power mode, the value of the COMP capacitor can be lowered to as low as 2.2 nF.
DAC A	O	PAL/NTSC Composite Video Output. Full-Scale Output is 180 IRE (1286 mV) for NTSC and 1300 mV for PAL.
DAC C	O	RED/S-Video C/V Analog Output
DAC D	O	GREEN/S-Video Y/Y Analog Output
DAC B	O	BLUE/Composite/U Analog Output
SCLOCK	I	MPU Port Serial Interface Clock Input
SDATA	I/O	MPU Port Serial Data Input/Output
ALSB	I	TTL Address Input. This signal set up the LSB of the MPU address.
$\overline{\text{RESET}}$	I	The input resets the on chip timing generator and sets the ADV7170/ADV7171 into default mode. This is NTSC operation, Timing Slave Mode 0, 8 Bit Operation, 2 × Composite and S Video out and DAC B powered ON and DAC D powered OFF.
TTX/V_{AA}	I	Teletext Data/Defaults to V_{AA} when Teletext not Selected (enables backward compatibility to ADV7175/ADV7176).
TTXREQ/GND	O	Teletext Data Request Signal/ Defaults to GND when Teletext not Selected (enables backward compatibility to ADV7175/ADV7176).
V_{AA}	P	Power Supply (3 V to 5 V)
GND	G	Ground Pin

GENERAL DESCRIPTION

The ADV7170/ADV7171 is an integrated digital video encoder that converts Digital CCIR-601 4:2:2 8 or 16-bit component video data into a standard analog baseband television signal compatible with worldwide standards.

The on-board SSAF (Super Sub-Alias Filter) with extended luminance frequency response and sharp stopband attenuation, enables studio quality video playback on modern TVs, giving optimal horizontal line resolution.

An advanced power management circuit enables optimal control of power consumption in both normal operating modes and power-down or sleep modes.

The ADV7170/ADV7171 also supports both PAL and NTSC square pixel operation. The parts also incorporate WSS and CGMS-A data control generation.

The output video frames are synchronized with the incoming data timing reference codes. Optionally, the encoder accepts (and can generate) $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, and FIELD timing signals. These timing signals can be adjusted to change pulsewidth and position while the part is in the master mode. The encoder requires a single two times pixel rate (27 MHz) clock for standard operation. Alternatively, the encoder requires a 24.5454 MHz clock for NTSC or 29.5 MHz clock for PAL square pixel mode operation. All internal timing is generated on-chip.

A separate teletext port enables the user to directly input teletext data during the vertical blanking interval.

The ADV7170/ADV7171 modes are set up over a two-wire serial bidirectional port (I^2C-Compatible) with two slave addresses.

Functionally, the ADV7171 and ADV7170 are the same with the exception that the ADV7170 can output the Macrovision anticopy algorithm.

The ADV7170/ADV7171 is packaged in a 44-lead MQFP package and a 44-lead TQFP package.

DATA PATH DESCRIPTION

For PAL B, D, G, H, I, M, N, and NTSC M, N modes, YCrCb 4:2:2 data is input via the CCIR-656 Compatible Pixel Port at a 27 MHz data rate. The pixel data is demultiplexed to form three data paths. Y typically has a range of 16 to 235, Cr and Cb typically have a range of 128 ± 112; however, it is possible to input data from 1 to 254 on both Y, Cb and Cr. The ADV7170/ADV7171 supports PAL (B, D, G, H, I, M, N) and NTSC (with and without pedestal) standards. The appropriate SYNC, $\overline{\text{BLANK}}$ and Burst levels are added to the YCrCb data. Macrovision AntiTaping (ADV7170 only), closed-captioning and Teletext levels are also added to Y and the resultant data is interpolated to a rate of 27 MHz. The interpolated data is filtered and scaled by three digital FIR filters.

The U and V signals are modulated by the appropriate subcarrier sine/cosine phases and added together to make up the chrominance signal. The luma (Y) signal can be delayed 1–3 luma cycles (each cycle is 74 ns) with respect to the chroma signal. The luma and chroma signals are then added together to make up the composite video signal. All edges are slew rate limited.

The YCrCb data is also used to generate RGB data with appropriate SYNC and $\overline{\text{BLANK}}$ levels. The RGB data is in synchronization with the composite video output. Alternatively, analog YUV data can be generated instead of RGB.

The four l0-bit DACs can be used to output:

1. Composite Video + RGB Video.
2. Composite Video + YUV Video.
3. Two Composite Video Signals + LUMA and CHROMA (Y/C) Signals.

Alternatively, each DAC can be individually powered off if not required.

Video output levels are illustrated in Appendix 6.

INTERNAL FILTER RESPONSE

The Y filter supports several different frequency responses, including two low-pass responses, two notch responses, an extended (SSAF) response, a CIF response and a QCIF response. The UV filter supports several different frequency responses, including four low-pass responses, a CIF response and a QCIF response, these can be seen in the following Figures 4 to 18.

FILTER TYPE	FILTER SELECTION			PASSBAND RIPPLE (dB)	3 dB BANDWIDTH (MHz)	STOPBAND CUTOFF (MHz)	STOPBAND ATTENUATION (dB)
	MR04	MR03	MR02				
LOW PASS (NTSC)	0	0	0	0.091	4.157	7.37	–56
LOW PASS (PAL)	0	0	1	0.15	4.74	7.96	–64
NOTCH (NTSC)	0	1	0	0.015	6.54	8.3	–68
NOTCH (PAL)	0	1	1	0.095	6.24	8.0	–66
EXTENDED (SSAF)	1	0	0	0.051	6.217	8.0	–61
CIF	1	0	1	0.018	3.0	7.06	–61
QCIF	1	1	0	MONOTONIC	1.5	7.15	–50

Figure 4. Luminance Internal Filter Specifications

FILTER TYPE	FILTER SELECTION			PASSBAND RIPPLE (dB)	3 dB BANDWIDTH (MHz)	STOPBAND CUTOFF (MHz)	STOPBAND ATTENUATION (dB)
	MR07	MR06	MR05				
1.3 MHz LOW PASS	0	0	0	0.084	1.395	3.01	–45
0.65 MHz LOW PASS	0	0	1	MONOTONIC	0.65	3.64	–58.5
1.0 MHz LOW PASS	0	1	0	MONOTONIC	1.0	3.73	–49
2.0 MHz LOW PASS	0	1	1	0.0645	2.2	5.0	–40
RESERVED	1	0	0				
CIF	1	0	1	0.084	0.7	3.01	–45
QCIF	1	1	0	MONOTONIC	0.5	4.08	–50

Figure 5. Chrominance Internal Filter Specifications

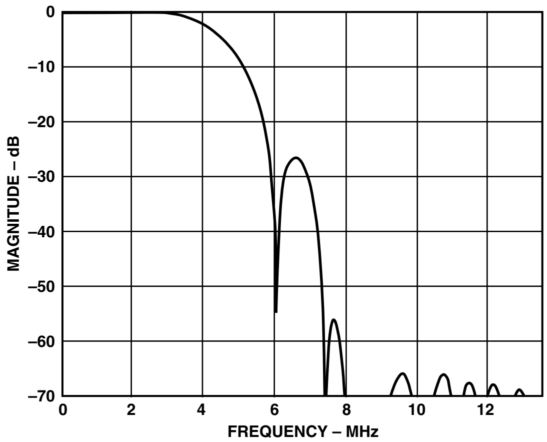


Figure 6. NTSC Low-Pass Luma Filter

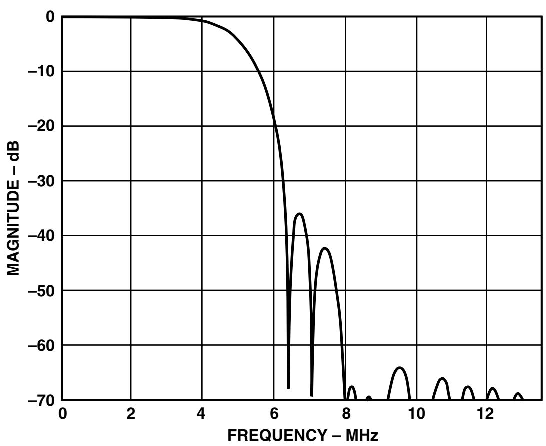


Figure 7. PAL Low-Pass Luma Filter

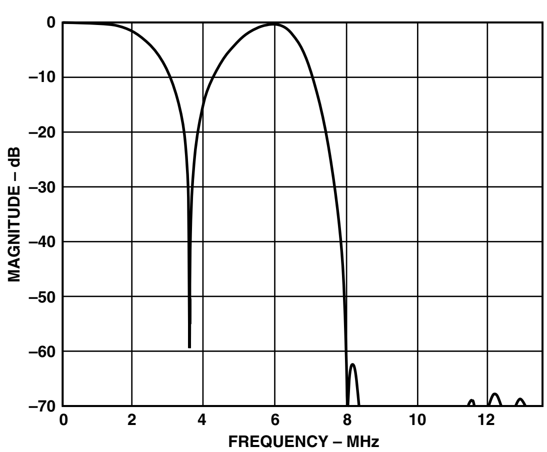


Figure 8. NTSC Notch Luma Filter

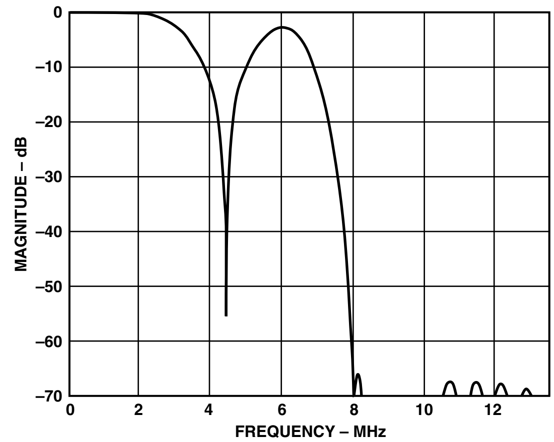


Figure 9. PAL Notch Luma Filter

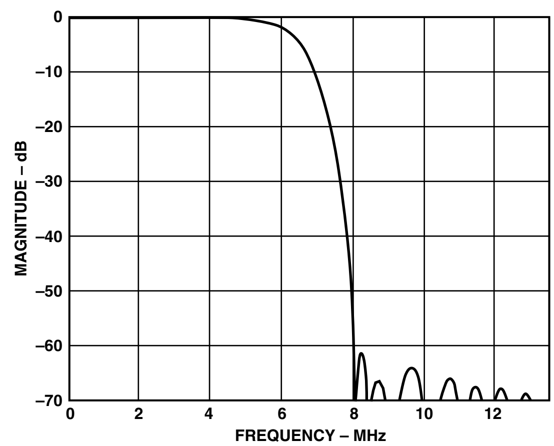


Figure 10. Extended Mode (SSAF) Luma Filter

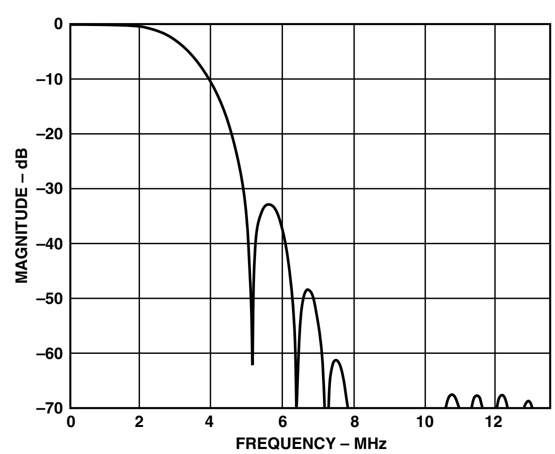


Figure 11. CIF Luma Filter

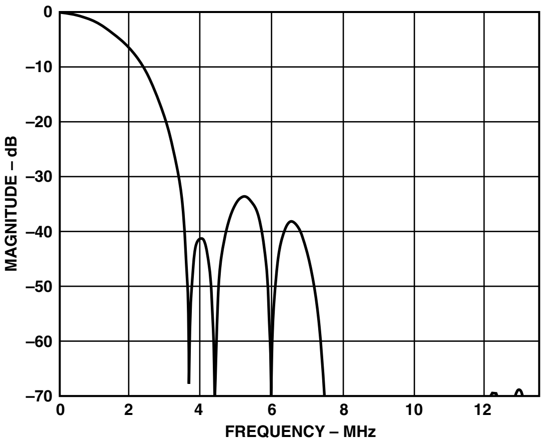


Figure 12. QCIF Luma Filter

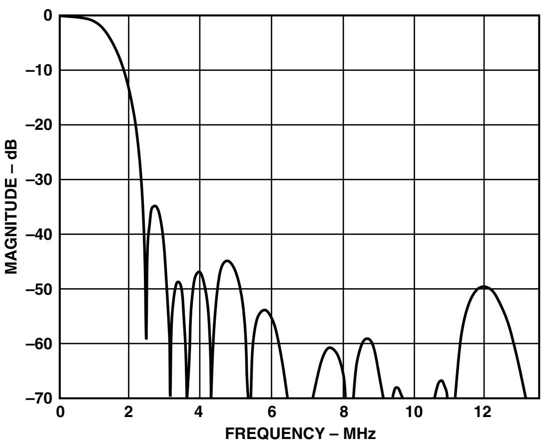


Figure 13. 1.3 MHz Low-Pass Chroma Filter

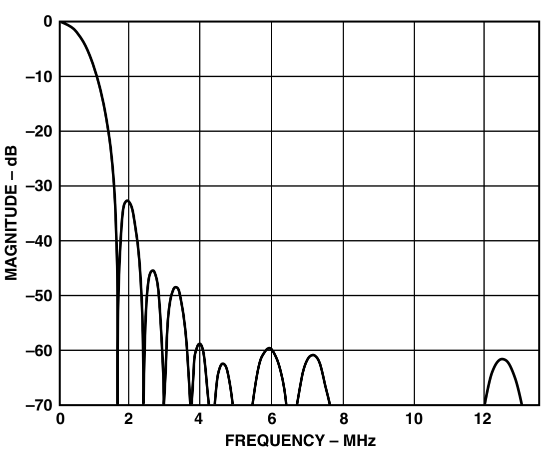


Figure 14. 0.65 MHz Low-Pass Chroma Filter

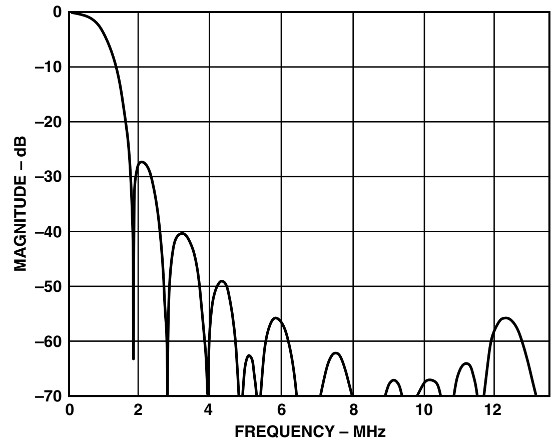


Figure 15. 1.0 MHz Low-Pass Chroma Filter

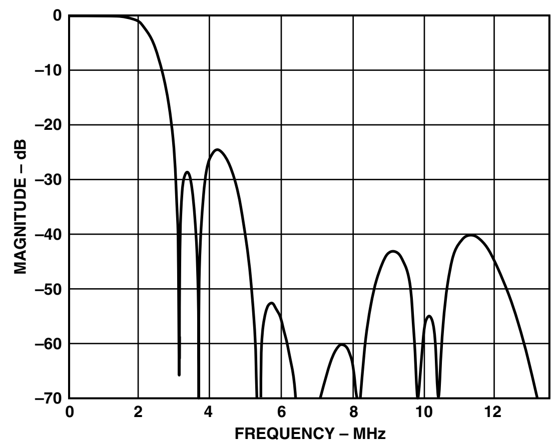


Figure 16. 2.0 MHz Low-Pass Chroma Filter

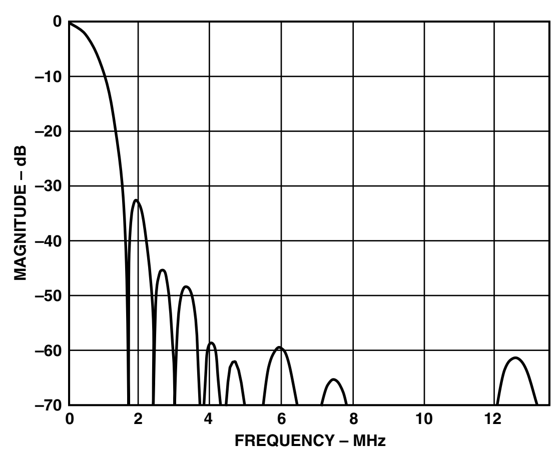


Figure 17. CIF Chroma Filter

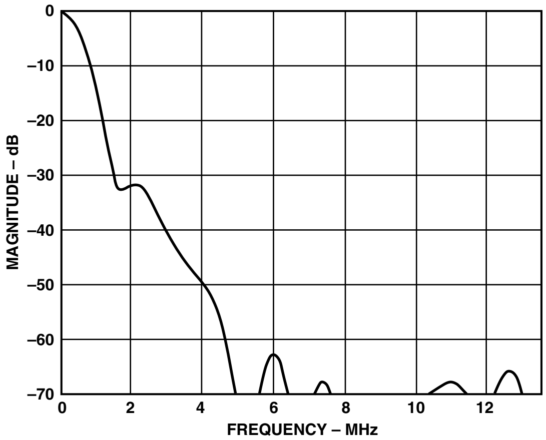


Figure 18. QCIF Chroma Filter

COLOR BAR GENERATION
The ADV7170/ADV7171 can be configured to generate 100/7.5/75/7.5 color bars for NTSC or 100/0/75/0 for PAL color bars. These are enabled by setting MR17 of Mode Register 1 to Logic "1."

SQUARE PIXEL MODE
The ADV7170/ADV7171 can be used to operate in square pixel mode. For NTSC operation, an input clock of 24.5454 MHz is required. Alternatively, for PAL operation, an input clock of 29.5 MHz is required. The internal timing logic adjusts accordingly for square pixel mode operation.

COLOR SIGNAL CONTROL
The color information can be switched on and off the video output using Bit MR24 of Mode Register 2.

BURST SIGNAL CONTROL
The burst information can be switched on and off the video output using Bit MR25 of Mode Register 2.

NTSC PEDESTAL CONTROL
The pedestal on both odd and even fields can be controlled on a line-by-line basis using the NTSC Pedestal Control Registers. This allows the pedestals to be controlled during the vertical blanking interval.

PIXEL TIMING DESCRIPTION
The ADV7170/ADV7171 can operate in either 8-bit or 16-bit YCrCb Mode.

8-Bit YCrCb Mode
This default mode accepts multiplexed YCrCb inputs through the P7-P0 pixel inputs. The inputs follow the sequence Cb0, Y0 Cr0, Y1 Cb1, Y2, etc. The Y, Cb and Cr data are input on a rising clock edge.

16-Bit YCrCb Mode
This mode accepts Y inputs through the P7–P0 pixel inputs and multiplexed CrCb inputs through the P15–P8 pixel inputs. The data is loaded on every second rising edge of CLOCK. The inputs follow the sequence Cb0, Y0 Cr0, Y1 Cb1, Y2, etc.

SUBCARRIER RESET
Together with the SCRESET/RTC pin, and bits MR22 and MR21 of Mode Register 2, the ADV7170/ADV7171 can be used in subcarrier reset mode. The subcarrier will reset to Field 0 at the start of the following field when a low-to-high transition occurs on this input pin.

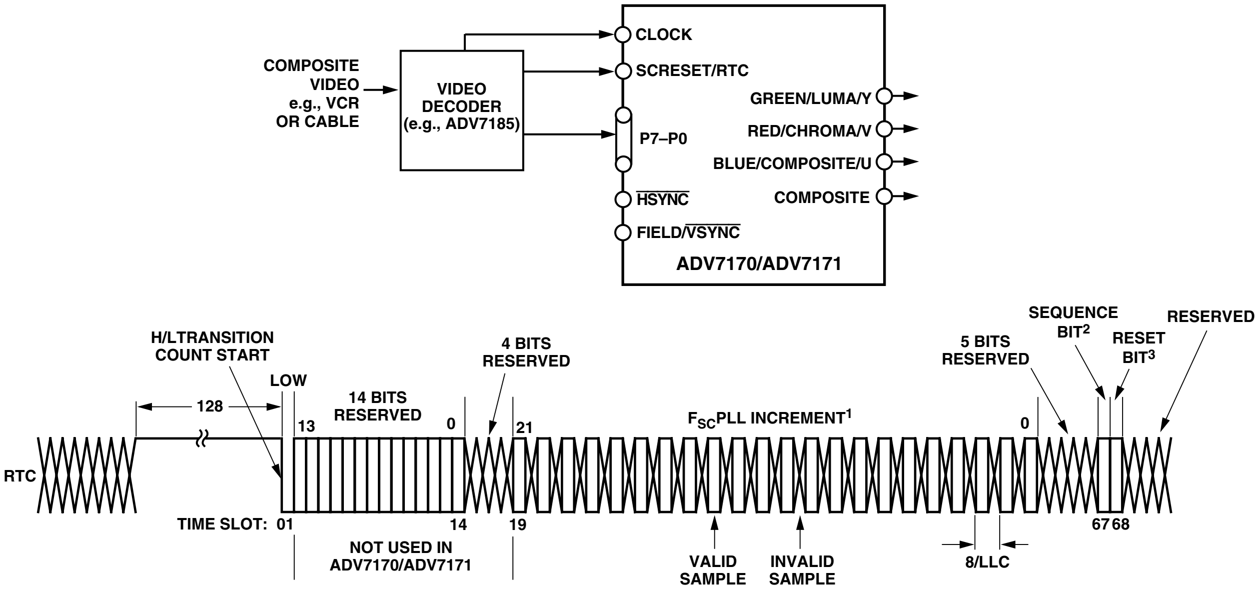
REAL-TIME CONTROL
Together with the SCRESET/RTC pin, and Bits MR22 and MR21 of Mode Register 2, the ADV7170/ADV7171 can be used to lock to an external video source. The real-time control mode allows the ADV7170/ADV7171 to automatically alter the subcarrier frequency to compensate for line length variation. When the part is connected to a device that outputs a digital datastream in the RTC format (such as a ADV7185 video decoder, see Figure 19), the part will automatically change to the compensated subcarrier frequency on a line-by-line basis. This digital datastream is 67 bits wide and the subcarrier is contained in Bits 0 to 21. Each bit is 2 clock cycles long. 00Hex should be written into all four subcarrier frequency registers when using this mode.

VIDEO TIMING DESCRIPTION
The ADV7170/ADV7171 is intended to interface to off-the-shelf MPEG1 and MPEG2 Decoders. Consequently, the ADV7170/ADV7171 accepts 4:2:2 YCrCb Pixel Data via a CCIR-656 pixel port and has several video timing modes of operation that allow it to be configured as either system master video timing generator or a slave to the system video timing generator. The ADV7170/ADV7171 generates all of the required horizontal and vertical timing periods and levels for the analog video outputs.

The ADV7170/ADV7171 calculates the width and placement of analog sync pulses, blanking levels and color burst envelopes. Color bursts are disabled on appropriate lines, and serration and equalization pulses are inserted where required.

In addition, the ADV7170/ADV7171 supports a PAL or NTSC square pixel operation in slave mode. The part requires an input pixel clock of 24.5454 MHz for NTSC and an input pixel clock of 29.5 MHz for PAL. The internal horizontal line counters place the various video waveform sections in the correct location for the new clock frequencies.

The ADV7170/ADV7171 has four distinct master and four distinct slave timing configurations. Timing Control is established with the bidirectional $\overline{\text{SYNC}}$, $\overline{\text{BLANK}}$, and FIELD/$\overline{\text{VSYNC}}$ pins. Timing Mode Register 1 can also be used to vary the timing pulsewidths and where they occur in relation to each other.



NOTES:

[1]F_{SC} PLL INCREMENT IS 22 BITS LONG, VALUE LOADED INTO ADV7170/ADV7171 FSC DDS REGISTER IS F_{SC} PLL INCREMENTS BITS 21:0 PLUS BITS 0:9 OF SUBCARRIER FREQUENCY REGISTERS. ALL ZEROS SHOULD BE WRITTEN TO THE SUBCARRIER FREQUENCY REGISTERS OF THE ADV7170/ADV7171.

[2]SEQUENCE BIT
PAL: 0 = LINE NORMAL, 1 = LINE INVERTED
NTSC: 0 = NO CHANGE

[3]RESET BIT
RESET ADV7170/ADV7171 DDS

Figure 19. RTC Timing and Connections

Vertical Blanking Data Insertion

It is possible to allow encoding of incoming YCbCr data on those lines of VBI that do not bear line sync or pre-/post-equalization pulses (see Figures 21 to 32). This mode of operation is called "Partial Blanking" and is selected by setting MR32 to 1. It allows the insertion of any VBI data (Opened VBI) into the encoded output waveform. This data is present in digitized incoming YCbCr data stream (e.g., WSS data, CGMS, VPS, etc.). Alternatively, the entire VBI may be blanked (no VBI data inserted) on these lines by setting MR32 to 0.

Mode 0 (CCIR-656): Slave Option

(Timing Register 0 TR0 = X X X X X 0 0 0)

The ADV7170/ADV7171 is controlled by the SAV (Start Active Video) and EAV (End Active Video) time codes in the pixel data. All timing information is transmitted using a 4-byte synchronization pattern. A synchronization pattern is sent immediately before and after each line during active picture and retrace. Mode 0 is illustrated in Figure 20. The $\overline{HSYNC}$, FIELD/$\overline{VSYNC}$, and $\overline{BLANK}$ (if not used) pins should be tied high during this mode.

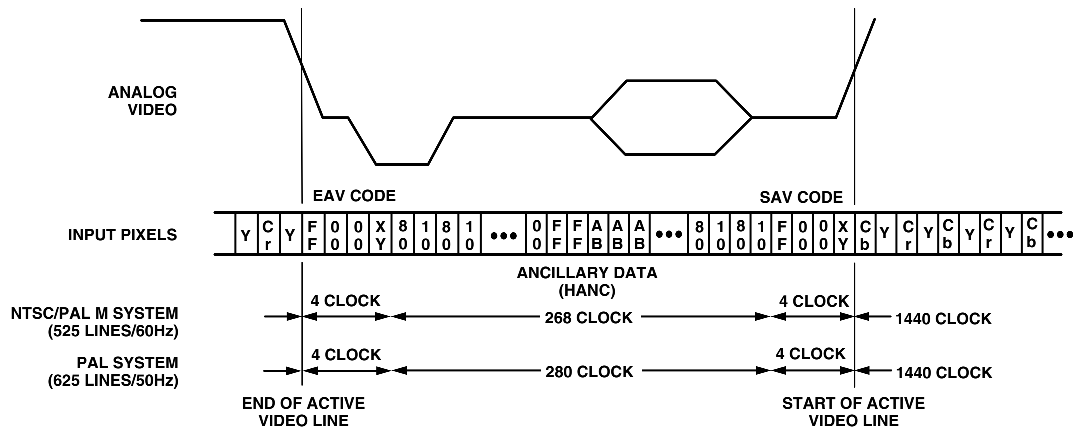


Figure 20. Timing Mode 0 (Slave Mode)

Mode 0 (CCIR-656): Master Option
(Timing Register 0 TR0 = X X X X X 0 0 1)

The ADV7170/ADV7171 generates H, V, and F signals required for the SAV (Start Active Video) and EAV (End Active Video) Time Codes in the CCIR656 standard. The H bit is output on the $\overline{\text{HSYNC}}$ pin, the V bit is output on the $\overline{\text{BLANK}}$ pin and the F bit is output on the FIELD/$\overline{\text{VSYNC}}$ pin. Mode 0 is illustrated in Figure 21 (NTSC) and Figure 22 (PAL). The H, V, and F transitions relative to the video waveform are illustrated in Figure 23.

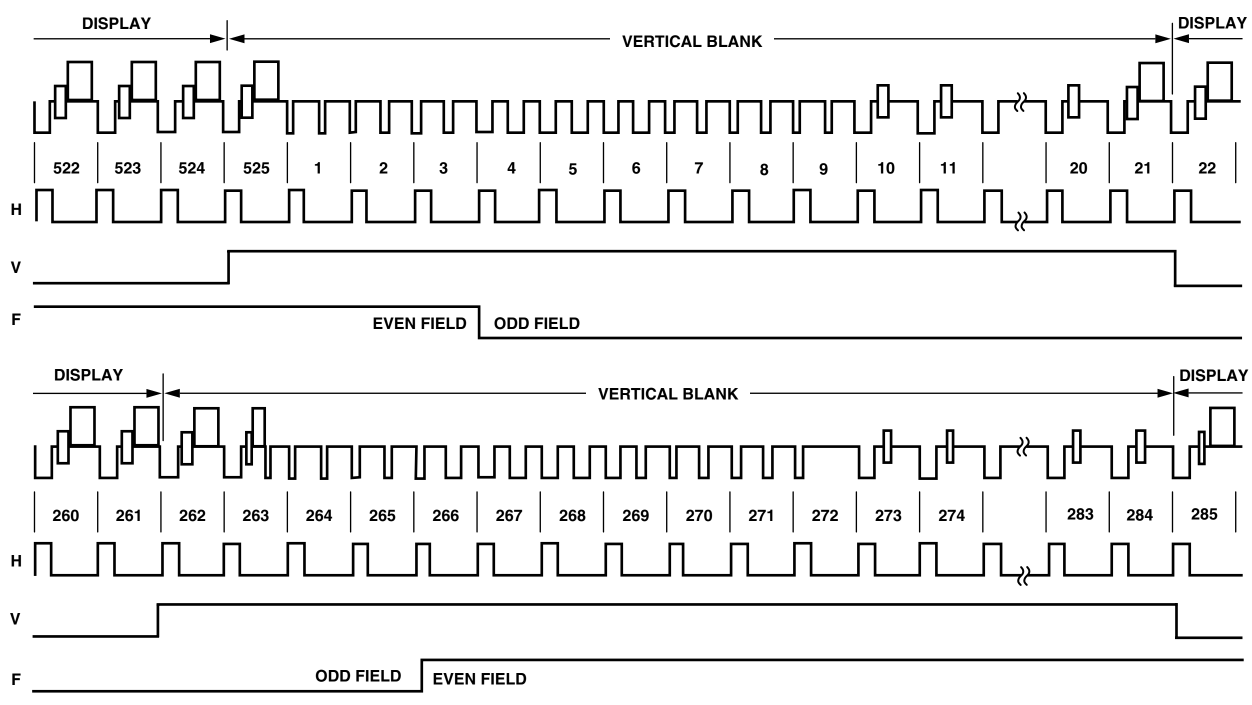


Figure 21. Timing Mode 0 (NTSC Master Mode)

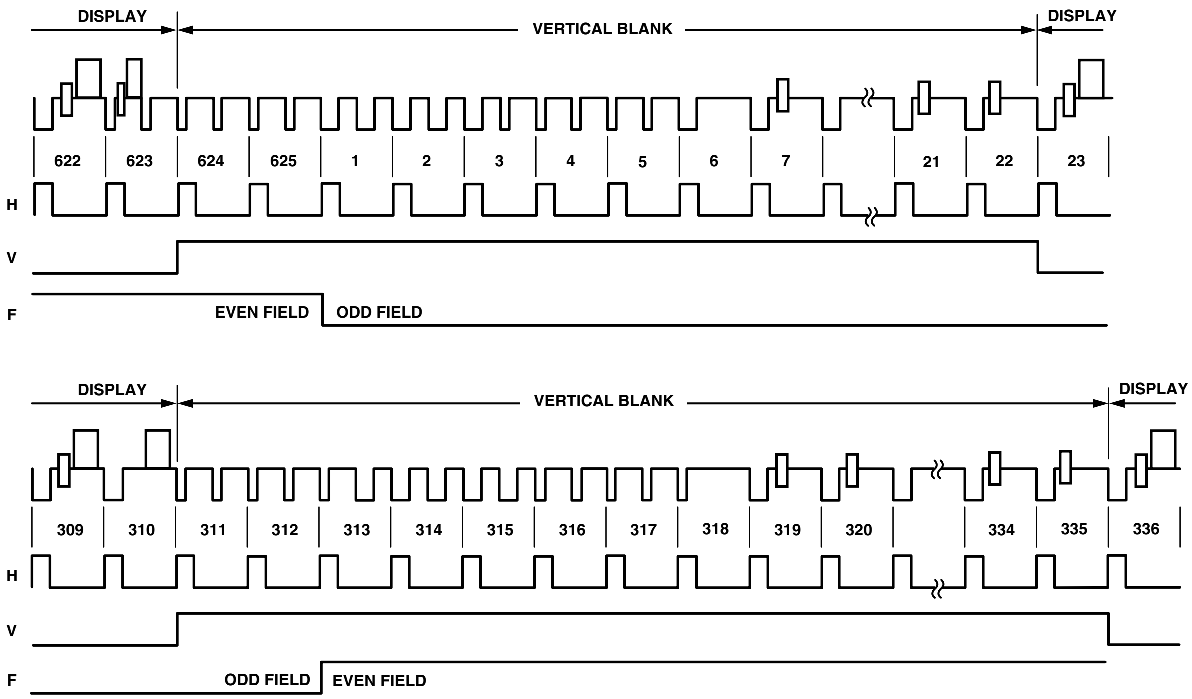


Figure 22. Timing Mode 0 (PAL Master Mode)

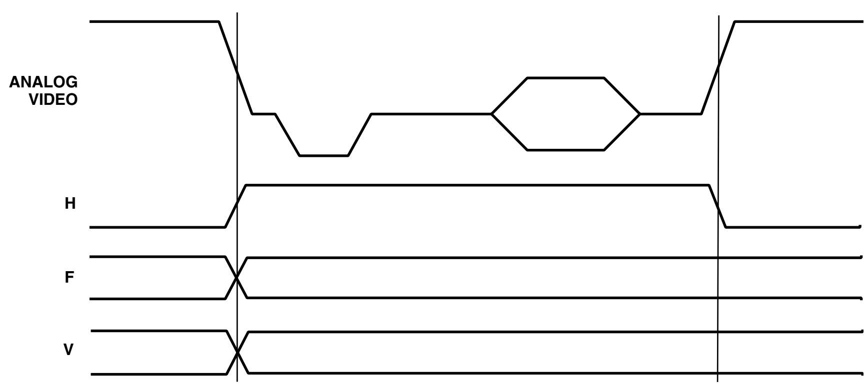


Figure 23. Timing Mode 0 Data Transitions (Master Mode)

Mode 1: Slave Option $\overline{\text{HSYNC}}$, $\overline{\text{BLANK}}$, FIELD
(Timing Register 0 TR0 = X X X X X 0 1 0)

In this mode the ADV7170/ADV7171 accepts horizontal SYNC and Odd/Even FIELD signals. A transition of the FIELD input when $\overline{\text{HSYNC}}$ is low indicates a new frame, i.e., vertical retrace. The $\overline{\text{BLANK}}$ signal is optional. When the $\overline{\text{BLANK}}$ input is disabled, the ADV7170/ADV7171 automatically blanks all normally blank lines as per CCIR-624. Mode 1 is illustrated in Figure 24 (NTSC) and Figure 25 (PAL).

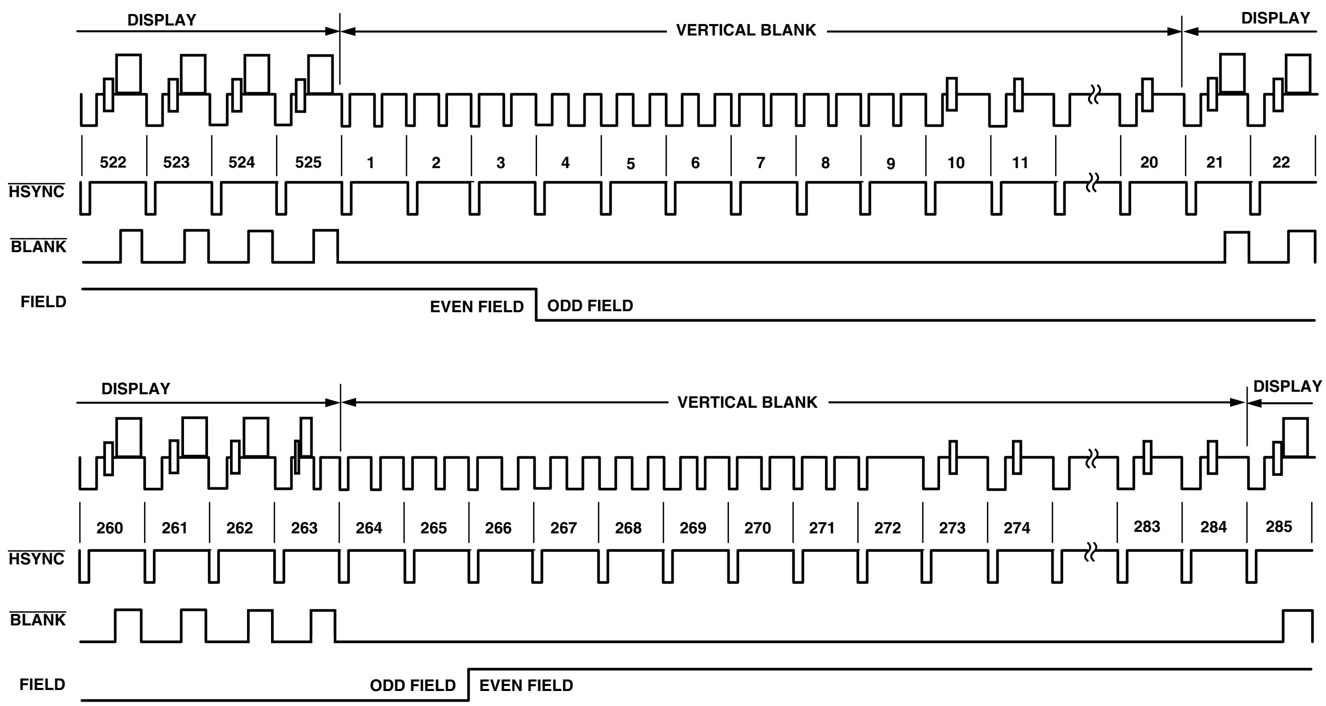


Figure 24. Timing Mode 1 (NTSC)

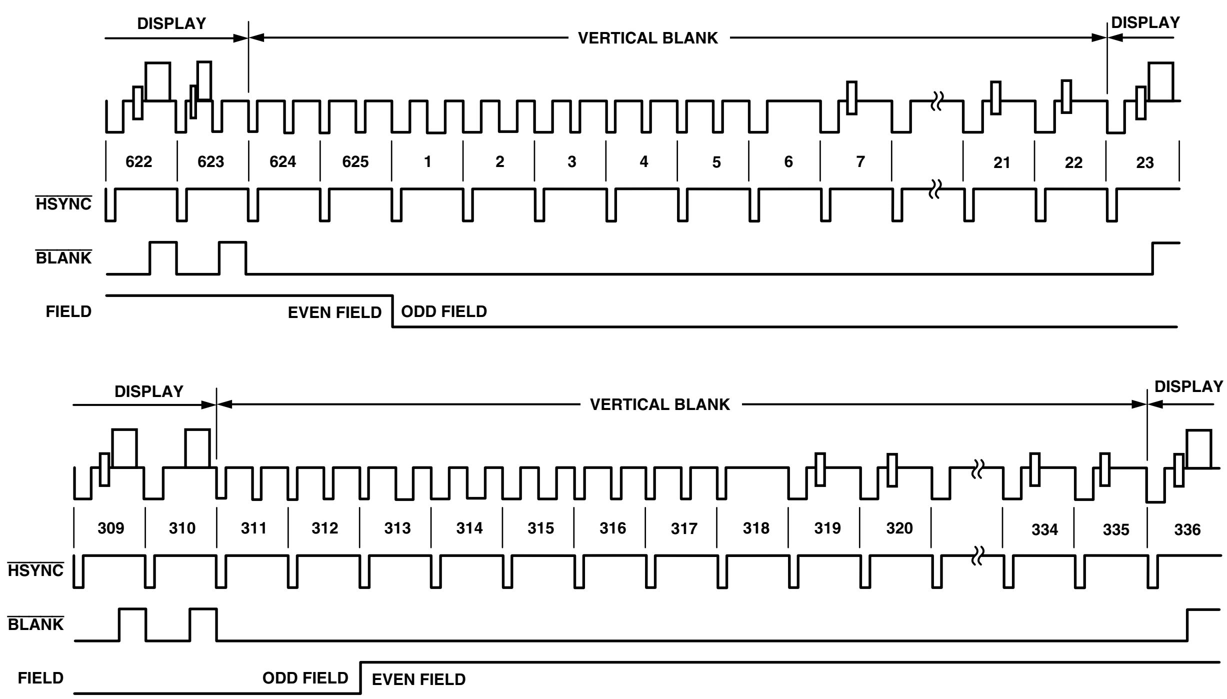


Figure 25. Timing Mode 1 (PAL)

Mode 1: Master Option HSYNC, BLANK, FIELD
(Timing Register 0 TR0 = X X X X X 0 1 1)

In this mode the ADV7170/ADV7171 can generate horizontal SYNC and Odd/Even FIELD signals. A transition of the FIELD input when HSYNC is low indicates a new frame, i.e., vertical retrace. The BLANK signal is optional. When the BLANK input is disabled, the ADV7170/ADV7171 automatically blanks all normally blank lines as per CCIR-624. Pixel data is latched on the rising clock edge following the timing signal transitions. Mode 1 is illustrated in Figure 24 (NTSC) and Figure 25 (PAL). Figure 26 illustrates the HSYNC, BLANK, and FIELD for an odd or even field transition relative to the pixel data.

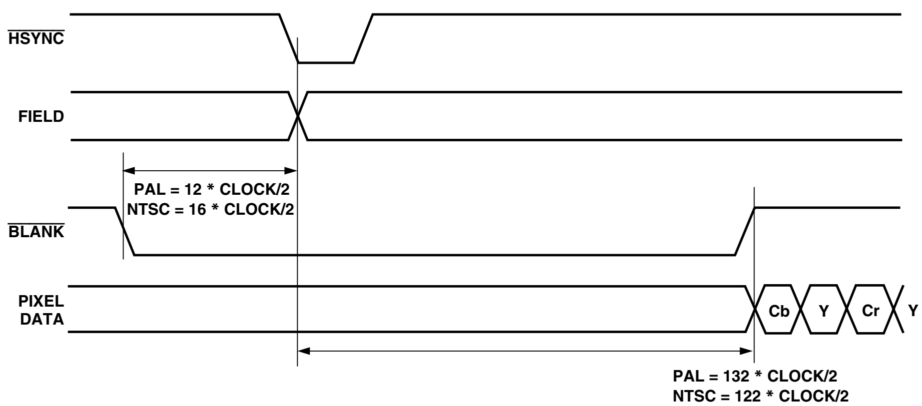


Figure 26. Timing Mode 1 Odd/Even Field Transitions Master/Slave

Mode 2: Slave Option HSYNC, VSYNC, BLANK
(Timing Register 0 TR0 = X X X X X 1 0 0)

In this mode the ADV7170/ADV7171 accepts horizontal and vertical SYNC signals. A coincident low transition of both HSYNC and VSYNC inputs indicates the start of an odd field. A VSYNC low transition when HSYNC is high indicates the start of an even field. The BLANK signal is optional. When the BLANK input is disabled, the ADV7170/ADV7171 automatically blanks all normally blank lines as per CCIR-624. Mode 2 is illustrated in Figure 27 (NTSC) and Figure 28 (PAL).

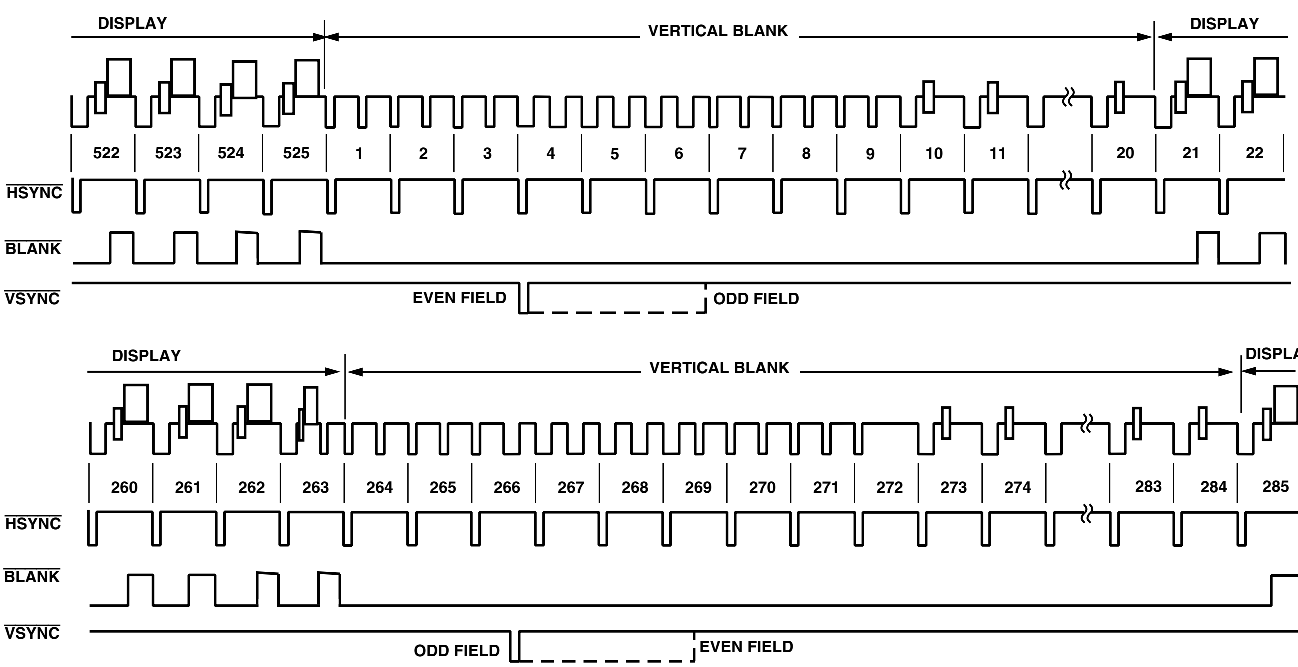


Figure 27. Timing Mode 2 (NTSC)

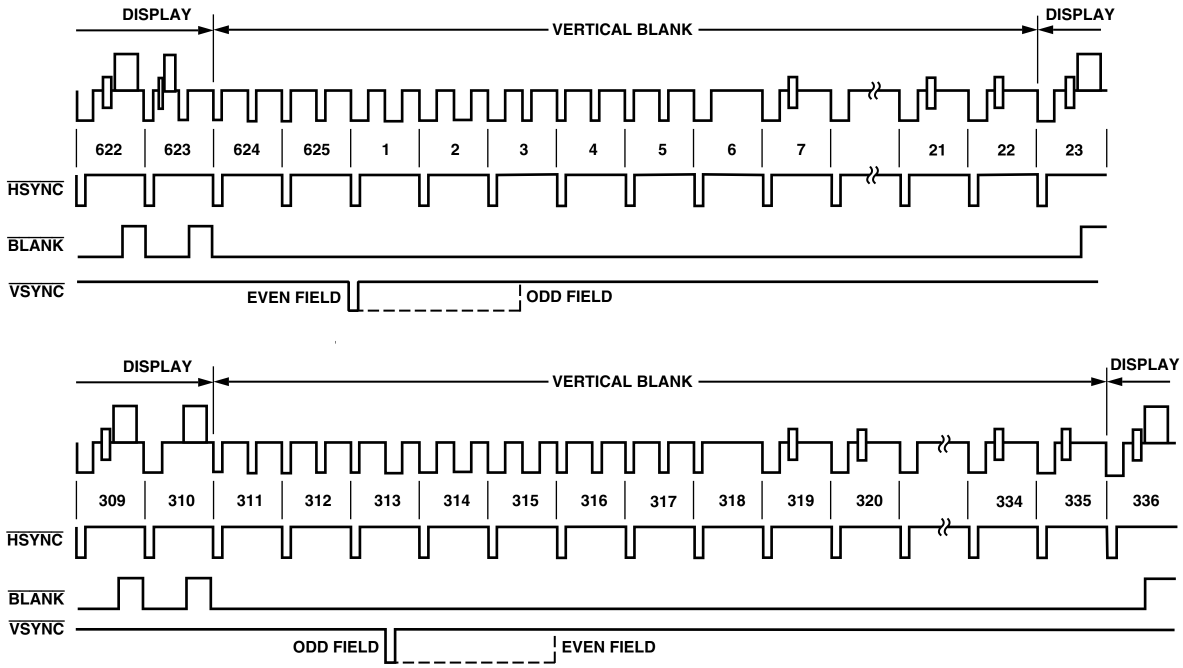


Figure 28. Timing Mode 2 (PAL)

Mode 2: Master Option $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, $\overline{\text{BLANK}}$
(Timing Register 0 TR0 = X X X X X 1 0 1)

In this mode the ADV7170/ADV7171 can generate horizontal and vertical SYNC signals. A coincident low transition of both $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ inputs indicates the start of an Odd Field. A $\overline{\text{VSYNC}}$ low transition when $\overline{\text{HSYNC}}$ is high indicates the start of an even field. The $\overline{\text{BLANK}}$ signal is optional. When the $\overline{\text{BLANK}}$ input is disabled, the ADV7170/ADV7171 automatically blanks all normally blank lines as per CCIR-624. Mode 2 is illustrated in Figure 27 (NTSC) and Figure 28 (PAL). Figure 29 illustrates the $\overline{\text{HSYNC}}$, $\overline{\text{BLANK}}$, and $\overline{\text{VSYNC}}$ for an even-to-odd field transition relative to the pixel data. Figure 30 illustrates the $\overline{\text{HSYNC}}$, $\overline{\text{BLANK}}$, and $\overline{\text{VSYNC}}$ for an odd-to-even field transition relative to the pixel data.

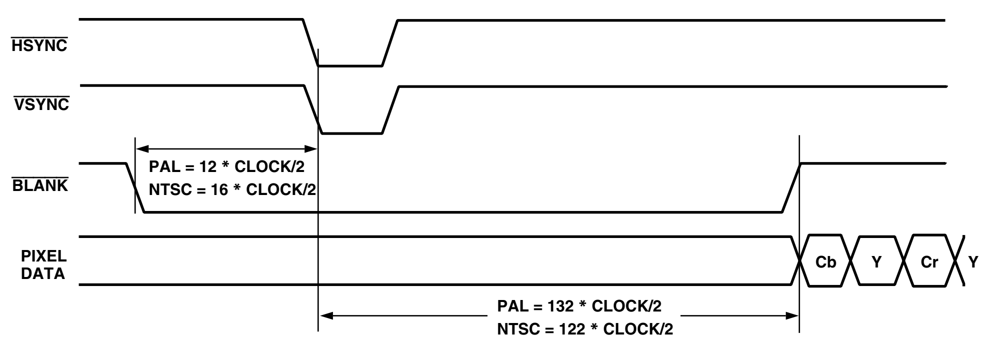


Figure 29. Timing Mode 2 Even-to-Odd Field Transition Master/Slave

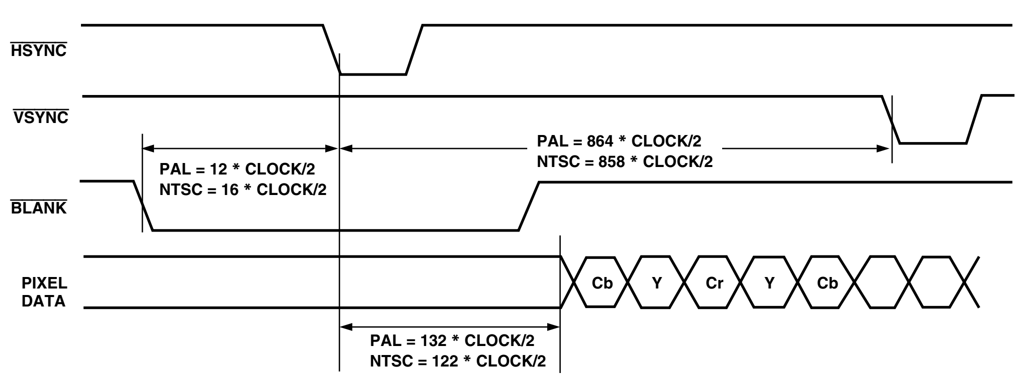


Figure 30. Timing Mode 2 Odd-to-Even Field Transition Master/Slave

Mode 3: Master/Slave Option $\overline{\text{HSYNC}}$, $\overline{\text{BLANK}}$, FIELD
(Timing Register 0 TR0 = X X X X X 1 1 0 or X X X X X 1 1 1)

In this mode the ADV7170/ADV7171 accepts or generates Horizontal SYNC and Odd/Even FIELD signals. A transition of the FIELD input when $\overline{\text{HSYNC}}$ is high indicates a new frame, i.e., vertical retrace. The $\overline{\text{BLANK}}$ signal is optional. When the $\overline{\text{BLANK}}$ input is disabled, the ADV7170/ADV7171 automatically blanks all normally blank lines as per CCIR-624. Mode 3 is illustrated in Figure 31 (NTSC) and Figure 32 (PAL).

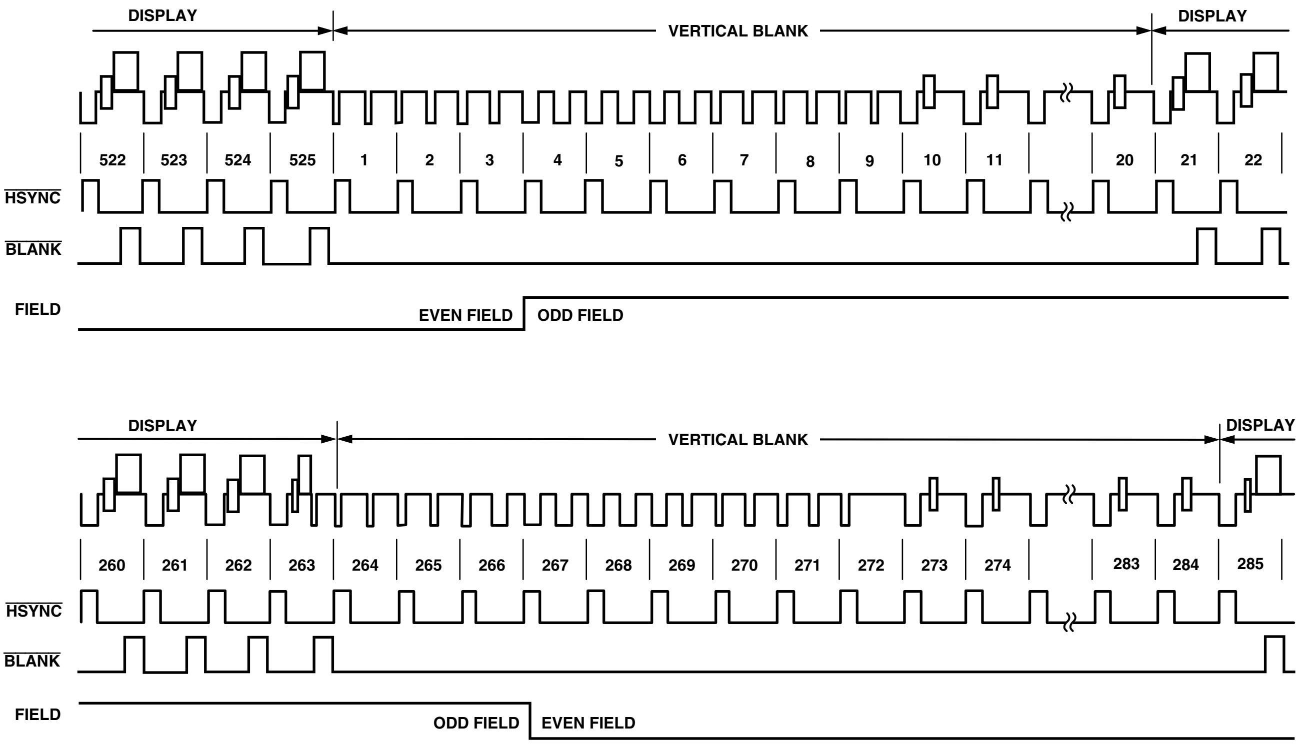


Figure 31. Timing Mode 3 (NTSC)

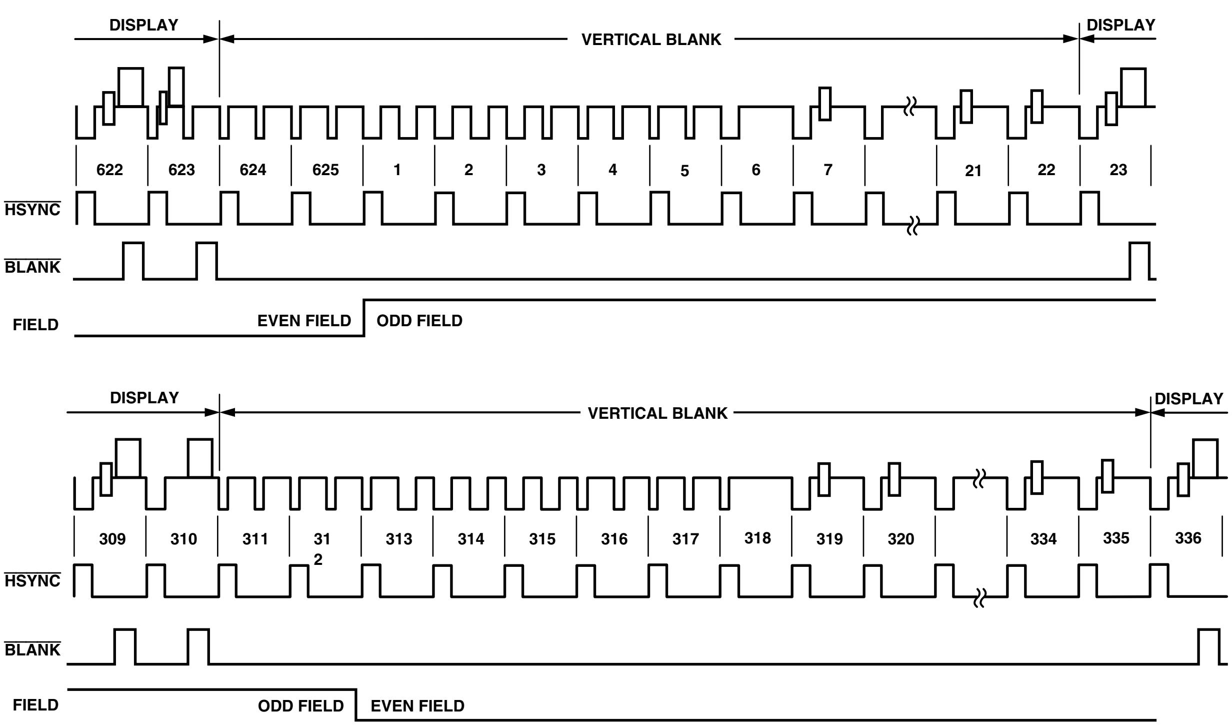


Figure 32. Timing Mode 3 (PAL)

POWER-ON RESET

After power-up, it is necessary to execute a reset operation. A reset occurs on the falling edge of a high-to-low transition on the $\overline{RESET}$ pin. This initializes the pixel port so that the pixel inputs, P7–P0 are selected. After reset, the ADV7170/ ADV7171 is automatically set up to operate in NTSC mode. Subcarrier frequency code 21F07C16HEX is loaded into the subcarrier frequency registers. All other registers, with the exception of Mode Register 0, are set to 00H. All bits in Mode Register 0 are set to Logic Level "0" except Bit MR44. Bit MR44 of Mode Register 4 is set to Logic "1." This enables the 7.5 IRE pedestal.

SCH PHASE MODE

The SCH phase is configured in default mode to reset every four (NTSC) or eight (PAL) fields to avoid an accumulation of SCH phase error over time. In an ideal system, zero SCH phase error would be maintained forever, but in reality, this is impossible to achieve due to clock frequency variations. This effect is reduced by the use of a 32-bit DDS, which generates this SCH.

Resetting the SCH phase every four or eight fields avoids the accumulation of SCH phase error, and results in very minor SCH phase jumps at the start of the four or eight field sequence.

Resetting the SCH phase should not be done if the video source does not have stable timing or the ADV7170/ADV7171 is configured in RTC mode (MR21 = 1 and MR22 = 1). Under these conditions (unstable video) the subcarrier phase reset should be enabled (MR22 = 0 and MR21 = 1) but no reset applied. In this configuration the SCH phase will never be reset, which means that the output video will now track the unstable input video. The subcarrier phase reset, when applied, will reset the SCH phase to Field 0 at the start of the next field (e.g., subcarrier phase reset applied in Field 5 [PAL] on the start of the next field SCH phase will be reset to Field 0).

MPU PORT DESCRIPTION

The ADV7170 and ADV7171 support a two-wire serial (I^2C Compatible) microprocessor bus driving multiple peripherals. Two inputs, serial data (SDATA) and serial clock (SCLOCK), carry information between any device connected to the bus. Each slave device is recognized by a unique address. The ADV7170 and ADV7171 each have four possible slave addresses for both read and write operations. These are unique addresses for each device and are illustrated in Figure 33 and Figure 34. The LSB sets either a read or write operation. Logic Level "1" corresponds to a read operation, while Logic Level "0" corresponds to a write operation. A "1" is set by setting the ALSB pin of the ADV7170/ADV7171 to Logic Level "0" or Logic Level "1."

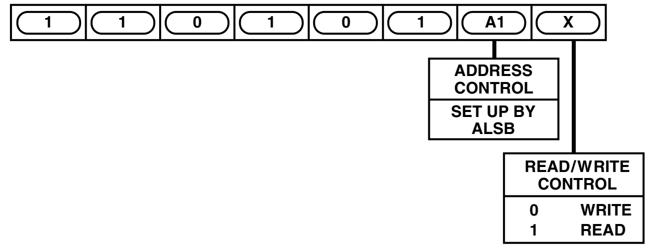


Figure 33. ADV7170 Slave Address

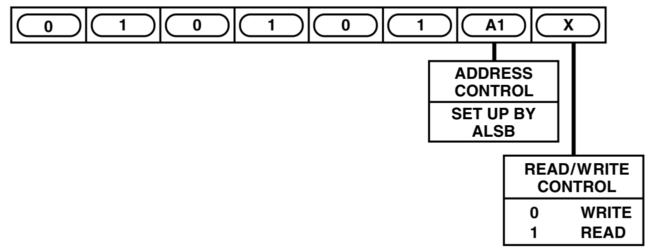


Figure 34. ADV7171 Slave Address

To control the various devices on the bus, the following protocol must be followed: first, the master initiates a data transfer by establishing a start condition, defined by a high-to-low transition on SDATA while SCLOCK remains high. This indicates that an address/data stream will follow. All peripherals respond to the start condition and shift the next eight bits (7-bit address + R/$\overline{W}$ bit). The bits transfer from MSB down to LSB. The peripheral that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This is known as an acknowledge bit. All other devices withdraw from the bus at this point and maintain an idle condition. The idle condition is where the device monitors the SDATA and SCLOCK lines waiting for the start condition and the correct transmitted address. The R/$\overline{W}$ bit determines the direction of the data. A Logic "0" on the LSB of the first byte means that the master will write information to the peripheral. A Logic "1" on the LSB of the first byte means that the master will read information from the peripheral.

The ADV7170/ADV7171 acts as a standard slave device on the bus. The data on the SDATA pin is 8 bits long, supporting the 7-bit addresses, plus the R/$\overline{W}$ bit. The ADV7170 has 48 subaddresses and the ADV7171 has 26 subaddresses to enable access to the internal registers. It therefore interprets the first byte as the device address and the second byte as the starting subaddress. The subaddresses auto increment allows data to be written to or read from the starting subaddress. A data transfer is always terminated by a stop condition. The user can also access any unique subaddress register on a one-by-one basis without having to update all the registers. There is one exception. The subcarrier frequency registers should be updated in sequence, starting with Subcarrier Frequency Register 0. The auto increment function should then be used to increment and access Subcarrier Frequency Registers 1, 2, and 3. The subcarrier frequency registers should not be accessed independently.

Stop and start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, they cause an immediate jump to the idle condition. During a given SCLOCK high period, the user should issue only one start condition, one stop condition or a single stop condition followed by a single start condition. If an invalid subaddress is issued by the user, the ADV7170/ ADV7171 will not issue an acknowledge and will return to the idle condition. If, in auto-increment mode the user exceeds the highest subaddress, the following action will be taken:

1. In Read Mode, the highest subaddress register contents will continue to be output until the master device issues a no-acknowledge. This indicates the end of a read. A no-acknowledge condition is where the SDATA line is not pulled low on the ninth pulse.
2. In Write Mode, the data for the invalid byte will not be loaded into any subaddress register, a no-acknowledge will be issued by the ADV7170/ADV7171 and the part will return to the idle condition.

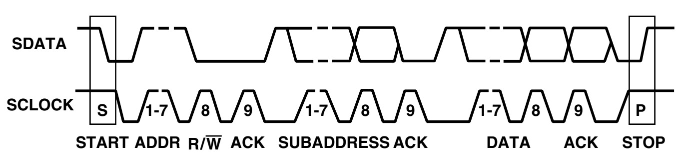


Figure 35. Bus Data Transfer

Figure 35 illustrates an example of data transfer for a read sequence and the start and stop conditions.

Figure 36 shows bus write and read sequences.

REGISTER ACCESSES

The MPU can write to or read from all of the ADV7170/ ADV7171 registers except the subaddress register, which is a write-only register. The subaddress register determines which register the next read or write operation accesses. All communications with the part through the bus start with an access to the subaddress register. A read/write operation is performed from/to the target address, which then increments to the next address until a stop command on the bus is performed.

REGISTER PROGRAMMING

The following section describes each register, including subaddress register, mode registers, subcarrier frequency registers, subcarrier phase register, timing registers, closed captioning extended data registers, closed captioning data registers and NTSC pedestal control registers, in terms of its configuration.

Subaddress Register (SR7–SR0)

The communications register is an 8-bit write-only register. After the part has been accessed over the bus, and a read/write operation is selected, the subaddress is set up. The subaddress register determines to/from which register the operation takes place.

Figure 37 shows the various operations under the control of the subaddress register. Zero should always be written to SR7–SR6.

Register Select (SR5–SR0)

These bits are set up to point to the required starting address.

MODE REGISTER 0 MR0 (MR07–MR00)
(Address [SR4–SR0] = 00H)

Figure 38 shows the various operations under the control of Mode Register 0. This register can be read from as well as written to.

MR0 BIT DESCRIPTION

Output Video Standard Selection (MR01–MR00)

These bits are used to set up the encode mode. The ADV7170/ ADV7171 can be set up to output NTSC, PAL (B, D, G, H, I) and PAL (M, N) standard video.

Luminance Filter Control (MR02–MR04)

These bits specify which luma filter is to be selected. The filter selection is made independent of whether PAL or NTSC is selected.

Chrominance Filter Control (MR05–MR07)

These bits select the chrominance filter. A low-pass filter can be selected with a choice of cutoff frequencies, 0.65 MHz, 1.0 MHz, 1.3 MHz or 2 MHz, along with a choice of CIF or QCIF filters.

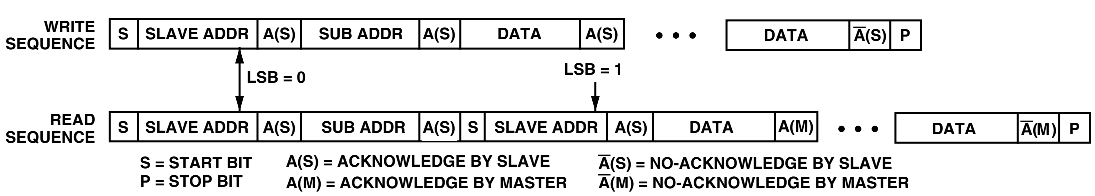


Figure 36. Write and Read Sequences

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0

SR7–SR5 (000)

ZERO SHOULD BE WRITTEN TO THESE BITS

ADV7171 SUBADDRESS REGISTER

SR5	SR4	SR3	SR2	SR1	SR0	
0	0	0	0	0	0	MODE REGISTER 0
0	0	0	0	0	1	MODE REGISTER 1
0	0	0	0	1	0	MODE REGISTER 2
0	0	0	0	1	1	MODE REGISTER 3
0	0	0	1	0	0	MODE REGISTER 4
0	0	0	1	0	1	RESERVED
0	0	0	1	1	0	RESERVED
0	0	0	1	1	1	TIMING MODE REGISTER 0
0	0	1	0	0	0	TIMING MODE REGISTER 1
0	0	1	0	0	1	SUBCARRIER FREQUENCY REGISTER 0
0	0	1	0	1	0	SUBCARRIER FREQUENCY REGISTER 1
0	0	1	0	1	1	SUBCARRIER FREQUENCY REGISTER 2
0	0	1	1	0	0	SUBCARRIER FREQUENCY REGISTER 3
0	0	1	1	0	1	SUBCARRIER PHASE REGISTER
0	0	1	1	1	0	CLOSED CAPTIONING EXTENDED DATA-BYTE 0
0	0	1	1	1	1	CLOSED CAPTIONING EXTENDED DATA-BYTE 1
0	1	0	0	0	0	CLOSED CAPTIONING DATA-BYTE 0
0	1	0	0	0	1	CLOSED CAPTIONING DATA-BYTE 1
0	1	0	0	1	0	NTSC PEDESTAL CONTROL REG 0/ PAL TTX CONTROL REG 0
0	1	0	0	1	1	NTSC PEDESTAL CONTROL REG 1/ PAL TTX CONTROL REG 1
0	1	0	1	0	0	NTSC PEDESTAL CONTROL REG 2/ PAL TTX CONTROL REG 2
0	1	0	1	0	1	NTSC PEDESTAL CONTROL REG 3/ PAL TTX CONTROL REG 3
0	1	0	1	1	0	CGMS_WSS_0
0	1	0	1	1	1	CGMS_WSS_1
0	1	1	0	0	0	CGMS_WSS_2
0	1	1	0	0	1	TELETEXT REQUEST CONTROL REGISTER

ADV7170 SUBADDRESS REGISTER

SR5	SR4	SR3	SR2	SR1	SR0	
0	0	0	0	0	0	MODE REGISTER 0
0	0	0	0	0	1	MODE REGISTER 1
0	0	0	0	1	0	MODE REGISTER 2
0	0	0	0	1	1	MODE REGISTER 3
0	0	0	1	0	0	MODE REGISTER 4
0	0	0	1	0	1	RESERVED
0	0	0	1	1	0	RESERVED
0	0	0	1	1	1	TIMING MODE REGISTER 0
0	0	1	0	0	0	TIMING MODE REGISTER 1
0	0	1	0	0	1	SUBCARRIER FREQUENCY REGISTER 0
0	0	1	0	1	0	SUBCARRIER FREQUENCY REGISTER 1
0	0	1	0	1	1	SUBCARRIER FREQUENCY REGISTER 2
0	0	1	1	0	0	SUBCARRIER FREQUENCY REGISTER 3
0	0	1	1	0	1	SUBCARRIER PHASE REGISTER
0	0	1	1	1	0	CLOSED CAPTIONING EXTENDED DATA-BYTE 0
0	0	1	1	1	1	CLOSED CAPTIONING EXTENDED DATA-BYTE 1
0	1	0	0	0	0	CLOSED CAPTIONING DATA-BYTE 0
0	1	0	0	0	1	CLOSED CAPTIONING DATA-BYTE 1
0	1	0	0	1	0	NTSC PEDESTAL CONTROL REG 0/ PAL TTX CONTROL REG 0
0	1	0	0	1	1	NTSC PEDESTAL CONTROL REG 1/ PAL TTX CONTROL REG 1
0	1	0	1	0	0	NTSC PEDESTAL CONTROL REG 2/ PAL TTX CONTROL REG 2
0	1	0	1	0	1	NTSC PEDESTAL CONTROL REG 3/ PAL TTX CONTROL REG 3
0	1	0	1	1	0	CGMS_WSS_0
0	1	0	1	1	1	CGMS_WSS_1
0	1	1	0	0	0	CGMS_WSS_2
0	1	1	0	0	1	TELETEXT REQUEST CONTROL REGISTER
0	1	1	0	1	0	RESERVED
0	1	1	0	1	1	RESERVED
0	1	1	1	0	0	RESERVED
0	1	1	1	0	1	RESERVED
0	1	1	1	1	0	MACROVISION REGISTERS
0	1	1	1	1	1	MACROVISION REGISTERS
1	0	0	0	0	0	MACROVISION REGISTERS
1	0	0	0	0	1	MACROVISION REGISTERS
1	0	0	0	1	0	MACROVISION REGISTERS
1	0	0	0	1	1	MACROVISION REGISTERS
1	0	0	1	0	0	MACROVISION REGISTERS
1	0	0	1	0	1	MACROVISION REGISTERS
1	0	0	1	1	0	MACROVISION REGISTERS
1	0	0	1	1	1	MACROVISION REGISTERS
1	0	1	0	0	0	MACROVISION REGISTERS
1	0	1	0	0	1	MACROVISION REGISTERS
1	0	1	0	1	0	MACROVISION REGISTERS
1	0	1	0	1	1	MACROVISION REGISTERS
1	0	1	1	0	0	MACROVISION REGISTERS
1	0	1	1	0	1	MACROVISION REGISTERS
1	0	1	1	1	0	MACROVISION REGISTERS
1	0	1	1	1	1	MACROVISION REGISTERS

Figure 37. Subaddress Register Map

MR07	MR06	MR05	MR04	MR03	MR02	MR01	MR00

CHROMA FILTER SELECT

MR07	MR06	MR05	
0	0	0	1.3 MHz LOW PASS FILTER
0	0	1	0.65 MHz LOW PASS FILTER
0	1	0	1.0 MHz LOW PASS FILTER
0	1	1	2.0 MHz LOW PASS FILTER
1	0	0	RESERVED
1	0	1	CIF
1	1	0	Q CIF
1	1	1	RESERVED

LUMA FILTER SELECT

MR04	MR03	MR02	
0	0	0	LOW PASS FILTER (NTSC)
0	0	1	LOW PASS FILTER (PAL)
0	1	0	NOTCH FILTER (NTSC)
0	0	1	NOTCH FILTER (PAL)
1	0	0	EXTENDED MODE
1	0	1	CIF
1	1	0	Q CIF
1	1	1	RESERVED

OUTPUT VIDEO STANDARD SELECTION

MR01	MR00	
0	0	NTSC
0	1	PAL (B, D, G, H, I)
1	0	PAL (M)
1	1	RESERVED

Figure 38. Mode Register 0

MODE REGISTER 1 MR1 (MR17–MR10)
(Address (SR4–SR0) = 01H)

Figure 39 shows the various operations under the control of Mode Register 1. This register can be read from as well as written to.

MR1 BIT DESCRIPTION

Interlace Control (MR10)

This bit is used to set up the output to interlaced or noninterlaced mode. This mode is only relevant when the part is in composite video mode.

Closed Captioning Field Selection (MR12–MR11)

These bits control the fields on which closed captioning data is displayed; closed captioning information can be displayed on an odd field, even field or both fields.

DAC Control (MR16–MR13)

These bits can be used to power down the DACs. This can be used to reduce the power consumption of the ADV7170/ADV7171 if any of the DACs are not required in the application.

Color Bar Control (MR17)

This bit can be used to generate and output an internal color bar test pattern. The color bar configuration is 100/7.5/75/7.5 for NTSC and 100/0/75/0 for PAL. It is important to note that when color bars are enabled the ADV7170/ADV7171 is configured in a master timing mode.

MODE REGISTER 2 MR2 (MR27–MR20)
(Address [SR4-SR0] = 02H)

Mode Register 2 is an 8-bit-wide register.

Figure 40 shows the various operations under the control of Mode Register 2. This register can be read from as well as written to.

MR2 BIT DESCRIPTION

Square Pixel Control (MR20)

This bit is used to set up square pixel mode. This is available in slave mode only. For NTSC, a 24.5454 MHz clock must be supplied. For PAL, a 29.5 MHz clock must be supplied.

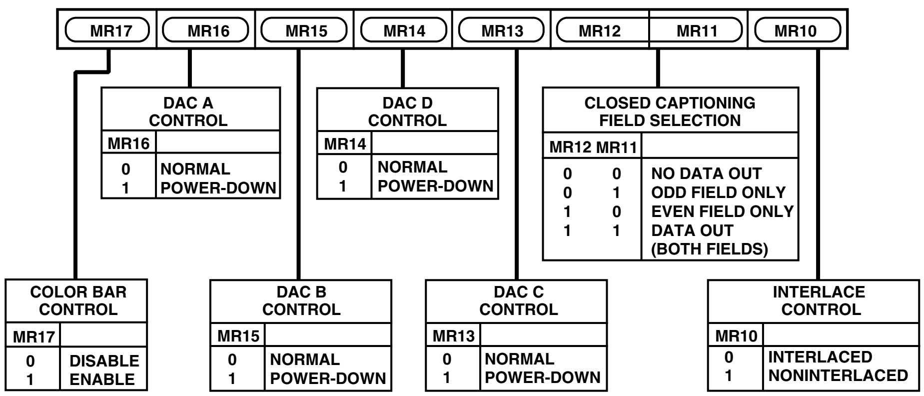


Figure 39. Mode Register 1

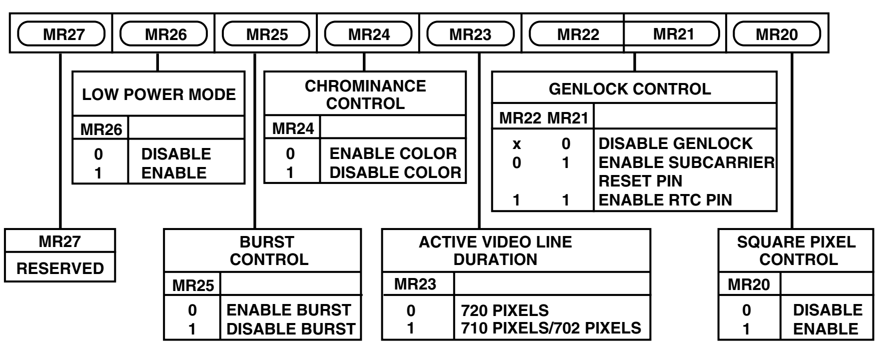


Figure 40. Mode Register 2

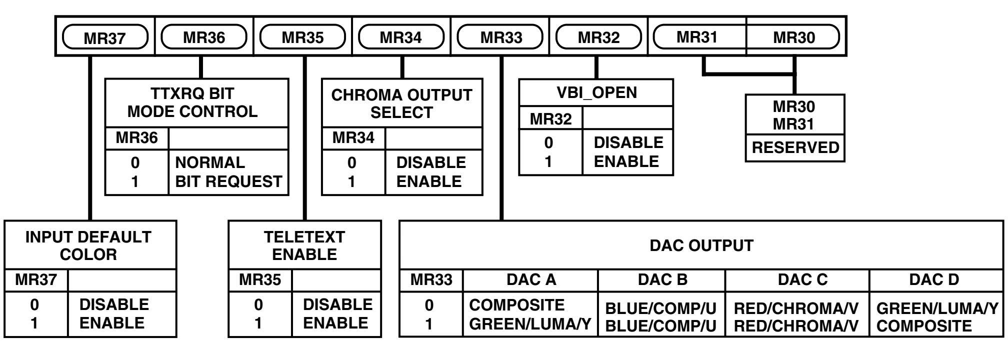


Figure 41. Mode Register 3

Genlock Control (MR22–MR21)
These bits control the genlock feature of the ADV7170/ADV7171. Setting MR21 to a Logic "1" configures the SCRESET/RTC pin as an input. Setting MR22 to Logic Level "0" configures the SCRESET/RTC pin as a subcarrier reset input. Therefore, the subcarrier will reset to Field 0 following a low-to-high transition on the SCRESET/RTC pin. Setting MR22 to Logic Level "1" configures the SCRESET/RTC pin as a real-time control input.

Active Video Line Duration (MR23)
This bit switches between two active video line durations. A zero selects CCIR REC601. (720 pixels PAL/NTSC) and a one selects ITU-R.BT470 standard for active video duration (710 pixels NTSC 702 pixels PAL).

Chrominance Control (MR24)
This bit enables the color information to be switched on and off the video output.

Burst Control (MR25)
This bit enables the burst information to be switched on and off the video output.

Low Power Mode (MR26)
This bit enables the lower power mode of the ADV7170/ADV7171. This will reduce the DAC current by 45%.

Reserved (MR27)
A Logical 0 must be written to this bit.

MODE REGISTER 3 MR3 (MR37–MR30)
(Address [SR4–SR0] = 03H)
Mode Register 3 is an 8-bit-wide register.
Figure 41 shows the various operations under the control of Mode Register 3.

MR3 BIT DESCRIPTION

Revision Code (MR30–MR31)
These bits are read only and indicates the revision of the device.

VBI Open (MR32)
This bit determines whether or not data in the vertical blanking interval (VBI) is output to the analog outputs or blanked. VBI data insertion is not available in Slave Mode 0. Also, when both, $\overline{\text{BLANK}}$ input control and VBI-open are enabled, $\overline{\text{BLANK}}$ input control has priority, i.e., VBI data insertion will not work.

DAC Output (MR33)
This bit is used to switch the DAC outputs from SCART to a EUROSCART configuration. A complete table of all DAC output configurations is shown below.

Chroma Output Select (MR34)
With this active high bit it is possible to output YUV data with a composite output on the fourth DAC or a chroma output on the fourth DAC (0 = CVBS; 1 = CHROMA).

Teletext Enable (MR35)
This bit must be set to "1" to enable teletext data insertion on the TTX pin.

TTXREQ Bit Mode Control (MR36)
This bit enables switching of the teletext request signal from a continuous high signal ("MR36 = 0") to a bit wise request signal ("MR36 = 1").

Input Default Color (MR37)
This bit determines the default output color from the DACs for zero input pixel data (or disconnected). A Logical "0" means that the color corresponding to 00000000 will be displayed. A Logical "1" forces the output color to black for 00000000 pixel input video data.

Table II. DAC Output Configuration Matrix

MR34	MR40	MR41	MR33	DAC A	DAC B	DAC C	DAC D	Simultaneous Output
0	0	0	0	CVBS	CVBS	C	Y	2 Composite and Y/C
0	0	0	1	Y	CVBS	C	CVBS	2 Composite and Y/C
0	0	1	0	CVBS	CVBS	C	Y	2 Composite and Y/C
0	0	1	1	Y	CVBS	C	CVBS	2 Composite and Y/C
0	1	0	0	CVBS	B	R	G	RGB and Composite
0	1	0	1	G	B	R	CVBS	RGB and Composite
0	1	1	0	CVBS	U	V	Y	YUV and Composite
0	1	1	1	Y	U	V	CVBS	YUV and Composite
1	0	0	0	C	CVBS	C	Y	1 Composite, Y and 2C
1	0	0	1	Y	CVBS	C	C	1 Composite, Y and 2C
1	0	1	0	C	CVBS	C	Y	1 Composite, Y and 2C
1	0	1	1	Y	CVBS	C	C	1 Composite, Y and 2C
1	1	0	0	C	B	R	G	RGB and C
1	1	0	1	G	B	R	C	RGB and C
1	1	1	0	C	U	V	Y	YUV and C
1	1	1	1	Y	U	V	C	YUV and C

CVBS: Composite Video Baseband Signal
Y: Luminance Component Signal (For YUV or Y/C Mode)
C: Chrominance Signal (For Y/C Mode)
U: Chrominance Component Signal (For YUV Mode)
V: Chrominance Component Signal (For YUV Mode)
R: RED Component Video (For RGB Mode)
G: GREEN Component Video (For RGB Mode)
B: BLUE Component Video (For RGB Mode)

NOTE
Each DAC can be powered ON or OFF individually with the following control bits ("0" = ON, "1" = OFF).
MR13-DAC C
MR14-DAC D
MR15-DAC B
MR16-DAC A

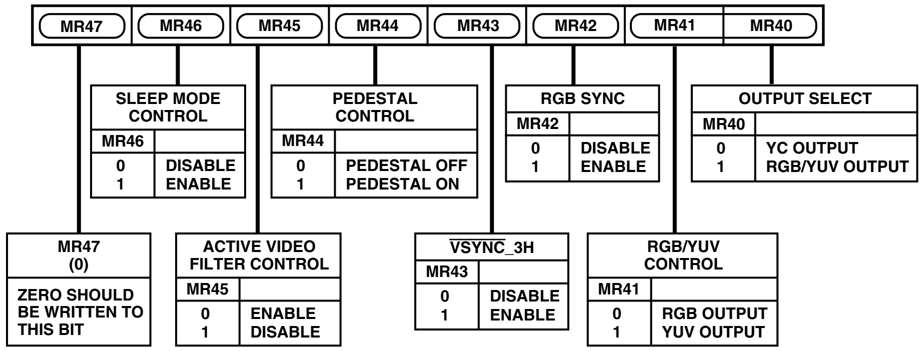


Figure 42. Mode Register 4

MODE REGISTER 4 MR4 (MR47–MR40)
(Address (SR4–SR0) = 04H)

Mode Register 4 is a 8-bit-wide register.

Figure 42 shows the various operations under the control of Mode Register 4.

MR4 BIT DESCRIPTION

Output Select (MR40)

This bit specifies if the part is in composite video or RGB/YUV mode. Note that in RGB/YUV mode the composite signal is still available.

RGB/YUV Control (MR41)

This bit enables the output from the RGB DACs to be set to YUV output video standard.

RGB Sync (MR42)

This bit is used to set up the RGB outputs with the sync information encoded on all RGB outputs.

$\overline{\text{VSYNC}}$_3H (MR43)

When this bit is enabled ("1") in slave mode, it is possible to drive the $\overline{\text{VSYNC}}$ active low input for 2.5 lines in PAL mode and 3 lines in NTSC mode. When this bit is enabled in master mode, the ADV7170/ADV7171 outputs an active low $\overline{\text{VSYNC}}$ signal for 3 lines in NTSC mode and 2.5 lines in PAL mode.

Pedestal Control (MR44)

This bit specifies whether a pedestal is to be generated on the NTSC composite video signal. This bit is invalid if the ADV7170/ADV7171 is configured in PAL mode.

Active Video Filter Control (MR45)

This bit controls the filter mode applied outside the active video portion of the line. This filter ensures that the Sync rise and fall times are always on spec regardless of which Luma filter is selected. A Logic "1" enables this mode.

Sleep Mode Control (MR46)

When this bit is set ("1") Sleep Mode is enabled. With this mode enabled, the ADV7170/ADV7171 power consumption is reduced to typically 200 nA. The I^2C registers can be written to and read from when the ADV7170/ADV7171 is in Sleep Mode. If MR46 is set to a ("0") when the device is in Sleep Mode, the ADV7170/ADV7171 will come out of Sleep Mode and resume normal operation. Also, if the $\overline{\text{RESET}}$ signal is applied during Sleep Mode the ADV7170/ADV7171 will come out of Sleep Mode and resume normal operation.

Reserved (MR47)

A Logical 0 should be written to this bit.

TIMING MODE REGISTER 0 (TR07–TR00)
(Address [SR4–SR0] = 07H)

Figure 43 shows the various operations under the control of Timing Register 0. This register can be read from as well as written to.

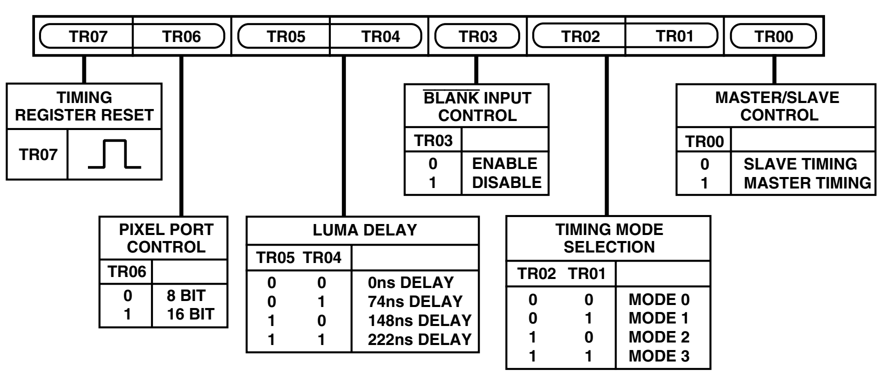


Figure 43. Timing Register 0

TR0 BIT DESCRIPTION

Master/Slave Control (TR00)
This bit controls whether the ADV7170/ADV7171 is in master or slave mode.

Timing Mode Selection (TR02–TR01)
These bits control the timing mode of the ADV7170/ADV7171. These modes are described in more detail in the Timing and Control section of the data sheet.

$\overline{\text{BLANK}}$ Control (TR03)
This bit controls whether the $\overline{\text{BLANK}}$ input is used when the part is in slave mode.

Luma Delay (TR05–TR04)
These bits control the addition of a luminance delay. Each bit represents a delay of 74 ns.

Pixel Port Control (TR06)
This bit is used to set the pixel port to accept 8-bit or 16-bit data. If an 8-bit input is selected the data will be set up on Pins P7–P0.

Timing Register Reset (TR07)
Toggling TR07 from low to high and low again resets the internal timing counters. This bit should be toggled after power-up, reset or changing to a new timing mode.

TIMING MODE REGISTER 1 (TR17–TR10) (Address (SR4–SR0) = 08H)

Timing Register 1 is a 8-bit-wide register.

Figure 44 shows the various operations under the control of Timing Register 1. This register can be read from as well written to. This register can be used to adjust the width and position of the master mode timing signals.

TR1 BIT DESCRIPTION

$\overline{\text{HSYNC}}$ Width (TR11–TR10)
These bits adjust the $\overline{\text{HSYNC}}$ pulsewidth.

$\overline{\text{HSYNC}}$ to FIELD/$\overline{\text{VSYNC}}$ Delay (TR13–TR12)
These bits adjust the position of the $\overline{\text{HSYNC}}$ output relative to the FIELD/$\overline{\text{VSYNC}}$ output.

$\overline{\text{HSYNC}}$ to FIELD Rising Edge Delay (TR15–TR14)
When the ADV7170/ADV7171 is in timing mode 1, these bits adjust the position of the $\overline{\text{HSYNC}}$ output relative to the FIELD output rising edge.

$\overline{\text{VSYNC}}$ Width (TR15–TR14)
When the ADV7170/ADV7171 is configured in Timing Mode 2, these bits adjust the $\overline{\text{VSYNC}}$ pulsewidth.

$\overline{\text{HSYNC}}$ to Pixel Data Adjust (TR17–TR16)
This enables the $\overline{\text{HSYNC}}$ to be adjusted with respect to the pixel data. This allows the Cr and Cb components to be swapped. This adjustment is available in both master and slave timing modes.

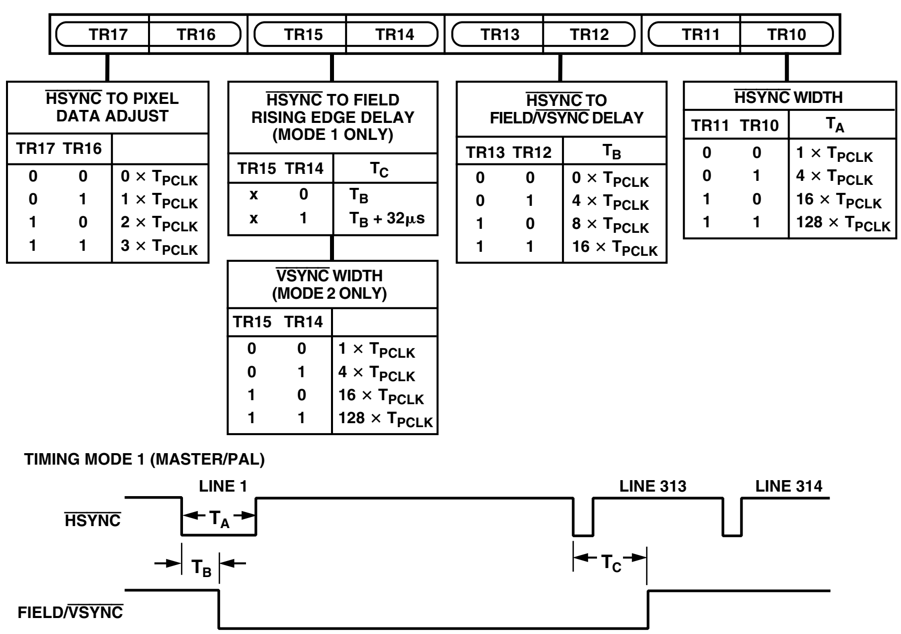


Figure 44. Timing Register 1

SUBCARRIER FREQUENCY REGISTER 3–0 (FSC3–FSC0) (Address [SR4–SR0] = 09H–0CH)

These 8-bit-wide registers are used to set up the subcarrier frequency. The value of these registers is calculated by using the following equation:

$$\textit{Subcarrier Frequency Register} = \frac{2^{32}\ 1}{F_{CLK}} \times F_{SCF}$$

i.e.: NTSC Mode,
F_{CLK} = 27 MHz,
F_{SCF} = 3.5795454 MHz

$$\textit{Subcarrier Frequency Value} = \frac{2^{32}\ 1}{27 \times 10^{6}} \times 3.579545 \times 10^{6}$$

$$= 21F07C16\textit{HEX}$$

Figure 45 shows how the frequency is set up by the four registers.

SUBCARRIER PHASE REGISTER (FP7–FP0) (Address [SR4–SR0] = 0DH)

This 8-bit-wide register is used to set up the subcarrier phase. Each bit represents 1.41°. For normal operation this register is set to 00Hex.

SUBCARRIER FREQUENCY REG 3	FSC31	FSC30	FSC29	FSC28	FSC27	FSC26	FSC25	FSC24
SUBCARRIER FREQUENCY REG 2	FSC23	FSC22	FSC21	FSC20	FSC19	FSC18	FSC17	FSC16
SUBCARRIER FREQUENCY REG 1	FSC15	FSC14	FSC13	FSC12	FSC11	FSC10	FSC9	FSC8
SUBCARRIER FREQUENCY REG 0	FSC7	FSC6	FSC5	FSC4	FSC3	FSC2	FSC1	FSC0

Figure 45. Subcarrier Frequency Register

CLOSED CAPTIONING EVEN FIELD DATA REGISTER 1–0 (CED15–CED0) (Address [SR4–SR0] = 0E–0FH)

These 8-bit-wide registers are used to set up the closed captioning extended data bytes on even fields. Figure 46 shows how the high and low bytes are set up in the registers.

BYTE 1	CED15	CED14	CED13	CED12	CED11	CED10	CED9	CED8
BYTE 0	CED7	CED6	CED5	CED4	CED3	CED2	CED1	CED0

Figure 46. Closed Captioning Extended Data Register

CLOSED CAPTIONING ODD FIELD DATA REGISTER 1–0 (CCD15–CCD0) (Subaddress [SR4–SR0] = 10–11H)

These 8-bit-wide registers are used to set up the closed captioning data bytes on odd fields. Figure 47 shows how the high and low bytes are set up in the registers.

BYTE 1	CCD15	CCD14	CCD13	CCD12	CCD11	CCD10	CCD9	CCD8
BYTE 0	CCD7	CCD6	CCD5	CCD4	CCD3	CCD2	CCD1	CCD0

Figure 47. Closed Captioning Data Register

NTSC PEDESTAL/PAL TELETEXT CONTROL REGISTERS 3–0 (PCE15–0, PCO15–0)/(TXE15–0, TXO15–0) (Subaddress [SR4–SR0] = 12–15H)

These 8-bit-wide registers are used to enable the NTSC pedestal/PAL Teletext on a line-by-line basis in the vertical blanking interval for both odd and even fields. Figures 48 and 49 show the four control registers. A Logic "1" in any of the bits of these registers has the effect of turning the Pedestal OFF on the equivalent line when used in NTSC. A Logic "1" in any of the bits of these registers has the effect of turning Teletext ON on the equivalent line when used in PAL.

	LINE 17	LINE 16	LINE 15	LINE 14	LINE 13	LINE 12	LINE 11	LINE 10
FIELD 1/3	PCO7	PCO6	PCO5	PCO4	PCO3	PCO2	PCO1	PCO0
	LINE 25	LINE 24	LINE 23	LINE 22	LINE 21	LINE 20	LINE 19	LINE 18
FIELD 1/3	PCO15	PCO14	PCO13	PCO12	PCO11	PCO10	PCO9	PCO8
	LINE 17	LINE 16	LINE 15	LINE 14	LINE 13	LINE 12	LINE 11	LINE 10
FIELD 2/4	PCE7	PCE6	PCE5	PCE4	PCE3	PCE2	PCE1	PCE0
	LINE 25	LINE 24	LINE 23	LINE 22	LINE 21	LINE 20	LINE 19	LINE 18
FIELD 2/4	PCE15	PCE14	PCE13	PCE12	PCE11	PCE10	PCE9	PCE8

Figure 48. Pedestal Control Registers

	LINE 14	LINE 13	LINE 12	LINE 11	LINE 10	LINE 9	LINE 8	LINE 7
FIELD 1/3	TXO7	TXO6	TXO5	TXO4	TXO3	TXO2	TXO1	TXO0
	LINE 22	LINE 21	LINE 20	LINE 19	LINE 18	LINE 17	LINE 16	LINE 15
FIELD 1/3	TXO15	TXO14	TXO13	TXO12	TXO11	TXO10	TXO9	TXO8
	LINE 14	LINE 13	LINE 12	LINE 11	LINE 10	LINE 9	LINE 8	LINE 7
FIELD 2/4	TXE7	TXE6	TXE5	TXE4	TXE3	TXE2	TXE1	TXE0
	LINE 22	LINE 21	LINE 20	LINE 19	LINE 18	LINE 17	LINE 16	LINE 15
FIELD 2/4	TXE15	TXE14	TXE13	TXE12	TXE11	TXE10	TXE9	TXE8

Figure 49. Teletext Control Registers

TELETEXT REQUEST CONTROL REGISTER TC07 (TC07–TC00) (Address [SR4–SR0] = 19H)

Teletext Control Register is an 8-bit-wide register. See Figure 50.

TTXREQ Rising Edge Control (TC07–TC04)

These bits control the position of the rising edge of TTXREQ. It can be programmed from zero CLOCK cycles to a max of 15 CLOCK cycles. See Figure 59.

TTXREQ Falling Edge Control (TC03–TC00)

These bits control the position of the falling edge of TTXREQ. It can be programmed from zero CLOCK cycles to a max of 15 CLOCK cycles. This controls the active window for Teletext data. Increasing this value reduces the amount of Teletext bits below the default of 360. If Bits TC03-TC00 are 00Hex when bits TC07–TC04 are changed, the falling edge of TTXREQ will track that of the rising edge (i.e., the time between the falling and rising edge remains constant). See Figure 59.

CGMS_WSS REGISTER 0 C/W0 (C/W07–C/W00) (Address [SR4–SR0] = 16H)

CGMS_WSS Register 0 is an 8-bit-wide register. Figure 51 shows the operations under the control of this register.

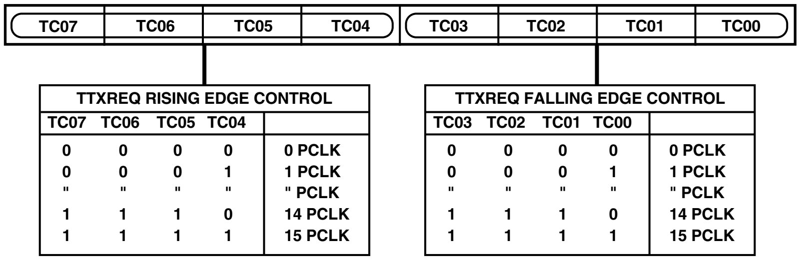


Figure 50. Teletext Control Register

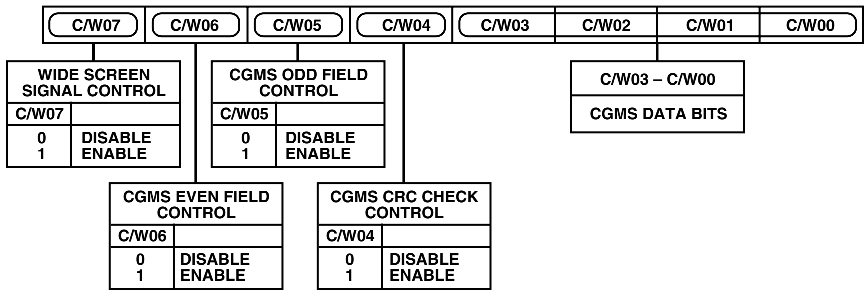


Figure 51. CGMS_WSS Register 0

C/W0 BIT DESCRIPTION

CGMS Data Bits (C/W03–C/W00)

These four data bits are the final four bits of CGMS data output stream. Note it is CGMS data ONLY in these bit positions, i.e., WSS data does not share this location.

CGMS CRC Check Control (C/W04)

When this bit is enabled ("1"), the last six bits of the CGMS data, i.e., the CRC check sequence, is calculated internally by the ADV7170/ADV7171. If this bit is disabled ("0") the CRC values in the register are output to the CGMS data stream.

CGMS Odd Field Control (C/W05)

When this bit is set ("1"), CGMS is enabled for odd fields. Note this is only valid in NTSC mode.

CGMS Even Field Control (C/W06)

When this bit is set ("1"), CGMS is enabled for even fields. Note this is only valid in NTSC mode.

WSS Control (C/W07)

When this bit is set ("1"), wide screen signaling is enabled. Note this is only valid in PAL mode.

CGMS_WSS REGISTER 1 C/W1 (C/W17–C/W10) (Address [SR4–SR0] = 17H)

CGMS_WSS register 1 is an 8-bit-wide register. Figure 52 shows the operations under the control of this register.

C/W1 BIT DESCRIPTION

CGMS/WSS Data Bits (C/W15–C/W10)

These bit locations are shared by CGMS data and WSS data. In NTSC mode these bits are CGMS data. In PAL mode these bits are WSS data.

CGMS Data Bits (C/W17–C/W16)

These bits are CGMS data bits only.

CGMS_WSS REGISTER 2 C/W1 (C/W27–C/W20) (Address [SR4–SR0] = 18H)

CGMS_WSS register 2 is an 8-bit-wide register. Figure 53 shows the operations under the control of this register.

C/W2 BIT DESCRIPTION

CGMS/WSS Data Bits (C/W27–C/W20)

These bit locations are shared by CGMS data and WSS data. In NTSC mode these bits are CGMS data. In PAL mode these bits are WSS data.

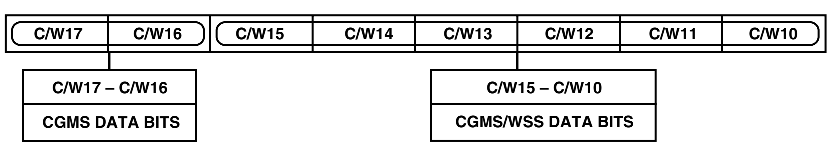


Figure 52. CGMS_WSS Register 1

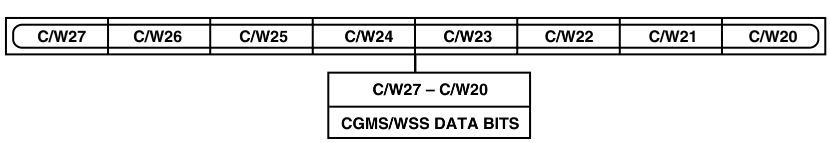


Figure 53. CGMS_WSS Register 2

APPENDIX 1

BOARD DESIGN AND LAYOUT CONSIDERATIONS

The ADV7170/ADV7171 is a highly integrated circuit containing both precision analog and high speed digital circuitry. It has been designed to minimize interference effects on the integrity of the analog circuitry by the high speed digital circuitry. It is imperative that these same design and layout techniques be applied to the system level design so that high speed, accurate performance is achieved. Figure 54, Recommended Analog Circuit Layout, shows the analog interface between the device and monitor.

The layout should be optimized for lowest noise on the ADV7170/ADV7171 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of V_{AA} and GND pins should by minimized to minimize inductive ringing.

Ground Planes

The ground plane should encompass all ADV7170/ADV7171 ground pins, voltage reference circuitry, power supply bypass circuitry for the ADV7170/ADV7171, the analog output traces, and all the digital signal traces leading up to the ADV7170/ADV7171. The ground plane is the board's common ground plane.

Power Planes

The ADV7170/ADV7171 and any associated analog circuitry should have its own power plane, referred to as the analog power plane (V_{AA}). This power plane should be connected to the regular PCB power plane (V_{CC}) at a single point through a ferrite bead. This bead should be located within three inches of the ADV7170/ADV7171.

The metallization gap separating device power plane and board power plane should be as narrow as possible to minimize the obstruction to the flow of heat from the device into the general board.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all ADV7170/ADV7171 power pins and voltage reference circuitry.

Plane-to-plane noise coupling can be reduced by ensuring that portions of the regular PCB power and ground planes do not overlay portions of the analog power plane unless they can be arranged so that the plane-to-plane noise is common-mode.

Supply Decoupling

For optimum performance, bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance. Best performance is obtained with 0.1 μF ceramic capacitor decoupling. Each group of V_{AA} pins on the ADV7170/ADV7171 must have at least one 0.1 μF decoupling capacitor to GND. These capacitors should be placed as close to the device as possible.

It is important to note that while the ADV7170/ADV7171 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a high frequency switching power supply is used, the designer should pay close attention to reducing power supply noise and consider using a three-terminal voltage regulator for supplying power to the analog power plane.

Digital Signal Interconnect

The digital inputs to the ADV7170/ADV7171 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane.

Due to the high clock rates involved, long clock lines to the ADV7170/ADV7171 should be avoided to reduce noise pickup.

Any active termination resistors for the digital inputs should be connected to the regular PCB power plane (V_{CC}) and not the analog power plane.

Analog Signal Interconnect

The ADV7170/ADV7171 should be located as close to the output connectors as possible to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the ground plane, not the analog power plane, to maximize the high frequency power supply rejection.

Digital inputs, especially pixel data inputs and clocking signals, should never overlay any of the analog signal circuitry and should be kept as far away as possible.

For best performance, the outputs should each have a 75 Ω load resistor connected to GND. These resistors should be placed as close as possible to the ADV7170/ADV7171 to minimize reflections.

The ADV7170/ADV7171 should have no inputs left floating. Any inputs that are not required should be tied to ground.

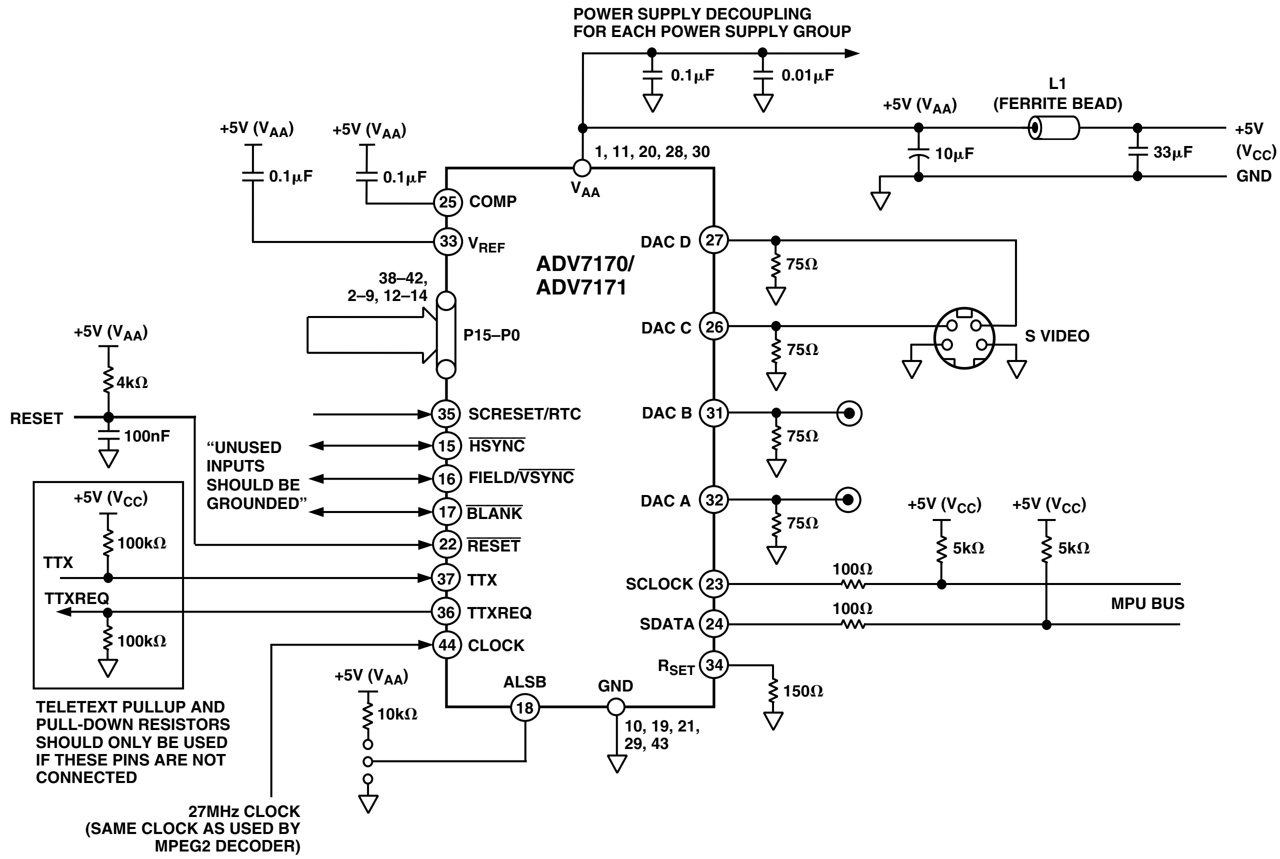


Figure 54. Recommended Analog Circuit Layout

The circuit below can be used to generate a 13.5 MHz waveform using the 27 MHz clock and the $\overline{\text{HSYNC}}$ pulse. This waveform is guaranteed to produce the 13.5 MHz clock in synchronization with the 27 MHz clock. This 13.5 MHz clock can be used if 13.5 MHz clock is required by the MPEG decoder. This will guarantee that the Cr and Cb pixel information is input to the ADV7170/ADV7171 in the correct sequence.

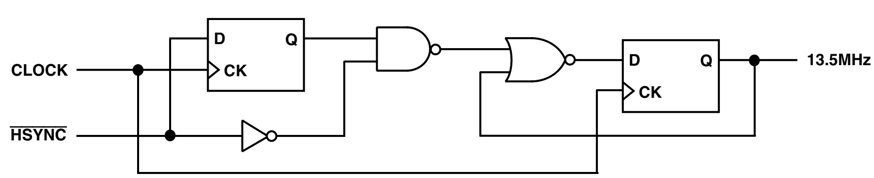


Figure 55. Circuit to Generate 13.5 MHz

APPENDIX 2

CLOSED CAPTIONING

The ADV7170/ADV7171 supports closed captioning, conforming to the standard television synchronizing waveform for color transmission. Closed captioning is transmitted during the blanked active line time of Line 21 of the odd fields and Line 284 of even fields.

Closed captioning consists of a 7-cycle sinusoidal burst that is frequency and phase locked to the caption data. After the clock run-in signal, the blanking level is held for two data bits and is followed by a Logic Level "1" start bit. 16 bits of data follow the start bit. These consist of two 8-bit bytes, seven data bits and one odd parity bit. The data for these bytes is stored in closed captioning Data Registers 0 and 1.

The ADV7170/ADV7171 also supports the extended closed captioning operation, which is active during even fields, and is encoded on scan Line 284. The data for this operation is stored in closed captioning extended Data Registers 0 and 1.

All clock run-in signals and timing to support closed captioning on Lines 21 and 284 are automatically generated by the ADV7170/ADV7171. All pixels inputs are ignored during Lines 21 and 284.

FCC Code of Federal Regulations (CFR) 47 Section 15.119 and EIA608 describe the closed captioning information for Lines 21 and 284.

The ADV7170/ADV7171 uses a single buffering method. This means that the closed captioning buffer is only one byte deep, therefore there will be no frame delay in outputting the closed captioning data unlike other 2-byte deep buffering systems. The data must be loaded at least one line before (Line 20 or Line 283) it is outputted on Line 21 and Line 284. A typical implementation of this method is to use $\overline{\text{VSYNC}}$ to interrupt a microprocessor, which will in turn load the new data (two bytes) every field. If no new data is required for transmission, you must insert zeros in both the data registers; this is called NULLING. It is also important to load "control codes," all of which are double bytes, on Line 21, or a TV will not recognize them. If you have a message like "Hello World," which has an odd number of characters, it is important to pad it out to an even number to get "end of caption" 2-byte control code to land in the same field.

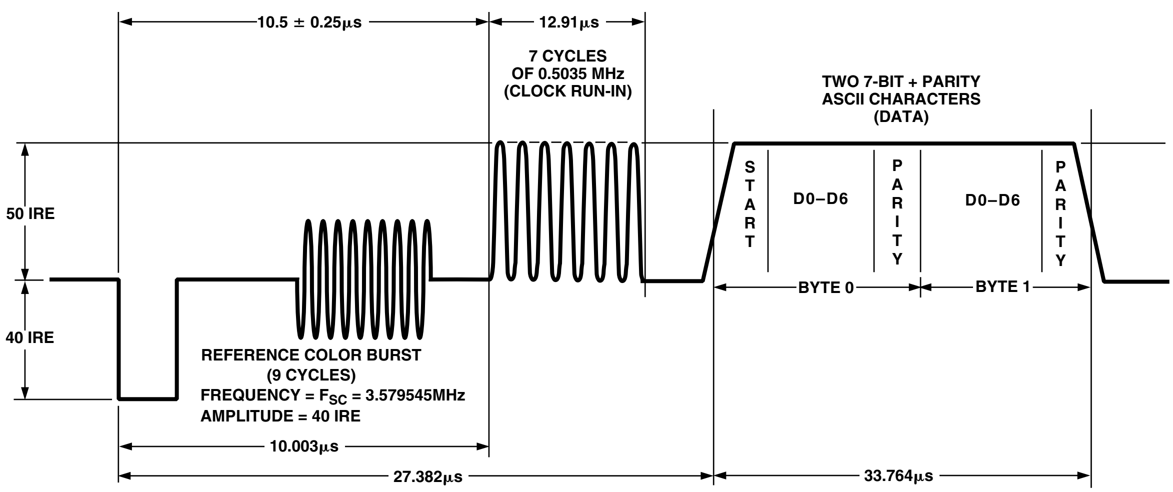


Figure 56. Closed Captioning Waveform (NTSC)

APPENDIX 3

COPY GENERATION MANAGEMENT SYSTEM (CGMS)

The ADV7170/ADV7171 supports Copy Generation Management System (CGMS) conforming to the standard. CGMS data is transmitted on Line 20 of the odd fields and Line 283 of even fields. Bits C/W05 and C/W06 control whether or not CGMS data is output on ODD and EVEN fields. CGMS data can only be transmitted when the ADV7170/ADV7171 is configured in NTSC mode. The CGMS data is 20 bits long, the function of each of these bits is as shown below. The CGMS data is preceded by a reference pulse of the same amplitude and duration as a CGMS bit (see Figure 57). The bits are output from the configuration registers in the following order; C/W00 = C16, C/W01 = C17, C/W02 = C18, C/W03 = C19, C/W10 = C8, C/W11 = C9, C/W12 = C10, C/W13 = C11, C/W14 = C12, C/W15 = C13, C/W16 = C14, C/W17 = C15, C/W20 = C0, C/W21 = C1, C/W22 = C2, C/W23 = C3, C/W24 = C4, C/W25 = C5, C/W26 = C6, C/W27 = C7. If the Bit C/W04 is set to a Logic "1," the last six bits, C19–C14, which comprise the 6-bit CRC check sequence, are calculated automatically on the ADV7170/ADV7171 based on the lower 14 bits (C0–C13) of the data in the data registers and output with the remaining 14 bits to form the complete 20 bits of the CGMS data. The calculation of the CRC sequence is based on the polynomial $X^6 + X + 1$ with a preset value of 111111. If C/W04 is set to a Logic "0," all 20 bits (C0–C19) are directly output from the CGMS registers (no CRC calculated, must be calculated by the user).

Function of CGMS Bits

Word 0 – 6 Bits
Word 1 – 4 Bits
Word 2 – 6 Bits
CRC – 6 Bits CRC Polynomial = $X^6 + X + 1$ (Preset to 111111)

Word 0	1	0	
B1	Aspect Ratio	16:94:3	
B2	Display Format	Letterbox	Normal
B3	Undefined		

Word 0
B4, B5, B6 Identification information about video and other signals (e.g., audio)

Word 1
B7, B8, B9, B10 Identification signal incidental to Word 0

Word 2
B11, B12, B13, B14 Identification signal and information incidental to Word 0

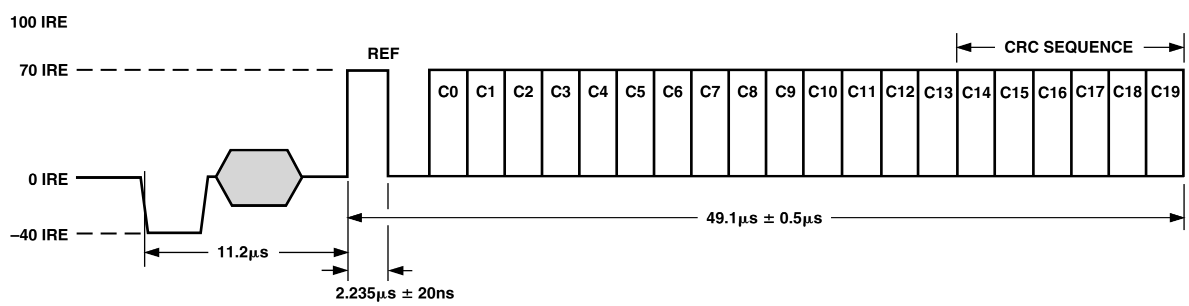


Figure 57. CGMS Waveform Diagram

APPENDIX 4

WIDE SCREEN SIGNALING

The ADV7170/ADV7171 supports Wide Screen Signalling (WSS) conforming to the standard. WSS data is transmitted on Line 23. WSS data can only be transmitted when the ADV7170/ADV7171 is configured in PAL mode. The WSS data is 14 bits long, the function of each of these bits is as shown below. The WSS data is preceded by a run-in sequence and a Start Code (see Figure 58). The bits are output from the configuration registers in the following order; C/W20 = W0, C/W21 = W1, C/W22 = W2, C/W23 = W3, C/W24 = W4, C/W25 = W5, C/W26 = W6, C/W27 = W7, C/W10 = W8, C/W11 = W9, C/W12 = W10, C/W13 = W11, C/W14 = W12, C/W15 = W13. If the bit C/W07 is set to a Logic "1" it enables the WSS data to transmitted on Line 23. The latter portion of Line 23 (42.5 µs from the falling edge of $\overline{\text{HSYNC}}$) is available for the insertion of video.

Function of CGMS Bits

Bit 0–Bit 2 Aspect Ratio/Format/Position

Bit 3 is odd parity check of Bit 0–Bit 2

B0	B1	B2	B3	Aspect Ratio	Format	Position
0	0	0	1	4:3	Full Format	Nonapplicable
1	0	0	0	14:9	Letterbox	Center
0	1	0	0	14:9	Letterbox	Top
1	1	0	1	16:9	Letterbox	Center
0	0	1	0	16:9	Letterbox	Top
1	0	1	1	>16:9	Letterbox	Center
0	1	1	1	14:9	Full Format	Center
1	1	1	0	16:9	Nonapplicable	Nonapplicable

B4	
0	Camera Mode
1	Film Mode

B5	
0	Standard Coding
1	Motion Adaptive Color Plus

B6	
0	No Helper
1	Modulated Helper

B7 RESERVED

B9	B10	
0	0	No Open Subtitles
1	0	Subtitles In Active Image Area
0	1	Subtitles Out of Active Image Area
1	1	Reserved

B11	
0	No Surround Sound Information
1	Surround Sound Mode

B12 RESERVED

B13 RESERVED

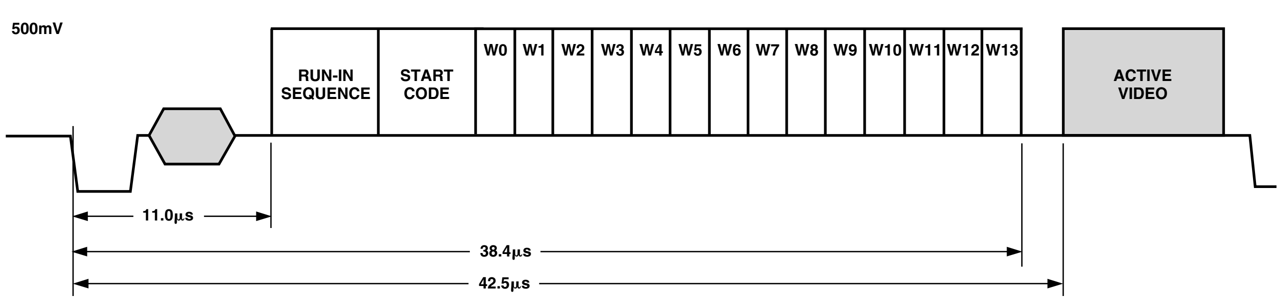


Figure 58. WSS Waveform Diagram

APPENDIX 5

TELETEXT INSERTION

t_{PD} is the time needed by the ADV7170/ADV7171 to interpolate input data on TTX and insert it onto the CVBS or Y outputs, such that it appears $t_{SYNTTXOUT}$ = 10.2 μs after the leading edge of the horizontal signal. Time TTX_{DEL} is the pipeline delay time by the source that is gated by the TTXREQ signal in order to deliver TTX data.

With the programmability offered with TTXREQ signal on the Rising/Falling edges, the TTX data is always inserted at the correct position of 10.2 μs after the leading edge of Horizontal Sync pulse, thus enabling a source interface with variable pipeline delays.

The width of the TTXREQ signal must always be maintained to allow the insertion of 360 (to comply with the Teletext Standard "PAL-WST") teletext bits at a text data rate of 6.9375 Mbits/s, this is achieved by setting TC03–TC00 to zero. The insertion window is not open if the Teletext Enable bit (MR35) is set to zero.

Teletext Protocol

The relationship between the TTX bit clock (6.9375 MHz) and the system CLOCK (27 MHz) for 50 Hz is given as follows:

$(27\ MHz/4) = 6.75\ MHz$

$(6.9375 \times 10^6/6.75 \times 10^6) = 1.027777$

Thus 37 TTX bits correspond to 144 clocks (27 MHz) and each bit has a width of almost four clock cycles. The ADV7170/ADV7171 uses an internal sequencer and variable phase interpolation filter to minimize the phase jitter and thus generate a bandlimited signal that can be outputted on the CVBS and Y outputs.

At the TTX input the bit duration scheme repeats after every 37 TTX bits or 144 clock cycles. The protocol requires that TTX Bits 10, 19, 28, and 37 are carried by three clock cycles, all other bits by four clock cycles. After 37 TTX bits, the next bits with three clock cycles are 47, 56, 65, and 74. This scheme holds for all following cycles of 37 TTX bits, until all 360 TTX bits are completed. All teletext lines are implemented in the say way. Individual control of teletext lines is controlled by Teletext Setup Registers.

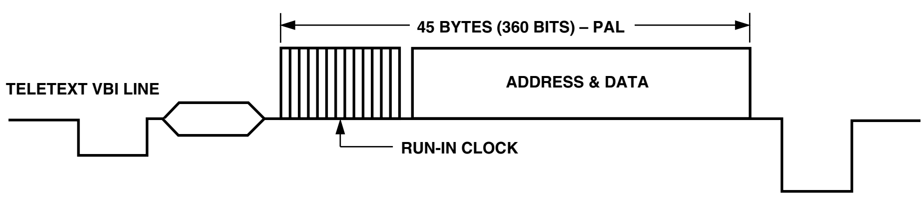
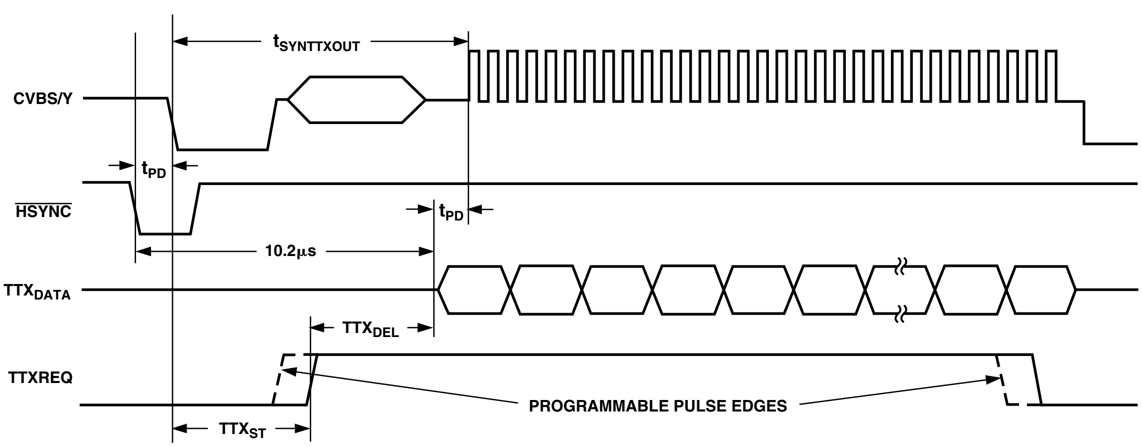


Figure 59. Teletext VBI Line



$t_{SYNTTXOUT}$ = 10.2µs
t_{PD} = PIPELINE DELAY THROUGH ADV7170/ADV7171
TTX_{DEL} = TTXREQ TO TTX (PROGRAMMABLE RANGE = 4 BITS [0–15 CLOCK CYCLES])

Figure 60. Teletext Functionality Diagram

APPENDIX 6

NTSC WAVEFORMS (WITH PEDESTAL)

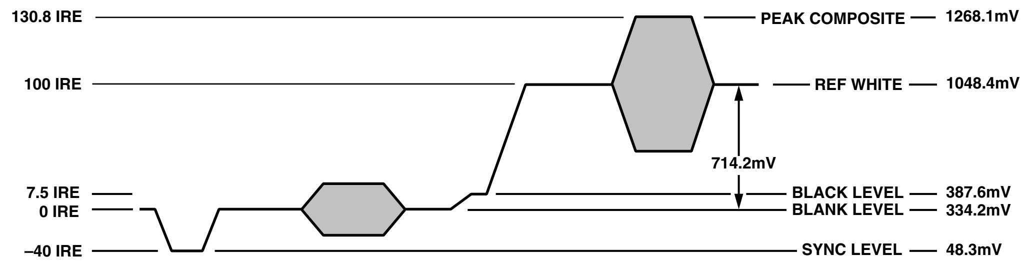


Figure 61. NTSC Composite Video Levels

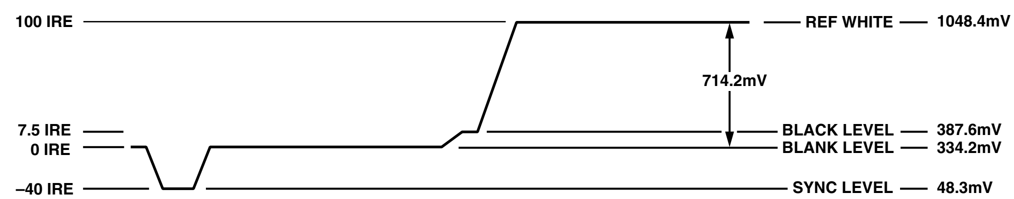


Figure 62. NTSC Luma Video Levels

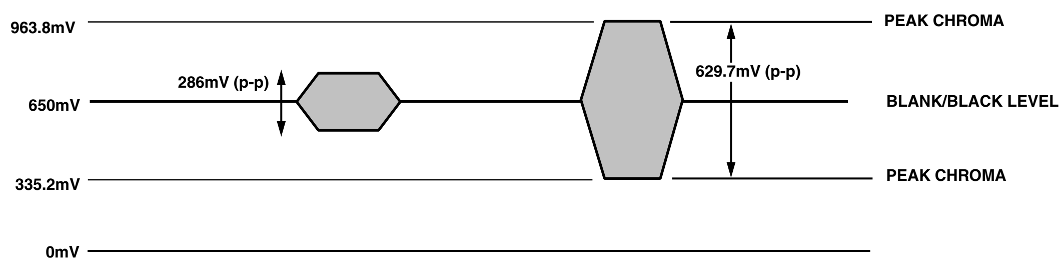


Figure 63. NTSC Chroma Video Levels

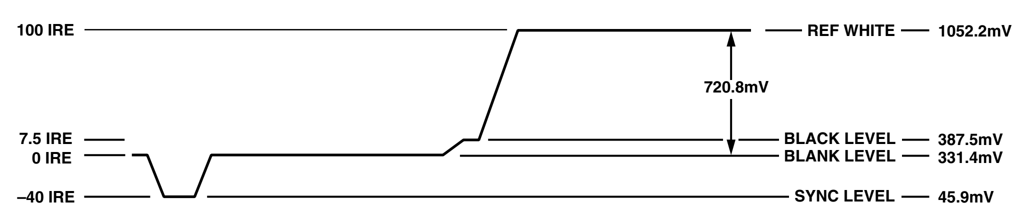


Figure 64. NTSC RGB Video Levels

NTSC WAVEFORMS (WITHOUT PEDESTAL)

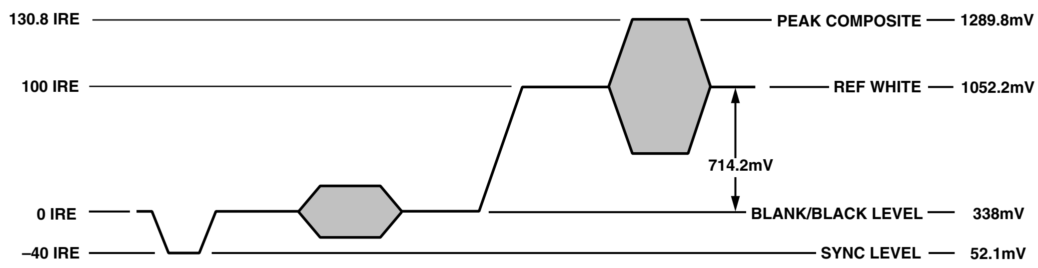


Figure 65. NTSC Composite Video Levels

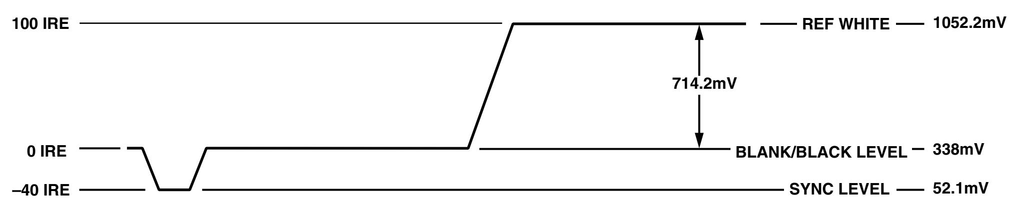


Figure 66. NTSC Luma Video Levels

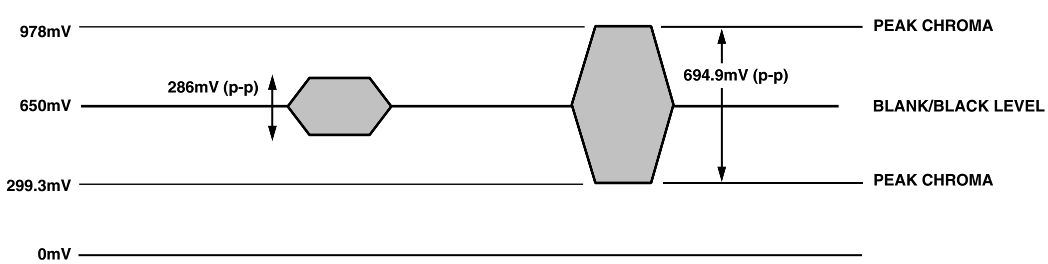


Figure 67. NTSC Chroma Video Levels

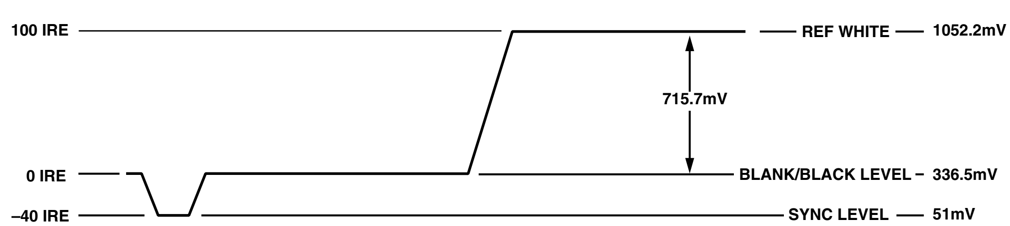


Figure 68. NTSC RGB Video Levels

PAL WAVEFORMS

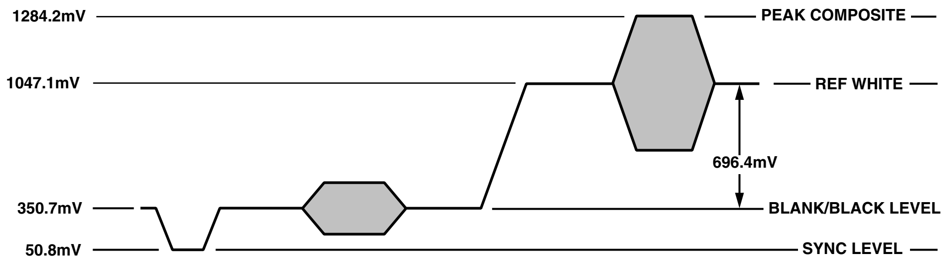


Figure 69. PAL Composite Video Levels

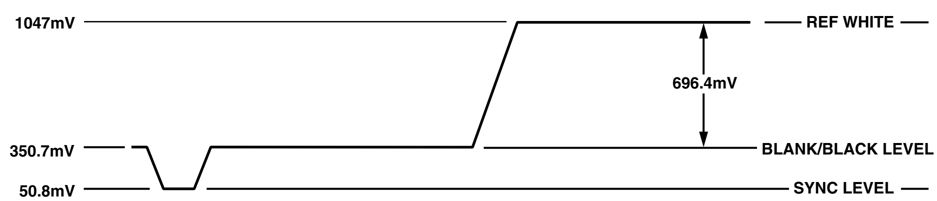


Figure 70. PAL Luma Video Levels

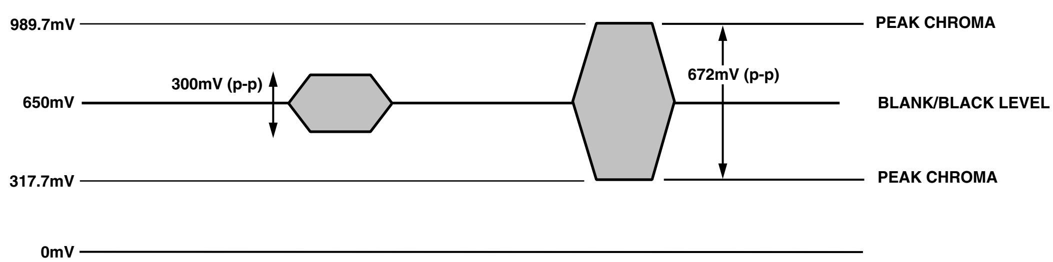


Figure 71. PAL Chroma Video Levels

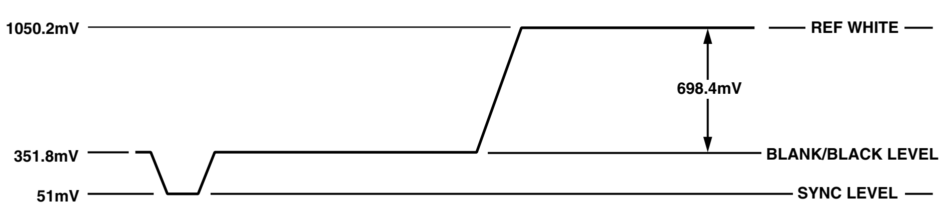


Figure 72. PAL RGB Video Levels

UV WAVEFORMS

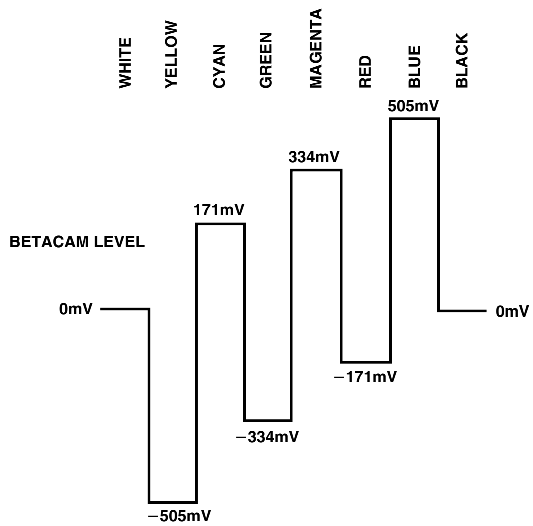


Figure 73. NTSC 100% Color Bars, No Pedestal U Levels

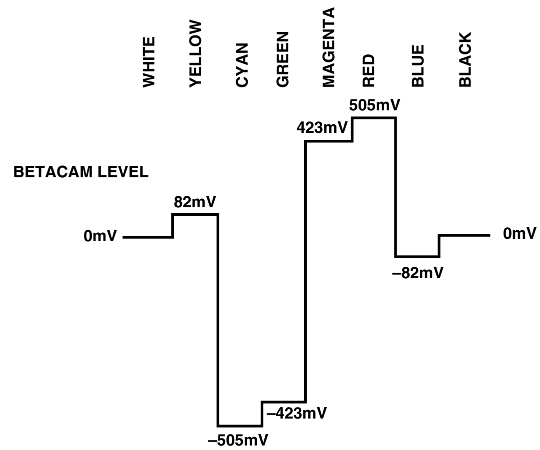


Figure 76. NTSC 100% Color Bars, No Pedestal V Levels

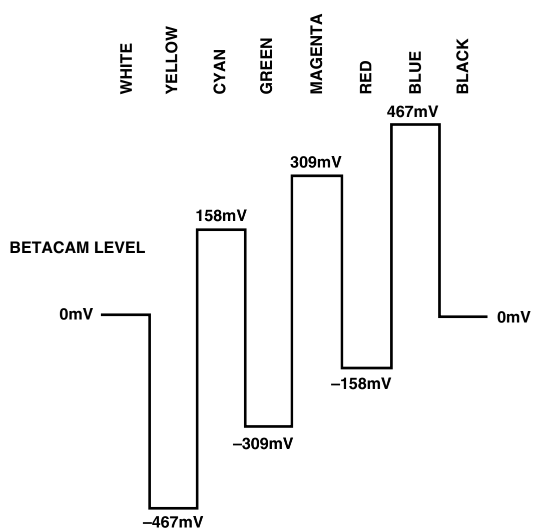


Figure 74. NTSC 100% Color Bars with Pedestal U Levels

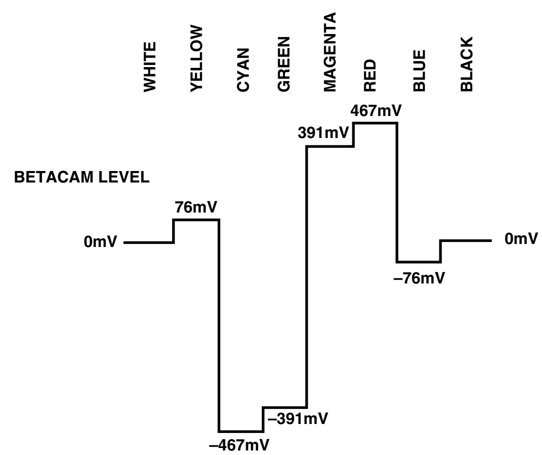


Figure 77. NTSC 100% Color Bars with Pedestal V Levels

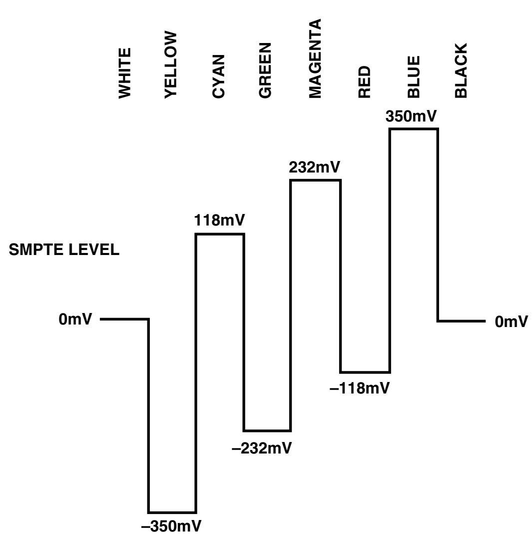


Figure 75. PAL 100% Color Bars, U Levels

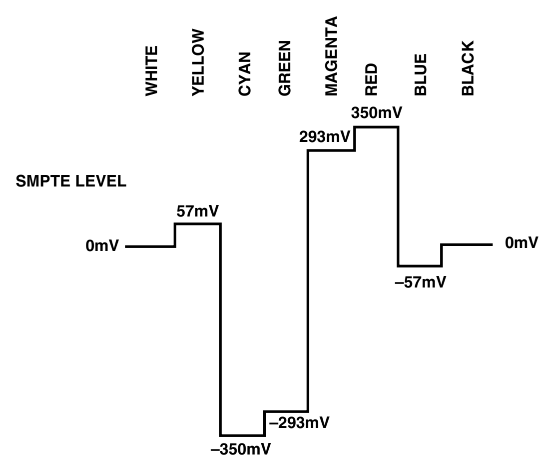


Figure 78. PAL 100% Color Bars, V Levels

APPENDIX 7

OPTIONAL OUTPUT FILTER

If an output filter is required for the CVBS, Y, UV, Chroma and RGB outputs of the ADV7170/ADV7171, the filter shown in Figure 79 can be used. Plots of the filter characteristics are shown in Figure 80. An Output Filter is not required if the outputs of the ADV7170/ADV7171 are connected to most analog monitors or analog TVs, however if the output signals are applied to a system where sampling is used (e.g., Digital TVs), then a filter is required to prevent aliasing.

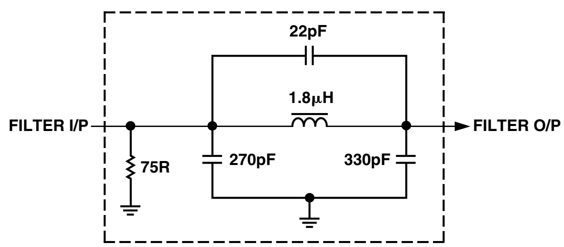


Figure 79. Output Filter

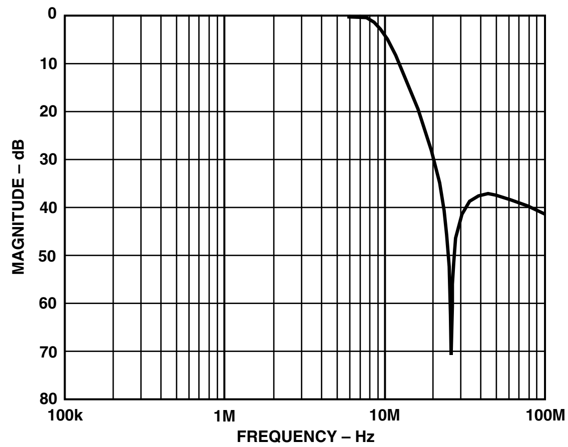


Figure 80. Output Filter Plot

APPENDIX 8

OPTIONAL DAC BUFFERING

When external buffering is needed of the ADV7170/ADV7171 DAC outputs, the configuration in Figure 81 is recommended. This configuration shows the DAC outputs running at half (18 mA) their full current (36 mA) capability. This will allow the ADV7170/ADV7171 to dissipate less power; the analog current is reduced by 50% with a R_{SET} of 300 Ω and a R_{LOAD} of 75 Ω. This mode is recommended for 3.3 V operation as optimum performance is obtained from the DAC outputs at 18 mA with a V_{AA} of 3.3 V. This buffer also adds extra isolation on the video outputs (see buffer circuit in Figure 82).

When calculating absolute output full-scale current and voltage, use the following equations:

$$V_{OUT} = I_{OUT} \times R_{LOAD}$$

$$I_{OUT} = \frac{(V_{REF} \times K)}{R_{SET}}$$

$$K = 4.2146 \text{ constant}, V_{REF} = 1.235 \text{ V}$$

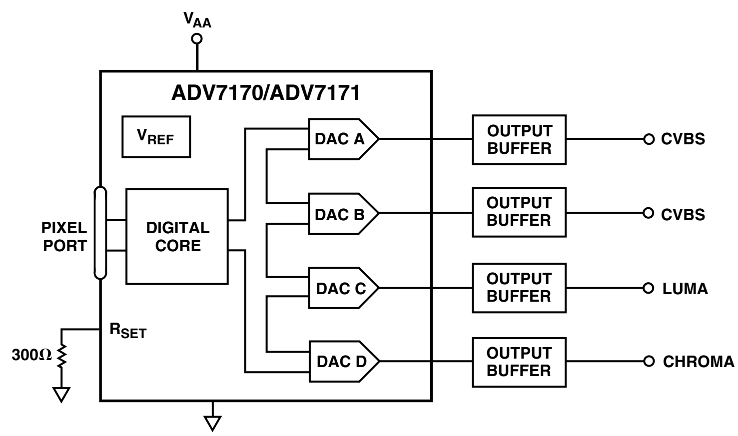


Figure 81. Output DAC Buffering Configuration

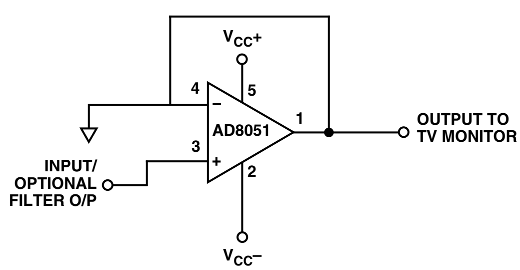


Figure 82. Recommended Output DAC Buffer

APPENDIX 9

RECOMMENDED REGISTER VALUES

The ADV7170/ADV7171 registers can be set depending on the user standard required.

The following examples give the various register formats for several video standards.

In each case the output is set to composite o/p with all DACs powered up and with the $\overline{\text{BLANK}}$ input control disabled. Additionally, the burst and color information are enabled on the output and the internal color bar generator is switched off. In the examples shown, the timing mode is set to Mode 0 in slave format. TR02–TR00 of the Timing Register 0 control the timing modes. For a detailed explanation of each bit in the command registers, please turn to the Register Programming section of the data sheet. TR07 should be toggled after setting up a new timing mode. Timing Register 1 provides additional control over the position and duration of the timing signals. In the examples, this register is programmed in default mode.

PAL B, D, G, H, I (F_{SC} = 4.43361875 MHz)

Address		Data
00Hex	Mode Register 0	05Hex
01Hex	Mode Register 1	00Hex
02Hex	Mode Register 2	00Hex
03Hex	Mode Register 3	00Hex
04Hex	Mode Register 4	00Hex
07Hex	Timing Register 0	00Hex
08Hex	Timing Register 1	00Hex
09Hex	Subcarrier Frequency Register 0	CBHex
0AHex	Subcarrier Frequency Register 1	8AHex
0BHex	Subcarrier Frequency Register 2	09Hex
0CHex	Subcarrier Frequency Register 3	2AHex
0DHex	Subcarrier Phase Register	00Hex
0EHex	Closed Captioning Ext Register 0	00Hex
0FHex	Closed Captioning Ext Register 1	00Hex
10Hex	Closed Captioning Register 0	00Hex
11Hex	Closed Captioning Register 1	00Hex
12Hex	Pedestal Control Register 0	00Hex
13Hex	Pedestal Control Register 1	00Hex
14Hex	Pedestal Control Register 2	00Hex
15Hex	Pedestal Control Register 3	00Hex
16Hex	CGMS_WSS Reg 0	00Hex
17Hex	CGMS_WSS Reg 1	00Hex
18Hex	CGMS_WSS Reg 2	00Hex
19Hex	Teletext Request Control Register	00Hex

PAL M (F_{SC} = 3.57561149 MHz)

Address		Data
00Hex	Mode Register 0	02Hex
01Hex	Mode Register 1	00Hex
02Hex	Mode Register 2	00Hex
03Hex	Mode Register 3	00Hex
04Hex	Mode Register 4	00Hex
07Hex	Timing Register 0	00Hex
08Hex	Timing Register 1	00Hex
09Hex	Subcarrier Frequency Register 0	A3Hex
0AHex	Subcarrier Frequency Register 1	EFHex
0BHex	Subcarrier Frequency Register 2	E6Hex
0CHex	Subcarrier Frequency Register 3	21Hex
0DHex	Subcarrier Phase Register	00Hex
0EHex	Closed Captioning Ext Register 0	00Hex
0FHex	Closed Captioning Ext Register 1	00Hex
10Hex	Closed Captioning Register 0	00Hex
11Hex	Closed Captioning Register 1	00Hex
12Hex	Pedestal Control Register 0	00Hex
13Hex	Pedestal Control Register 1	00Hex
14Hex	Pedestal Control Register 2	00Hex
15Hex	Pedestal Control Register 3	00Hex
16Hex	CGMS_WSS Reg 0	00Hex
17Hex	CGMS_WSS Reg 1	00Hex
18Hex	CGMS_WSS Reg 2	00Hex
19Hex	Teletext Request Control Register	00Hex

PAL N (F_{SC} = 4.43361875 MHz)

Address		Data
00Hex	Mode Register 0	05Hex
01Hex	Mode Register 1	00Hex
02Hex	Mode Register 2	00Hex
03Hex	Mode Register 3	00Hex
04Hex	Mode Register 4	00Hex
07Hex	Timing Register 0	00Hex
08Hex	Timing Register 1	00Hex
09Hex	Subcarrier Frequency Register 0	CBHex
0AHex	Subcarrier Frequency Register 1	8AHex
0BHex	Subcarrier Frequency Register 2	09Hex
0CHex	Subcarrier Frequency Register 3	2AHex
0DHex	Subcarrier Phase Register	00Hex
0EHex	Closed Captioning Ext Register 0	00Hex
0FHex	Closed Captioning Ext Register 1	00Hex
10Hex	Closed Captioning Register 0	00Hex
11Hex	Closed Captioning Register 1	00Hex
12Hex	Pedestal Control Register 0	00Hex
13Hex	Pedestal Control Register 1	00Hex
14Hex	Pedestal Control Register 2	00Hex
15Hex	Pedestal Control Register 3	00Hex
16Hex	CGMS_WSS Reg 0	00Hex
17Hex	CGMS_WSS Reg 1	00Hex
18Hex	CGMS_WSS Reg 2	00Hex
19Hex	Teletext Request Control Register	00Hex

PAL-60 (F_{SC} = 4.43361875 MHz)

Address		Data
00Hex	Mode Register 0	04Hex
01Hex	Mode Register 1	00Hex
02Hex	Mode Register 2	00Hex
03Hex	Mode Register 3	00Hex
04Hex	Mode Register 4	00Hex
07Hex	Timing Register 0	00Hex
08Hex	Timing Register 1	00Hex
09Hex	Subcarrier Frequency Register 0	CBHex
0AHex	Subcarrier Frequency Register 1	8AHex
0BHex	Subcarrier Frequency Register 2	09Hex
0CHex	Subcarrier Frequency Register 3	2AHex
0DHex	Subcarrier Phase Register	00Hex
0EHex	Closed Captioning Ext Register 0	00Hex
0FHex	Closed Captioning Ext Register 1	00Hex
10Hex	Closed Captioning Register 0	00Hex
11Hex	Closed Captioning Register 1	00Hex
12Hex	Pedestal Control Register 0	00Hex
13Hex	Pedestal Control Register 1	00Hex

PAL-60 (Continued) (F_{SC} = 4.43361875 MHz)

Address		Data
14Hex	Pedestal Control Register 2	00Hex
15Hex	Pedestal Control Register 3	00Hex
16Hex	CGMS_WSS Reg 0	00Hex
17Hex	CGMS_WSS Reg 1	00Hex
18Hex	CGMS_WSS Reg 2	00Hex
19Hex	Teletext Request Control Register	00Hex

Power-Up Reset Values

NTSC (F_{SC} = 3.5795454 MHz)

Address		Data
00Hex	Mode Register 0	00Hex
01Hex	Mode Register 1	58Hex
02Hex	Mode Register 2	00Hex
03Hex	Mode Register 3	00Hex
04Hex	Mode Register 4	10Hex
07Hex	Timing Register 0	00Hex
08Hex	Timing Register 1	00Hex
09Hex	Subcarrier Frequency Register 0	16Hex
0AHex	Subcarrier Frequency Register 1	7CHex
0BHex	Subcarrier Frequency Register 2	F0Hex
0CHex	Subcarrier Frequency Register 3	21Hex
0DHex	Subcarrier Phase Register	00Hex
0EHex	Closed Captioning Ext Register 0	00Hex
0FHex	Closed Captioning Ext Register 1	00Hex
10Hex	Closed Captioning Register 0	00Hex
11Hex	Closed Captioning Register 1	00Hex
12Hex	Pedestal Control Register 0	00Hex
13Hex	Pedestal Control Register 1	00Hex
14Hex	Pedestal Control Register 2	00Hex
15Hex	Pedestal Control Register 3	00Hex
16Hex	CGMS_WSS Reg 0	00Hex
17Hex	CGMS_WSS Reg 1	00Hex
18Hex	CGMS_WSS Reg 2	00Hex
19Hex	Teletext Request Control Register	00Hex

APPENDIX 10

OUTPUT WAVEFORMS

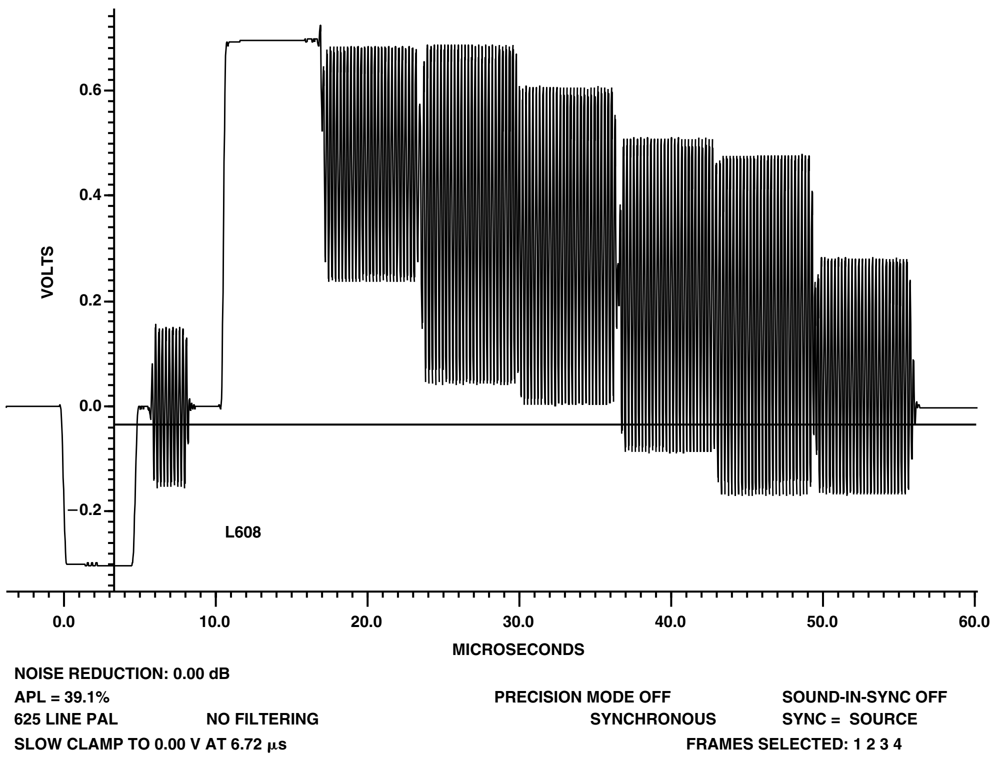


Figure 83. 100/0/75/0 PAL Color Bars

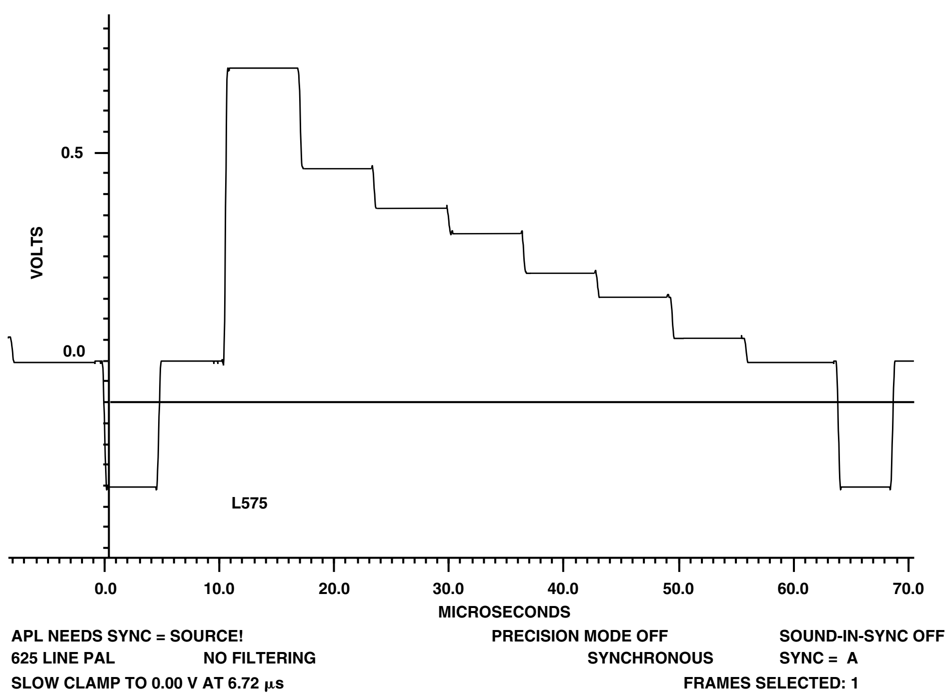


Figure 84. 100/0/75/0 PAL Color Bars Luminance

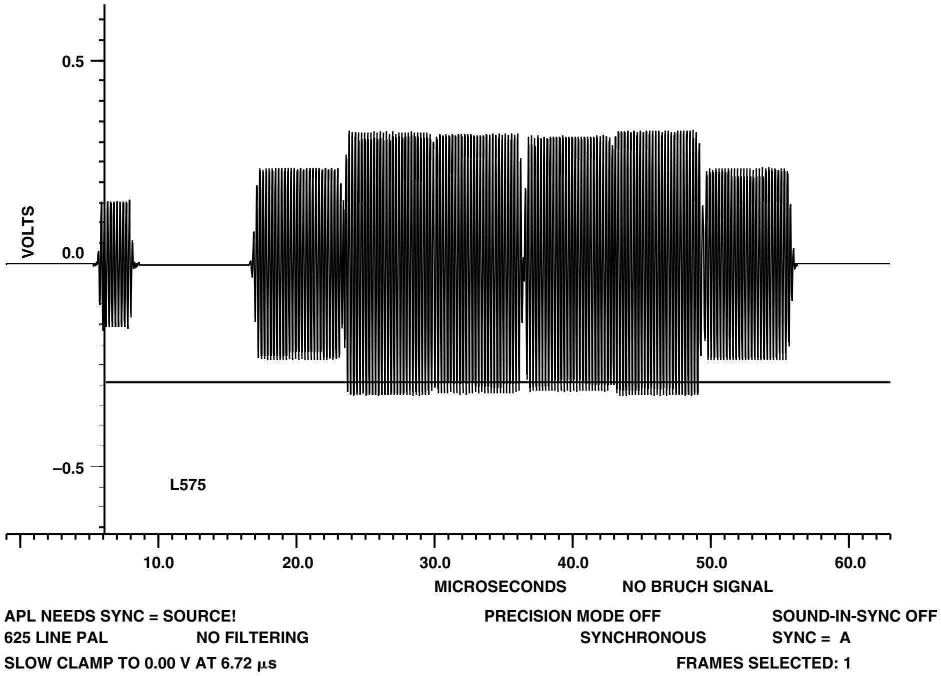


Figure 85. 100/0/75/0 PAL Color Bars Chrominance

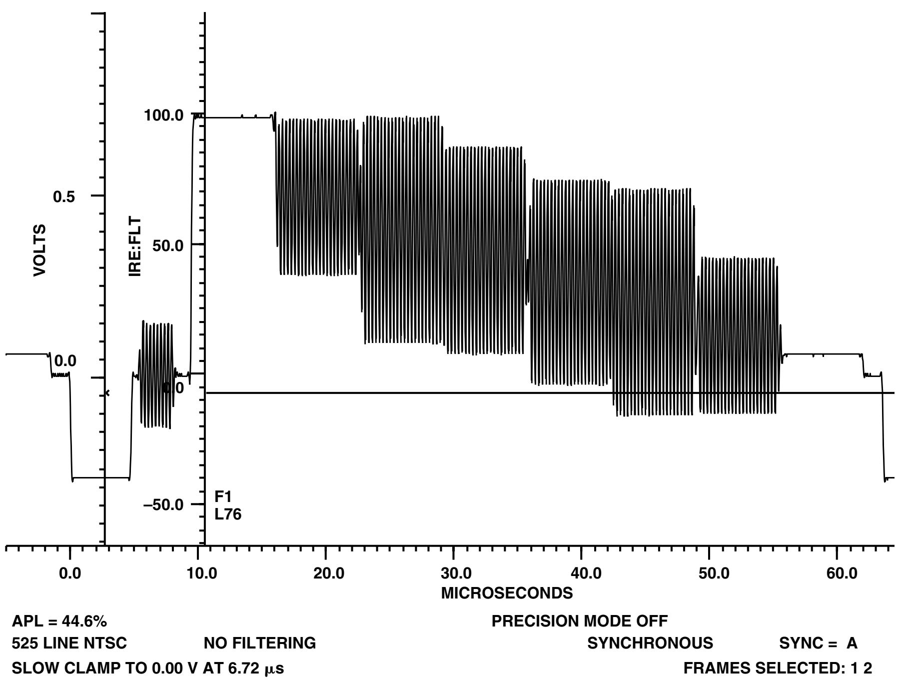


Figure 86. 100/7.5/75/7.5 NTSC Color Bars

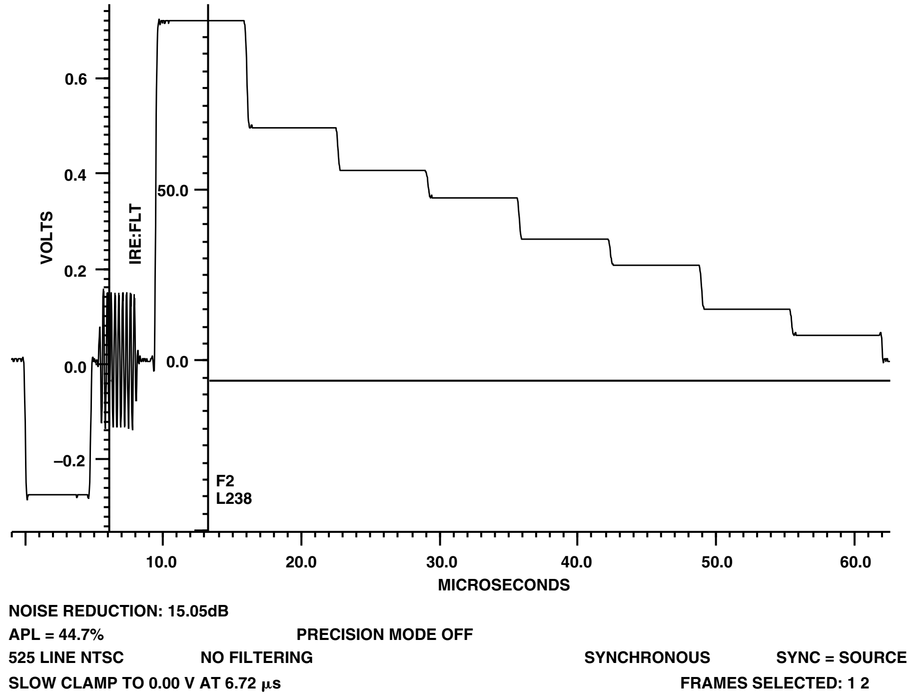


Figure 87. 100/7.5/75/7.5 NTSC Color Bars Luminance

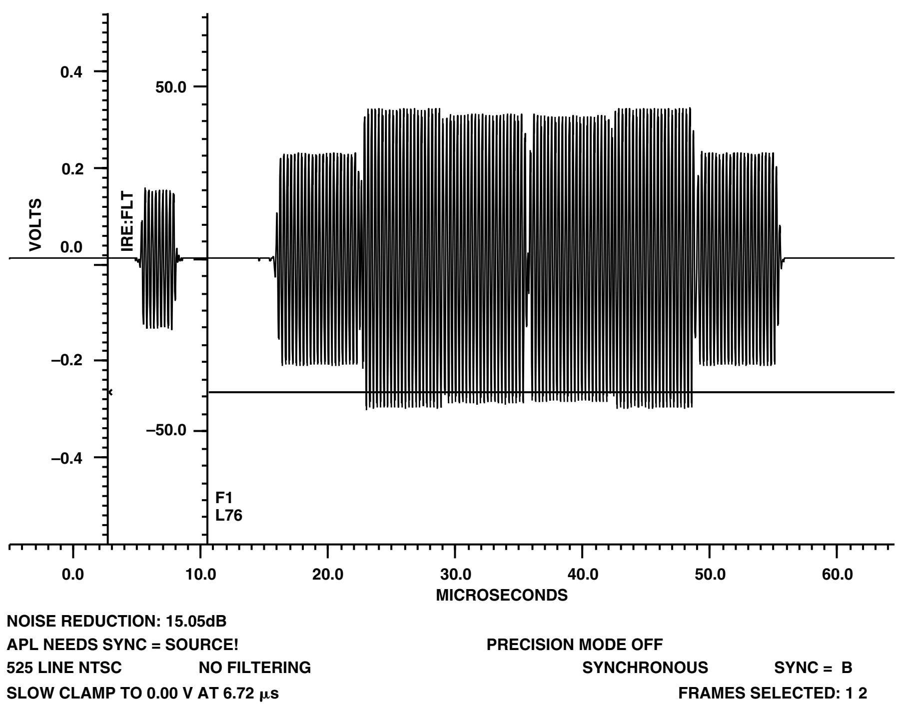


Figure 88. 100/7.5/75/7.5 NTSC Color Bars Chrominance

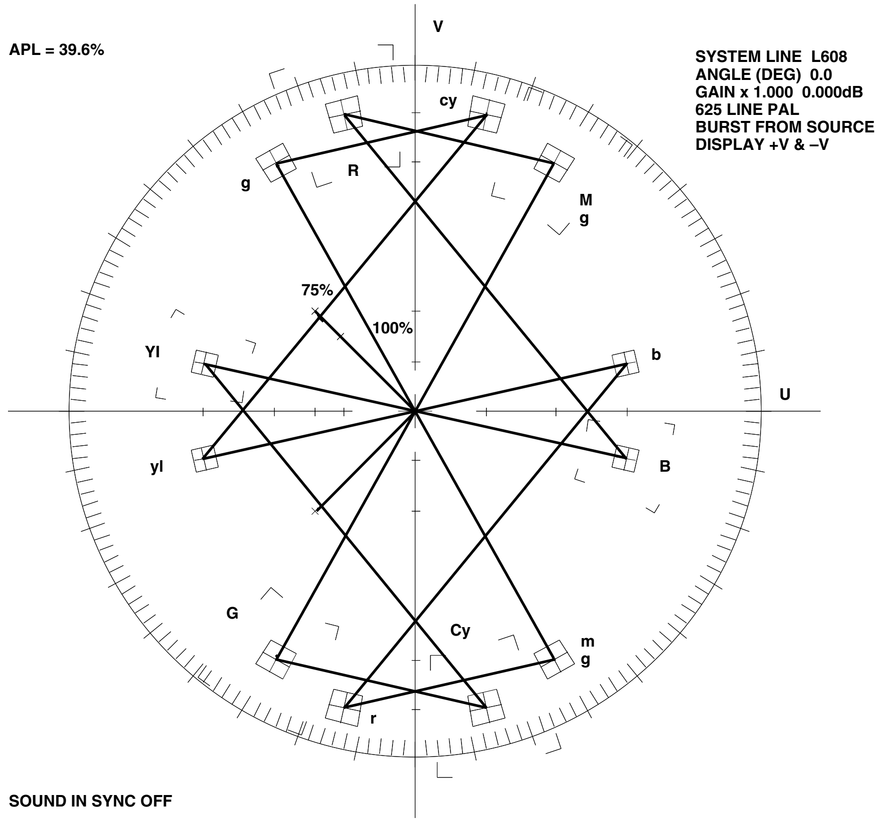


Figure 89. PAL Vector Plot

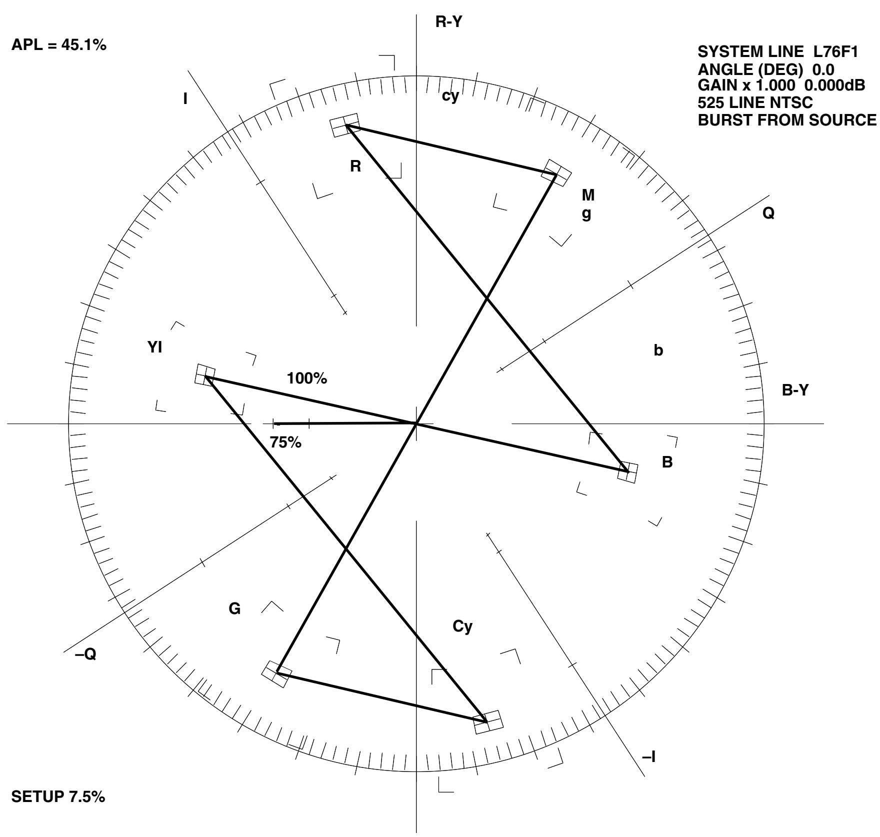


Figure 90. NTSC Vector Plot

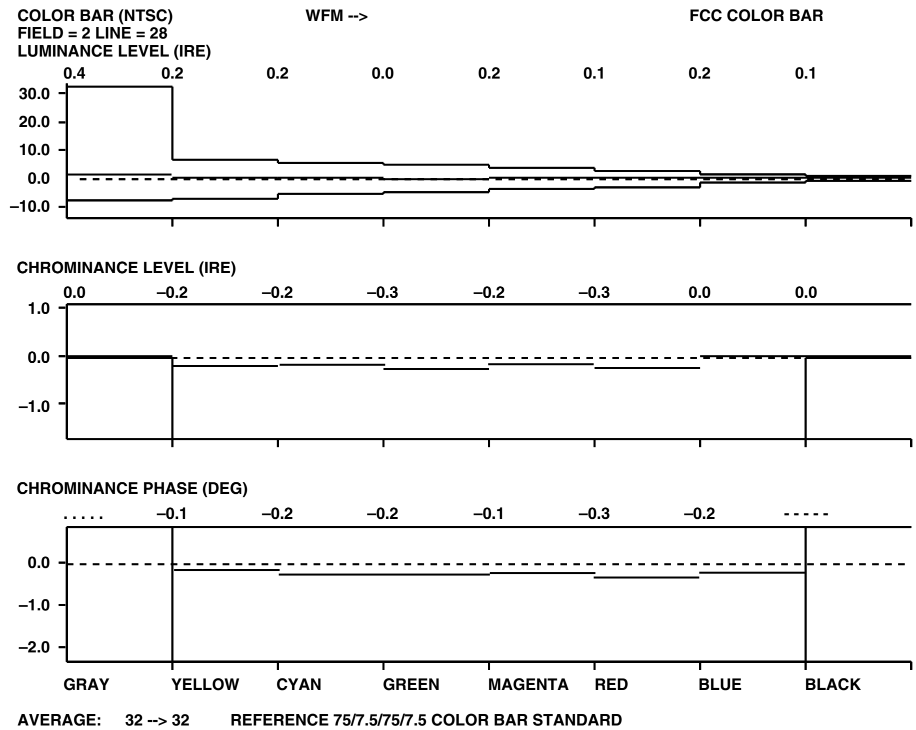


Figure 91. NTSC Color Bar Measurement

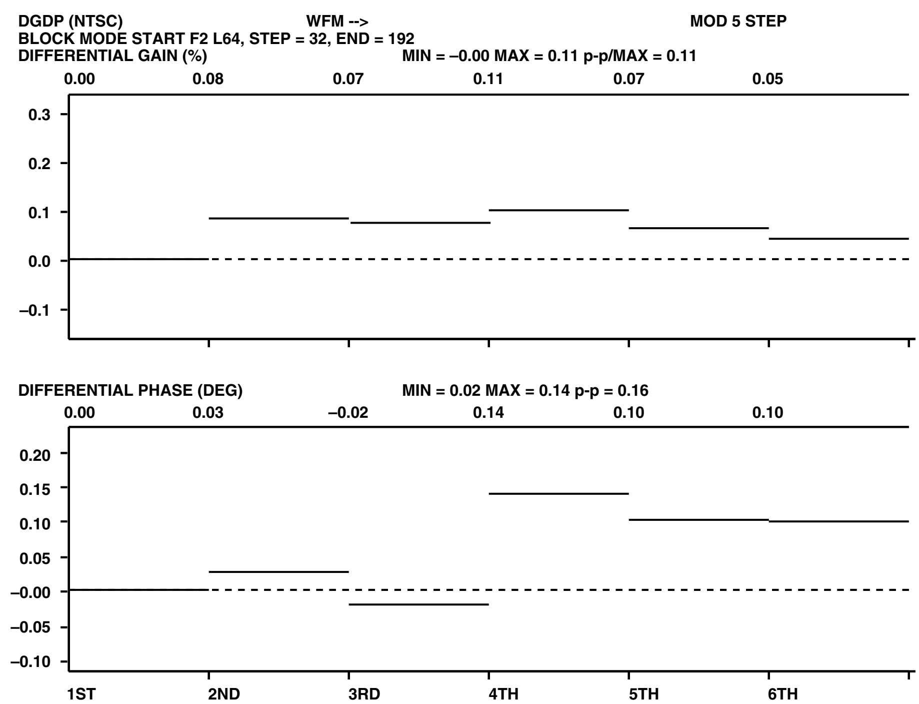


Figure 92. NTSC Differential Gain and Phase Measurement

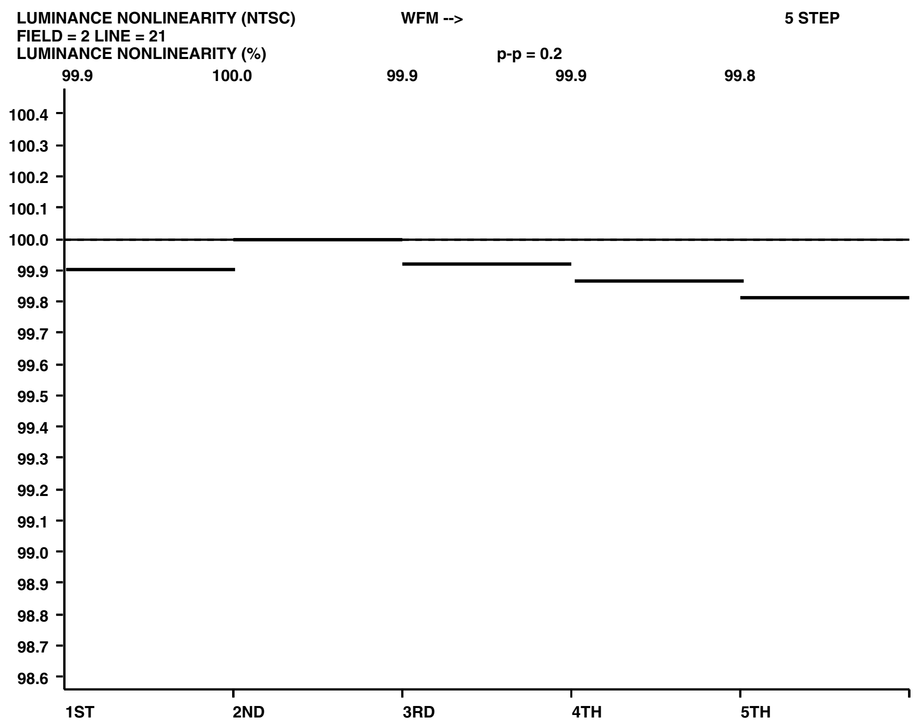


Figure 93. NTSC Luminance Nonlinearity Measurement

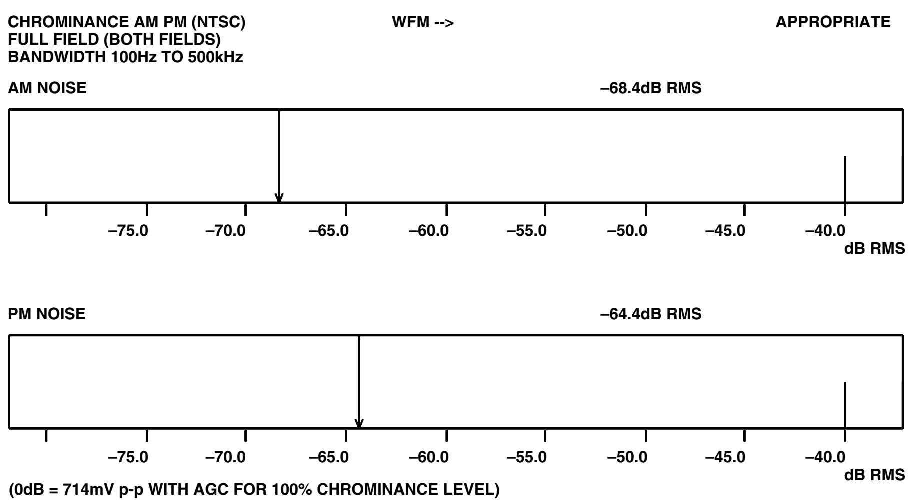


Figure 94. NTSC AMPM Noise Measurement

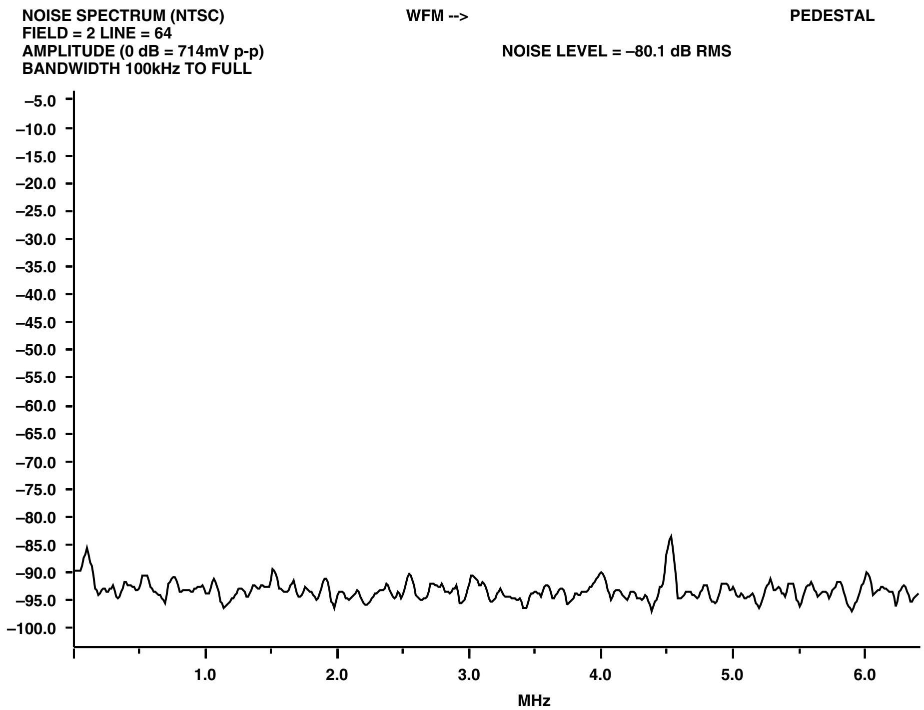


Figure 95. NTSC SNR Pedestal Measurement

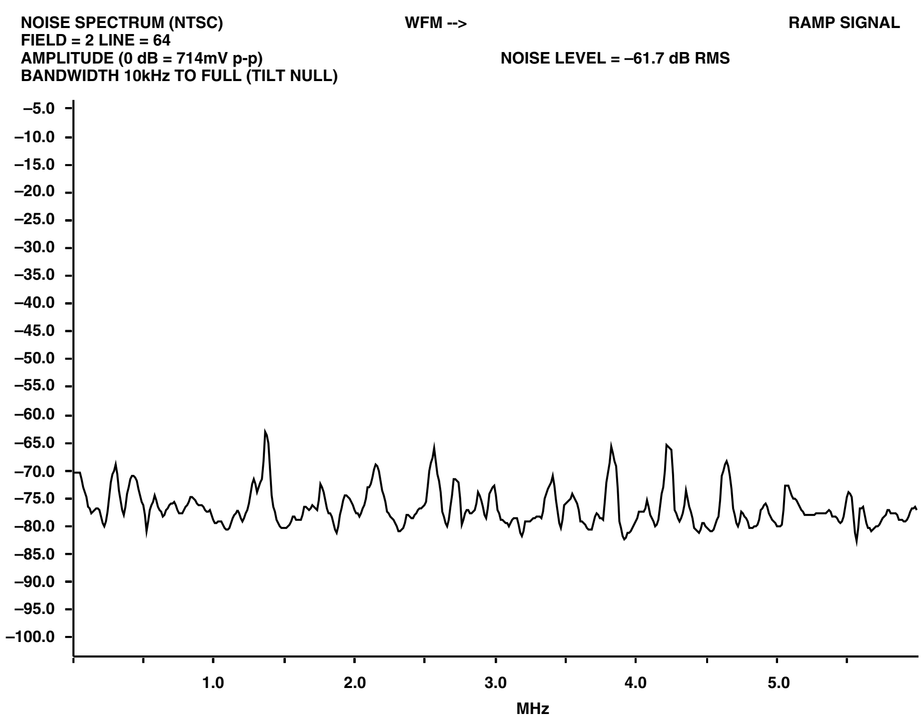


Figure 96. NTSC SNR Ramp Measurement

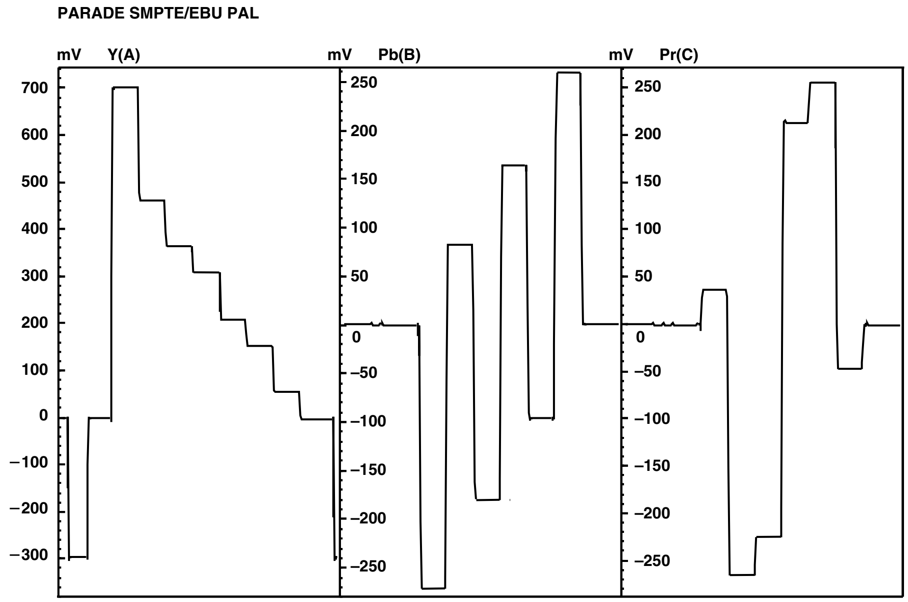


Figure 97. PAL YUV Parade Plot

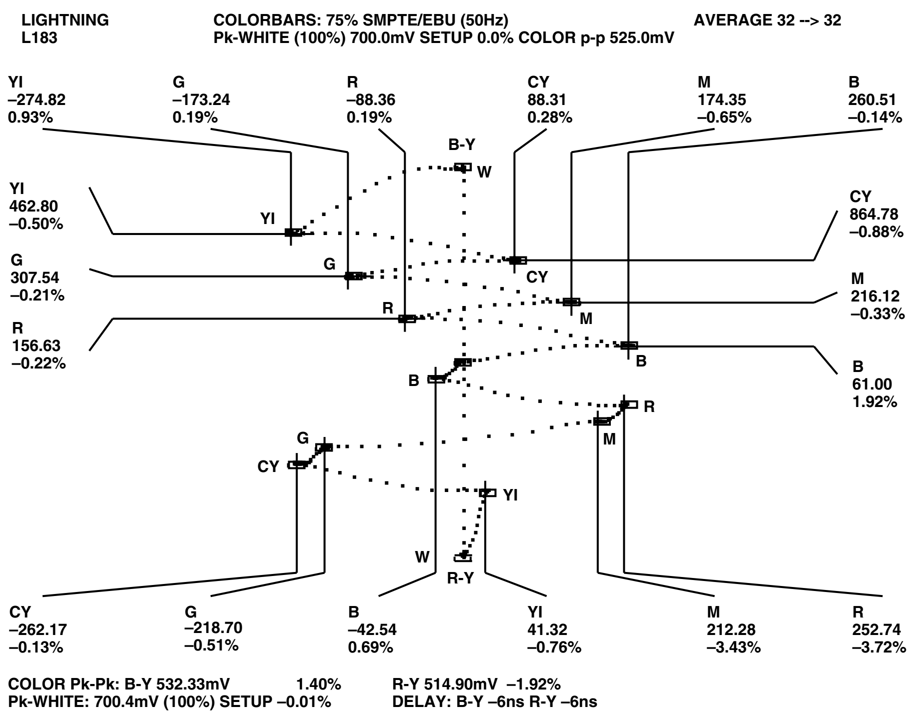


Figure 98. PAL YUV Lighting Plot

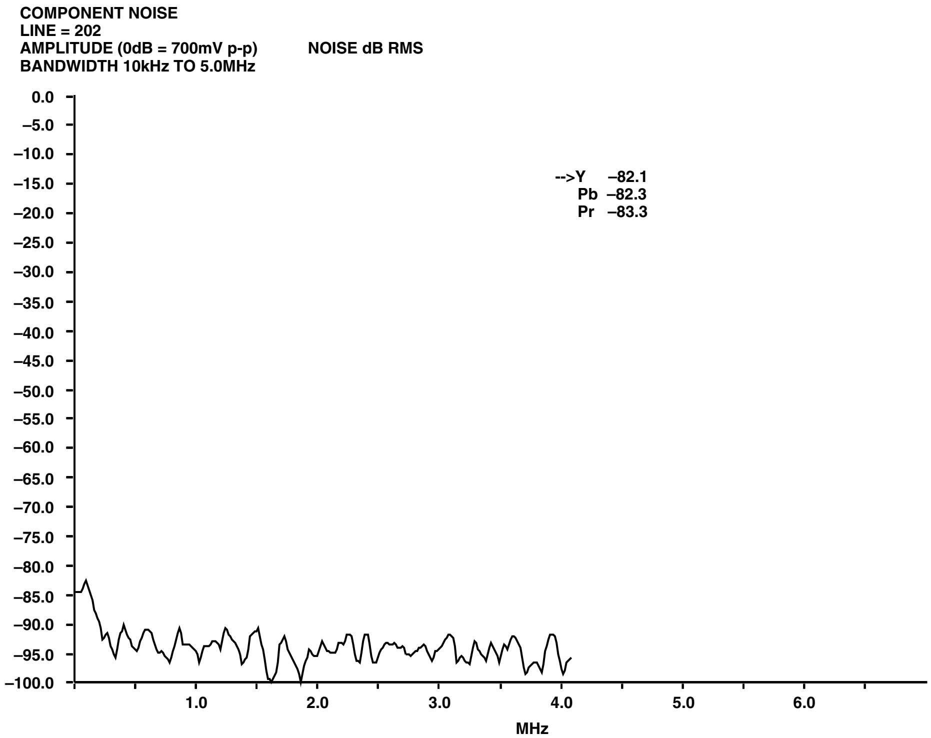


Figure 99. PAL YUV SNR Plot

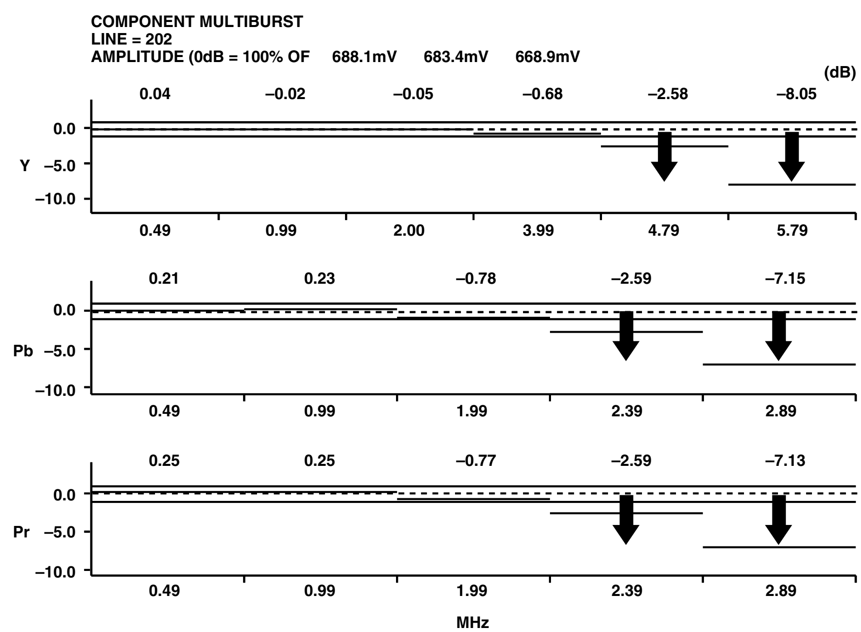


Figure 100. PAL YUV Multiburst Response

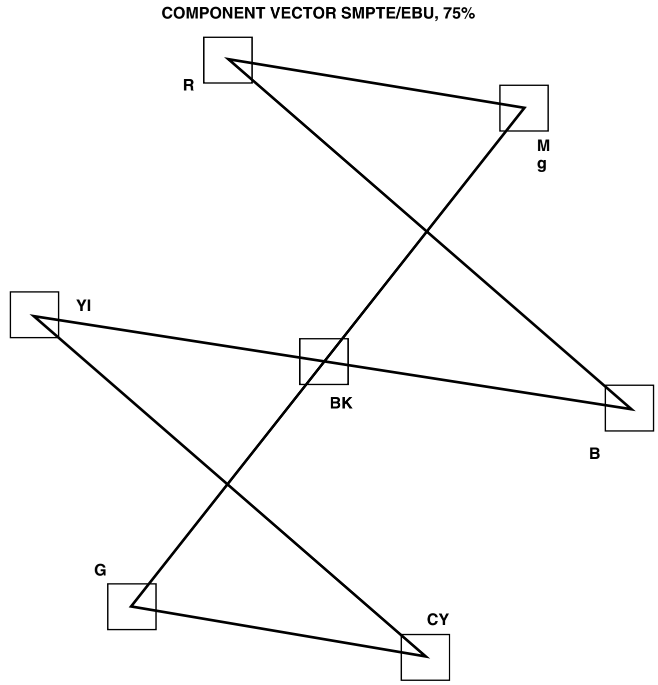


Figure 101. PAL YUV Vector Plot

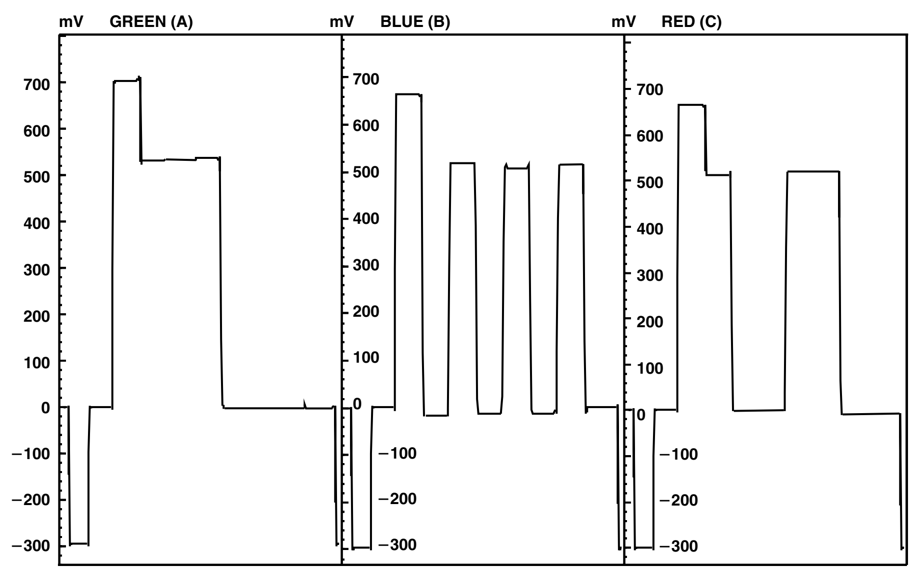


Figure 102. PAL RGB Waveforms

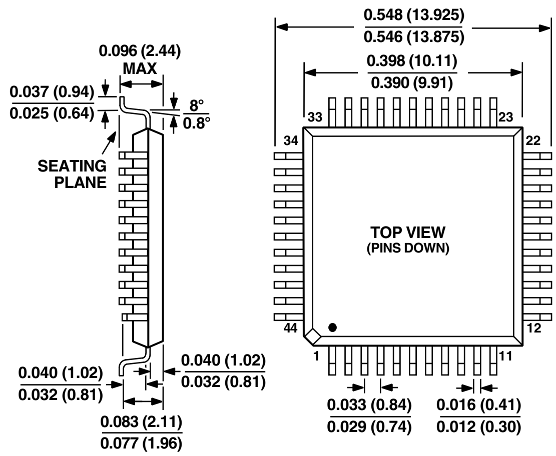
INDEX

Contents **Page No.**

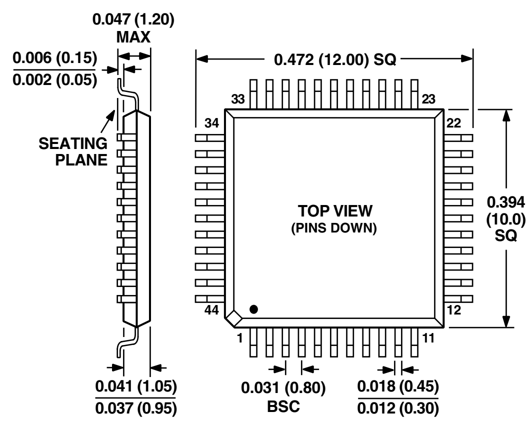
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

44-Lead Plastic Quad Flatpack (MQFP) (S-44)



44-Lead Thin Plastic Quad Flatpack (TQFP) (SU-44)



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