1 MHz - 3 GHz VGA with 60dB Gain Control Range

Preliminary Technical Data

ADL5330

FEATURES

Voltage-Controlled Amplifier/Attenuator
Operating Frequency 1 MHz to 3 GHz
Optimized for Controlling Output Power
High Linearity: OIP3 31 dBm @ 900 MHz
Output Noise Floor -150 dBm/Hz @ 900 MHz
Fully-Balanced Differential Signal Path
Differential Input at 50 Ω
Wide Gain-Control Range: -34 dB to +22 dB @ 900 MHz
Linear-in-dB Gain Control Function, 20 mV/dB
Single Supply 4.75 – 6 V

APPLICATIONS

Output Power Control for Wireless Infrastructure

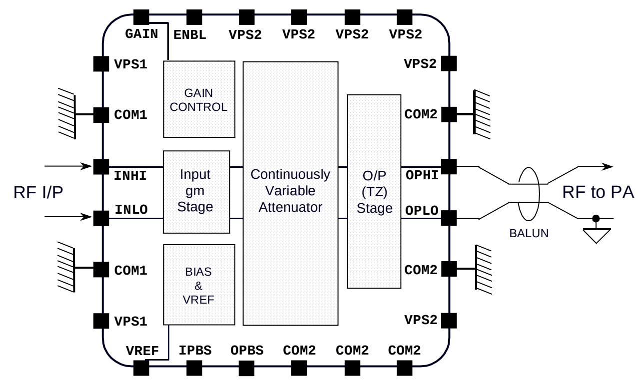

Figure 1. Functional Block Diagram

PRODUCT DESCRIPTION

The ADL5330 is a high-performance voltage-controlled variable-gain amplifier/attenuator, for use up to 3 GHz. The signal path is fully differential; the balanced structure minimizes distortion, and reduces the risk of spurious feed-forward at low gains and high frequencies due to substrate coupling. While operation between a balanced source and load is recommended, a single-sided input is internally converted to differential from. The input impedance is 50-Ω from **INHI** to **INLO**. The outputs will usually be coupled into a 50-Ω grounded load via a 1:1 balun. However, the output pins, **OPHI** and **OPLO**, may also be used separately, with some noise degradation. A single supply of 4.75 to 6 V is required.

With a 2140 MHz W-CDMA 3GPP forward path signal, the ADL5330 is capable of producing greater than –3 dBm output power while maintaining ACPR greater than 55 dB, and an output noise floor less than -144 dBm/Hz.

Three cascaded sections are used. The 50-Ω input system converts the applied voltage to a pair of differential currents with high linearity and good common rejection if driven by a single-sided source. The signal currents are then applied to a proprietary voltage-controlled attenuator, which provides precise definition of the overall gain, under the control of the Linear-in-dB interface. Pin **GAIN** accepts a voltage from 0 V at minimum gain to 1.4 V at full gain. The scaling factor is 20 mV/dB. Optional external control of the input-stage and/or output-stage biasing is provided using pins **IPBS** and **OPBS** respectively.

The output of the high-accuracy wideband attenuator is applied to a differential trans-impedance output stage. Higher output power is attainable at the lower operating frequencies by raising the supply voltage to 6 V. When powered-down by a logic LO input on the **ENBL** pin, the current consumption is < TBD μA.

The ADL5330 is available in a 24-lead (4 x 4mm) CSP package and is specified for operation from ambient temperatures of −40°C to +85°C.

Multiple Patents Pending

Rev. PrK

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ADL5330 SPECIFICATIONS

Table 1. V_S = 5 V; T_A = 25°C; 800 MHz < *f* < 2.2GHz.1:1 balun at input and output for single-ended 50 Ω match

Parameter	Conditions	Min	Typ	Max	Unit
General					
Usable Frequency Range		0.001		3	GHz
Nominal Input Impedance	via 1:1 Single-Sided to Differential Balun		50		Ω
Nominal Output Impedance	via 1:1 Differential to Single-Sided Balun		50		Ω
100 MHz					
Gain Control Span	+/-3 dB Gain Law Conformance		58		dB
Max Gain	V_{GAIN} = 1.4 V		+23		dB
Min Gain	V_{GAIN} = 0.1 V		-35		dB
Gain Control Slope			21		mV/dB
Input Compression Point	V_{GAIN} = 1.3 V		+2		dBm
Output Compression Point - P1dB	V_{GAIN} = 1.3 V		+22		dBm
Third-Order Intercept - OIP3	V_{GAIN} = 1.3 V		+36		dBm
900 MHz					
Gain Control Span	+/-3 dB Gain Law Conformance		52		dB
Max Gain	V_{GAIN} = 1.4 V		22		dB
Min Gain	V_{GAIN} = 0.1 V		-34		dB
Gain Control Slope			20		mV/dB
Input Compression Point	V_{GAIN} = 1.3 V		+3		dBm
Output Compression Point - P1dB	V_{GAIN} = 1.3 V		+22		dBm
Third-Order Intercept - OIP3	V_{GAIN} = 1.3 V		+31		dBm
Output Noise Floor	20 MHz Carrier Offset, V_{GAIN} = 1.3 V, Pout = -2 dBm		-144		dBm/Hz
1900 MHz					
Gain Control Span	+/-3 dB Gain Law Conformance		47		dB
Max Gain	V_{GAIN} = 1.4 V		19		dB
Min Gain	V_{GAIN} = 0.5 V		-27		dB
Gain Control Slope			18		mV/dB
Input Compression Point	V_{GAIN} = 1.3 V		+1		dBm
Output Compression Point - P1dB	V_{GAIN} = 1.3 V		+17		dBm
Third-Order Intercept - OIP3	V_{GAIN} = 1.3 V		+24		dBm
Output Noise Floor	20 MHz Carrier Offset, V_{GAIN} = 1.3 V, Pout = -7 dBm		-148		dBm/Hz
2200 MHz					
Gain Control Span	+/-3 dB Gain Law Conformance		48		dB
Max Gain	V_{GAIN} = 1.4 V		17		dB
Min Gain	V_{GAIN} = 0.5 V		-31		dB
Gain Control Slope			17		mV/dB
Input Compression Point	V_{GAIN} = 1.3 V		+1		dBm
Output Compression Point - P1dB	V_{GAIN} = 1.3 V		+14		dBm
Third-Order Intercept - OIP3	V_{GAIN} = 1.3 V		+20		dBm
GAIN CONTROL INPUT	Pin **GAIN**				
Gain Control Voltage Range		0		1.4	V
Incremental Input Resistance	Pin **GAIN** to **COM1**	TBD			MΩ
Full-Scale Response Time	V_{GN} 0 - 1.6V, to within 0.25 dB of final gain		500		ns
POWER SUPPLIES	Pins **VPS1**, **VPS2**, **COM1**, **COM2**, **ENBL**				
Voltage		4.75	5	6	V
Current, Nominal Active	V_{GN} = 0 V		TBD		mA
	V_{GN} = 1.4 V		240		mA
Current, Disabled	**ENBL** = LO		TBD	TBD	µA

Table 2. Pin Function Description

Pin	Name	Description
1,6	**VPS1**	Positive Supply for input stage. Nominally equal to 5 V
2,5	**COM1**	Common for input stage
3, 4	**INHI,INLO**	Differential inputs
7	**VREF**	Voltage reference output of 1.5 volts
8	**IPBS**	Input bias, normally no connection. This function is subject to change. PCB designs should include the possibility to connect a capacitor between Pin 8 and Pin 9.
9	**OPBS**	Output bias, normally no connection. This function is subject to change. PCB designs should include the possibility to connect a capacitor between Pin 8 and Pin 9.
10,11,12,14, 17	**COM2**	Common for output stage
13,18,19,20, 21,22	**VPS2**	Positive Supply for output stage. Nominally equal to 5 V
15	**OPLO**	Low side of differential output, bias to V_P with RF chokes
16	**OPHI**	High side of differential output, bias to V_P with RF chokes
23	**ENBL**	Device enable, apply logic high for normal operation. Enable Threshold = 1.6 V
24	**GAIN**	Gain-control voltage input. Nominal Range 0 to 1.4 V.

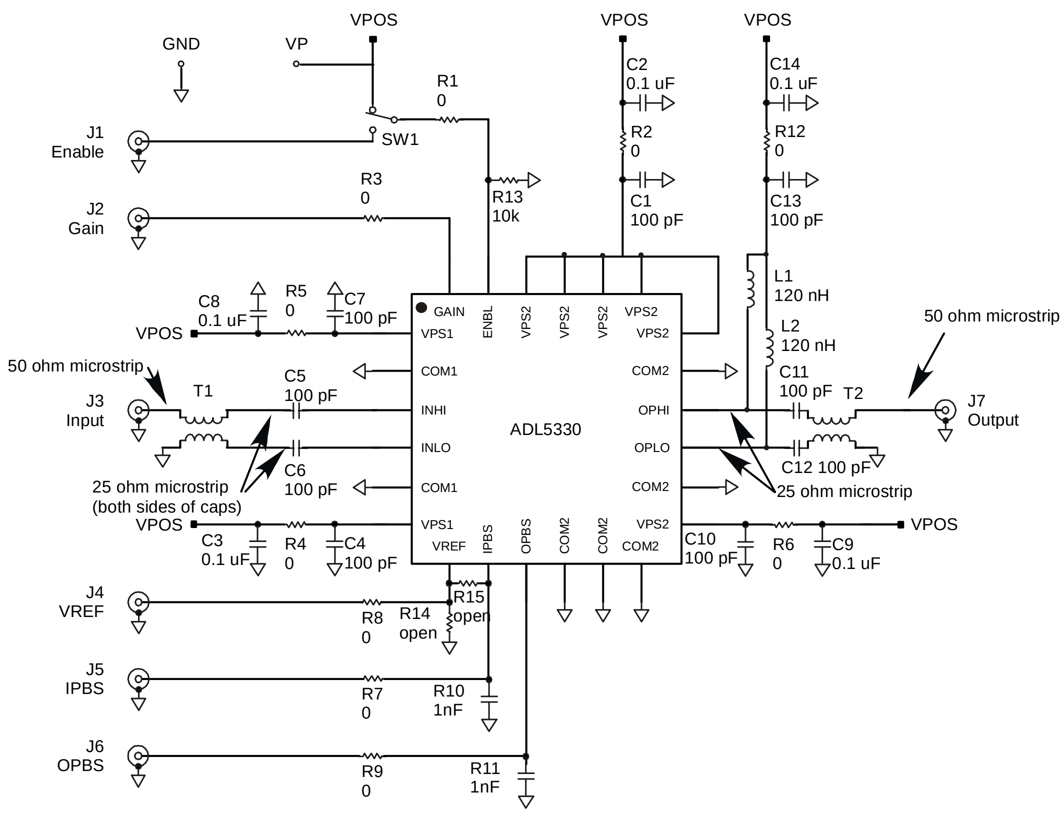


Figure 2. ADL5330 Evaluation Board Schematic

Typical Performance Characteristics

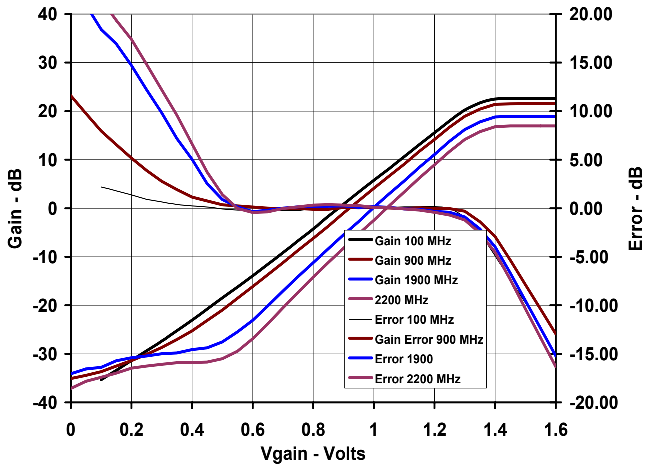


Figure 3. Gain and Gain Law Conformance vs. Vgain

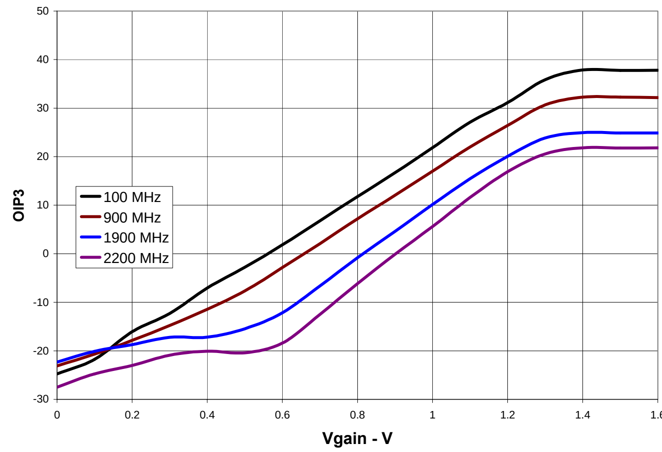


Figure 5. OIP3 vs. Gain

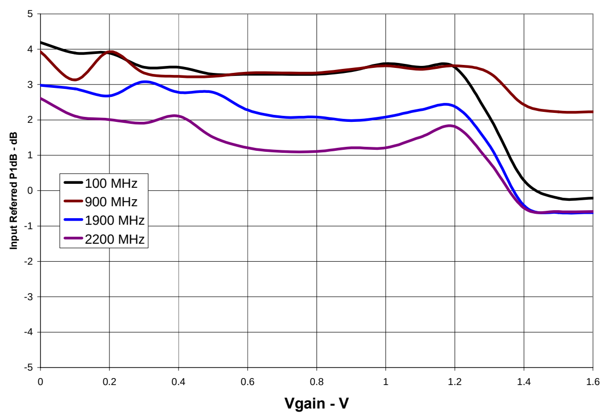


Figure 4. Input Referred Compression Point vs. Gain

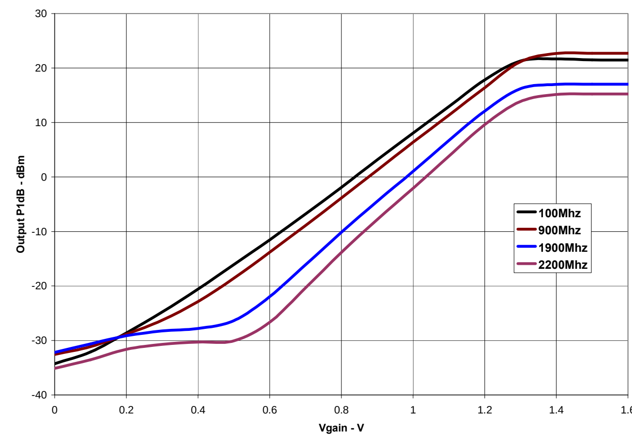


Figure 7. Output Referred Compression Point vs. Gain

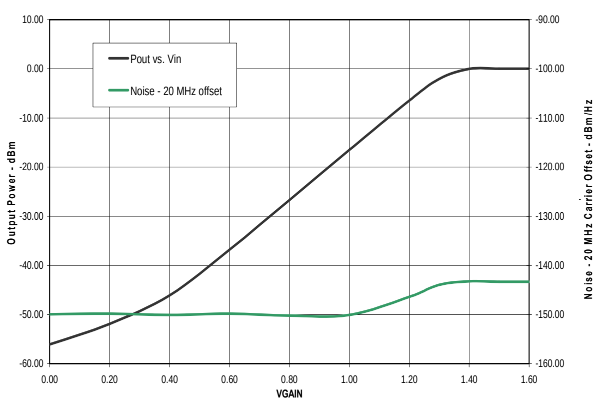


Figure 8. Pout and Noise Floor vs. Gain, 900 MHz. Pin = -21 dBm

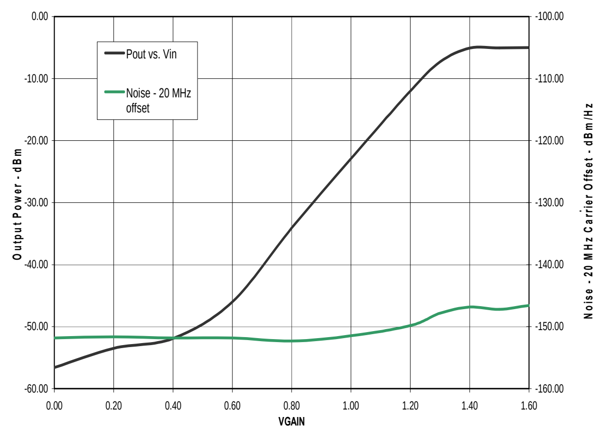
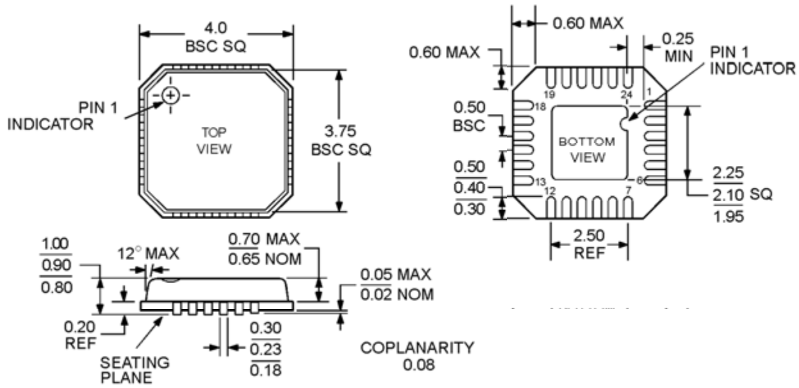


Figure 8. Pout and Noise Floor vs. Gain 1.9 GHz. Pin = -22 dBm

OUTLINE DIMENSIONS

24-Lead Chip Scale Package [LFCSP]
4 mm x 4 mm Body
(CP-24)

Dimensions shown in millimeters



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