Low Power, High Output Current, Quad Op Amp, Dual-Channel ADSL/ADSL2+ Line Driver

AD8392

FEATURES

- Four current feedback, high current amplifiers
- Ideal for use as ADSL/ADSL2+ dual-channel Central Office (CO) line drivers
- Low power operation
  - Power supply operation from ±5 V (+10 V) up to ±12 V (+24 V)
  - Less than 3 mA/Amp quiescent supply current for full power ADSL/ADSL2+ CO applications (20.4 dBm line power, 5.5 CF)
  - Three active power modes plus shutdown
- High output voltage and current drive
  - 400 mA peak output drive current
  - 44 V p-p differential output voltage
- Low distortion
  - –72 dBc @1 MHz second harmonic
  - –82 dBc @ 1 MHz third harmonic
- High speed: 900 V/µs differential slew rate
- Additional functionality of AD8392ACP
  - On-chip common-mode voltage generation

APPLICATIONS

- ADSL/ADSL2+ CO line drivers
- XDSL line drives
- High output current, low distortion amplifiers
- DAC output buffer

GENERAL DESCRIPTION

The AD8392 is comprised of four high output current, low power consumption, operational amplifiers. It is particularly well suited for the CO driver interface in digital subscriber line systems, such as ADSL and ADSL2+. The driver is capable of providing enough power to deliver 20.4 dBm to a line, while compensating for losses due to hybrid insertion and back termination resistors. In addition, the low distortion, fast slew rate, and high output current capability make the AD8392 ideal for many other applications, including medical, instrumentation, DAC output drivers, and other high peak current circuits.

The AD8392 is available in two thermally enhanced packages, a 28-lead TSSOP EP (AD8392ARE) and a 5 mm × 5 mm 32-lead LFCSP (AD8392ACP). Four bias modes are available via the use of two digital bits (PD1, PD0).

PIN CONFIGURATIONS

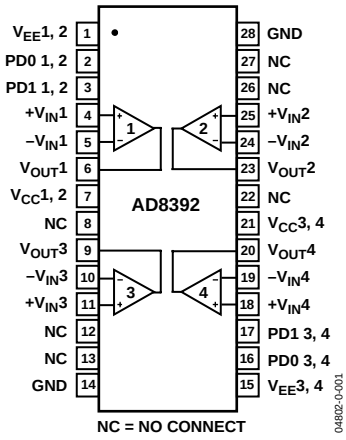


Figure 1. AD8392ARE, 28-Lead TSSOP/EP

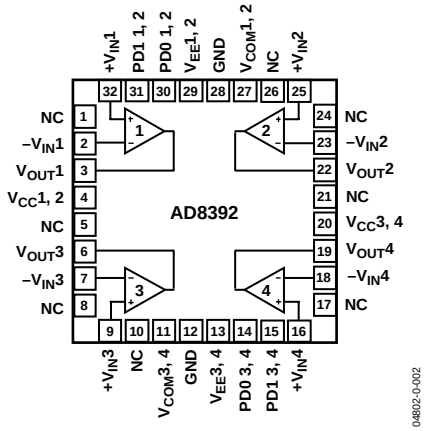


Figure 2. AD8392ACP, 32-Lead LFCSP 5 mm × 5 mm

Additionally, the AD8392ACP provides V_{COM} pins for on-chip common mode voltage generation.

The low power consumption, high output current, high output voltage swing, and robust thermal packaging enable the AD8392 to be used as the CO line drivers in ADSL and other xDSL systems, as well as other high current, single-ended or differential amplifier applications.

Rev. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.326.8703

TABLE OF CONTENTS

REVISION HISTORY

7/04—Revision 0: Initial Version

SPECIFICATIONS

V_S = ±12 V or +24 V, R_L = 100 Ω, G = +5, PD = (0, 0), T = 25°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE					
−3 dB Small Signal Bandwidth	30	40		MHz	V_{OUT} = 0.1 V p-p, R_F = 2 kΩ
−3 dB Large Signal Bandwidth	20	25		MHz	V_{OUT} = 4 V p-p, R_F = 2 kΩ
Peaking		0.05		dB	V_{OUT} = 0.1 V p-p, R_F = 2 kΩ
Slew Rate	850	900		V/µs	V_{OUT} = 20 V p-p, R_F = 2 kΩ
NOISE/DISTORTION PERFORMANCE					
Second Harmonic Distortion		−72		dBc	f_C = 1 MHz, V_{OUT} = 2 V p-p
Third Harmonic Distortion		−82		dBc	f_C = 1 MHz, V_{OUT} = 2 V p-p
Multitone Input Power Ratio		−70		dBc	26 kHz to 2.2 MHz, Z_{LINE} = 100 Ω Differential Load
Voltage Noise (RTI)		4.3		nV/√Hz	f = 10 kHz
+Input Current Noise		10		pA/√Hz	f = 10 kHz
−Input Current Noise		13		pA/√Hz	f = 10 kHz
INPUT CHARACTERISTICS					
RTI Offset Voltage	−5.0	±3.0	+5.0	mV	$V_{+IN} - V_{-IN}$
+Input Bias Current		5.0	10.0	µA	
−Input Bias Current		10.0	15.0	µA	
Input Resistance		400		kΩ	
Input Capacitance		2.0		pF	
Common-Mode Rejection Ratio	64	68		dB	$(\Delta V_{OS, DM (RTI)})/(\Delta V_{IN, CM})$
OUTPUT CHARACTERISTICS					
Differential Output Voltage Swing	42.0	44.0	46.0	V	ΔV_{OUT}
Single-Ended Output Voltage Swing	21.0	22.0	23.0	V	ΔV_{OUT}
Linear Output Current		400		mA	R_L = 10 Ω, f_C = 100 kHz
POWER SUPPLY					
Operating Range (Dual Supply)	±5		±12	V	
Operating Range (Single Supply)	10		24	V	
Total Quiescent Current					
PD1, PD0 = (0, 0)		6.0	7.0	mA/Amp	
PD1, PD0 = (0, 1)		3.6	4.0	mA/Amp	
PD1, PD0 = (1, 0)		2.8	3.3	mA/Amp	
PD1, PD0 = (1, 1) (Shutdown State)		0.4	1.2	mA/Amp	
PD = 0 Threshold			0.8	V	
PD = 1 Threshold	1.8			V	
+Power Supply Rejection Ratio	64	68		dB	$\Delta V_{OS, DM (RTI)}/\Delta V_{CC}$, ΔV_{CC} = ±1 V
−Power Supply Rejection Ratio	76	79		dB	$\Delta V_{OS, DM (RTI)}/\Delta V_{EE}$, ΔV_{EE} = ±1 V

V_S = ±5 V or +10 V, R_L = 100 Ω, G = +5, PD = (0, 0), T = 25°C, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE					
−3 dB Small Signal Bandwidth	30	40		MHz	V_{OUT} = 0.1 V p-p, R_F = 2 kΩ
−3 dB Large signal Bandwidth	20	25		MHz	V_{OUT} = 4 V p-p, R_F = 2 kΩ
Peaking		0.05		dB	V_{OUT} = 0.1 V p-p, R_F = 2 kΩ
Slew Rate (Rise)	300	350		V/µs	V_{OUT} = 7 V p-p, R_F = 2 kΩ
Slew Rate (Fall)	400	450		V/µs	V_{OUT} = 7 V p-p, R_F = 2 kΩ
NOISE/DISTORTION PERFORMANCE					
Second Harmonic Distortion		−72		dBc	f_C = 1 MHz, V_{OUT} = 2 V p-p
Third Harmonic Distortion		−82		dBc	f_C = 1 MHz, V_{OUT} = 2 V p-p
Voltage Noise (RTI)		4.3		nV/√Hz	f = 10 kHz
+Input Current Noise		10		pA/√Hz	f = 10 kHz
−Input Current Noise		13		pA/√Hz	f = 10 kHz
INPUT CHARACTERISTICS					
RTI Offset Voltage	−5.0	±3.0	+5.0	mV	$V_{+IN} - V_{-IN}$
+Input Bias Current		5.0	10.0	µA	
−Input Bias Current		10.0	15.0	µA	
Input Resistance		400		kΩ	
Input Capacitance		2.0		pF	
Common-Mode Rejection Ratio	62	66		dB	$(\Delta V_{OS, DM (RTI)})/(\Delta V_{IN, CM})$
OUTPUT CHARACTERISTICS					
Differential Output Voltage Swing	14.0	16.0	18.0	V	ΔV_{OUT}
Single-Ended Output Voltage Swing	7.0	8.0	9.0	V	ΔV_{OUT}
Linear Output Current		400		mA	R_L = 10 Ω, f_C = 100 kHz
POWER SUPPLY					
Operating Range (Dual Supply)	±5		±12	V	
Operating Range (Single Supply)	+10		+24	V	
Total Quiescent Current					
PD1, PD0 = (0, 0)		5.4	6.0	mA/Amp	
PD1, PD0 = (0, 1)		3.5	4.0	mA/Amp	
PD1, PD0 = (1, 0)		2.6	3.0	mA/Amp	
PD1, PD0 = (1, 1) (Shutdown State)		0.4	1.0	mA/Amp	
PD = 0 Threshold			0.8	V	
PD = 1 Threshold	1.8			V	
+Power Supply Rejection Ratio	72	76		dB	$\Delta V_{OS, DM (RTI)}/\Delta V_{CC}$, ΔV_{CC} = ±1 V
−Power Supply Rejection Ratio	64	68		dB	$\Delta V_{OS, DM (RTI)}/\Delta V_{EE}$, ΔV_{EE} = ±1 V

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	±13 V (+26 V)
Power Dissipation	See Figure 3
Storage Temperature	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature Range (Soldering 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, i.e., θ_{JA} is specified for device soldered in circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	Unit
LFCSP-32 (CP)	27.27	°C/W
TSSOP-28/EP (RE)	35.33	°C/W

Maximum Power Dissipation

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). Assuming that the load (R_L) is midsupply, the total drive power is $V_S/2 \times I_{OUT}$, some of which is dissipated in the package and some in the load ($V_{OUT} \times I_{OUT}$).

RMS output voltages should be considered. If R_L is referenced to V_{S-} as in single-supply operation, the total power is $V_S \times I_{OUT}$.

In single supply with R_L to V_{S-}, worst case is $V_{OUT} = V_S/2$.

Airflow increases heat dissipation, effectively reducing θ_{JA}. Also, more metal directly in contact with the package leads from metal traces, through holes, ground, and power planes reduces the θ_{JA}.

Figure 3 shows the maximum safe power dissipation in the package versus the ambient temperature for the LFCSP-32 and TSSOP-28/EP packages on a JEDEC standard 4-layer board. θ_{JA} values are approximations.

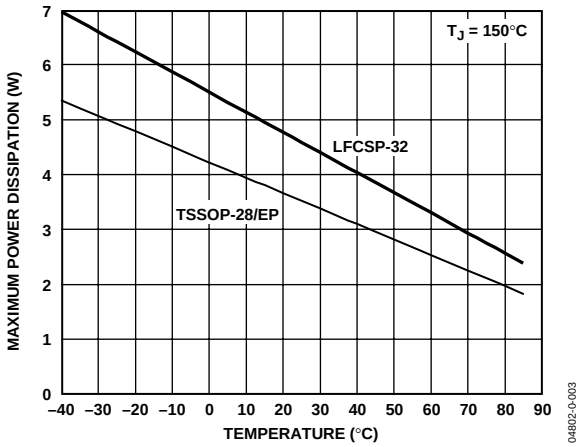


Figure 3. Maximum Power Dissipation vs. Temperature for a 4-Layer Board

See the Thermal Considerations section for additional thermal design guidance.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

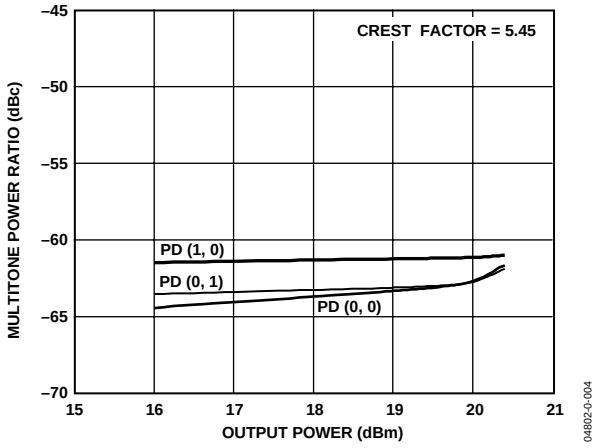


Figure 4. MTPR vs. Output Power (1.75 MHz Empty Bin)
ADSL/ADSL2+ Circuit (Figure 32)
V_S = ±12 V, R_{LOAD} = 100 Ω, CF = 5.45

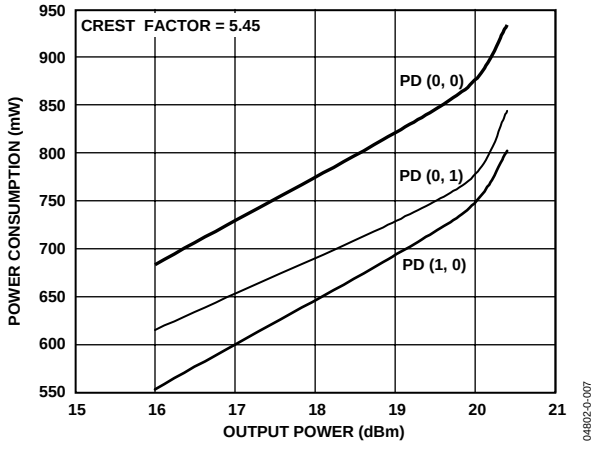


Figure 7. Power Consumption vs. Output Power (26 kHz to 2.2 MHz)
ADSL/ADSL2+ Circuit (Figure 32)
V_S = ±12 V, R_{LOAD} = 100 Ω, CF = 5.45

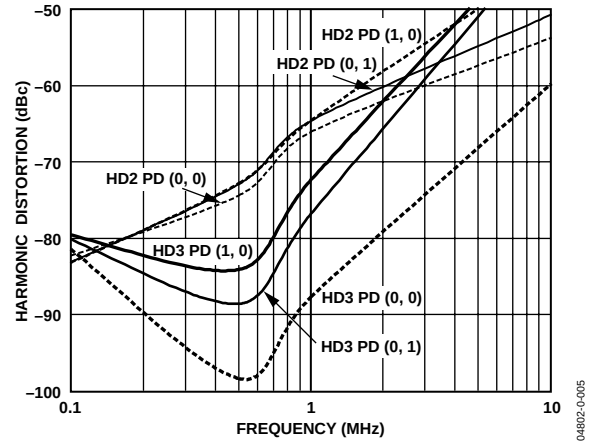


Figure 5. Harmonic Distortion vs. Frequency
Dual Differential Driver Circuit (Figure 30)
V_S = ±12 V, R_{LOAD} = 100 Ω, G = +5, V_{OUT} = 2 V p-p

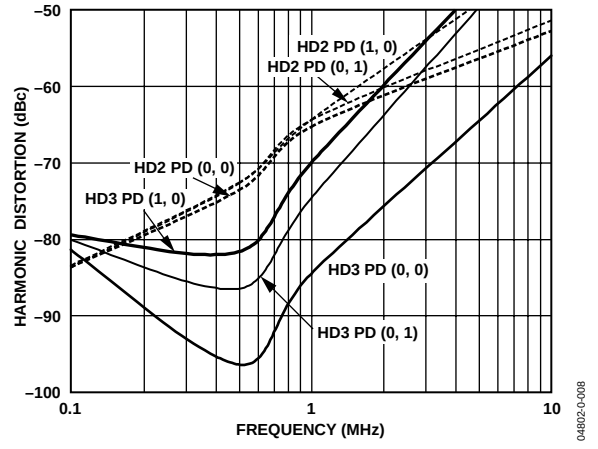


Figure 8. Harmonic Distortion vs. Frequency
Dual Differential Driver Circuit (Figure 30)
V_S = ±5 V, R_{LOAD} = 100 Ω, G = +5, V_{OUT} = 2 V p-p

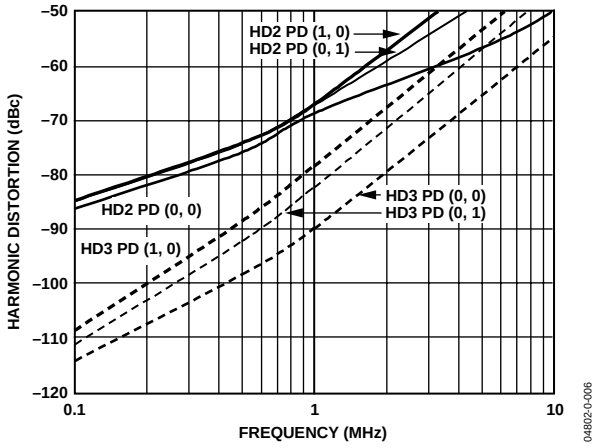


Figure 6. Harmonic Distortion vs. Frequency
Quad Op Amp Circuit (Figure 29)
V_S = ±12 V, R_{LOAD} = 100 Ω, G = +5, V_{OUT} = 2 V p-p

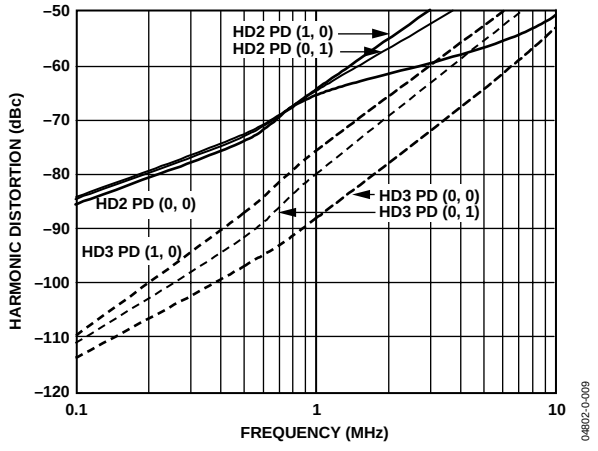


Figure 9. Harmonic Distortion vs. Frequency
Quad Op Amp Circuit (Figure 29)
V_S = ±5 V, R_{LOAD} = 100 Ω, G = +5, V_{OUT} = 2 V p-p

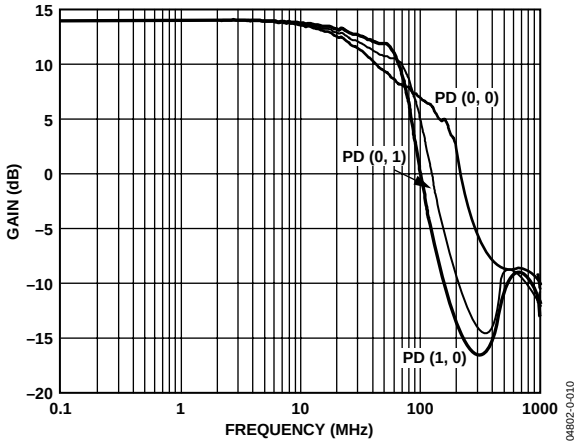


Figure 10. Small Signal Frequency Response
Quad Op Amp Circuit (Figure 29)
V_S = ±12 V, R_{LOAD} = 100 Ω, G = +5, V_{OUT} = 100 mV p-p

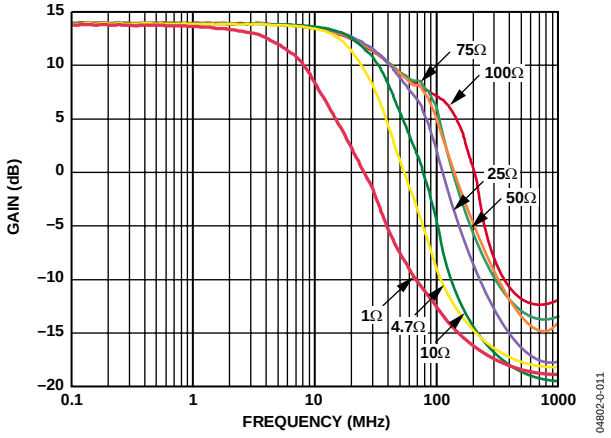


Figure 11. Small Signal Frequency Response vs. Load
Quad Op Amp Circuit (Figure 29)
V_S = ±12 V, G = +5, V_{OUT} = 100 mV p-p

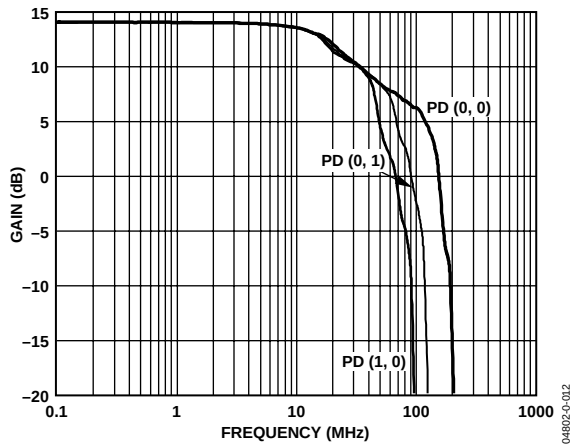


Figure 12. Large Signal Frequency Response
Quad Op Amp Circuit (Figure 29)
V_S = ±12 V, R_{LOAD} = 100 Ω, G = +5, V_{OUT} = 4 V p-p

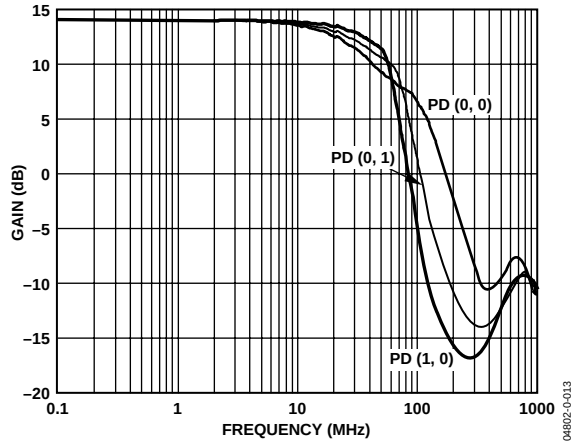


Figure 13. Small Signal Frequency Response
Quad Op Amp Circuit (Figure 29)
V_S = ±5 V, R_{LOAD} = 100 Ω, G = +5, V_{OUT} = 100 mV p-p

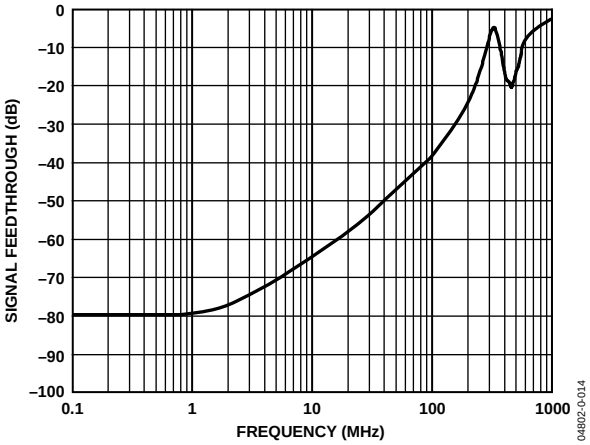


Figure 14. Signal Feedthrough vs. Frequency
Quad Op Amp Circuit (Figure 29)
V_S = ±12 V, G = +5, V_{IN} = 800 mV p-p, PD (1, 1)

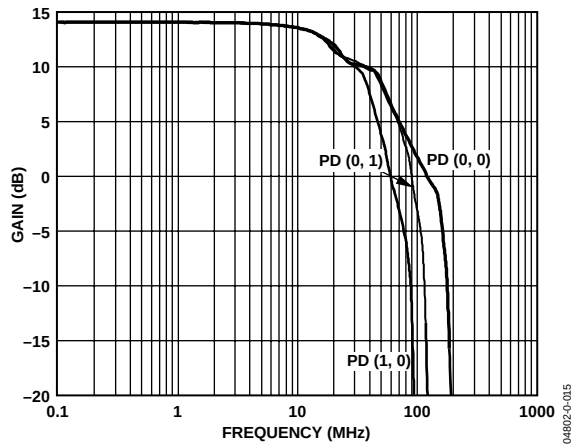


Figure 15. Large Signal Frequency Response
Quad Op Amp Circuit (Figure 29)
V_S = ±5 V, R_{LOAD} = 100 Ω, G = +5, V_{OUT} = 4 V p-p

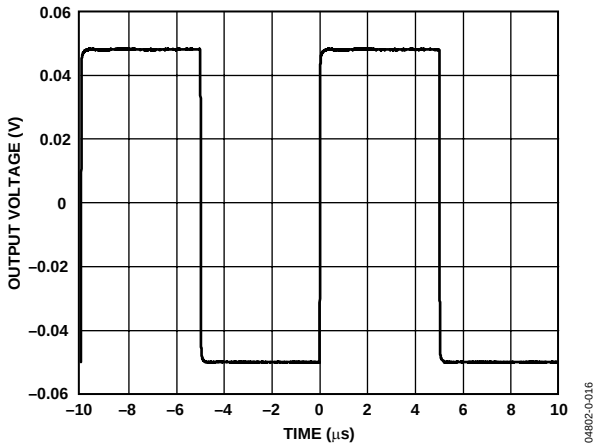


Figure 16. Small Signal Pulse Response
Quad Op Amp Circuit (Figure 29)
V_S = ±12 V, R_{LOAD} = 100 Ω, G = +5, 100 mV Step

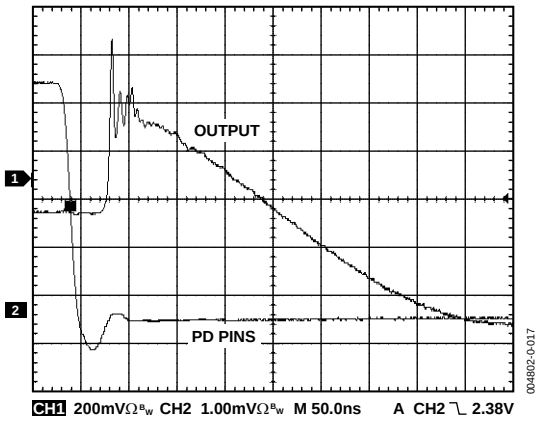


Figure 17. Power-Up Time: PD (1, 1) to PD (0, 0)
Quad Op Amp Circuit (Figure 29)
V_S = ±12 V, R_{LOAD} = 100 Ω, G = +5, V_{OUT} = 1 V p-p

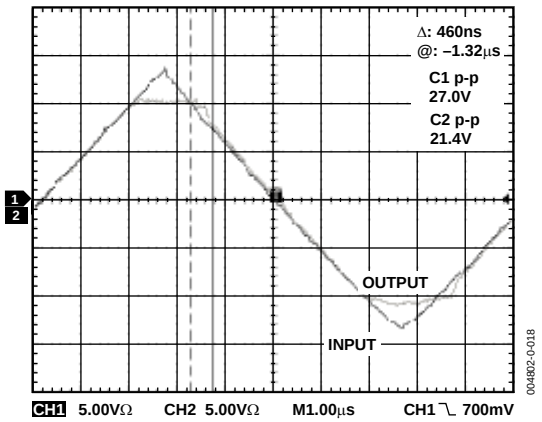


Figure 18. Input Overdrive Recovery
Quad Op Amp Circuit (Figure 29)
V_S = ±12 V, R_{LOAD} = 100 Ω, G = +1, V_{IN} = 27 V p-p

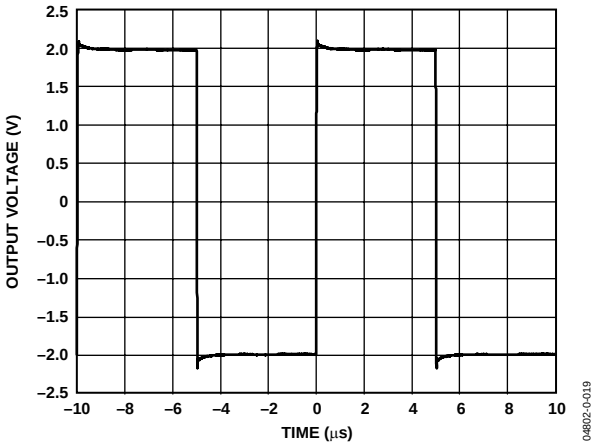


Figure 19. Large Signal Pulse Response
Quad Op Amp Circuit (Figure 29)
V_S = ±12 V, R_{LOAD} = 100 Ω, G = +5, 4 V Step

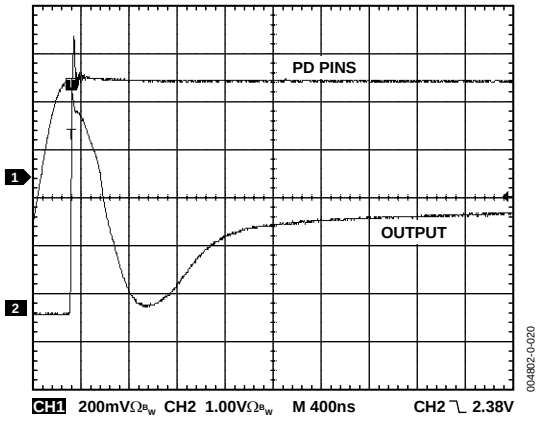


Figure 20. Power-Down Time: PD (0, 0) to PD (1, 1)
Quad Op Amp Circuit (Figure 29)
V_S = ±12 V, R_{LOAD} = 100 Ω, G = +5, V_{OUT} = 1 V p-p

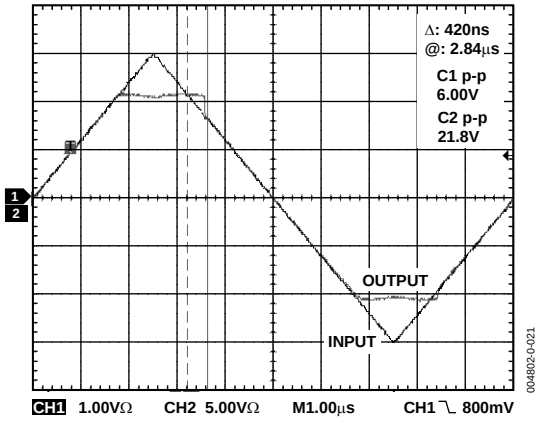


Figure 21. Output Overdrive Recovery
Quad Op Amp Circuit (Figure 29)
V_S = ±12 V, R_{LOAD} = 100 Ω, G = +5, V_{IN} = 6 V p-p

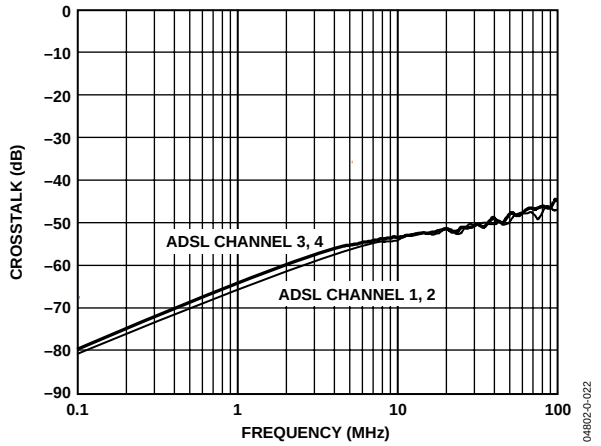


Figure 22. Crosstalk vs. Frequency
ADSL/ADSL2+ Circuit (Figure 32)
V_S = ±12 V, G = +11, R_{LOAD} = 100 Ω, V_{IN} = 200 mV p-p

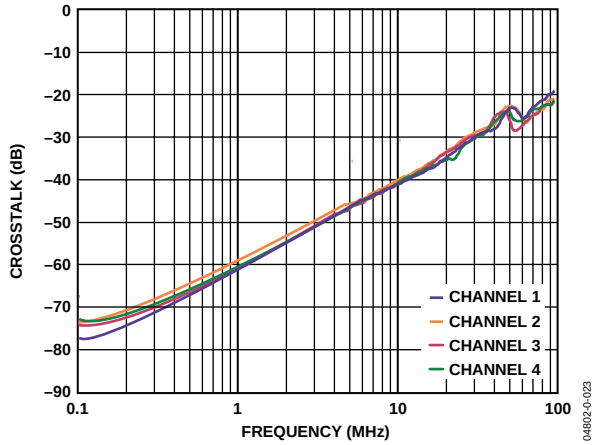


Figure 23. Crosstalk vs. Frequency
Quad Op Amp Circuit (Figure 29)
V_S = ±12 V, G = +5, R_{LOAD} = 100 Ω, V_{IN} = 200 mV p-p

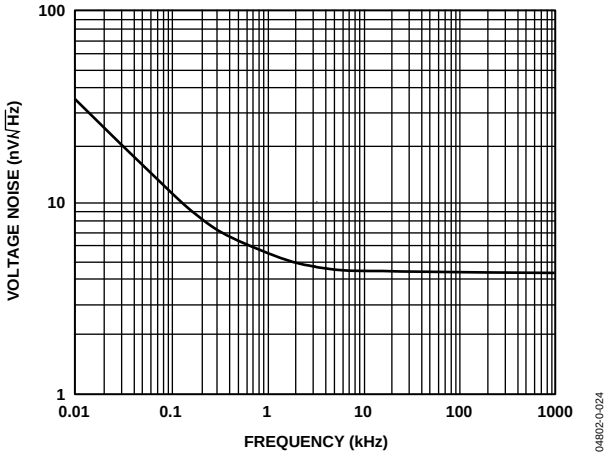


Figure 24. Voltage Noise vs. Frequency

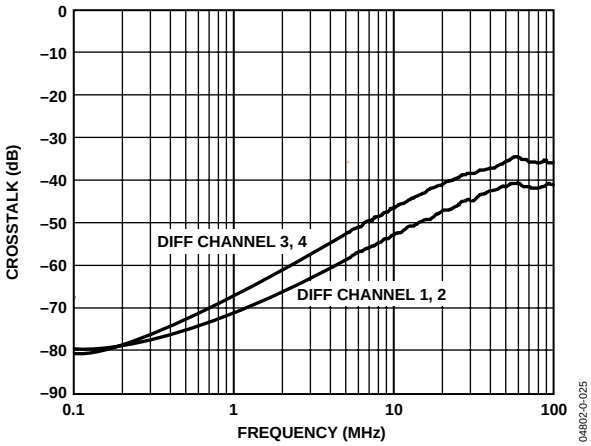


Figure 25. Crosstalk vs. Frequency
Dual Differential Driver Circuit (Figure 30)
V_S = ±12 V, G = +5, R_{LOAD} = 100 Ω, V_{IN} = 200 mV p-p

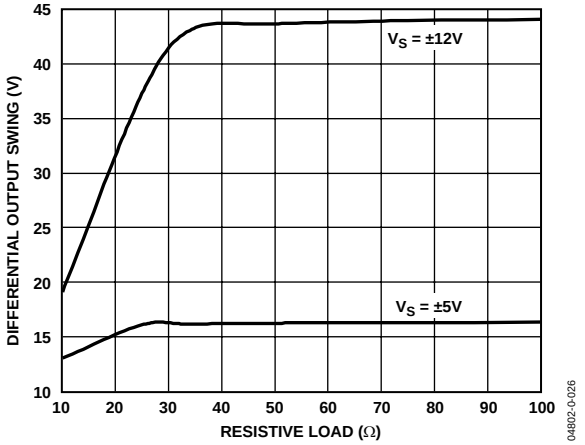


Figure 26. Differential Output Swing vs. R_{LOAD}
ADSL/ADSL2+ Circuit (Figure 32)
G = +11

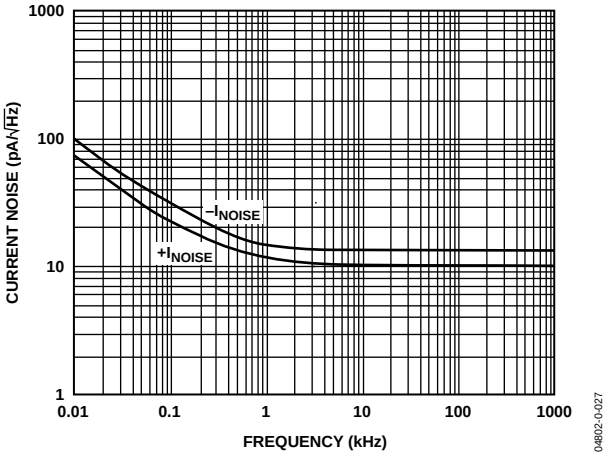


Figure 27. Current Noise vs. Frequency

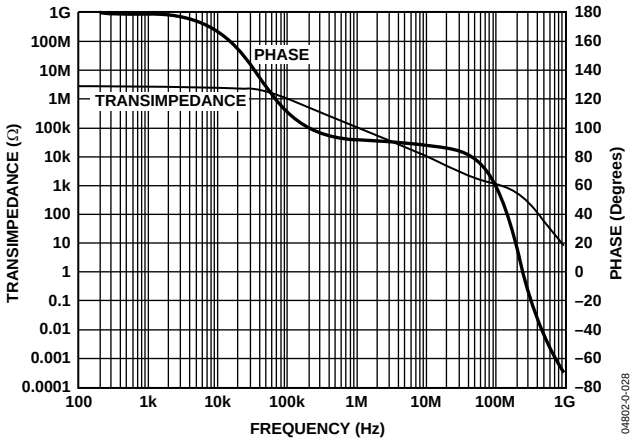


Figure 28. Open-Loop Transimpedance and Phase

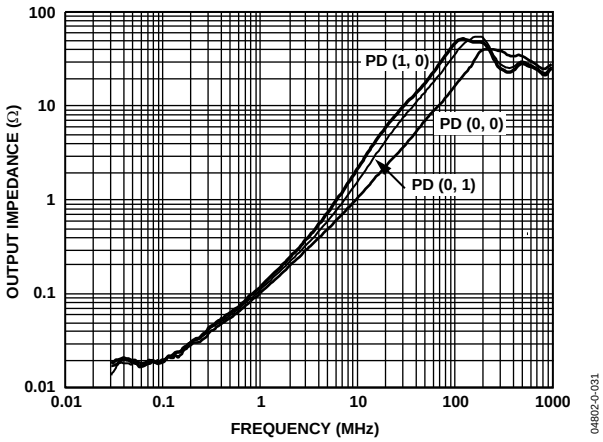


Figure 31. Output Impedance vs. Frequency
Quad Op Amp Circuit (Figure 29)
$V_S = \pm 12$ V, G = +5, PD (0, 0)

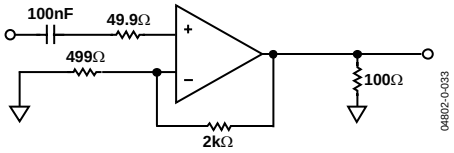


Figure 29. Quad Op Amp Circuit

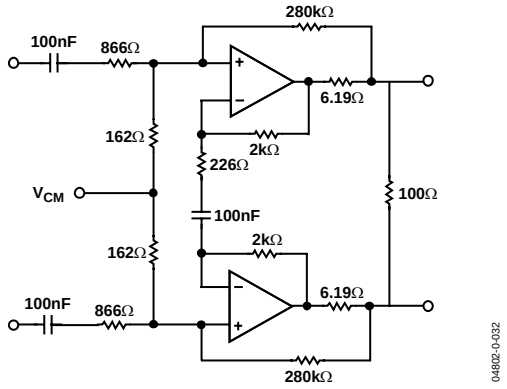


Figure 32. ADSL/ADSL2+ Circuit

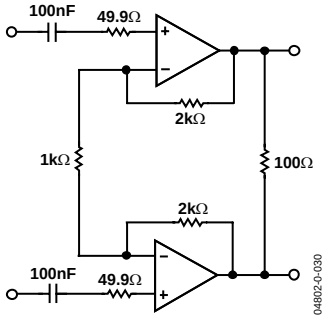


Figure 30. Dual Differential Driver Circuit

THEORY OF OPERATION

The AD8392 is a current feedback amplifier with high (400 mA) output current capability. With a current feedback amplifier, the current into the inverting input is the feedback signal, and the open-loop behavior is that of a transimpedance, dV_O/dI_{IN} or T_Z.

The open-loop transimpedance is analogous to the open-loop voltage gain of a voltage feedback amplifier. Figure 33 shows a simplified model of a current feedback amplifier. Since R_{IN} is proportional to $1/g_m$, the equivalent voltage gain is just $T_Z \times g_m$, where g_m is the transconductance of the input stage. Basic analysis of the follower with gain circuit yields

$$\frac{V_O}{V_{IN}} = G \times \frac{T_Z(S)}{T_Z(S) + G \times R_{IN} + R_F}$$

where:

$$G = 1 + \frac{R_F}{R_G}$$

$$R_{IN} = \frac{1}{g_m} \approx 50\ \Omega$$

Since $G \times R_{IN} << R_F$ for low gains, a current feedback amplifier has relatively constant bandwidth versus gain, the 3 dB point being set when $|T_Z| = R_F$.

Of course, for a real amplifier there are additional poles that contribute excess phase, and there is a value for R_F below which the amplifier is unstable. Tolerance for peaking and desired flatness determines the optimum R_F in each application.

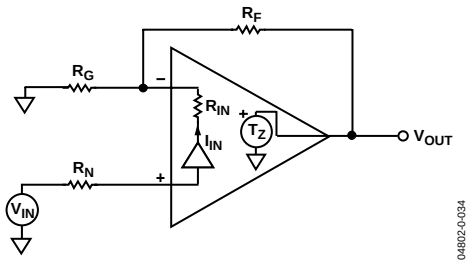


Figure 33. Simplified Block Diagram

The AD8392 is capable of delivering 400 mA of output current while swinging to within 2 V of either power supply rail. The AD8392 also has a power management system included on-chip. It features four user-programmable power levels (three active power modes as well as the provision for complete shutdown).

APPLICATIONS

SUPPLIES, GROUNDING, AND LAYOUT

The AD8392 can be powered from either single or dual supplies, with the total supply voltage ranging from 10 V to 24 V. For optimum performance, a well regulated low ripple supply should be used.

As with all high speed amplifiers, close attention should be paid to supply decoupling, grounding, and overall board layout. Low frequency supply decoupling should be provided with 10 µF tantalum capacitors from each supply to ground. In addition, all supply pins should be decoupled with 0.1 µF quality ceramic chip capacitors placed as close as possible to the driver. An internal low impedance ground plane should be used to provide a common ground point for all driver and decoupling capacitor ground requirements. Whenever possible, separate ground planes should be used for analog and digital circuitry.

High speed layout techniques should be followed to minimize parasitic capacitance around the inverting inputs. Some practical examples of these techniques are keeping feedback traces as short as possible and clearing away ground plane in the area of the inverting inputs. Input and output traces should be kept short and as far apart from each other as practical to avoid crosstalk. When used as a differential driver, all differential signal traces should be kept as symmetrical as possible.

RESISTOR SELECTION

In current feedback amplifiers, selection of feedback and gain resistors can impact harmonic distortion performance, bandwidth, and gain flatness. Care should be exercised in the selection of these resistors so that optimum performance is achieved. Table 5 shows some suggested resistor values for use in a variety of gain settings. These values are suggested as a good starting point when designing for any application.

Table 5. Resistor Selection Guide

Gain	R_F	R_G
1	2.0k	Open
2	1.5k	1.5k
5	1.0k	249
10	750	82.5

POWER MANAGEMENT

The AD8392 can be configured in any of three active bias states as well as a shutdown state via the use of two sets of digitally programmable logic pins. Pins PD(0, 1) 1, 2 control Amplifiers 1 and 2, while PD(0, 1) 3, 4 control Amplifiers 3 and 4. These pins can be controlled directly with either 3.3 V or 5 V CMOS logic by using the GND pins as a reference. If left unconnected, the PD pins float low, placing the amplifier in the full bias mode. Refer to the Specifications for the per amplifier quiescent current for each of the available bias states.

The AD8392 exhibits low output impedance for the three active states. However, the output impedance in the shutdown state (PD1, 0 = 1, 1) is undefined.

DRIVING CAPACITIVE LOADS

When driving a capacitive load, most op amps exhibit peaking in their frequency response. In general, to minimize peaking or to ensure device stability for larger values of capacitive loads, a small series resistor can be added between the op amp output and the load capacitor. Figure 34 shows the frequency response of the AD8392 for various capacitive loads without any series resistance. In this condition, the maximum recommended capacitive load is around 20 pF. As shown in Figure 35, the addition of a 5.1 Ω series resistor limits peaking to approximately 3 dB when driving capacitive loads up to 100 pF.

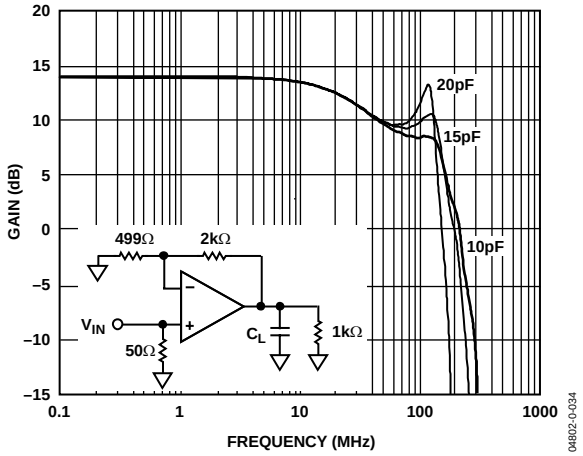


Figure 34. AD8392 Capacitive Load Frequency Response without Series Resistance

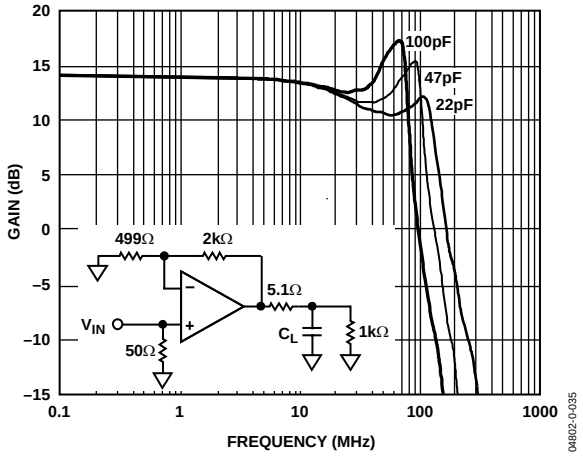


Figure 35. AD8392 Capacitive Load Frequency Response with Series Resistance

THERMAL CONSIDERATIONS

When using a quad, high output current amplifier, such as the AD8392, special consideration should be given to system level thermal design. In applications such as ADSL/ADSL2+, the AD8392 could be required to dissipate as much as 1.4 W or more on chip. Under these conditions, particular attention should be paid to the thermal design in order to maintain safe operating temperatures on the die. To aid in the thermal design, the thermal information in the Thermal Resistance section can be combined with what follows here.

The information in Table 4 and Figure 3 is based on a standard JEDEC 4-layer board and a maximum die temperature of 150°C. To provide additional guidance and design suggestions, a thermal study was performed under a set of conditions more closely aligned with an actual ADSL/ADSL2+ application.

In a typical ADSL/ADSL2+ line card, component density usually dictates that most of the copper plane used for thermal dissipation be internal. Additionally, each ADSL/ADSL2+ port may be allotted only 1 square inch, or even less, of board space. For these reasons, a special thermal test board was constructed for this study. The 4-layer board measured approximately 4 inches × 4 inches and contained two internal 1 oz copper ground planes, each measuring 2 inches × 3 inches. The top layer contained signal traces and an exposed copper strip ¼ inch × 3 inches to accommodate heat sinking, with no other copper on the top or bottom of the board.

Three 28-lead TSSOPs were placed on the board representing six ADSL channels, or one channel per square inch of copper, with each channel dissipating 700 mW on-chip (1.4 W per package). The die temperature is then measured in still air and in a wind tunnel with calibrated airflow of 100 LFM, 200 LFM, and 400 LFM. Figure 36 shows the power dissipation versus the ambient temperature for each airflow condition. The figure assumes a maximum die temperature of 135°C. No heat sink was used.

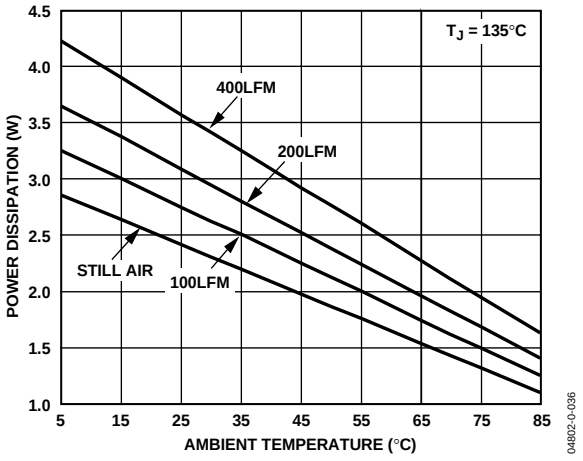


Figure 36. Power Dissipation vs. Ambient Temperature and Air Flow 28-Lead TSSOP/EP

This data is only provided as guidance to assist in the thermal design process. Due diligence should be performed with regards to power dissipation because there are many factors that can affect thermal performance.

TYPICAL ADSL/ADSL2+ APPLICATION

In a typical ADSL/ADSL2+ application, a differential line driver is used to take the signal from the analog front end (AFE) and drive it onto the twisted pair telephone line. Referring to the typical circuit representation in Figure 37, the differential input appears at V_{IN+} and V_{IN-} from the AFE, while the differential output is transformer coupled to the telephone line at tip and ring. The common-mode operating point, generally midway between the supplies, is set through V_{COM}.

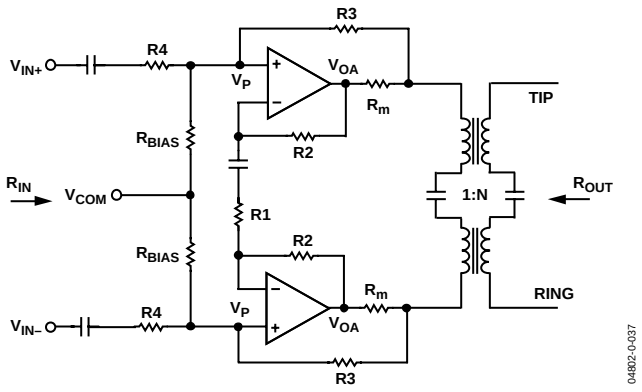


Figure 37. Typical ADSL/ADSL2+ Application Circuit

In ADSL/ADSL2+ applications, it is common practice to conserve power by using positive feedback to synthesize the output resistance, thereby lowering the required ohmic value of the line matching resistors, R_m. The circuit in Figure 37 is somewhat unique in that the positive feedback introduced via R3 has the effect of synthesizing the input resistance as well. The following definitions and equations can be used to calculate the resistor values necessary to obtain the desired gain, input resistance, and output resistance for a given application. For simplicity the following calculations assume a lossless transformer.

The following values are used in the design equations and are assumed already known or chosen by the designer.

V_{IN}	Differential input voltage
R_{IN}	Desired differential input resistance
N	Transformer turns ratio
V_{LINE}	Differential output voltage at tip and ring
R_m	Each is typically 5% to 15% of the transformer reflected line impedance
$R2$	Recommended in the amplifier data sheet
V_P	Voltage at the + inputs to the amplifier, approximately ½ V_{IN} (must be less than V_{IN} for positive input resistance)
R_L	Transformer reflected line impedance

Additional definitions for calculating resistor values include:

V_{OA}	Voltage at the amplifier outputs
k	Matching resistance reduction factor
A_V	Gain from V_{IN} to transformer primary
β	Negative feedback factor
α	Positive feedback factor

Note: R1 must be calculated before β and α.

$$V_{OA} = \frac{V_{LINE}(1+k)}{N} \qquad k = \frac{2\,R_m}{R_L} \qquad A_V = \frac{V_{LINE}}{N\,V_{IN}}$$

$$\beta = \frac{R1}{R1 + 2\,R2} \qquad \alpha = \beta(1-k)$$

With the above known quantities and definitions, the remaining resistors can readily be calculated.

$$R1 = \frac{2\,V_P\,R2}{V_{OA} - V_P}$$

$$R4 = \frac{R_{IN}\,(V_{IN} - V_P)}{2\,V_{IN}}$$

$$R3 = \frac{A_V\,R4\left(2\,R1R_m + R1R_L - \alpha\,R1R_L - 2\alpha\,R2\,R_L\right)}{\alpha\,R_L\left(R1 + 2\,R2\right)}$$

$$R_{BIAS} = \frac{\alpha\,R3\,R4}{R4 - \alpha\,(R3 + R4)}$$

After building the circuit with the closest 1% resistor values, the actual gain, input resistance, and output resistance can be verified with the following equations.

$$GAIN_{(V_{IN}\ to\ LINE)} = \frac{N}{\beta(k+1)\left(1 + \frac{R4}{R3} + \frac{R4}{R_{BIAS}}\right) - \frac{R4}{R3}}$$

$$R_{IN} = \frac{2}{\frac{1}{R4} - A_V\,\beta\left(\frac{2\,R_m + R_L}{R4\,R_L}\right)}$$

$$R_{OUT} = \frac{2\,R_m\,N^2}{1 - \left(\frac{R4\,R_{BIAS}}{R1(R4 + R_{BIAS})}\right)\left(\frac{R1 + 2R2}{R3 + \frac{R4\,R_{BIAS}}{R4 + R_{BIAS}}}\right)}$$

MULTITONE POWER RATIO

The DMT signal used in ADSL/ADSL2+ systems carries data in discrete tones or bins, which appear in the frequency domain in evenly spaced 4.3125 kHz intervals. In applications using this type of waveform, multitone power ratio (MTPR) is a commonly used measure of linearity. Generally, there are two types of MTPR that designers are typically concerned with: in-band and out-of-band MTPR. In-band MTPR is defined as the measured difference from the peak of one tone that is loaded with data to the peak of an adjacent tone that is intentionally left empty. Out-of-band MTPR is more loosely defined as the spurious emissions that occur in the receive band located between 25.875 kHz and the first downstream tone at 138 kHz. Figure 38 and Figure 39 show the AD8392 in-band MTPR for a 5.5 crest factor waveform for empty bins in the ADSL and extended ADSL2+ bandwidths. Figure 40 shows the AD8392 out-of-band MTPR for the same waveform.

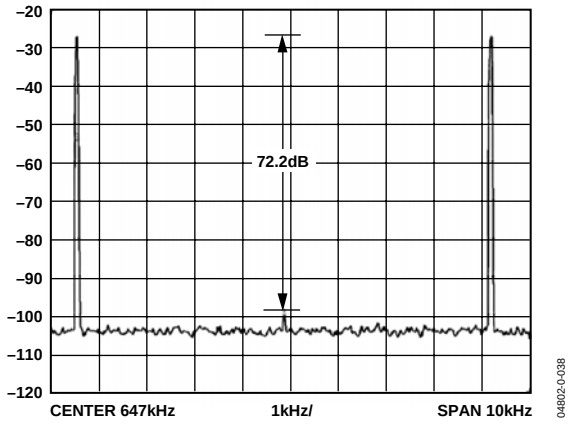


Figure 38. In-Band MTPR at 647 kHz

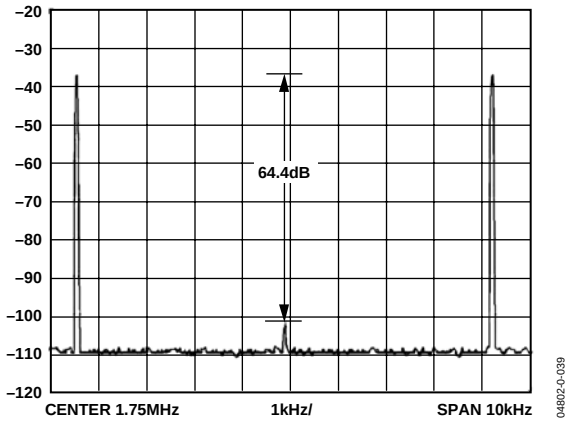


Figure 39. In-Band MTPR at 1.751 MHz

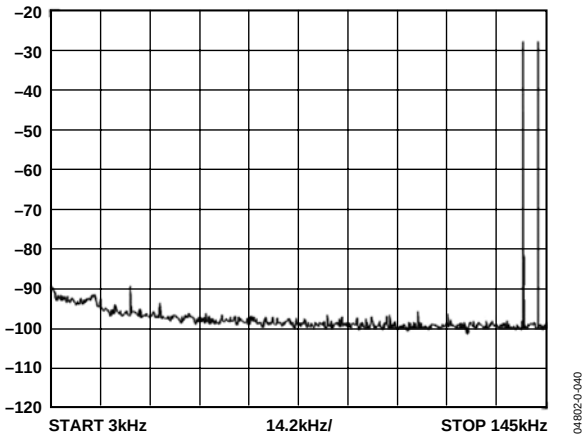
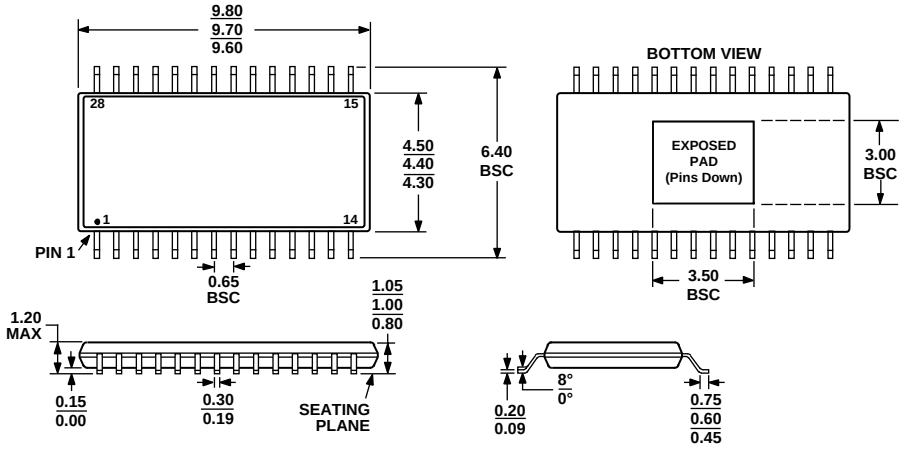


Figure 40. Out-of-Band MTPR

LIGHTNING AND AC POWER FAULT

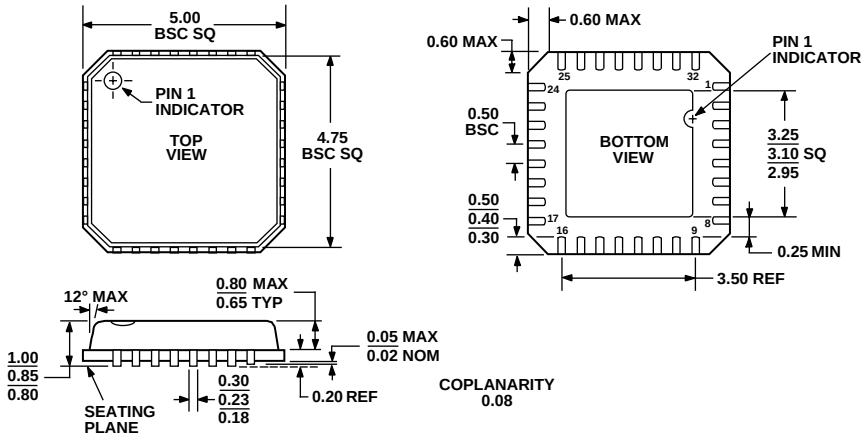
The AD8392 can be used is as an ADSL/ADSL2+ line driver. In this application, the line driver is transformer-coupled to the twisted pair telephone line and could be subjected to large line transients resulting from events such as lightning strikes or downed power lines. In this type of environment, additional circuitry may be required to protect the AD8392 from damage that may occur as a result of these events. Using a minimal amount of external protection, the AD8392 has successfully passed overvoltage and overcurrent compliance testing per the ITU K-20 specification. For details on the external protection circuitry, contact the high current driver product line at high_current_drivers.com@analog.com.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153AET

Figure 41. 28-Lead Thin Shrink Small Outline with Exposed Pad [TSSOP/EP]
(RE-28-1)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VHHD-2

Figure 42. 32-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm Body (CP-32-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Outline
AD8392ARE	−40°C to +85°C	28-Lead Thin Shrink Small Outline Package (TSSOP)	RE-28-1
AD8392ARE-REEL	−40°C to +85°C	28-Lead Thin Shrink Small Outline Package (TSSOP)	RE-28-1
AD8392ARE-REEL7	−40°C to +85°C	28-Lead Thin Shrink Small Outline Package (TSSOP)	RE-28-1
AD8392ACP-R2	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package (LFCSP)	CP-32-2
AD8392ACP-REEL	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package (LFCSP)	CP-32-2
AD8392ACP-REEL7	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package (LFCSP)	CP-32-2

D04802–0–7/04(0)

ANALOG DEVICES

www.analog.com