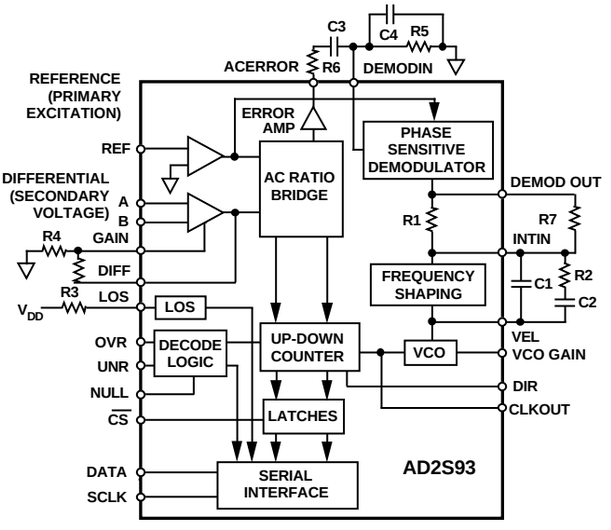
Low Cost LVDT-to-Digital Converter

AD2S93

FEATURES
Full Function Monolithic LVDT-to-Digital Converter
Absolute Serial Data Output
Uncommitted Differential Input
Repeatability
Remote Diagnostics
14-Bit Resolution
Industrial Temperature Range
28-Pin PLCC
Low Power

APPLICATIONS
Industrial Gauging
Industrial Process Control
Linear Positioning Systems
Linear Actuator Control
Automotive Motion Sensing and Control
Torque Sensing Conditioner
AC Strain Gages Conditioning
Avionics

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD2S93 is a complete 14-bit resolution tracking LVDT-to-digital converter. A Type II tracking loop is employed to track the A–B input and produce a digital output equal to (A–B)/(REF/2), where REF is a fixed amplitude ac reference phase coherent with the A–B input. This allows the measurement of any 2-, 3-, 4- and 5-wire LVDT or linear amplitude modulated input. The operating frequency range is from 360 Hz to 10 kHz with user definable bandwidth set externally within a range of 45 Hz to 1250 Hz.

The AD2S93 has a 16-bit serial output. The MSB (LOS), read first, indicates a loss of the signal A, B, or reference inputs to the converter or transducer. The second and third MSBs are flags indicating whether [–REF/2 (UNR) ≤ A–B ≤ +REF/2 (OVR]) is outside the linear operating range of the converter. The displacement data is presented as 13-bit offset binary giving a ±12-bit operating range. LOS, OVR and UNR are pinned out on the device, in addition a NULL flag is available which is set when (A–B) = 0.

Absolute displacement information is accessed when $\overline{CS}$ is taken LO followed by the application of an external clock (SCLK) with a maximum rate of 2 MHz. Data is read MSB first. When $\overline{CS}$ is high the DATA output is high impedance; this allows daisy chaining of more than one converter onto a common bus.

The A, B differential input allows the user to scale the A, B inputs between 1 and 10. This enables the user to accurately set up the inputs matching the REF input to the DIFF output. The DIFF output is the resultant A–B. The AD2S93 operates using ±5 V ± 5% power supplies and is fabricated on Analog Devices' linear compatible CMOS process (LC^2MOS). The (LC^2MOS) is a mixed technology process that combines precision bipolar circuits with low power logic.

PRODUCT HIGHLIGHTS

Complete LVDT-to-Digital Interface. The AD2S93 provides the complete solution for digitizing LVDT signals to 14-bit resolution.

Serial 16-Bit Output Data. One 16-bit read from the AD2S93 determines input signal continuity (LOS), over and underrange detection and 13 bits of offset binary displacement information.

High Accuracy Grade in Low Cost Package. 0.05% and 0.1% integral linearity over the full –40°C to +85°C operating temperature range.

Uncommitted Differential Input. Allows configuration of 2-, 3-, 4- and 5-wire LVDTs.

Multiple Converter Interfacing. High impedance data output and a simple three-wire interface reduces cabling and eliminates bus contention.

Low Power. 70 mW power consumption (typ).

REV. A

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AD2S93–SPECIFICATIONS (V_{DD} = +5 V ± 5%; V_{SS} = –5 V ± 5%, AGND = DGND = 0 V, T_A = –40°C to +85°C unless otherwise noted)

Parameter	Test Conditions	Min	Typ	Max	Units
SIGNAL INPUTS					
Frequency		0.36	1.0	10	kHz
Max Voltage Level[1]		0.8	1.0	1.2	V rms
Nominal Full Scale[2]			1.0		V rms
Input Bias Current	@ +25°C			1.1	µA
Input Impedance			1.0		MΩ
CMRR			57		dB
Maximum Sensitivity[3]	$V_{A–B}$ = 1 V rms, G = 1		342		µV pk/LSB
REFERENCE INPUT					
Frequency		0.36		10	kHz
Voltage Level		1.8	2.0	2.2	V rms
Input Bias Current	@ 0 V +25°C			1	µA
Input Impedance			1.0		MΩ
Permissible Phase Shift[4]	Signal to Reference	–10		+10	Degrees
CONVERTER DYNAMICS					
Bandwidth	Set by User				
VCO Mode = 1	VCO Gain Connected to VCO I/P	500		1250	Hz
VCO Mode = 2	VCO Gain No Connect	45		500	Hz
Maximum Slew Rate					
Mode = 1			2400	3000	LSB/ms
Mode = 2			800	1000	LSB/ms
ACCURACY					
Integral Linearity	AP			0.1	% FSD
	BP			0.05	% FSD
Differential Linearity	AP			<2	LSB
	BP			<1	LSB
Repeatability				±1	LSB
Zero Position Offset	AP @ +25°C	–3		3	LSB
	BP @ +25°C	–1		1	LSB
	AP @ –40°C to +85°C	–4		4	LSB
	BP @ –40°C to +85°C	–2		2	LSB
Gain Error				±0.7	% FS
VELOCITY OUTPUT					
Max Output Voltage	Denotes Max Input Speed			±4.0	V dc
Load Drive Capability				±250	µA
LOGIC INPUTS SCLK, $\overline{CS}$					
Input High Voltage V_{INH}		3.5			V dc
Input Low Voltage V_{INL}				1.5	V dc
Input Current I_{IN}				500	nA
Input Capacitance			10		pF
LOGIC OUTPUTS					
OVR, UNR, NULL, DATA, A, B CLKOUT DIR					
Output High Voltage	@ 1 mA	4.0			V dc
Output Low Voltage	@ 1 mA			1.0	V dc
LOS OUTPUT	Open Drain Output Pull-Up to +V_{DD} via 12 kΩ			400	µA
Drive Capability					
Signal Threshold (A-B)		0.1		0.2	V rms
REF Threshold			0.22		V rms
Timeout Threshold				50	ms

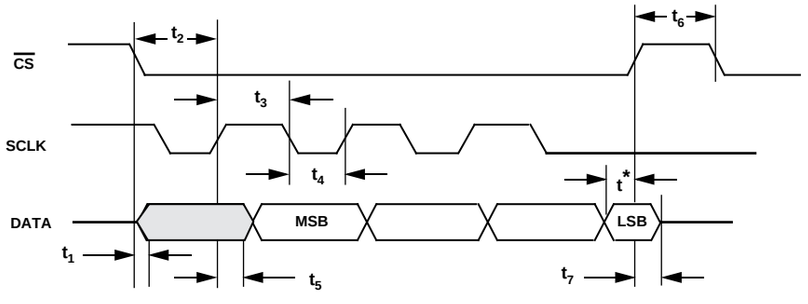
Parameter	Test Conditions	Min	Typ	Max	Units
SERIAL CLOCK (SCLK)					
SCK Input Rate				2	MHz
Maximum Read Rate (16 Bits)	Continuous			9.2	µs
POWER SUPPLY					
I_{DD}		5	7	10	mA
I_{SS}		5	7	10	mA

NOTES
[1]The signal input voltage maximum should always be set at 10% less than the reference input.
[2]Nominal + FS = $V_{A-B} = V_{REF}/2$, FS = $-V_{A-B} = V_{REF}/2$
[3]With G = 10; Sensitivity 34.2 µV pk/LSB
[4]Phase shift cause gain errors. "See Phase Shift and Quadrative Effects."
Specifications subject to change without notice.

TIMING CHARACTERISTICS (V_{DD} = +5 V ± 5%, AGND = DGND = 0 V, T_A = –40°C to +85°C unless otherwise noted)

Parameter	AD2S93	Units	Test Conditions
t_1[1]	150	ns max	$\overline{CS}$ to DATA Enable
t_2	600	ns min	$\overline{CS}$ to 1st SCLK Positive Edge
t_3	250	ns min	SCLK High Pulse
t_4	250	ns min	SCLK Low Pulse
t_5	100	ns max	SCLK Positive Edge to DATA Valid
t_6	600	ns min	$\overline{CS}$ High Pulse Width
t_7	150	ns max	$\overline{CS}$ High to DATA High Z (Bus Relinquish)

NOTE
[1]SCLK can only be applied after t_2 has elapsed.



t * = THE MINIMUM ACCESS TIME: USER DEPENDENT
TOTAL MAX READ TIME = t_2 + 16. (t_3 + t_4) + t_7
TOTAL MAX READ TIME = 600 +16 (250 + 250) + 150 ns
TOTAL MAX READ TIME = 600 + 8000 + 150 ns
TOTAL MAX READ TIME = 8.750 µs (SINGLE READ ONLY)

Timing Diagram

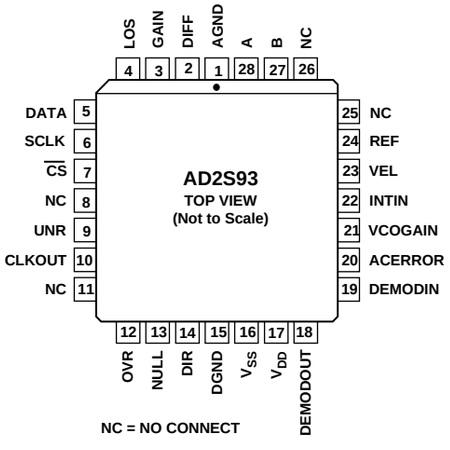
RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage (V_{DD}–V_{SS}) . . . . . ±5 V dc ± 5%
Analog Input Voltage (A, B) . . . . . 1 V rms ± 10%
Analog Reference Input (REF) . . . . . 2 V rms ± 10%
Signal and Reference Harmonic Distortion . . . . . <10%
Operating Temperature Range
Industrial (AP, BP) . . . . . –40°C to +85°C

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to AGND . . . . . –0.3 V dc to + 7.0 V dc
V_{SS} to AGND . . . . . +0.3 V dc to – 7.0 V dc
AGND to DGND . . . . . –0.3 V dc to V_{DD} + 0.3 V dc
Analog Inputs to AGND REF . . . . V_{SS} – 0.3 V to V_{DD} + 0.3 V
A, B . . . . . V_{SS} – 0.3 V to V_{DD} + 0.3 V
Analog Output to AGND VEL . . . . . V_{SS} to V_{DD}
Digital Inputs to DGND
$\overline{CS}$, SCLK . . . . . –0.3 V to V_{DD} + 0.3 V
Digital Outputs to DGND
NULL, DIR, CLKOUT, DATA . . . . –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
Industrial (A, B) . . . . . –40°C to +85°C
Lead Temperature (Soldering 10 sec) . . . . . +300°C
Power Dissipation to +75°C . . . . . +100 mW
Derates above +75°C by . . . . . 10 mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



ORDERING GUIDE

Model	Temperature Range	Linearity	Package Option
AD2S93AP	–40°C to +85°C	0.1%	P-28A
AD2S93BP	–40°C to +85°C	0.05%	P-28A

PIN DESIGNATIONS

Pin No.	Mnemonic	Description
1	AGND	Analog Ground.
2	DIFF	Output of Signal Input Preamplifier.
3	GAIN	Connect GAIN Pin to DIFF for nominal × 1. Gains greater than 1 can be resistively scaled. Do not leave unconnected.
4	LOS	Denotes A or B lines loss of connection and/or loss of reference to transducer or converter.
5	DATA	16-bit serial data output 13 bits of absolute position information plus overrange and underrange plus LOS.
6	SCLK	Serial Clock. Maximum rate = 2 MHz.
7	$\overline{CS}$	Chip Select. Loads serial interface with current positional information and enable output.
9, 12	UNR, OVR	Two pins that denote whether the input signals are underrange or overrange.
10	CLKOUT	Updates every LSB.
13	NULL	Denotes Null Position.
14	DIR	Indicates direction. DIR is HI for positive displacement and LO for negative displacement.
15	DGND	Digital Ground.
16	V_{SS}	Negative Power Supply –5.0 V dc ± 5%.
17	V_{DD}	Positive Power Supply +5.0 V dc ± 5%.
18	DEMODOUT	Output of the Phase Sensitive Demodulator.
19	DEMODIN	Input to Phase Sensitive Demodulator.
20	ACERROR	AC Error Output.
21	VCO GAIN	Sets the VCO gain internally. Connect to VEL for 2400 LSB/s. Disconnect for 800 LSB/s.
22	INTIN	Determines system dynamics connect C and RC (serial) parallel combination across INTIN and VEL to determine loop dynamics.
23	VEL	Analog Velocity Output.
24	REF	Single ended input for fixed amplitude reference.
27, 28	B, A	Uncommitted differential inputs for the A, B signal inputs.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD2S93 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

GLOSSARY OF TERMS

INTEGRAL LINEARITY

Integral linearity deviation as a percent of full scale. A 0.1% deviation is equivalent to 8-LSB change on the output.

Gain

The converter gain is the maximum variation in the ratio of A–B/REF/2 to the maximum digital input.

Output Offset

The output offset is the digital output code when the analog input signal A–B = 0.

Overrange (OVR)

OVR goes high when A–B is in phase with REF and larger than REF/2.

Underrange (UNR)

UNR goes high when A–B is out of phase with REF and larger than REF/2.

PRINCIPLE OF OPERATION

The AD2S93 is based on a Type 2 tracking closed-loop principle. The output tracks the position of the LVDT without the need for external convert and wait states. As the transducer moves through a position equivalent to the least significant bit weighting, the output is updated by one LSB. On the AD2S93, CLKOUT updates corresponding to one LSB increment. Figure 1 illustrates the principle of operation.

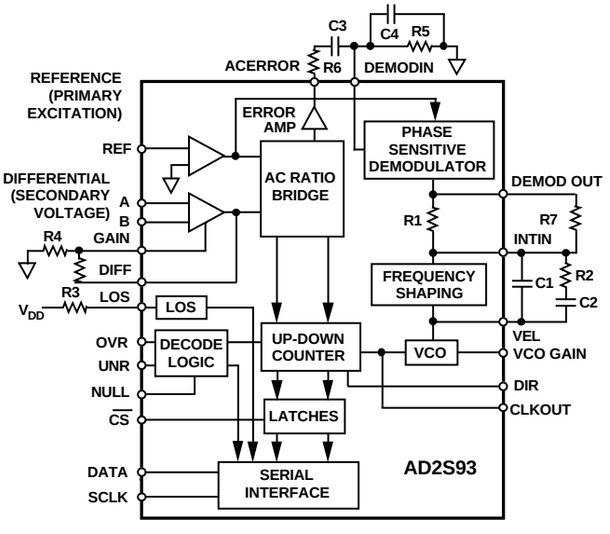


Figure 1. Functional Block Diagram

Because the conversion depends on the ratio of the input signals (ratiometric ac bridge), the AD2S93 is remarkably tolerant of input amplitude and frequency. This, combined with the definable Type 2 tracking closed-loop guarantees the AD2S93's repeatability for a given input. A phase sensitive detector, integrator and voltage controlled oscillator (VCO) form a closed loop system which seeks to null the output of the ACERROR. When this is accomplished the word state of the up/down counter equals within the rated accuracy of the converter, the LVDT position output.

For more information on the operation of the converter, see "Circuit Dynamics" section.

DATA FORMAT

OPERATING RANGE

The AD2S93 operating range is defined in Figure 2. The linearity and specified operating range of the converter is the central two 12-bit quadrants through zero. The corresponding input relationship is –REF/2 ≤ A–B ≤ +REF/2, (± is used to denote phase coherency). The sign bit is low for inputs with A–B in phase with REF. The two remaining 12-bit quadrants are used to denote over (OVR) and underrange (UNR). OVR goes high when A–B is in phase with REF and larger than REF/2. UNR goes high when A–B is out of phase with REF and larger than REF/2. LOS is an open drain output which pulls high when A and/or B are removed or REF is removed (see "Inbuilt Diagnostics"), or A + B is less than 100 mV.

SCALING THE INPUTS

In order to match the LVDT output to the AD2S93 output, the inputs to the AD2S93 need to be scaled. The operating range is illustrated in Figure 2. The AD2S93 operates across ±12-bit range where the remaining 12-bit quadrants are used to denote overrange and underrange. The output position word is a function of the ratio between A–B and V_{REF} (see Figure 2) where:

$$\pm FSR = \frac{(A-B)}{V_{REF}/2}$$

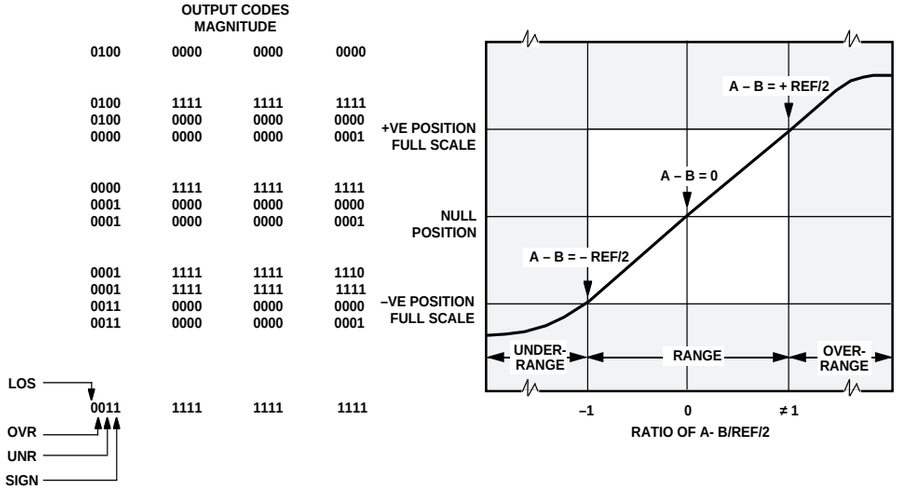


Figure 2. Output Code Format

If the maximum operating stroke of an LVDT yielded a 1 V rms A–B output, the weighting of the LVDT to AD2S93 digital output would be:

$$\frac{Input\ Signal\ Full\ Scale}{Full\text{-}Scale\ Operating\ Range\ (\pm 2^{12})}$$

$$\frac{1 \times 2\sqrt{2}}{2^{13}}$$

$$Input\ Scaling = 345\ \mu V/LSB$$

This can be equated directly to the LVDT sensitivity specification in mm/v/v.

Note: The overrange and underrange quadrants can be utilized by decoding the overrange and underrange MSBs and decoding the 12 magnitude bits. This will increase the operating range of the AD2S93 accordingly. However, if the input A–B > V_{REF} then the converter will lose track of the input and will only regain track when the input signal returns to within the operating range of the converter.

INPUT GAIN

Since the transformation ratio of an LVDT or RVDT from excitation voltage to signal voltage can be 1:0.15, provision for gain scaling has been provided. The gain can, therefore, be selected to ensure that the full-scale output of converter represents the maximum stroke position of the transducer.

The gain setting is accomplished by connecting Pin 2, (DIFF) and Pin 3 (GAIN) together (unity gain) or connecting two resistors as shown in Figure 3.

The gain of the input stage is calculated using the following equation:

$$\frac{DIFF(A-B)}{(A-B)\ IN} = 1 + \frac{R_3}{R_4}$$

e.g., For a gain of 5, R3 = 12 kΩ, R4 = 3 kΩ
For a gain of 10, R3 = 18 kΩ, R4 = 2 kΩ

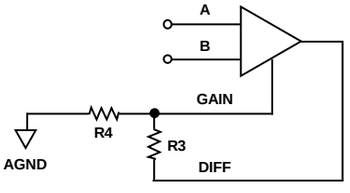


Figure 3. Pre-Amp Gain Block

SETTING THE CONVERTER BANDWIDTH

The AD2S93 bandwidth is set by placing three external components, C1, C2, and R2, around the integrator as illustrated by the figure below.

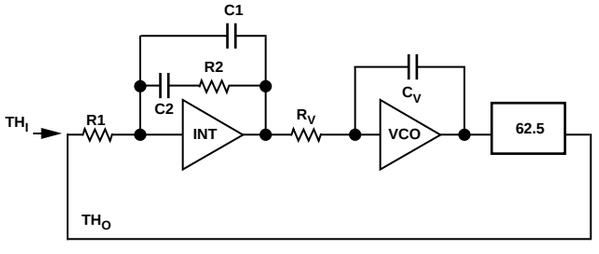


Figure 4. Integrator and VCO

Before the bandwidth can be set, the corresponding VCO gain setting must be determined. The VCO gain is directly related to the slew rate of the converter. This is set internally to two different rates defined internally by R_V.

Typical converter slew rates are defined below,

G (1) = 2400 *LSB/ms–Mode* 1
G (2) = 800 *LSB/ms–Mode* 2

Calculation of the component values for the bandwidth is detailed below. For more detailed information on component value selection for the AD2S93, please consult the "Passive Component Selection and Dynamic Modeling Software for the AD2S93 LVDT-to-Digital Converter."

VCO Gain G (1) Mode 1
The available bandwidth with this option is from 0.5 kHz to 1.25 kHz.

$$F_{REF} > 8 \times Fo$$
$$C1 = 1/(800 \times Fo^2)$$
$$C2 = 8 \times C1$$
$$R2 = 45 \times Fo$$

Where F_{REF} is the reference frequency, Fo is the closed-loop 3 dB point.

VCO Gain G (2) Mode 2
The available bandwidth with this option is from 45 Hz to 500 Hz.

$$F_{REF} > 8 \times Fo$$
$$C1 = 1/(2400 \times Fo^2)$$
$$C2 = 8\ C1$$
$$R2 = 45 \times Fo$$

Where F_{REF} is the reference frequency, Fo is the closed-loop 3 dB point.

INTERFACING TO THE AD2S93 (SEE "TIMING CHARACTERISTICS")
The absolute position information is extracted via a three-wire interface, DATA, $\overline{CS}$ and SCLK. The DATA output is held in a high impedance state when $\overline{CS}$ is high.

Upon the application of logic low to the $\overline{CS}$ pin, the DATA is enabled and the current position information is transferred from the counters to the serial interface. Data is retrieved by applying an external clock to the SCLK pin. The maximum data rate of the SCLK is 2 MHz. To ensure secure data retrieval, it is important to note that SCLK should not be applied until a minimum period of 600 ns after the application of logic low to $\overline{CS}$. Data is then clocked out on successive positive edges of SCLK: 16 clock edges are required to extract the entire data word. Subsequent positive edges greater than the defined resolution of the converter will clock zeros from the data output if $\overline{CS}$ remains in a low state. The format of the data read is shown in Table I.

Table I.

	DB0	DB1	DB2	DB3	DATA DB4–D15 MSB LSB
Function	LOS	OVR	UNR	SIGN	MAGNITUDE

If less than the full 16-bit word is required, then the data read can be terminated by releasing $\overline{CS}$ after the required number of bits have been read.

$\overline{CS}$ can be released a minimum of 100 ns after the last positive edge. If the user is reading data continuously, $\overline{CS}$ can be reapplied after a minimum of 600 ns after it is released. The minimum repetitive read time of the same converter is given by (16 bits read @ 2 MHz). Min RD Time = [600 + (16 × 500) + 600] = 9.2 μs.

IN-BUILT DIAGNOSTICS
The first three bits read from the serial interface preceding the sign and magnitude data can be used to determine whether the data is valid or not. Over and underrange (OVR, UNR) denote the two extremes of the LVDT stroke where linearity of the LVDT may degrade. Loss of signal LOS is an open drain output which pulls high (12 kΩ pull up) when one of the following conditions is satisfied:

1. A and/or B is disconnected.
2. REF is disconnected.

Note: LOS has a response time of 50 ms max to the conditions stated above, see "Specifications."

CONNECTING THE CONVERTER
Positive power supply V_{DD} = +5 V dc ± 5% should be connected to Pin 17 and negative power supply V_{SS} = –5 V dc ± 5% to Pin 16. *Reversal of these power supplies will destroy this device.* For LVDT connections to the converter please refer to Figures 5 through 7. On all connections, the maximum input reference signal V_{REF} = 2.0 V rms ± 10%. To operate within the standard operating range, A–B should not exceed 1.0 V rms ± 10%. The AD2S93 AGND point is the point at which all analog signal grounds should be connected. Ground returns from the LVDT should be connected to AGND. The AD2S93 DGND pin should be connected to the AD2S93 AGND pin. Ancillary Digital circuitry must be connected to the Star Point and not to the AD2S93 AGND pin.

In all cases, the AD2S93 has been configured with the following dynamics.

Reference Frequency	5 *kHz*
3 *dB Bandwidth*	625 *Hz*

Vco Gain is set in MODE 1 where VCO GAIN is connected to VEL.

Using the procedure described in "setting the converter bandwidth" the following preferred values (E12 series) were calculated:

$$C1 = 3.3\ nF$$
$$C2 = 27\ nF$$
$$R2 = 27\ k\Omega$$

CALCULATING HF FILTER (C3, C4, R5, R6)

$$15\ k\Omega \le R5 = R6 \le 56\ k\Omega$$

$$C3 = C4 = \frac{1}{2\pi\ R5\ F_{REF}}$$

So, C3 = 1 nF, R5 = R6 = 33 kΩ, C4 = 1 nF and in all cases R7 = 15 kΩ.

Half-Bridge Type LVDT Connection
In this method of connection, it is necessary to add two additional bridge completion resistors R_C and R_C, in order to derive a reference for the AD2S93. In selecting the bridge completion resistor, it is important to remember that mismatch between R_{C1} and R_{C2} will cause nonzero errors at null. If two LVDTs are being used for differential measurements, the resistors can be replaced by the second LVDT.

Three- or Four-Wire LVDT Connection

In this method of connection, shown in Figure 6, the converters digital output is proportional to the ratio:

$$\frac{(A-B)}{(A+B)/2}$$

where A and B are the individual LVDT secondary output voltages. Inspection of Figure 6 should demonstrate why this relationship is true. (A–B) is simply the voltage across the series connected secondaries of the LVDT and is applied to the A, B input to the converter. (A + B)/2 is effectively the average of the two secondary voltages as computed by the balanced bridge completion resistors and the grounding of the secondary center-tap.

Note: This method of connection is appropriate only for where (A + B) is a constant, independent of LVDT position. Any lack of constancy in (A + B) will be reflected as an additional non-linearity in the output. It is up to the user to determine if (A + B) is sufficiently constant over the particular stroke length employed.

This method will usually restrict the usable LVDT range to half of its full range. The restriction can be eliminated, however, by attenuating DIFF by a factor of 2 or increasing V_{REF} by a factor of 2. This connection method has the tremendous advantage of being insensitive to temperature related phase shifts and excitation oscillator instability effects usually associated with more conventional LVDT conversion systems.

As in the case of the half-bridge type LVDT connection, R_{C1} and R_{C2} are the bridge completion resistors and are matched to a degree sufficient to ensure that the digital output representing the null position does not vary from the LVDT's natural null position. If null adjustment is required, a potentiometer can be used in place of the common connection between the two resistors.

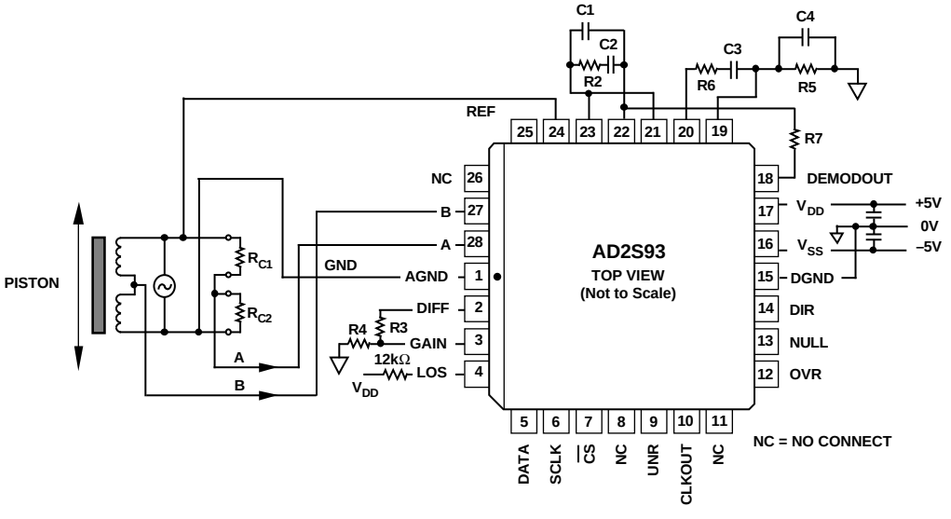


Figure 5. Half-Bridge Type LVDT Connection

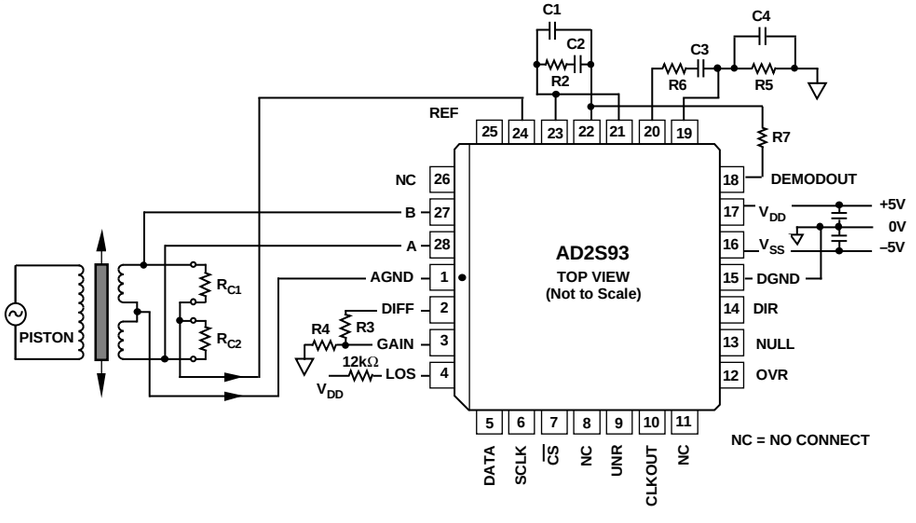


Figure 6. Three- or Four-Wire LVDT Connection

Two-Wire LVDT Connection

This method should be used in cases where the sum of the LVDT secondary output voltages (A + B) is not constant with LVDT displacement over the desired stroke length. This method of connection, shown in Figure 7, still maintains the ratiometric operation and the insensitivity to variations in reference amplitude and frequency. However, the phase shift between V_{REF} and V1 should be minimized to maintain accuracy (see Section "PHASE SHIFT AND QUADRATURE EFFECTS"). Suggested phase compensation circuits are shown in Figure 7.

PHASE SHIFT AND QUADRATURE EFFECTS

Reference to signal phase shift can be high in LVDTs, sometimes in the order of 70 degrees. If the converter is connected as in Figures 5 and 6, any effects due to this phase shift are minimized. This connection method, therefore, provides outstanding benefits.

The additional gain error caused by reference to signal phase shifts is given by:

$$(1 - \cos\theta) \times 100\% \text{ of FSR}$$

where

θ = *phase shift between* V_{REF} *and DIFF.*

When the phase shift between V_{REF} and V1 is zero, additional quadrature on the signal will have no effect on the converter. This is another benefit of the conversion method. For example, when a REF lags (A–B) by approximately 10°, the gain error is approximately 1%. When (A–B) lags REF by approximately 10°, the gain error is approximately 2%.

REMOTE MULTIPLE SENSOR INTERFACING

The DATA output of the AD2S93 is held in a high impedance state until $\overline{CS}$ is taken LO. This allows a user to operate the AD2S93 in an application with more than one converter connected on the same line. Figure 8 shows four LVDTs interfaced to four AD2S93s. Excitation for the LVDT is provided locally by an oscillator.

SCLK, DATA and two address lines are fed down low loss cables suitable for communication links. The two address lines are decoded locally into $\overline{CS}$ for the individual converters. Data is received and transmitted using transmitters and receivers.

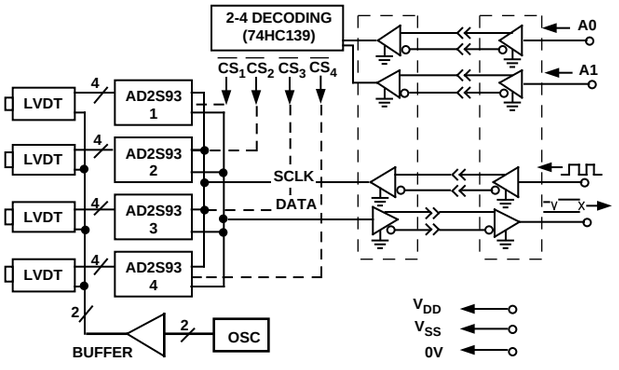


Figure 8. Remote Sensor Interface

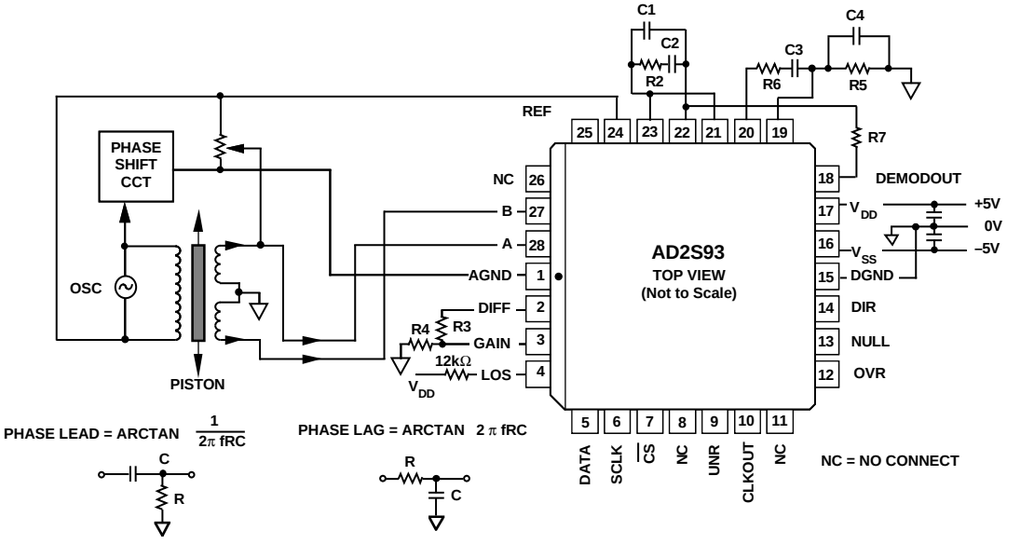


Figure 7. Two-Wire LVDT Connection

CIRCUIT DYNAMICS/ERROR SOURCES

TRANSFER FUNCTION

The AD2S93 operates as a Type 2 tracking servo loop. An integrator and VCO/counter perform the two integrations inherent in a Type 2 loop.

The overall system response of the AD2S93 is that of a unity gain second order low-pass filter, with the position of the LVDT as the input and the digital position data as the output. Figure 9 illustrates the AD2S93 system diagram.

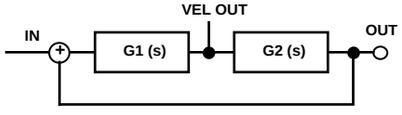


Figure 9. AD2S93 Transfer Function

Note: The AD2S93 has been configured with the following dynamics.

Reference Frequency	10 kHz
3 dB Bandwidth	1250 Hz

VCO Gain is set in MODE 1 where VCOGAIN is connected to VEL.

Using the procedure described in "SETTING THE CONVERTER BANDWIDTH," the following preferred values (E12 series) were calculated:

$C1$ = 820 pF
$C2$ = 6.8 nF
$R2$ = 56 kΩ

C3 = C4 = 470 pF, R7 = 15 kΩ, R5 = R6 = 33 kΩ, C4 = 470 pF

The open-loop transfer function is given by:

$$G1(s) = \frac{K_1}{s} \quad \frac{1+st_1}{1+st_2}$$

$$G2(s) = \frac{K_2}{s}$$

where:

$$t_2 = R_2\left(\frac{C_1 \times C_2}{C_1 + C_2}\right)$$

$t_1 = R_2\, C_2$

and:

$$K_1 = \frac{4\times10^{-3}}{25\times10^{3}} = 160\times10^{-9}\times\frac{1}{C_1+C_2} = 21$$

$$K_2 = \frac{4}{R_V \times C_V}$$

Note A_2 has two values depending on which mode is being used

$K_{2\ (MODE1)} = 640 \times 10^3$
$K_{2\ (MODE2)} = 160 \times 10^3$

The AD2S93 acceleration constant is given by:

$$K_a = K_1 \times K_2$$

Therefore in the example given,

$$K_a = K_1 \times K_2 = 21 \times 640 \times 10^3 = 13.44 \times 10^6\ s^{-2}$$

The AD2S93's design has been optimized with a critically damped response. The closed-loop transfer function is given by:

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{1+st_1}{1+st_1+\frac{s_2}{K_1K_2}+\frac{s_3t_2}{K_1K_2}} \quad \frac{\theta_{OUT}}{\theta_{IN}} = \frac{K_1K_2}{s^2}\ \frac{(1+st_1)}{1+st_2}$$

The normalized gain and phase diagrams are given in Figures 10 and 11 with a bandwidth of 1.25 kHz.

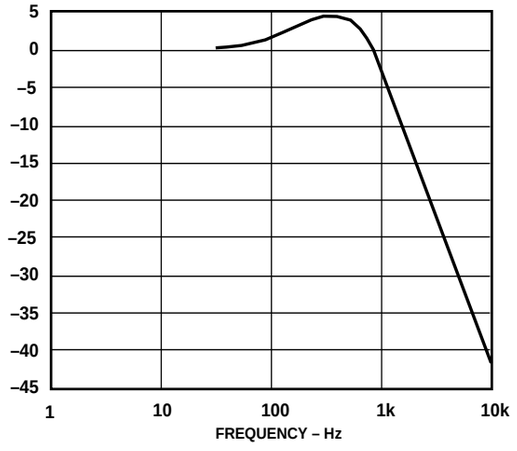


Figure 10. AD2S93 Gain Plot

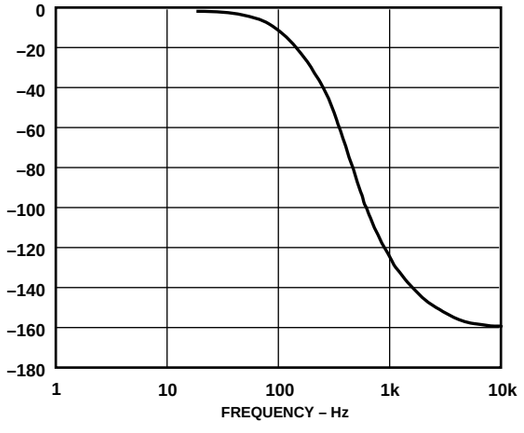


Figure 11. AD2S93 Phase Plot

The small step response is given in Figure 12, and is the time taken for the converter to settled to within 1 LSB.

$$ts = 7\ ms\ (14\text{-}bit\ resolution)$$

The large step response (steps >5% of FSR) applies when the error voltage will exceed the linear range of the converter. Typically it will take three times longer to reach the first peak FSR.

In response to a velocity step [VELOUT/(dθ/dt)] the velocity output will exhibit the same response characteristics as outlined above.

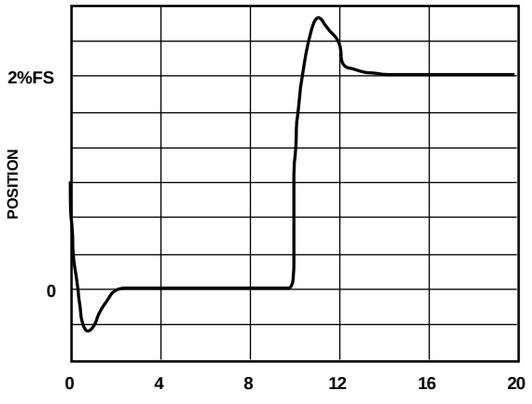


Figure 12. Small Step Response

SOURCES OF ERROR

ACCELERATION ERROR

A tracking converter employing a Type 2 servo loop does not suffer any velocity lag, however, there is an additional error due to acceleration. This additional error can be defined using the acceleration constant K_a of the converter.

$$K_a = \frac{input\ acceleration}{position}$$

The numerator and denominator's units must be consistent. *K_a does not define maximum input acceleration*, only the error due to its acceleration. The maximum acceleration allowable before the converter loses track is dependent on the positional accuracy requirement of the system.

$$Position\ Error \times K_a = LSB/sec^2$$

K_a can be used to predict the output position error for a given input acceleration. The AD2S93 in the example has a $K_a = 13.44 \times 10^6\ sec^{-2}$ if we apply an input accelerating at $100 \times 2^{14}\ LSB/sec^2$.

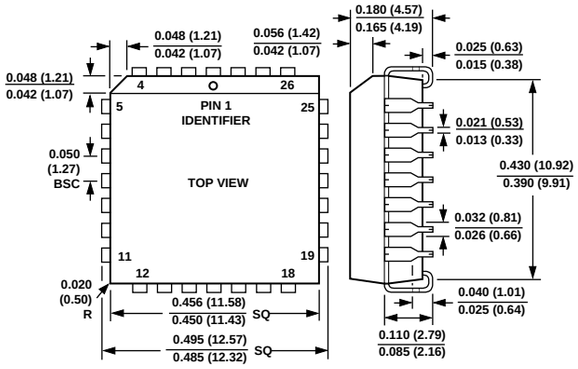
$$Error\ in\ LSBs = \frac{input\ acceleration\left[LSB/sec^2\right]}{K_a\left[sec^{-2}\right]}$$

$$= \frac{100 \times 2^{14}}{13.44 \times 10^6} = 0.12\ LSBs$$

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

P-28A



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