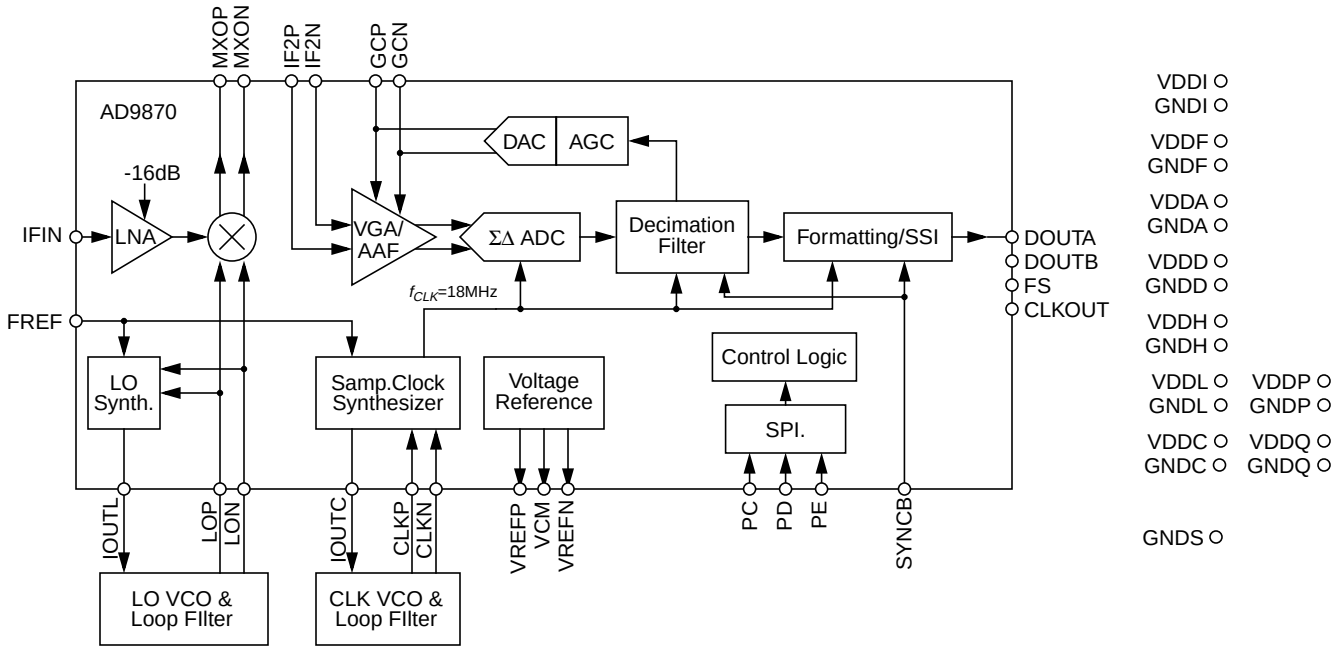
ANALOG DEVICES

IF Digitizing Subsystem

PRELIMINARY TECHNICAL DATA AD9870

FUNCTIONAL BLOCK DIAGRAM



FEATURES

10-300 MHz Input Frequency
Baseband (I/Q) Digital Output
10-150 kHz Output Signal Bandwidth
12 dB SSB NF
> -5 dBm IIP3 (High IIP3 Mode)
25 dB Continuous AGC Range + 16 dB Gain Step
Support for LO and Sampling Clock Synthesis
Programmable Decimation Rate, Output Format, AAF cutoff, AGC and Synthesizer settings
300Ω Input Impedance
2.7-3.6 V Supply Voltage
Low Current: 40 mA typ. (High IIP3 Mode), 30 mA typ. (Low IIP3, Fixed Gain Mode)
48-Pin LQFP package (1.4mm thick)

APPLICATIONS

Portable and Mobile Radio Products
Digital UHF/VHF FDMA products
TETRA

PRODUCT DESCRIPTION

The AD9870 is a general-purpose IF subsystem which digitizes a low-level 10-300 MHz IF input with a bandwidth of up to 150 kHz. The signal chain of the AD9870 consists of a low-noise amplifier, a mixer, a variable gain amplifier with integral anti-alias filter, a bandpass sigma-delta analog-to-digital converter and a decimation filter with programmable decimation factor. An automatic gain control (AGC) circuit provides the AD9870 with 25 dB of continuous gain adjustment. The high dynamic range of the bandpass sigma-delta converter allows the AD9870 to cope with blocking signals which are as much as 70 dB stronger than the desired signal. Auxiliary blocks include clock and LO synthesizers as well as a serial peripheral interface (SPI) port.

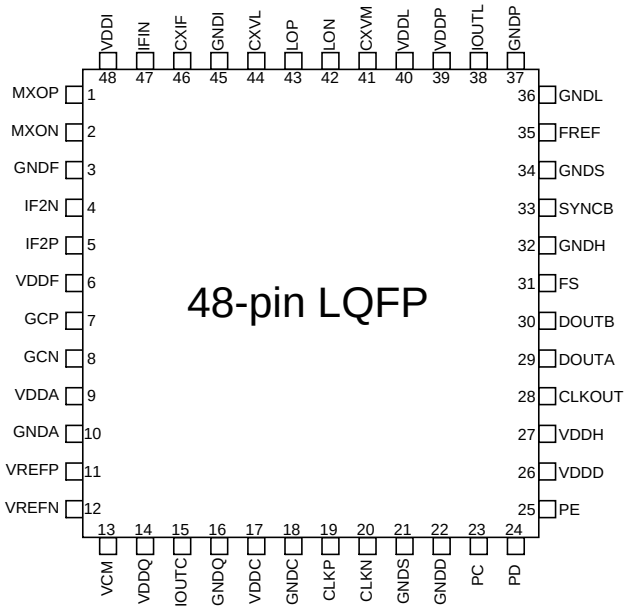
The SPI port programs numerous parameters of the AD9870, including the synthesizer divide ratios, the AGC attack and decay times, the AGC target signal level, the decimation factor, the output data format, the 16 dB attenuator and the bias currents of several blocks. Reducing bias currents allows the user to reduce power consumption at the expense of reduced performance.

AD9870 SPECIFICATIONS

Parameter	Conditions*	Min.	Typ.	Max.	**Units**
OVERALL					
Analog Supply Voltage		2.7	3.0	3.6	V
Digital Supply Voltage		2.7	3.0	3.6	V
Interface Supply Voltage		1.8		3.6	V
Charge Pump Supply Voltage		2.7	3.0	5.5	V
Total Current	High Performance Mode		40		mA
	Low Power Mode		30		mA
	Standby		0.1		mA
SSB Noise Figure	Normal		12		dB
	Low IIP3 setting			TBD	dB
Input Third-Order Intercept (IIP3)	Normal	-5			dBm
	Low IIP3 setting		TBD		dBm
Input Impedance			300		Ω
Gain Variation Over Temperature			2.5		dB
PRE-AMP + MIXER					
Maximum Input and LO Frequencies			300		MHz
LO SYNTHESIZER					
LO Input Frequency		7.75		300	MHz
LO Input Amplitude		0.3		1.0	Vpp
FREF (Reference) Frequency		0.1		25	MHz
FREF Input Amplitude		0.3		3	Vpp
Charge Pump Output Current	Programmable in 0.625 mA steps	0.625		5	mA
Charge Pump Output Voltage		0.25		V_{DDP}-0.25	V
Synthesizer Resolution		6.25			kHz
CLOCK SYNTHESIZER					
CLK Input Frequency		13		18	MHz
CLK Input Amplitude	Clock VCO off	0.3			Vpp
Charge Pump Output Current	Programmable in 0.625 mA steps	0.625		5	mA
Charge Pump Output Voltage		0.25		V_{DDQ}-0.25	V
Synthesizer Resolution		2.2			kHz
MODULATOR					
Clock Frequency (f_{CLK})		13		18	MHz
Center frequency			f_{CLK}/8		
Dynamic Range	BW = 10kHz		88		dB
Passband Gain Variation				0.5	dB
DECIMATOR					
Decimation Factor	programmable in steps of 60	60		960	
Passband Width			50%		
Passband Gain Variation				1	dB
Alias Attenuation		85			dB
GAIN CONTROL					
Programmable gain step			16		dB
AGC Gain Range (continuous)			25		dB
AGC Attack Time	programmable	40		7000	µs
SPI					
PC Clock Frequency				10	MHz
PD Hold Time		10			ns
SSI					
CLKOUT Frequency		1		18	MHz
Output Rise/Fall Time	CMOS output mode, Drive Strength=0			120	ns
	CMOS output mode, Drive Strength=1			45	ns
	CMOS output mode, Drive Strength=2			16	ns
	CMOS output mode, Drive Strength=3			10	ns
Differential Output Voltage	Low-swing differential output mode;		250		mVp
Common-Mode Output Voltage	680Ω between DOUTA and DOUTB		V_{DDH}/2		V
Output Current	Steered-current output mode.		250		µA
OPERATING TEMPERATURE RANGE					
Basic Functions		-40		+85	°C
Meets all specifications		-30		+85	°C

* Standard operating mode: high IIP3 setting, synthesizers in normal (not fast acquire) mode, f_{CLK} = 18 MHz, 25 pF load on SSI output pins; VDD* = 3.0V.

AD9870 PIN-OUT



Pin	Name	Description
1	MXOP	Mixer Output, Positive
2	MXON	Mixer Output, Negative
3	GNDF	Ground for VGA
4	IF2N	Second IF Input (to VGA), Negative
5	IF2P	Second IF Input (to VGA), Positive
6	VDDF	Positive Power Supply for Anti-Alias Filter/VGA
7	GCP	Filter Capacitor for VGA Gain Control, Positive
8	GCN	Filter Capacitor for VGA Gain Control, Negative
9	VDDA	Positive Power Supply for ADC
10	GNDA	Ground for ADC
11	VREFP	Voltage Reference, Positive
12	VREFN	Voltage Reference, Negative
13	VCM	Common Mode Voltage for ADC
14	VDDQ	Pos. Power Supply for Clock Synth. Charge Pump
15	IOUTC	Clock Synth. Charge Pump Output Current
16	GNDQ	Ground for Clock Synth. Charge Pump
17	VDDC	Positive Power Supply for Clock Synthesizer
18	GNDC	Ground for Clock Synthesizer
19	CLKP	Sampling Clock Input/Clock VCO tank, Positive
20	CLKN	Sampling Clock Input/Clock VCO tank, Negative
21	GNDS	Substrate Ground
22	GNDD	Ground for digital functions
23	PC	Clock input for SPI port
24	PD	Data I/O for SPI port

Pin	Name	Description
25	PE	Enable input for SPI port
26	VDDD	Positive Power Supply for internal digital functions
27	VDDH	Positive Power Supply for digital Interface
28	CLKOUT	Clock output for SSI port
29	DOUTA	Data output for SSI port
30	DOUTB	Data output for SSI port, inverted
31	FS	Frame Sync for SSI port
32	GNDH	Ground for digital Interface
33	SYNCB	Resets the SSI and Decimator counters
34	GNDS	Substrate Ground
35	FREF	Reference Frequency Input for both synthesizers
36	GNDL	Ground for LO Synthesizer
37	GNDP	Ground for LO Synthesizer Charge Pump
38	IOUTL	LO Synthesizer Charge Pump Output Current
39	VDDP	Positive Power Supply for LO Synth. Charge Pump
40	VDDL	Positive Power Supply for LO Synthesizer
41	CXVM	External Capacitor for Mixer bias
42	LON	LO Input to Mixer and LO Synthesizer, Negative
43	LOP	LO Input to Mixer and LO Synthesizer, Positive
44	CXVL	External Capacitor for Pre-amp power supply
45	GNDI	Ground for Mixer and Pre-amp
46	CXIF	External Capacitor for Pre-amp bias
47	IFIN	First IF Input (to Pre-amp)
48	VDDI	Positive Power Supply for Mixer and Pre-amp

SERIAL PERIPHERAL INTERFACE (SPI)

The Serial Peripheral Interface (SPI) is a bidirectional serial port. It is used to load configuration information into the registers listed below as well as to read back their contents. Table 1 provides a list of the registers which may be programmed through the SPI port. Addresses and default values are given in hexadecimal form.

Address (hex)	Bit Breakdown	Width	Default Value	Name	Description
Power Control Registers					
0x00	(7:0)	8	0xFF	STBY	Standby control bits (REF, LO, CKO, CK, GC, LNAMX, VGA, ADC).
0x01	(7:6) (5:4) (3:2) (1:0)	2 2 2 2	0 0 0 1	LNAB MIXB CKOB ADCB	LNA Bias Current (0=0.5 mA, 1=1 mA, 2=2 mA, 3=3 mA). Mixer Bias Current (0=1 mA, 1=2 mA, 2=3 mA, 3=4 mA). CK Oscillator Bias (0=0.25 mA, 1=0.35 mA, 2=0.53 mA, 3=0.85 mA) ADC Amplifier Bias (0=2.4 mA, 1=3.2 mA, 2=4.0 mA, 3=4.8 mA).
0x02	(7) (6) (5) (4) (3:0)	1 1 1 1 4	0 0 0 X 0	FGM ABB ASVG Not Used LSTP	Put the VGA into fixed gain mode. Enable automatic bias boost of the LNA/Mixer for large signals. Enable automatic switching of VGA into variable gain mode. Large signal trip point. (0=FS/16, 1=2FS/16, 2=3FS/16,… F=16FS/16).
AGC					
0x03	(7) (6:0)	1 7	0 0x3F	ATTEN AGCG(14:8)	Apply 16 dB attenuation in the front end. AGC gain setting (7 MSBs of a 15-bit two's-complement word).
0x04	(7:0)	8	0xFF	AGCG(7:0)	AGC gain setting (8 LSBs of a 15-bit two's-complement word). Default corresponds to maximum gain.
0x05	(7:4) (3:0)	4 4	0 0	AGCA AGCD	AGC attack time setting. Default yields 50 Hz raw loop bandwidth. AGC decay time setting. Default is decay time = attack time
0x06	(7:4) (3) (2:0)	4 1 3	0 0 0	AGCO AGCF AGCR	AGC overload update setting. Default is slowest update. Fast AGC. (Minimizes resistance seen between GCN and GCP.) AGC enable/reference level (disabled, 3, 6, 9, 12,15 dB below clip).
Decimation Factor					
0x07	(3:0)	4	4	M	Decimation factor = 60×(M+1). Default is decimate-by-300.
LO Synthesizer					
0x08	(5:0)	6	0x00	LOR(13:8)	Reference frequency divisor (6 MSBs of a 14-bit word)
0x09	(7:0)	8	0x38	LOR(7:0)	Reference frequency divisor (8 LSBs of a 14-bit word) Default (56) yields 300 kHz from F_{REF}=16.8 MHz.
0x0A	(7:5) (4:0)	3 5	0x5 0x00	LOA LOB(12:8)	"A" counter (prescaler control counter) "B" counter MSBs (5 MSBs of a 13-bit word) Default LOA and LOB values yield 300 kHz from 73.35 -2.25 MHz.
0x0B	(7:0)	8	0x1D	LOB(7:0)	"B" counter LSBs (8 LSBs of a 13-bit word).
0x0C	(6) (5) (4:2) (1:0)	1 1 3 2	0 0 0 0	LOF LOINV LOI LOTM	Enable fast acquire. Invert charge pump (0 = Pump_Up ⇒ IOUTL sources current) Charge pump current in normal operation. I_{pump} = (LOI+1) × 0.625mA Manual control of LO charge pump. (0=off, 1=up, 2=down, 3=normal.)
0x0D	(5:0)	6	0x0	LOFA(13:8)	LO Fast acquire time unit (4 MSBs of a 14-bit word)
0x0E	(7:0)	8	0x04	LOFA(7:0)	LO Fast acquire time unit (8 LSBs of a 14-bit word)
Clock Synthesizer					
0x10	(5:0)	6	00	CKR(13:8)	Reference frequency divisor (6 MSBs of a 14-bit word)

Table 1: SPI Address Map

Address (hex)	Bit Breakdown	Width	Default Value	Name	Description
0x11	(7:0)	8	0x38	CKR(7:0)	Reference frequency divisor (8 LSBs of a 14-bit word) Default yields 300 kHz from F_{REF} =16.8 MHz Min=3, Max = 16383
0x12	(4:0)	5	0x00	CKN(12:8)	Synthesized frequency divisor (5 MSBs of a 13-bit word)
0x13	(7:0)	8	0x3C	CKN(7:0)	Synthesized frequency divisor (8 LSBs of a 13-bit word) Default yields 300 kHz from F_{CLK}=18 MHz Min=3, Max =8191.
0x14	(6) (5) (4:2) (1:0)	1 1 3 2	0 0 0 0	CKF CKINV CKI CKTM	Enable fast acquire. Invert charge pump (0 = Pump_Up ⇒ IOUTC sources current) Charge pump current in normal operation. I_{pump} = (CKI+1)× 0.625mA Manual control of CLK charge pump (0=off,1=up, 2=down, 3=normal).
0x15	(3:0)	4	0x0	CKFA(13:8)	CK Fast acquire time unit (4 MSBs of a 14-bit word)
0x16	(7:0)	8	0x04	CKFA(7:0)	CK Fast acquire time unit (8 LSBs of a 14-bit word)
SSI Control					
0x18	(7:0)	8	0x12	SSICRA	SSI control register A. See Table 2. (Default is FS and CLKOUT tri-stated.)
0x19	(7:0)	8	0x00	SSICRB	SSI control register B. See Table 2.
0x1A	(3:0)	4	1	SSIORD	Output rate divisor. F_{CLKOUT} = F_{CLK}/SSIORD
AAF Capacitor Setting/Calibration					
0x1C	(7:0)	8	0x00	AAR	Anti-alias response selector. 0x60 is recommended.
0x1D	5 (4:0)	1 5	0 0x0	ERRN CAPN	Error flag AAF N-well capacitor setting
0x1E	5 (4:0)	1 5	0 0x0	ERRP CAPP	Error flag AAF Poly-poly capacitor setting
Test Registers					
0x38	7 (6:3) (2:0)	1 4 3	0 0x0 0x0	BLOW unused TRIM	Blow the fuses. Spare fuses Trim-fuse settings.
0x39	0	1	0	MFUSE	Blow master fuse
0x3A	(7:6) (5:4) (3) (2) (1:0)	2 2 1 1 2	0x0 0x0 0 0 0x0	TESTMUX OUTMUX SPIREN AGCM CCTEST	Output test data via SSI output pins. See Table 3. Enable data onto outputs (0= normal mode; 1=modulator; 2=synthesizers, c.f. LOTEST and CKTEST; 3=test data, c.f. TESTMUX field above). Enable read from SPI port. Sigma-delta modulate the AGC DAC. Calibration Counter Test (0=fref, 1=capn, 2=capp)
0x3B	(7) (6) (5) (4) (3) (2) (1) (0)	1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0	LFSR SCAN INOTQ | | TESTB | |	Enable LFSR for decimator test Enable decimator scan out Choose scan of I/Q channel unused Make DOUTB an input Make DOUTA an input Make CLKOUT an input Make FS an input

Table 1: SPI Address Map

Address (hex)	Bit Breakdown	Width	Default Value	Name	Description
0x3C	(7:3) (2) (1) (0)	5 1 1 1	0x00 1 0 0	unused | TESTC |	 Enable reset if modulator indicates instability. Enable AGC test. Enable LO test (select external clock).t
0x3D	(5:3) (2:0)	3 3	0x0 0x0	CKTEST LOTEST	Synthesizer test modes, see Table 4.
0x3E	(7:0)	8	0x40	ADCCR	VGA/ADC control register (Enable turbo reference, VGA offset servo, VGA bias boost, ADC no ESL; ADC fctrl(2:0), bypass VGA)
0x3F	(7:0)	8	01	ID	Revision ID (Read only)

Table 1: SPI Address Map

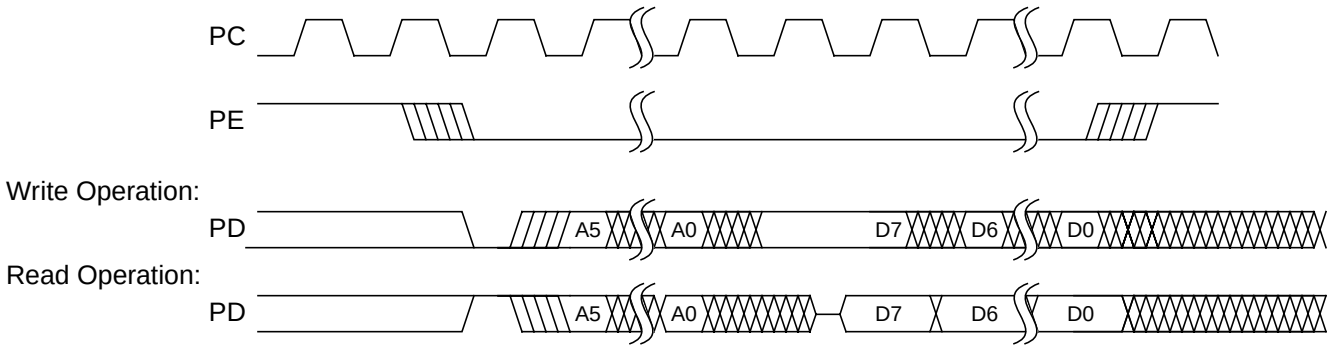


Figure 1. SPI Timing

Fig. 1 illustrates the timing for the SPI port. After the peripheral enable signal (PE) goes low, data (PD) is read on the rising edges of the clock (PC). The first bit is a read/not-write indicator; the next 6 bits are address bits; the 8th bit is ignored; the last 8 bits are data. Address and data are given MSB first. If the read/not-write indicator is a zero, a write operation occurs and the data bits are shifted in. If the read/not-write indicator is a one and if the read-back enable bit has been set, a read operation occurs and data is shifted out the data pin on the falling edges of the clock. PE stays low during the operation and goes high at the end of the transfer. If PE rises before an additional 8 clock cycles have passed, the operation is aborted.

If PE stays low for an additional 8 clock cycles, the destination address is incremented and another 8 bits of data are shifted in. Again, should PE rise early, the current byte is ignored. By using this

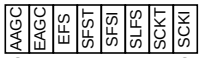
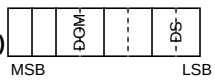
Name	Width	Description
SSICRA (ADDR=0x18) 		
AAGC	1	Alternate AGC data bytes
EAGC	1	Embed AGC data
EFS	1	Embed frame sync
SFST	1	Tristate frame sync
SFSI	1	Invert frame sync
SLFS	1	Late frame sync (1=late, 0=early)
SCKT	1	Tristate CLKOUT
SCKI	1	Invert CLKOUT
SSICRB (ADDR=0x19) 		
DOM	2	DOUT mode (0=CMOS, 1=differential voltage, 2=low-level current)
DS	2	FS, CLKOUT and DOUT drive strength (in CMOS mode)

Table 2. SSI Control Registers

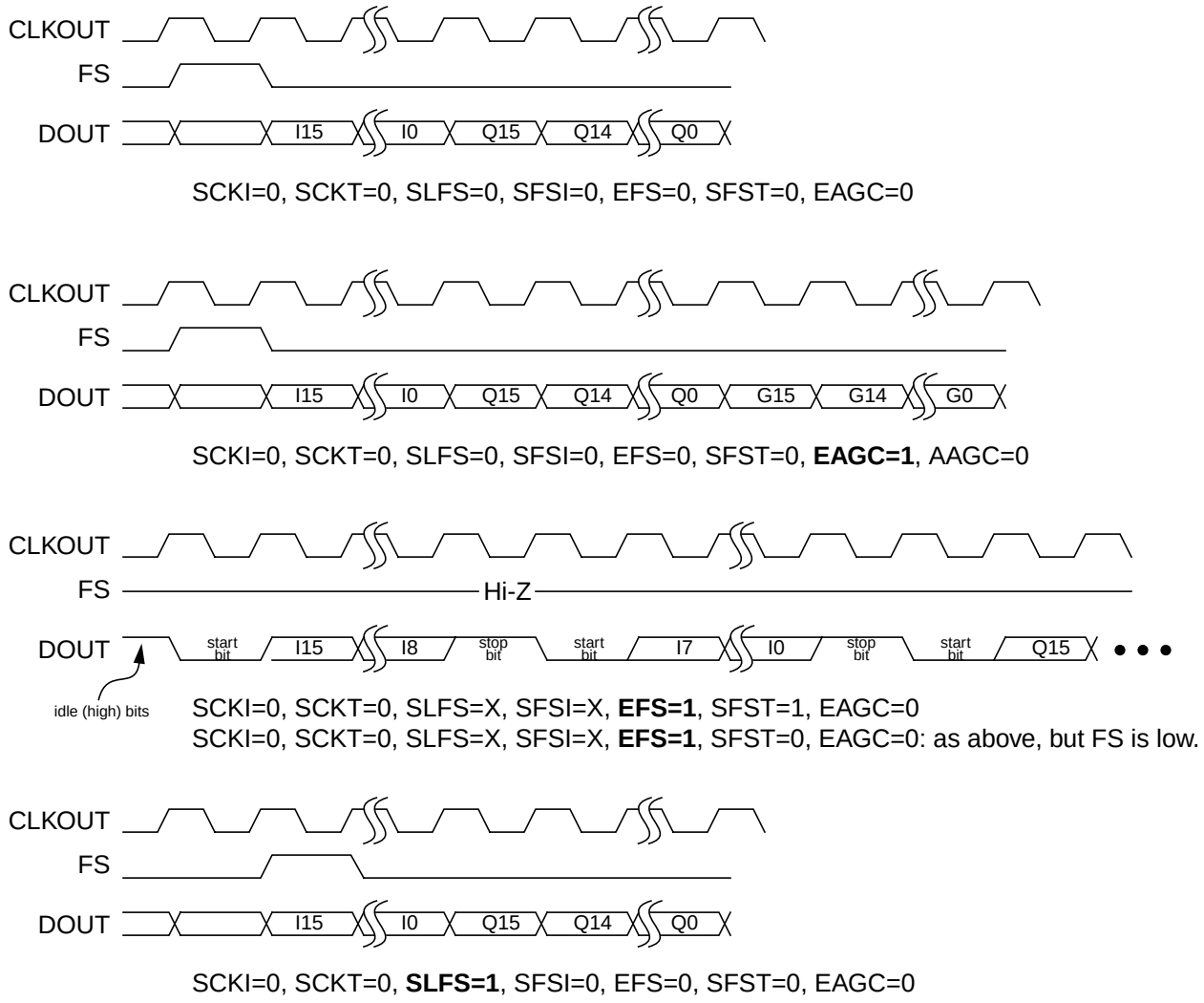


Figure 2. SSI timing for several SSICR settings.

implicit addressing mode, the entire chip can be configured with a single write operation. Registers identified as being subject to frequent updates, namely those associated with power control and AGC operation, have been assigned adjacent addresses to minimize the time required to update them. The auto-increment mode is not supported for read operations.

Multi-byte registers are "big-endian" (the most significant byte has the lower address) and are updated when a write to the least significant byte occurs.

SYNCHRONOUS SERIAL INTERFACE (SSI)

The primary output of the AD9870 is the converted signal, which is available from the SSI port as a serial bit stream. The bit stream consists of a 16-bit I word followed by a 16-bit Q word, where each word is given MSB first and is in 2's-complement form. AGC, signal strength, and synchronization information may also be embedded in the data stream. The output bit rate (f_{CLKOUT}) is equal to the modulator clock frequency (f_{CLK}) divided by the contents of the SSIORD register. Users must verify that the output bit rate is sufficient to

accommodate the required number of bits per frame (see Table 5) and that the chosen output rate does not introduce harmful spurs. Idle (high) bits are used to fill out each frame; the frame lengths listed in Table 5 assume that with embedded frame sync (EFS=1), at least 10 idle bits are desired.

Fig. 2 illustrates the output timing of the SSI port for several SSI control register settings. In the default mode of operation, data is shifted out on rising edges of CLKOUT after a pulse is output from the frame sync (FS) pin. As described above, the output data consists of a 16-bit I sample followed by a 16-bit Q sample plus two optional bytes containing AGC and status information.

The two optional bytes are output if the EAGC bit of SSICRA is set. The first byte contains the 8 most significant bits of the AGC DAC setting while the second byte contains a 2-bit overload field, a 2-bit reset field, a 2-bit large-signal field, a copy of the FGM bit from SPI register 0x02 and a trailing high bit. The overload, reset and large-signal fields contain the number of overload, reset and large-signal events since the last report, respectively, saturating at 3 should the number of events equal or exceed this amount. The two optional bytes follow the I and Q data as a 16-bit word provided the AAGC bit of SSICRA is not set. If the AAGC bit is set, the two bytes follow the I and Q data in an alternating fashion. In this "alternate AGC data" mode, the LSB of the byte containing the AGC DAC setting is zero; the LSB of the byte containing reset/overload information is always a one. Fig. 3 illustrates the fields of the SSI data frames.

OUTMUX	TESTMUX	FS	DOUTB	DOUTA	CLKOUT
0	X	FS	DOUTB	DOUTA	CLKOUT
1	X	V[3]	V[2]	V[1]	V[0]
2	X	LOSYN	0	0	CLKSYN
3	0	MODRB	0	0	dec1_scan
3	1	CC[3]	CC[2]	CC[1]	CC[0]
3	2	0	0	0	0
3	3	0	0	0	0

CKTEST 3D(5:3)	Signal from CLK synthesizer to CLKOUT mux
0	GND
1	CPD
2	CPU
3	R counter
4	N counter
5	
6	
7	

LOTEST 3D(2:0)	Signal from LO synthesizer to FS mux
0	GND
1	LOPD
2	LOPU
3	R counter
4	B counter
5	A counter
6	Prescaler
7	

Table 4. Synthesizer test modes

M	Dec'n Factor	Output Sample Rate (ksps, for f_{CLK}=18MHz)	Max. SSIORD Setting (decimal)			
			EAGC=0		EAGC=1	
			EFS=0	EFS=1	EFS=0	EFS=1
Bits per sample (min. no. of bits per frame)			32	49	48/40*	69/59*
0	60	300	1	1	1	1
1	120	150	3	2	2	1
2	180	100	5	3	3	2
3	240	75	7	4	5	3
4	300	60	9	5	6	4
5	360	50	11	7	7	5
6	420	42.857	13	8	8	5
7	480	37.5	14	9	10	6
8	540	33.333	15	10	11	7
9	600	30	15	11	12	8
10	660	27.272	15	13	13	9
11	720	25	15	14	14	10
12	780	23.077	15	15	15	11
13	840	21.428	15	15	15	11
14	900	20	15	15	15	12
15	960	18.75	15	15	15	13

Table 5. Max. legal SSIORD values.
$f_{CLKOUT} = f_{CLK}/SSIORD$

* If the AAGC bit of SSICRA is set.

When the embedded frame sync bit (EFS) is set, FS is either low or tri-stated (as determined by the SFST bit) and framing information is embedded in the data stream. In this mode, each 8 bits of data are surrounded by a start bit (low) and a stop bit (high), and each frame ends with at least 10 high bits. Other control bits can be used to invert the frame sync (SFSI), to delay the frame sync pulse by one clock period (SLFS), to invert the clock (SCKI), or to tri-state the clock (SCKT). Note that if EFS is set, SLFS is a don't-care.

The AD9870 also provides the means for controlling the switching characteristics of the digital output signals. With a 25 pF load, the rise and fall times of these signals are no more than 120, 45, 16 or 10 ns if the DS (drive strength) setting is 0, 1, 2 or 3, respectively.

If greater control of the digital output spectrum is required, the mode of the DOUT signal can be selected from one of three formats using the DOM bit-field. In the single-ended CMOS output mode (DOM=0), DOUTA is active, DOUTB is low and the switching characteristics are controlled by the DS bit-field. In the differential output mode (DOM=1), DOUTA and DOUTB are complementary low-swing signals whose difference is nominally 250mV, assuming a 680 Ω resistor is tied between the DOUTA and DOUTB terminals. In this mode, a logic one is indicated if DOUTA is higher than DOUTB. In the steered current output mode (DOM=2), a logic one is represented with DOUTA sourcing 250 µA and DOUTB tri-stated, and vice versa for a logic zero.

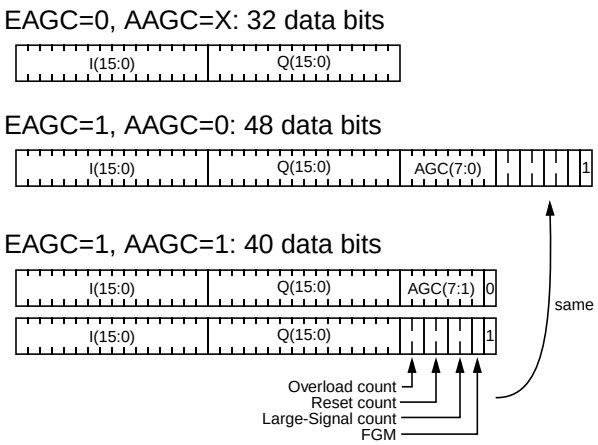


Figure 3. SSI frame structure.

POWER CONTROL

To allow power consumption to be minimized, the AD9870 possesses numerous SPI-programmable power-down and bias control bits.

Each major block may be powered down through the appropriate bit of the STBY register. This scheme provides the greatest flexibility for configuring the IC to a specific application as well as for tailoring the IC's power-down and wake-up characteristics. Table 6 summarizes the function of each of the STBY bits.

The AD9870 also allows control over the bias current in several key blocks. The effects on current consumption and system performance are de-

STBY bit	Effect	Current Reduction (mA)*	Wake-up Time (ms)
REF	Voltage reference off; VREFP, VREN tri-state;	1.5	1.0 (C_{REF}= 4.7µF)
LO	LO synthesizer off; IOUTL tri-state.	4.8	†
CKO	Clock oscillator off;	0.25	†
CK	Clock synthesizer off; IOUTC tri-state. Clock buffer off if ADC is off;	1.4	†
GC	Gain control DAC off. GCP, GCN tri-state.	3	Depends on C_{GC}
LNAMX	LNA and Mixer off. I(VDDI)=0 CXVM, CXVL, CXIF tri-state.	10	TBD
VGA	VGA/AAF off IF2P, IF2N tri-state.	6	0.1
ADC	ADC off; Clock buffer off if CK synth. off; VCM tri-stated; clock to digital filter suspended; digital outputs static.	13.8	0.1

Table 6. Standby control bits.

* When all blocks are in standby, the master reference circuit is also put into standby and thus the current is reduced by a further 0.4 mA.
† Wake-up time is application-dependent.

scribed in the section dealing with the affected block.

LO SYNTHESIZER

The LO synthesizer is a fully programmable integer-*N* PLL capable of 6.25 kHz resolution at input frequencies up to 300 MHz and reference clocks of up to 25 MHz. The circuit includes a 14-bit reference divider, a dual-modulus 8/9 prescaler, and a 13-bit main counter. The charge pump current is programmable from 0.625 mA to 5.0 mA. An on-chip lock detect function (enabled by the LOF bit) automatically increases the output current for faster settling during channel changes. The loop filter resides off-chip, as does the VCO. The synthesizer may be disabled using the LO standby bit if it is not needed.

The fast acquire circuit attempts to boost the output current when the phase difference between the divided-down LO and the divided-down reference frequency exceeds the threshold determined by the LOFA (0x0D, 0x0E) register. The LOFA register specifies a divisor for the FREF signal, and it is the period (*T*) of this divided-down clock that specifies the time interval which controls the fast acquire algorithm. Assume for the moment that the nominal charge pump current is at its lowest setting (i.e. LOI=0) and denote this minimum current by I_0. Then when the output pulse from the phase comparator exceeds *T*, the output current for the next pulse is $2I_0$; when the pulse is wider than 2*T*, the output current for the next pulse is $3I_0$, and so forth, up to eight times the minimum output current. If the nominal charge pump current is more than the minimum value (i.e. LOI > 0), the preceding rule is only applied if it results in an increase in the instantaneous charge pump current. If the charge pump current is set to its lowest value (LOI = 0) and the fast acquire circuit is enabled, the instantaneous charge pump current will never fall below $2I_0$, even when the pulse width is less than *T*. Thus the charge pump current when fast acquire is enabled is given by

$$I = I_0(1 + max(1, \text{LOI}, \text{Pulse\_Width}/T)).$$

The recommended setting for LOFA is LOR/16. Choosing a larger value for LOFA will increase *T*. Thus, for a given phase difference between the LO input and the FREF input, the instantaneous charge pump current will be less than that available for a LOFA value of LOR/16. Similarly, a smaller value for LOFA will decrease *T*, making more current available for the same phase difference. In other words, in general, a smaller value of LOFA will enable the synthesizer to settle faster in response to a frequency hop than will a large LOFA value. Care must be taken to choose a value of LOFA which is large enough (values greater than 4 recommended) to prevent the loop from oscillating back and forth in response to a frequency hop.

The synthesized frequency is related to the reference frequency and the LO register contents as follows:

$$f_{LO} = \frac{8 \cdot \text{LOB} + \text{LOA}}{\text{LOR}} f_{REF}.$$

The minimum allowable value in the LOB register is 3.

CLOCK SYNTHESIZER

The clock synthesizer is a fully programmable integer-*N* PLL capable of 2.2 kHz resolution at clock input frequencies up to 18 MHz and reference frequencies up to 25 MHz. The circuit includes a 14-bit reference divider, a 13-bit main counter and a fast acquire subcircuit controlled by the CKFA (0x15, 0x16) register in the same manner as the LO synthesizer is controlled by the LOFA register. The charge pump current has the same range as that of the LO synthesizer. The loop filter resides off-chip, but a negative-resistance core is integrated on-chip so that only an external LC tank is needed to realize an oscillator. The synthesizer may be disabled via the CK standby bit to allow the user to employ an external synthesizer and/or VCO in place of those resident on the IC.

MIXB / LNAB	00	01	10	11
00	3.3	4.1	5.1	6.0
01	3.7	4.6	5.5	6.4
10	5.0	5.9	6.8	7.7
11	5.8	6.7	7.6	8.5

Table 7. Current consumption (mA) through the VDDI pin as a function of the LNAB and MIXB bias current settings.

MIXB / LNAB	00	01	10	11
00	-21	-13	-9	-7
01	-21	-13	-8	-5
10	-20	-12	-6	-3
11	-20	-11	-5	-2

Table 8. IIP3 (dBm) as a function of the LNAB and MIXB bias current settings at f_{IF1}=73 MHz.

MIXB / LNAB	00	01	10	11
00	7.8	7.4	7.7	6.9
01	7.9	7.6	7.0	6.9
10	7.7	7.5	7.0	7.6
11	8.0	7.8	7.0	7.6

Table 9. Noise figure as a function of the LNAB and MIXB bias current settings.

IF1 INPUT

The input resistance at the IFIN pin is 300 Ω ± 20% and has no significant variation with respect to the programmable bias settings. Tables 7 to 9 show how the current consumption, IIP3 and NF vary as functions of the LNAB and MIXB bias current settings. These tables apply to the LNA/Mixer only; they do not include contributions from either the VGA or the ADC.

ANTI-ALIAS FILTER

The AD9870 includes a programmable continuous-time anti-alias filter (AAF) which consists of a programmable capacitor at the mixer output plus a programmable filter built into the VGA. Fig. 4 shows the response of the anti-alias filter when it has been tuned with AAR=0x60 at an ADC clock frequency of 18 MHz. The capacitor across the mixer load resistors yields a pole at 5 MHz, which degrades the mixer gain at 2.25 MHz by approximately 0.8 dB. The nominal -3 dB cutoff frequency of the anti-alias filter is 5.6 MHz. The nominal attenuation at the first alias (15.75 MHz) is 28 dB and falls at 60 dB/decade so that the nominal attenuation at 100 MHz is 78 dB.

The shape of the AAF response is effectively fixed, but the frequency axis can be scaled so that

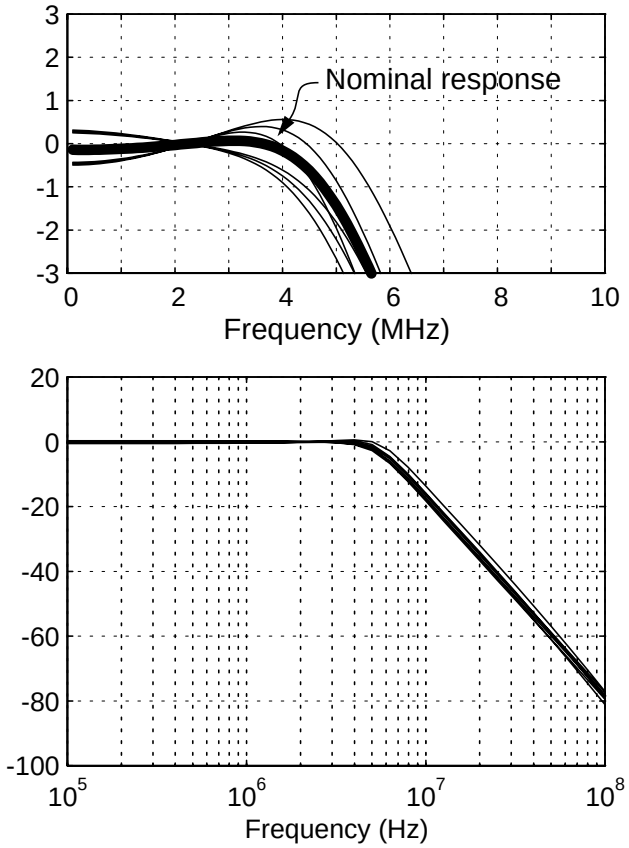


Figure 4. Anti-alias filter response with AAR=0x60 and f_{CLK} = 18 MHz. The curves have been normalized individually to 0 dB at f_0 = 2.25 MHz.

the -3 dB cutoff frequency ranges from 3.5 to 13 MHz. The recommended cutoff is f_{CLK}/3.2, and for this setting the frequency-scaling resolution is sufficient to yield less than 10% tuning error with clock frequencies between 13 and 18 MHz.

The user initiates tuning of the AAF by writing a value to the AAR (anti-alias response) register. The AD9870 measures the oscillation frequency of an on-chip RC oscillator relative to the frequency applied to the CLKP,CLKN pins and then uses this measurement in conjunction with the AAR setting to program the capacitors of the AAF. Since the frequency measurements are performed relative to the clock frequency, the anti-alias characteristics (e.g image attenuation) are independent of the ADC clock frequency.

The on-chip circuitry sets the capacitor-programming registers (CAPN and CAPP) to the required values based on the clock frequency and the AAR setting. There is guaranteed to be sufficient range in the programmable capacitor arrays to support the response of Fig. 4 for clock frequencies between 13 and 18 MHz with the resolution indicated. If the user specifies an unattainable response, the on-chip circuitry sets CAPN and/or CAPP to the limit of their ranges and also sets the ERRN and/or ERRP bit to indicate that the specified response cannot be supported.

Changing the AAR setting from the recommended value of 0x60 scales the frequency axis in an inverse way. For example, to scale the frequency response shown in Fig. 4 down by a factor of 1.5 (which would increase the attenuation at the first alias by 10 dB, lower the -3 dB cutoff from 5.6 to 3.7 MHz for f_{CLK} = 18 MHz, and reduce the mixer gain by 0.8 dB due to the reduced mixer pole frequency), set the AAR register to 1.5 times 0x60, i.e. 0x90. This AAR setting will not cause an error flag to be set for f_{CLK} = 18 MHz since the 3.7 MHz cutoff is within the guaranteed range. However, AAR=0x90 will result in programming errors at f_{CLK} = 13 MHz in many parts since the -3 dB cutoff of 2.7 MHz is well below the 3.5 MHz lower limit.

AAF parameter	Location	
	AAR=0x60 and f_{CLK}= 18 MHz	General Formula
Mixer pole	5.0 MHz	f_{CLK}/(AAR/27)
-1 dB point	4.7 MHz	f_{CLK}/(AAR/25)
-3 dB point	5.6 MHz	f_{CLK}/(AAR/35)
-20 dB point	11.5 MHz	f_{CLK}/(AAR/61)

Table 10. Nominal AAF response points.

Table 10 lists key points on the AAF response and their values for the standard operating mode as well as for the general case.

FIXED VS. VARIABLE GAIN

As one of the power-saving features of the AD9870, the VGA can be programmed to operate as a fixed-gain amplifier which consumes 4.7 mA less current than the full-function VGA. The fixed-gain amplifier is intended for use under “small-signal” conditions where gain control using the VGA is not necessary. The gain in fixed-gain mode is within 1 dB of the maximum gain of the VGA.

When in the fixed gain mode, the user may choose to have the AD9870 detect the presence of large signals and automatically switch to variable gain mode; this feature is enabled by setting the ASVG bit. The switch back to fixed gain is done by writing a ‘1’ to the FGM bit. Furthermore, by setting the ABB bit, the user may also choose to have the LNA and mixer bias currents set to maximum if large signals are detected. The detection of large signals is done at the input of the ADC and the trip point is programmable in steps of FS/16 via the LSTP bit field. As described in the section on the SSI, the number of “large signal” events which were detected since the last report as well as a bit indicating that the VGA is in fixed-gain mode may be included in the SSI data stream. This feature allows the user to decide when it is safe to switch back to a lower

current mode or to implement a more sophisticated power control scheme.

AUTOMATIC GAIN CONTROL (AGC)

When in variable gain mode (FGM=0), the gain of the VGA can be adjusted automatically or held at a specific setting. The gain is set by writing to the 16-bit AGCG register. The MSB of this register is the bit which enables 16 dB of attenuation in the pre-amp. The maximum update rate of the AGCG register is f_{CLK}/100. If fixed-gain mode (FGM=1), the VGA gain control is at maximum and writes to the VGA gain control bits have no effect. Other registers which control various parameters used in the AGC algorithm may be updated at f_{CLK}/20. A description of the adjustable parameters follows.

The 3-bit AGCR field enables automatic gain control and sets the reference (target) signal level. Reference levels of 3, 6, 9, 12 and 15 dB below the saturation (clip) level of the ADC (which is defined as -2 dB relative to full-scale) can be chosen by writing values from 1 to 5 to the AGCR field. If AGCR is 0, automatic gain control is disabled.

The 4-bit code in the AGCA field sets the raw bandwidth of the AGC loop. If AGCA is 0, the AGC loop bandwidth is approximately 50 Hz. Increasing AGCA by one multiplies the bandwidth by a factor of $\sqrt{2}$; thus the maximum loop bandwidth is $50 \times 2^{7.5} = 9\ \text{kHz}$. A general expression for the attack bandwidth is

$$BW_A = 50\left(\frac{f_{\text{CLK}}}{18\ \text{MHz}}\right) \times 2^{\left(\frac{\text{AGCA}}{2}\right)}\ \text{Hz},$$

and the corresponding attack time is

$$t_{\text{attack}} = \frac{2.2}{2\pi BW_A} = \frac{0.35}{BW_A}.$$

The 4-bit code in the AGCD field sets the ratio of the attack time to the decay time in the amplitude estimation circuitry. When AGCD is zero, this ratio is one. Incrementing AGCD multiplies the decay time-constant by $\sqrt{2}$, allowing a 180:1 range in the decay time relative to the attack time. The decay time may be computed from

$$t_{\text{decay}} = t_{\text{attack}} \times 2^{\left(\frac{\text{AGCD}}{2}\right)}.$$

The 4-bit code in the AGCO field sets the weighting applied to gain updates when overload is detected. Each increment in AGCO doubles the weighting factor. At the highest AGCO setting, each reset event will cause a 6.25 dB reduction in the VGA gain.

Lastly, the AGCF bit reduces the DAC source resistance by a factor of 10. This facilitates fast acquisition by lowering the RC time constant which is formed with the external capacitors connected from the GCP and GCN pins to ground. For an overshoot-free step response in the AGC loop, the capacitors should be chosen such that the RC time constant is less than one quarter that of the raw loop. Specifically,

$$RC \le \frac{1}{8\pi BW}, \qquad \textbf{(1)}$$

where R is the resistance between the GCN and GCP pins and ground (30 kΩ±30% if AGCF=0, <3 kΩ if AGCF=1) and BW is the raw loop bandwidth. Note that with C chosen at this upper limit, the loop bandwidth increases by approximately 30%.

DECIMATION FILTER

The decimation filter consists of a complex mix by f_{CLK}/8 and a cascade of three linear phase FIR filters: DEC1, DEC2 and DEC3. DEC1 downsamples by a factor of 20 using a 4^{th}-order comb filter. DEC2 also uses a 4^{th}-order comb filter, but its decimation factor is set by the M control register. DEC3 is a decimate-by-3 FIR filter.

Fig. 6 shows the response of the complete decimation filter on a linear frequency axis for frequencies up to the third alias. As this figure shows, the alias with the least attenuation is located at the lower end of the third alias band and has an attenuation of 83 dB.

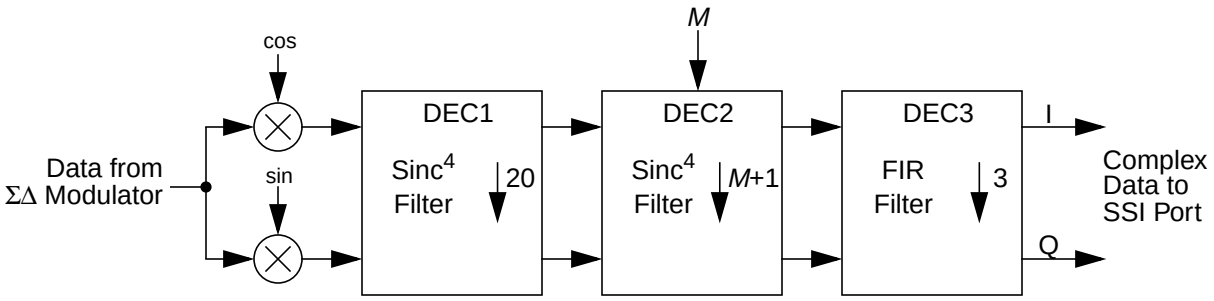


Figure 5. Decimation Filter Architecture

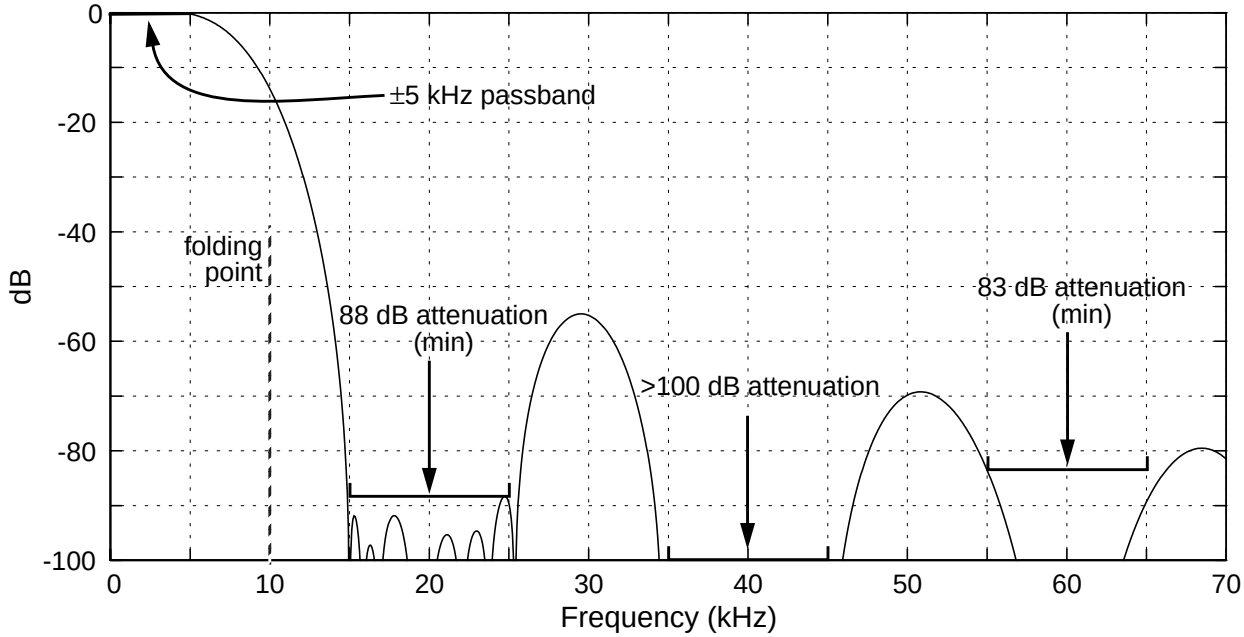


Figure 6. Frequency Response for f_{CLKOUT} = 20kHz, showing the first three alias bands.

Fig. 7 shows the full response of the decimation filter with the decimation factor set to 60 on a logarithmic frequency scale, while Fig. 8 shows the folded frequency response on a linear frequency scale and Fig. 9 shows a blowup of the passband. The location of the cutoff frequency shown in Fig. 7 is inversely proportional to the decimation factor. However, since both DEC1 and DEC2 are 4th-order comb filters, their combination is also a 4th-order comb filter and thus the shapes of the frequency responses shown in Figs. 8 and 9 are independent of the decimation factor.

As Fig. 9 shows, the gain variation across the passband is approximately 0.4 dB. Normalization of full-scale is accurate to within 0.4 dB across all decimation modes.

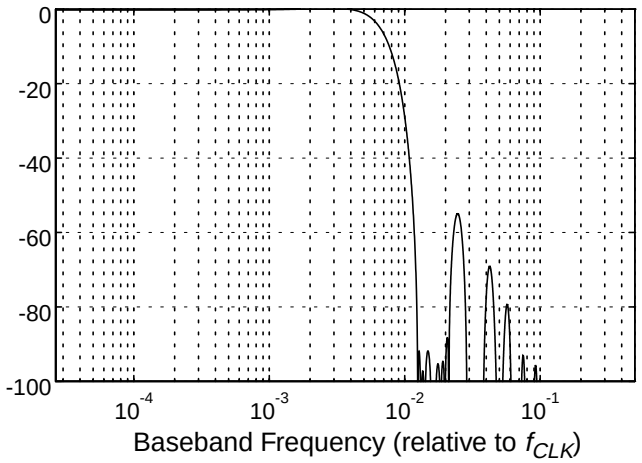


Figure 7. Decimator Frequency Response

SPECIAL OPERATING MODES

Synchronization

SYNCB is an active-low signal which clears the clock counters in both the decimation filter and the SSI port so that the output data of several chips can be synchronized. The counters in the clock synthesizers are not reset, as it is presumed that the CLK signals of multiple chips would be connected together. SYNCB also clears the registers in the decimation filter and resets the ΔΣ modulator.

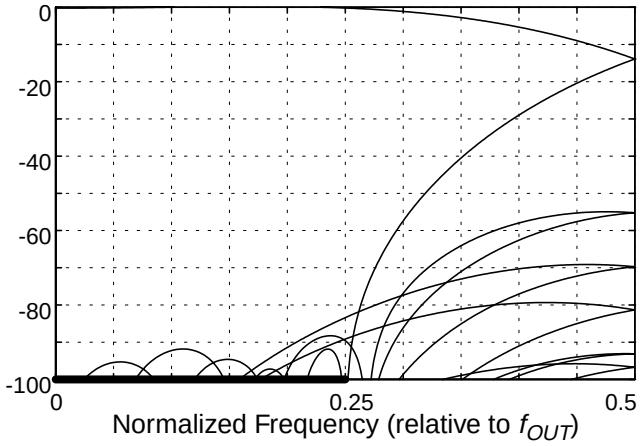


Figure 8. Folded Decimator Frequency Response

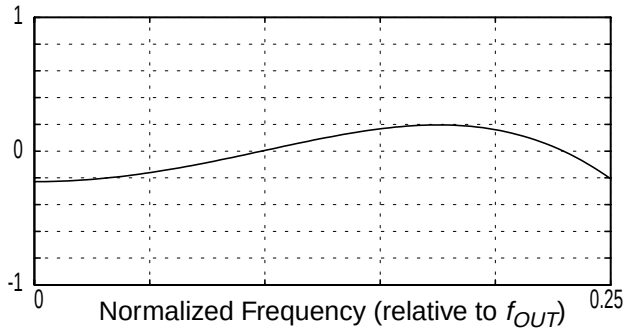


Figure 9. Passband Frequency Response of the Decimator