DUAL LOOP 2.5Gbps LASER DIODE DRIVER

Preliminary Technical Data — ADN2840

FEATURES

2.5 Gbps Operation
Typical rise/fall time 80 ps
Bias Current range 2 to 100 mA
Modulation Current range 5 to 80 mA
Monitor Photo Diode current 50 to 1300uA
Closed loop control of Power and Extinction Ratio
Laser fail and laser degrade alarms
Automatic laser shutdown, ALS
Dual MPD functionality for DWDM
PECL data interface, AC coupled
Optional clocked data
Full current parameter monitoring
5 V operation
48 pin LQFP package

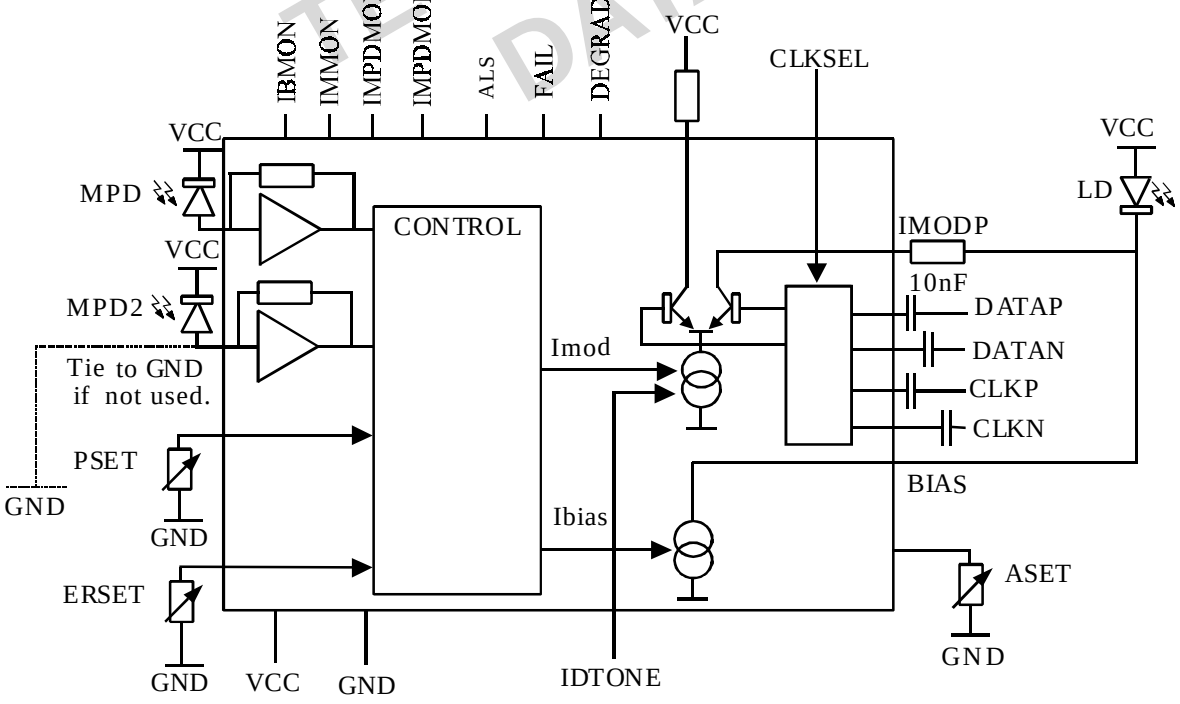
APPLICATIONS

DWDM dual MPD wavelength fixing
SONET OC-48
SDH STM-16

GENERAL DESCRIPTION

The ADN2840 uses a unique control algorithm to control both average power and extinction ratio of the laser diode, LD, after initial factory set-up. External component count and PCB area are low as both power and extinction ratio control are fully integrated. Programmable alarms are provided for laser fail (end of life), and laser degrade (impending fail).

Optional Dual MPD current monitoring is designed into the ADN2840 specifically for DWDM wavelength control.



FUNCTIONAL BLOCK DIAGRAM

REV. PrM_TQFP 12/11

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ADN2840 SPECIFICATIONS

(V_{CC} = 5V +/-10%. All specifications T_{MIN} to T_{MAX} unless otherwise noted[1]. Typical values at specified at 25°C)

PARAMETER	Min	Typ	Max	Units	Conditions/Comments
LASER BIAS (BIAS)					
Output current Ibias	2		100	mA	
Compliance Voltage	0.7		Vcc	V	
Ibias during ALS			0.1	mA	
ALS response time		10		µs	
MODULATION CURRENT (IMODP, IMODN)					
Output Current Imod	5		80	mA	
Compliance Voltage	1.8		Vcc	V	
Imod during ALS			0.1	mA	
Rise time		80	130	ps	
Fall time		80	130	ps	
Jitter			TBD	mUI	
Pulse Width Distortion		20		ps	
MONITOR PD (MPD,MPD2)					
Current	50		1300	µA	
Input voltage			2.5	V	
POWER SET INPUT (PSET)					
Capacitance			80	pF	
Input current	50		1300	µA	
Voltage	1.15	1.23	1.35	V	
EXTINCTION RATIO SET INPUT (ERSET)					
Allowable Resistance Range	1		25	Kohm	
Voltage	1.15	1.23	1.35	V	
ALARM SET (ASET)					
Allowable Input Range	1		25	Kohm	
Voltage	1.15	1.23	1.35	V	
Hysterisis		5		**%**	
DATA INPUTS (DATAP,DATAN,CLKP, CLKN)A.C. Coupled[2]					
Vp-p (single ended pk to pk)	100mV		500mV	V	
Input impedance		50		ohm	
t_{setup}		50		ps	
t_{hold}		50		ps	
LOGIC INPUTS (ALS,IDTONE)					
Vih	2.4			V	
Vil			0.8	V	
ALARM OUTPUTS (Internal 30K Ohm Pull up)					
Voh	2.4			V	
Vol			0.8	V	
IDTONE					
Fin[3]	0.1		10	MHz	
IBMON,IMMON IMPDMON,IMPDMON2					
IBMON Division Ratio		800		A/A	
IMMON Division Ratio		200		A/A	
IMPDMON,IMPDMON2		1		A/A	
IMPDMON to IMPDMON2 Matching			1		%
Compliance Voltage	0		Vcc-1.2	V	
SUPPLY					
Icc[4]		0.060		A	Ibias = Imod = 0
Vcc	4.5	5.0	5.5	V	

NOTES:
[1]Temperature Range is as follows: -40°C to +85°C
[2]When the Voltage on DATAP is greater than the voltage on DATAN the modulation current flows in the IMODP pin.
[3]IDTONE may cause eye distortion
[4]Icc for power calculation is the typical Icc given.
Specifications subject to change without notice

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{CC} to GND..... 7V

Voltage at DATAP, DATAN,CLKP,CLKN
..... min=(GND-0.3V), max=(VCC+0.3V)

Differential Voltage between CLKP&CLKN..... 2Vmax

Differential Voltage between DATAP&DATAN.. 2Vmax

.Operating Temperature Range

Industrial ..... -40°C to +85°C

Storage Temperature Range..... -65°C to +150°C

Junction Temperature (T_J max)..... +150°C

48-lead LQFP Package,

Power Dissipation.....(T_J max - T_A)/θ_{JA} mW

θ_{JA} Thermal Impedance.....40°C /W

Lead Temperature (soldering for 10sec).....+300°C.

NOTES:

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Transient currents of up to 100mA will not cause SCR latch-up

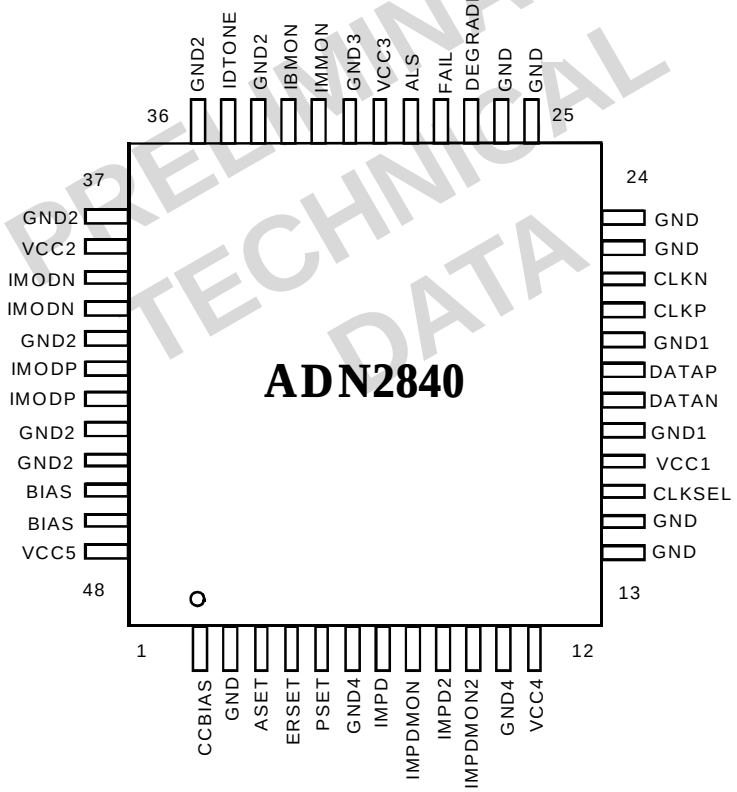


Figure 1. Laser Diode Driver Pinout

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADN2840 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTION

Pin No.	ADN2840	Function
1	CCBIAS	Extra Laser Diode bias when AC coupled
2	GND	Ground
3	ASET	Alarm current threshold setting pin
4	ERSET	Extinction Ratio set pin
5	PSET	Average Optical Power set pin
6	GND4	Supply Ground
7	IMPD	Monitor Photo Diode input
8	IMPDMON	Mirrored current from Monitor Photo Diode
9	IMPD2	Monitor Photo Diode input 2- (for use with two MPD's)
10	IMPDMON2	Mirrored current from Monitor Photo Diode2(for use with two MPD's)
11	GND4	Supply Ground
12	VCC4	Supply Voltage
13	GND	Ground
14	GND	Ground
15	CLKSEL	Clock Select (Active =Vcc), used if data is clocked into chip.
16	VCC1	Supply Voltage
17	GND1	Supply Ground
18	DATAN	Data, negative differential terminal
19	DATAP	Data, positive differential terminal
20	GND1	Supply Ground
21	CLKP	Data Clock positive differential terminal, used if CLKSEL = Vcc
22	CLKN	Data Clock negative differential terminal, used if CLKSEL = Vcc
23	GND	Ground
24	GND	Ground
25	GND	Ground
26	GND	Ground
27	DEGRADE	DEGRADE Alarm output, open collector
28	FAIL	FAIL Alarm output, open collector
29	ALS	Automatic Laser Shutdown
30	VCC3	Supply Voltage
31	GND3	Supply Ground
32	IMMON	Modulation current mirror output
33	IBMON	Bias current mirror output
34	GND2	Supply Ground
35	IDTONE	IDTONE input
36	GND2	Supply Ground
37	GND2	Supply Ground
38	VCC2	Supply Voltage
39	IMODN	Modulation Current negative output, connect to 25 Ohms
40	IMODN	Modulation Current negative output, connect to 25 Ohms
41	GND2	Supply Ground
42	IMODP	Modulation Current positive output, connect to laser diode
43	IMODP	Modulation Current positive output, connect to laser diode
44	GND2	Supply Ground
45	GND2	Supply Ground
46	BIAS	Laser Diode Bias Current
47	BIAS	Laser Diode Bias Current
48	VCC5	Supply Voltage

GENERAL

Laser diodes have current-in to light-out transfer functions as shown in Figure 2. Two key characteristics of this transfer function are the threshold current and slope in the linear region beyond the threshold current, referred to as slope efficiency, LI.

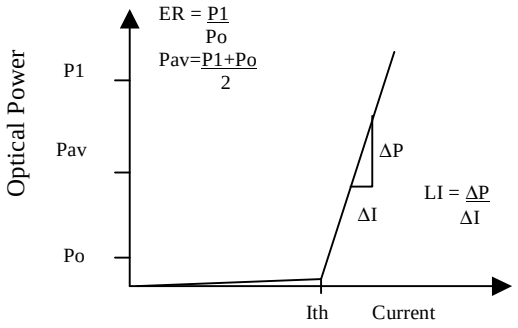


Figure 2. Laser Transfer Function

CONTROL

A monitor photo diode, MPD, is required to control the LD. The MPD current is fed into the ADN2840 to control the power and extinction ratio, continuously adjusting the bias current and modulation current in response to the laser's changing threshold current and light to current, LI, slope (slope efficiency).

The ADN2840 uses automatic power control, APC, to maintain a constant power over time and temperature.

The ADN2840 uses closed loop extinction ratio control to allow optimum setting of extinction ratio for every device. Hence SONET/SDH interface standards can be met over device variation, temperature and time. Closed loop modulation control eliminates the need to either over modulate the LD or include external components for temperature compensation. Thus reducing R&D time and second sourcing issues due to laser diode variation.

Power and Extinction Ratio are set using the PSET and ERSET pins respectively. A resistor is placed between the pin and GND to set the current, increasing current out of PSET increases Ibias. Both PSET and ERSET are kept 1.23V above GND.

The ratios of current-in-to-current-out are given by the following formulae:

$$R_{PSET} = \frac{1.23}{I_{av}} \quad (\Omega)$$

where I_{av} is average MPD current

$$R_{ERSET} = \frac{1.23}{\frac{I_{MPD\_CW}}{P_{CW}} * \frac{ER-1}{ER+1}} \quad (\Omega)$$

where P_{CW} is the DC optical power at some measured point given on the laser datasheet.

I_{MPD_CW} is MPD current at optical power equal to P_{CW}.

Note that I_{ERSET} and I_{PSET} will change from laser to laser. However the control loops will determine actual values. It is not required to know exact values for LI or MPD optical coupling.

ALARMS

The ADN2840 alarms are designed to allow interface compliance to ITU-T-G958 (11/94) section 10.3.1.1.2 (transmitter fail) and section 10.3.1.1.3 (transmitter degrade). The ADN2840 has two active high alarms, DEGRADE and FAIL. A resistor between ground and the ASET pin is used to set the current at which these alarms are raised. The current through the ASET resistor is a ratio of 100:1 to the FAIL alarm threshold. The DEGRADE alarm will be raised at 90% of this level.

Example: $I_{FAIL} = 50mA$ so $I_{DEGRADE} = 45mA$

$$I_{ASET} = \frac{Ibiastrip}{100} = \frac{50mA}{100} = 500\mu A$$

$$**R_{ASET} = \frac{1.23\ V}{I_{ASET}} = \frac{1.23}{500\mu A} = 2.4\ k\Omega$$

The laser degrade alarm, DEGRADE, is provided to give a warning of imminent laser failure if the laser diode degrades further or environmental conditions continue to stress the LD, eg. increasing temperature.

The laser fail alarm, FAIL, is activated when the transmitter can no longer be guaranteed to be SONET/SDH compliant. This occurs when one of the following conditions arise:

- The ASET threshold is reached.
- The maximum bias current of the ADN2840 is reached and the APC loop can no longer maintain control.
- The LD has stopped working. In this case, no current is being developed by the MPD.
- The ALS pin is set high. This shuts off the modulation and bias currents to the LD, resulting in the MPD current dropping to zero. This gives closed loop feedback to the system that ALS has been enabled.

DEGRADE will not be raised when ALS is high.

MONITOR CURRENTS

IBMON, IMMON and IMPDMON and IMPDMON2 are current controlled current sources from Vcc. They mirror the bias, modulation and MPD current for increased monitoring functionality. An external resistor to GND gives a voltage proportional to the current monitored.

****Note: The smallest valid value for R_{ASET} is 1.2kΩ, as this corresponds to the I_{BIAS} maximum of 100mA.**

DUAL MPD DWDM FUNCTION

The ADN2840 has circuitry for a second monitor photo diode, MPD2.

The second photo diode current is mirrored to IMPDMON2 for wavelength control purposes and is summed internally for the power control loop. **For single MPD circuits the MPD2 pin is tied to GND**.

This enables the system designer to use the two currents to control the wavelength of the laser diode using various optical filtering techniques inside the laser module.

IDTONE

The IDTONE pin is supplied for fibre identification/ supervisory channels or control purposes in WDM. This pin modulates the optical one level by 3%.

Note that using IDTONE during transmission may cause optical eye degradation.

DATA, CLOCK INPUTS

Data and Clock inputs are AC coupled (10nF recommended) and terminated via a 100 ohm internal resistor between DATAP,DATAN and CLKP,CLKN. There is a high impedance circuit to set the common mode voltage which is designed to change over temperature. It is recommended that AC coupling is used to eliminate the need for matching between Common Mode Voltages.

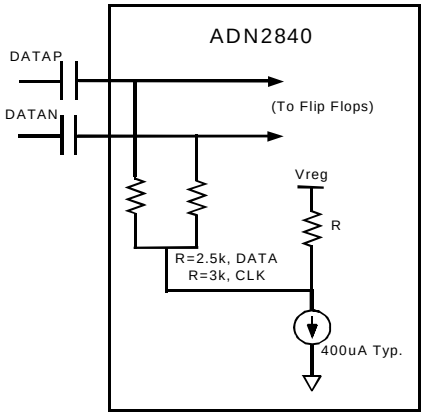


Figure 3. AC Coupling of Data Inputs

CCBIAS

CCBIAS should be connected to the BIAS pin if the Laser Diode is connected to the ADN2840 using a capacitor. CCBIAS is a current sink to GND.

AUTOMATIC LASER SHUTDOWN

The ADN2840 ALS allows compliance to ITU-T-G958 (11/94), section 9.7.

When ALS is logic high, both bias and modulation currents are turned off.

Correct operation of ALS can be confirmed by the fail alarm being raised when ALS is asserted. Note this is the only time that DEGRADE will be low while FAIL is high.

ALARM INTERFACES

The alarm voltages are open collector. An internal pull up resistor of 30k is used to pull the digital high value to Vcc. However this can be over driven with an external resistor allowing alarm interfacing to non Vcc levels. **Non Vcc alarm output levels must be below the Vcc used for the ADN2840.**

POWER CONSUMPTION

The ADN2840 die temperature must be kept below 125°C. The Θja is 40°C/W in a Four layer P.C.B (JEDEC 1S2P). The TQFP package has an exposed Paddle and as such needs to be soldered to the P.C.B to achieve the Thermal performance.

$$Tdie = Tambient + \Theta ja \cdot P$$

$$Icc = Iccmin + 0.3 * Imod$$

$$P = Vcc.Icc + (Ibias.Vbias\_pin) + (Imod.Vmod\_pin)$$

Hence the maximum combination of Ibias + Imod must be calculated.

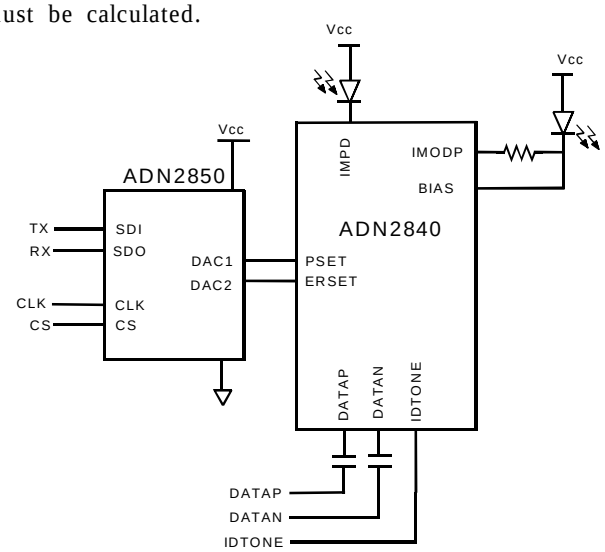


Figure 4. Application using optical supervisor
**ADN2850 is a dual 10 bit EEpot using thinfilm resistor technology to give very low temperature coefficients*

Note : If you wish to use the ADN2840 at data rates lower than OC48 please contact your local Analog Devices representative.

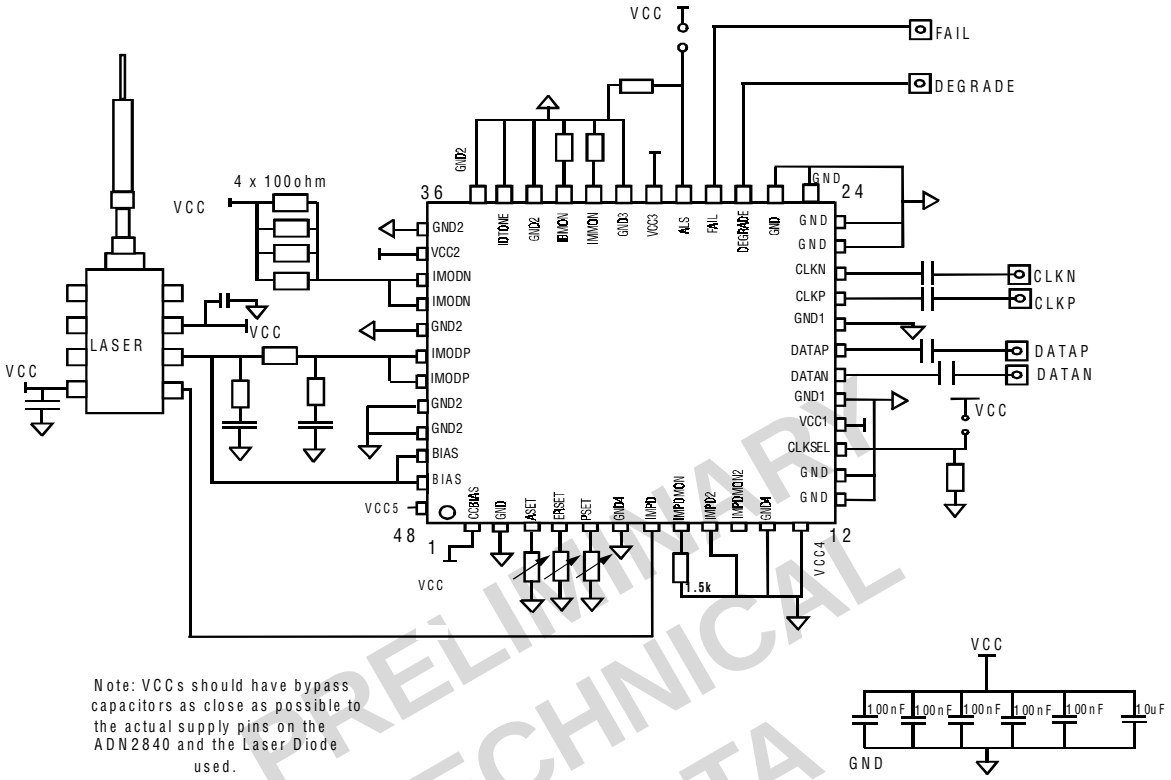


Figure 5. Test Circuit, data not clocked.

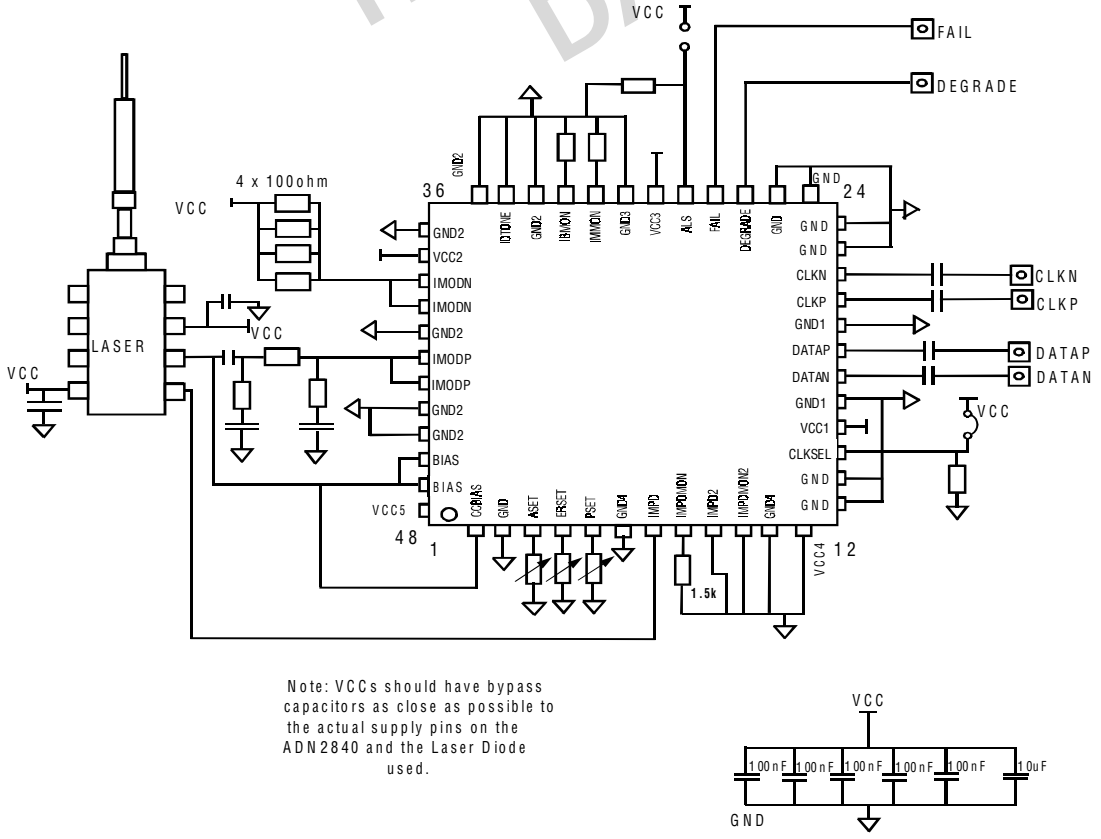
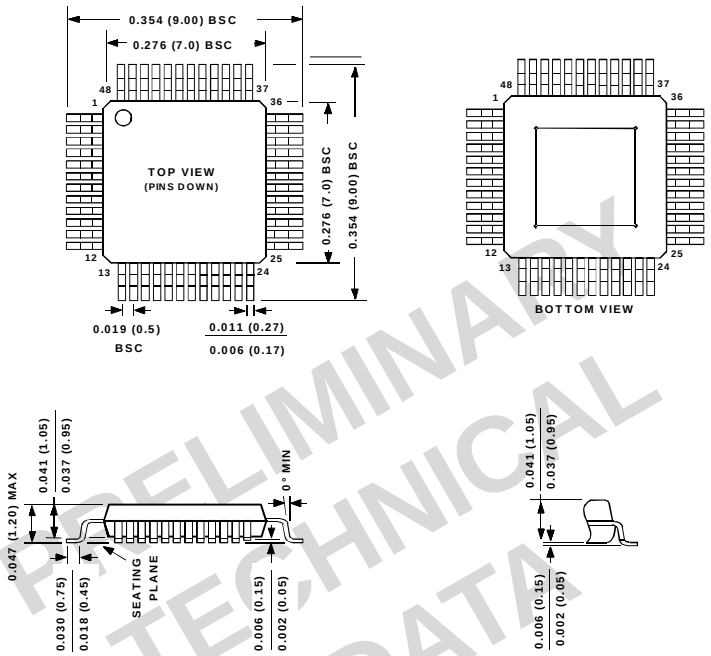


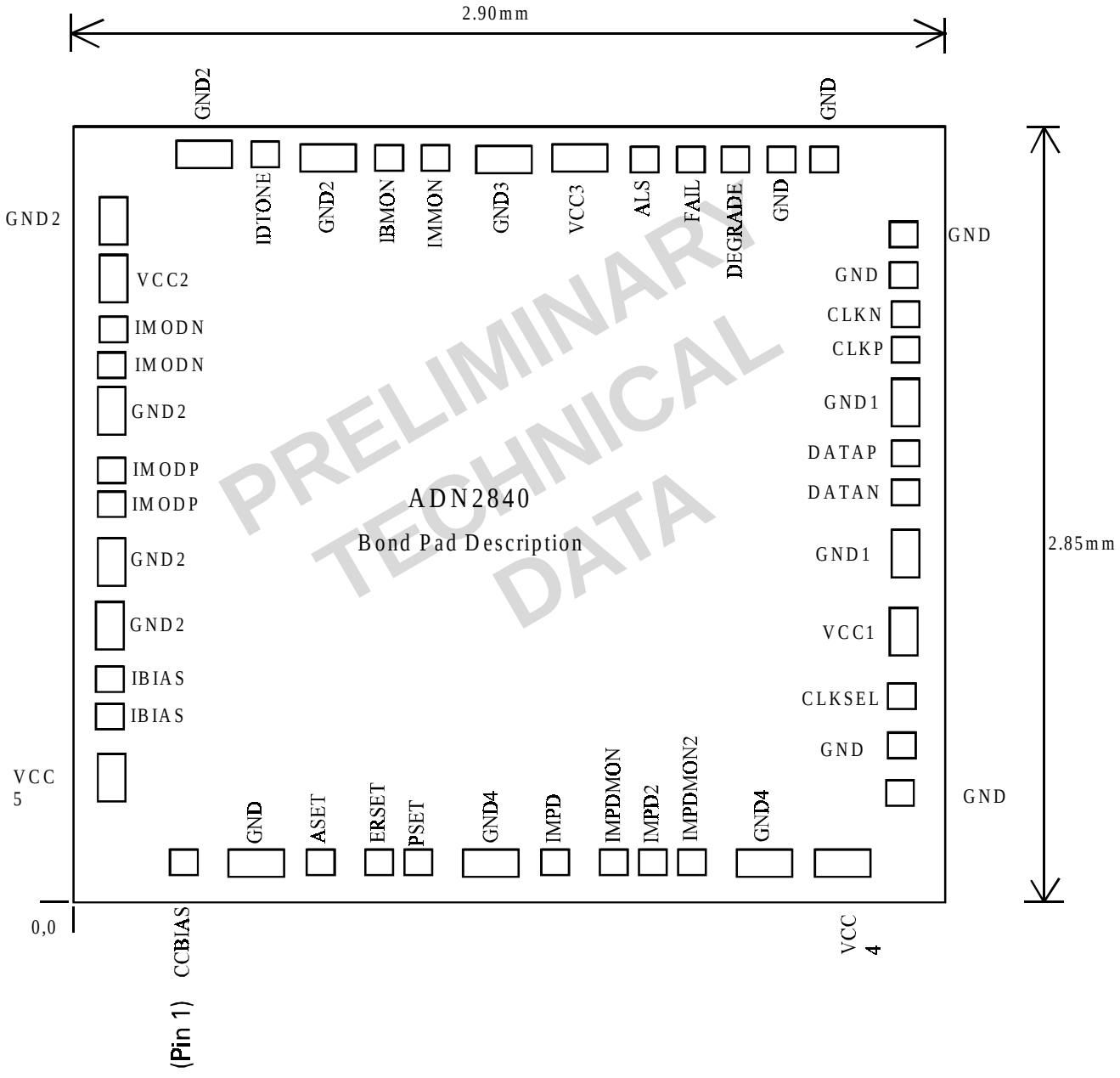
Figure 6. Test circuit, capacitively coupled, data clocked.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

48-Lead EP (Exposed Paddle) TQFP (ST-48)




2.90mm
2.85mm
GND2
GND
IDTONE
GND2
IBMON
IMMON
GND3
VCC3
ALS
FAIL
DEGRADE
GND
GND2
VCC2
IMODN
IMODN
GND2
IMODP
IMODP
GND2
GND2
IBIAS
IBIAS
VCC 5
GND
GND
CLKN
CLKP
GND1
DATAP
DATAN
GND1
VCC1
CLKSEL
GND
GND
ASET
ERSET
PSET
GND4
IMPD
IMPDMON
IMPD2
IMPDMON2
GND4
0,0
CCBIAS
(Pin 1)
VCC 4
ADN2840
Bond Pad Description
PRELIMINARY TECHNICAL DATA