+2.5 V to +5.5 V, 120 μA, 2-Wire Interface, Voltage Output 8-/10-/12-Bit DACs

AD5301/AD5311/AD5321*

FEATURES

AD5301: Buffered Voltage Output 8-Bit DAC
AD5311: Buffered Voltage Output 10-Bit DAC
AD5321: Buffered Voltage Output 12-Bit DAC
6-Lead SOT-23 and 8-Lead μSOIC Packages
Micropower Operation: 120 μA @ 3 V
2-Wire (I^2C® Compatible) Serial Interface
Data Readback Capability
+2.5 V to +5.5 V Power Supply
Guaranteed Monotonic By Design Over All Codes
Power-Down to 50 nA @ 3 V
Reference Derived from Power Supply
Power-On-Reset to Zero Volts
On-Chip Rail-to-Rail Output Buffer Amplifier
Three Power-Down Functions

APPLICATIONS

Portable Battery Powered Instruments
Digital Gain and Offset Adjustment
Programmable Voltage and Current Sources
Programmable Attenuators

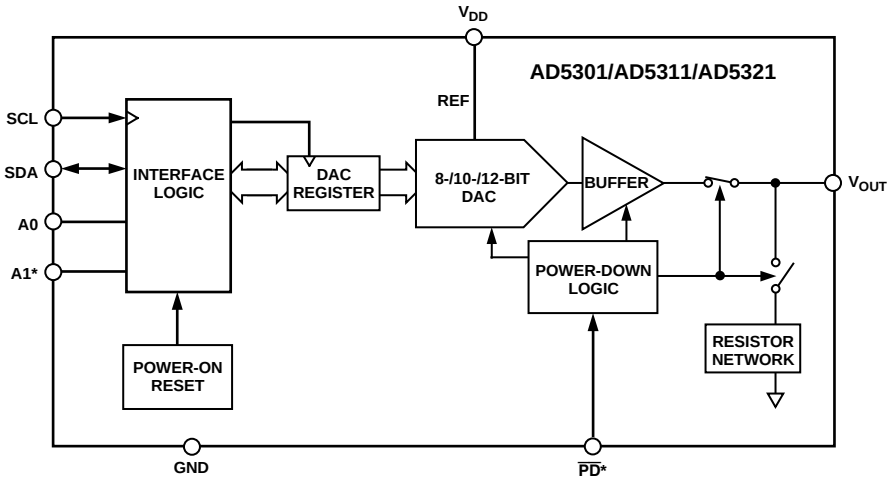
GENERAL DESCRIPTION

The AD5301/AD5311/AD5321 are single 8-, 10- and 12-bit buffered voltage-output DACs that operate from a single +2.5 V to +5.5 V supply consuming 120 μA at 3 V. The on-chip output amplifier allows rail-to-rail output swing with a slew rate of 0.7 V/μs. It uses a 2-wire (I^2C compatible) serial interface that operates at clock rates up to 400 kHz. Multiple devices can share the same bus.

The reference for the DAC is derived from the power supply inputs and thus gives the widest dynamic output range. These parts incorporate a power-on-reset circuit, which ensures that the DAC output powers-up to zero volts and remains there until a valid write takes place. The parts contain a power-down feature which reduces the current consumption of the device to 50 nA at 3 V and provides software-selectable output loads while in power-down mode.

The low power consumption in normal operation make these DACs ideally suited to portable battery-operated equipment. The power consumption is 0.75 mW at 5 V, 0.36 mW at 3 V reducing to 1 μW in all power-down modes.

FUNCTIONAL BLOCK DIAGRAM



*AVAILABLE ON 8-LEAD VERSION ONLY

I^2C is a registered trademark of Philips Corporation.
*Protected by U.S. Patent No. 5684481, other patent pending.

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AD5301/AD5311/AD5321–SPECIFICATIONS (V_{DD} = +2.5 V to +5.5 V; R_L = 2 kΩ to GND; C_L = 200 pF to GND; All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter[1]	B Version[2] Min	Typ	Max	Units	Conditions/Comments
DC PERFORMANCE[3, 4]					
AD5301					
Resolution		8		Bits	
Relative Accuracy		±0.15	±1	LSB	
Differential Nonlinearity		±0.02	±0.25	LSB	Guaranteed Monotonic by Design Over All Codes
AD5311					
Resolution		10		Bits	
Relative Accuracy		±0.5	±4	LSB	
Differential Nonlinearity		±0.05	±0.5	LSB	Guaranteed Monotonic by Design Over All Codes
AD5321					
Resolution		12		Bits	
Relative Accuracy		±2	±16	LSB	
Differential Nonlinearity		±0.3	±0.8	LSB	Guaranteed Monotonic by Design Over All Codes
Zero Code Error		+5	+20	mV	All Zeros Loaded to DAC, See Figure 9
Full-Scale Error		±0.15	±1.25	% of FSR	All Ones Loaded to DAC, See Figure 9
Gain Error		±0.15	±1	% of FSR	
Zero Code Error Drift[5]		–20		µV/°C	
Gain Error Drift[5]		–5		ppm of FSR/°C	
OUTPUT CHARACTERISTICS[5]					
Minimum Output Voltage		0.001		V min	This is a measure of the minimum and maximum drive
Maximum Output Voltage		V_{DD} – 0.001		V max	capability of the output amplifier.
DC Output Impedance		1		Ω	
Short Circuit Current		50		mA	V_{DD} = +5 V
		20		mA	V_{DD} = +3 V
Power-Up Time		2.5		µs	Coming Out of Power-Down Mode. V_{DD} = +5 V
		6		µs	Coming Out of Power-Down Mode. V_{DD} = +3 V
LOGIC INPUTS (A0, A1, $\overline{PD}$)[5]					
Input Current			±1	µA	
V_{IL}, Input Low Voltage			0.8	V	V_{DD} = +5 V ± 10%
			0.6	V	V_{DD} = +3 V ± 10%
			0.5	V	V_{DD} = +2.5 V
V_{IH}, Input High Voltage	2.4			V	V_{DD} = +5 V ± 10%
	2.1			V	V_{DD} = +3 V ± 10%
	2.0			V	V_{DD} = +2.5 V
Pin Capacitance		3		pF	
LOGIC INPUTS (SCL, SDA)[5]					
V_{IH}, Input High Voltage	0.7 V_{DD}		V_{DD} + 0.3	V	
V_{IL}, Input Low Voltage	–0.3		0.3 V_{DD}	V	
I_{IN}, Input Leakage Current			±1	µA	V_{IN} = 0 V to V_{DD}
V_{HYST}, Input Hysteresis	0.05 V_{DD}			V	
C_{IN}, Input Capacitance		6		pF	
Glitch Rejection[6]			50	ns	Pulsewidth of Spike Suppressed
LOGIC OUTPUT (SDA)[5]					
V_{OL}, Output Low Voltage			0.4	V	I_{SINK} = 3 mA
			0.6	V	I_{SINK} = 6 mA
Three-State Leakage Current			±1	µA	
Three-State Output Capacitance		6		pF	
POWER REQUIREMENTS					
V_{DD}	2.5		5.5	V	I_{DD} Specification Is Valid for All DAC Codes
I_{DD} (Normal Mode)					DAC Active and Excluding Load Current
V_{DD} = +4.5 V to +5.5 V		150	250	µA	V_{IH} = V_{DD} and V_{IL} = GND
V_{DD} = +2.5 V to +3.6 V		120	220	µA	V_{IH} = V_{DD} and V_{IL} = GND
I_{DD} (Power-Down Mode)					
V_{DD} = +4.5 V to +5.5 V		0.2	1	µA	V_{IH} = V_{DD} and V_{IL} = GND
V_{DD} = +2.5 V to +3.6 V		0.05	1	µA	V_{IH} = V_{DD} and V_{IL} = GND

NOTES
[1]See Terminology.
[2]Temperature ranges are as follows: B Version: –40°C to +105°C.
[3]DC specifications tested with the outputs unloaded.
[4]Linearity is tested using a reduced code range: AD5301 (Code 7 to 250); AD5311 (Code 28 to 1000); AD5321 (Code 112 to 4000).
[5]Guaranteed by Design and Characterization, not production tested.
[6]Input filtering on both the SCL and SDA inputs suppress noise spikes that are less than 50 ns.

Specifications subject to change without notice.

AC CHARACTERISTICS[1] (V_{DD} = +2.5 V to +5.5 V; R_L = 2 kΩ to GND; C_L = 200 pF to GND; All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter[2]	B Version[3] Min	Typ	Max	Units	Conditions/Comments
Output Voltage Settling Time					V_{DD} = +5 V
AD5301		6	8	µs	1/4 Scale to 3/4 Scale Change (40 Hex to C0 Hex)
AD5311		7	9	µs	1/4 Scale to 3/4 Scale Change (100 Hex to 300 Hex)
AD5321		8	10	µs	1/4 Scale to 3/4 Scale Change (400 Hex to C00 Hex)
Slew Rate		0.7		V/µs	
Major-Code Change Glitch Impulse		12		nV-s	1 LSB Change Around Major Carry
Digital Feedthrough		0.3		nV-s	

NOTES
[1]See Terminology
[2]Guaranteed by design and characterization, not production tested.
[3]Temperature ranges are as follows: B Version: –40°C to +105°C.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{DD} = +2.5 V to +5.5 V. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter[2]	Limit at T_{MIN}, T_{MAX} (B Version)	Units	Conditions/Comments
f_{SCL}	400	kHz max	SCL Clock Frequency
t_1	2.5	µs min	SCL Cycle Time
t_2	0.6	µs min	t_{HIGH}, SCL High Time
t_3	1.3	µs min	t_{LOW}, SCL Low Time
t_4	0.6	µs min	$t_{HD,STA}$, Start/Repeated Start Condition Hold Time
t_5	100	ns min	$t_{SU,DAT}$, Data Setup Time
t_6[3]	0.9	µs max	$t_{HD,DAT}$, Data Hold Time
	0	µs min	
t_7	0.6	µs min	$t_{SU,STA}$, Setup Time for Repeated Start
t_8	0.6	µs min	$t_{SU,STO}$, Stop Condition Setup Time
t_9	1.3	µs min	t_{BUF}, Bus Free Time Between a STOP Condition and a START Condition
t_{10}	300	ns max	t_R, Rise Time of Both SCL and SDA when Receiving
	0	ns min	May be CMOS Driven
t_{11}	250	ns max	t_F, Fall Time of SDA when Receiving
	300	ns max	t_F, Fall Time of Both SCL and SDA when Transmitting
	$20 + 0.1C_b$[4]	ns min	
C_b	400	pF max	Capacitive Load for Each Bus Line

NOTES
[1]See Figure 1.
[2]Guaranteed by design and characterization, not production tested.
[3]A master device must provide a hold time of at least 300 ns for the SDA signal (referred to the $V_{IH\,MIN}$ of the SCL signal) in order to bridge the undefined region of SCL's falling edge.
[4]C_b is the total capacitance of one bus line in pF. t_R and t_F measured between 0.3 V_{DD} and 0.7 V_{DD}.

Specifications subject to change without notice.

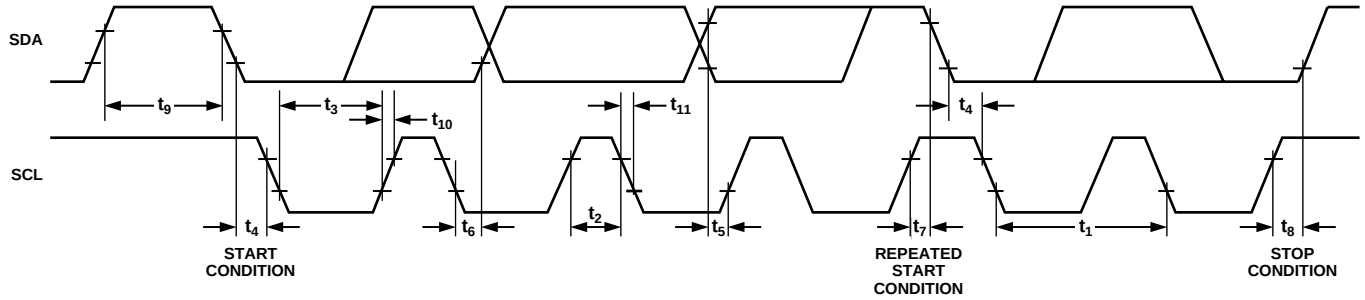


Figure 1. 2-Wire Serial Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1, 2]

(T_A = +25°C unless otherwise noted)

V_{DD} to GND ..... –0.3 V to +7 V
SCL, SDA to GND ..... –0.3 V to V_{DD} + 0.3 V
$\overline{PD}$, A1, A0 to GND ..... –0.3 V to V_{DD} + 0.3 V
V_{OUT} to GND ..... –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
  Industrial (B Version) ..... –40°C to +105°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature (T_J max) .....+150°C
SOT-23 Package
  Power Dissipation ..... (T_J max – T_A)/θ_{JA}
  θ_{JA} Thermal Impedance ..... 229.6°C/W
µSOIC Package
  Power Dissipation ..... (T_J max – T_A)/θ_{JA}
  θ_{JA} Thermal Impedance ..... 206°C/W
Lead Temperature, Soldering
  Vapor Phase (60 sec) ..... +215°C
  Infrared (15 sec) ..... +220°C

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Transient currents of up to 100 mA will not cause SCR latch-up.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding Information
AD5301BRT	–40°C to +105°C	SOT-23	RT-6	D8B
AD5301BRM	–40°C to +105°C	µSOIC	RM-8	D8B
AD5311BRT	–40°C to +105°C	SOT-23	RT-6	D9B
AD5311BRM	–40°C to +105°C	µSOIC	RM-8	D9B
AD5321BRT	–40°C to +105°C	SOT-23	RT-6	DAB
AD5321BRM	–40°C to +105°C	µSOIC	RM-8	DAB

CAUTION

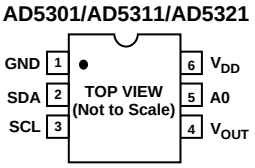
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5301/AD5311/AD5321 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTION

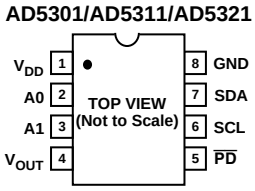
μSOIC Pin No.	SOT-23 Pin No.	Mnemonic	Function
1	6	V_{DD}	Power Supply Input. These parts can be operated from +2.5 V to +5.5 V and the supply should be decoupled with a 10 μF in parallel with a 0.1 μF capacitor to GND.
2	5	A0	Address Input. Sets the Least Significant Bit of the 7-bit slave address.
3	N/A	A1	Address Input. Sets the 2nd Least Significant Bit of the 7-bit slave address.
4	4	V_{OUT}	Buffered analog output voltage from the DAC. The output amplifier has rail-to-rail operation.
5	N/A	$\overline{PD}$	Active low control input that acts as a hardware power-down option. This pin overrides any software power-down option. The DAC output goes three-state and the current consumption of the part drops to 50 nA @ 3 V (200 nA @ 5 V).
6	3	SCL	Serial Clock Line. This is used in conjunction with the SDA line to clock data into the 16-bit input shift register. Clock rates of up to 400 kbit/s can be accommodated in the I^2C compatible interface. SCL may be CMOS/TTL driven.
7	2	SDA	Serial Data Line. This is used in conjunction with the SCL line to clock data into the 16-bit input shift register during the write cycle and used to read back one or two bytes of data (one byte for the AD5301, two bytes for the AD5311/AD5321) during the read cycle. It is a bidirectional open-drain data line that should be pulled to the supply with an external pull-up resistor. If not used in readback mode, SDA may be CMOS/TTL driven.
8	1	GND	Ground reference point for all circuitry on the part.

PIN CONFIGURATIONS

6-Lead SOT-23 (RT-6)



8-Lead μSOIC (RM-8)



TERMINOLOGY

RELATIVE ACCURACY

For the DAC, Relative Accuracy or Integral Nonlinearity (INL) is a measure of the maximum deviation, in LSBs, from a straight line passing through the actual endpoints of the DAC transfer function. Typical INL vs. Code plots can be seen in Figures 2 to 4.

DIFFERENTIAL NONLINEARITY

Differential Nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. These DACs are guaranteed monotonic by design over all codes. Typical DNL vs. Code plots can be seen in Figures 5 to 7.

ZERO CODE ERROR

Zero Code Error is a measure of the output error when zero code (00H) is loaded to the DAC register. Ideally, the output should be 0 V. The Zero Code Error of the AD5301/AD5311/AD5321 is always positive because the output of the DAC cannot go below 0 V. It is due to a combination of the offset errors in the DAC and output amplifier. It is expressed in mV, see Figure 9.

FULL-SCALE ERROR

Full-Scale Error is a measure of the output error when full scale is loaded to the DAC register. Ideally, the output should be V_{DD} – 1 LSB. Full-scale error is expressed in percent of FSR (full-scale range). A plot can be seen in Figure 9.

GAIN ERROR

This is a measure of the span error of the DAC. It is the deviation in slope of the actual DAC transfer characteristic from the ideal expressed as a percentage of the full-scale range.

ZERO CODE ERROR DRIFT

This is a measure of the change in zero code error with a change in temperature. It is expressed in µV/°C.

GAIN ERROR DRIFT

This is a measure of the change in gain error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

MAJOR CODE TRANSITION GLITCH ENERGY

Major Code Transition Glitch Energy is the energy of the impulse injected into the analog output when the code in the DAC register changes state. It is normally specified as the area of the glitch in nV-secs and is measured when the digital code is changed by 1 LSB at the major carry transition (011 . . . 11 to 100 . . . 00 or 100 . . . 00 to 011 . . . 11).

DIGITAL FEEDTHROUGH

Digital Feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital input pins of the device but is measured when the DAC is not being written to. It is specified in nV-secs and is measured with a full-scale change on the digital input pins, i.e., from all 0s to all 1s and vice versa.

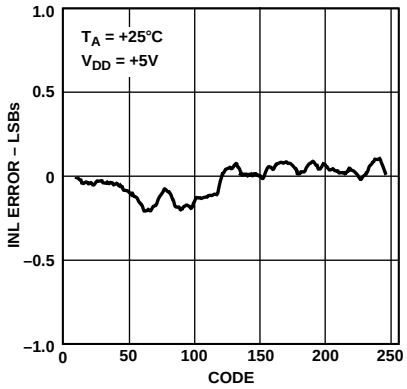


Figure 2. AD5301 Typical INL Plot

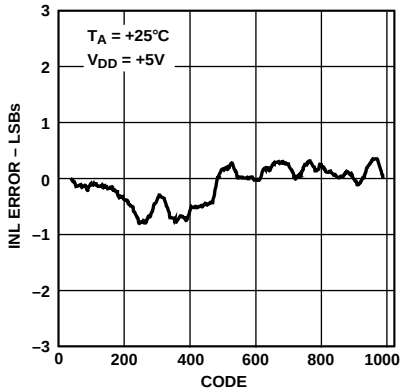


Figure 3. AD5311 Typical INL Plot

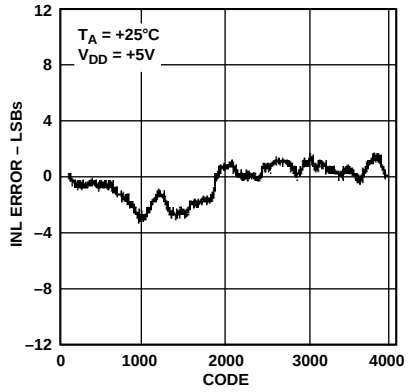


Figure 4. AD5321 Typical INL Plot

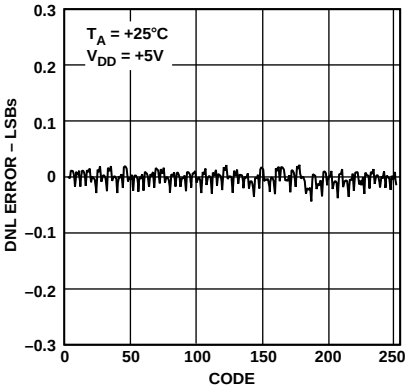


Figure 5. AD5301 Typical DNL Plot

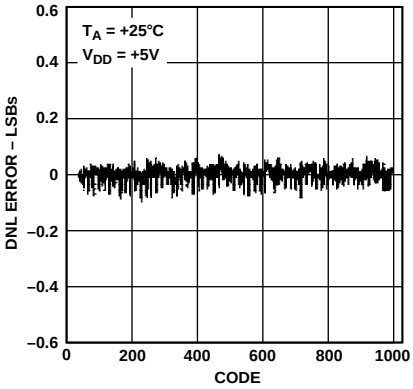


Figure 6. AD5311 Typical DNL Plot

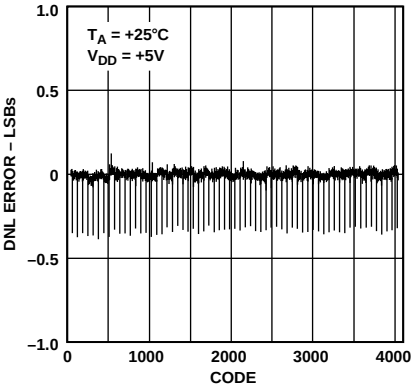


Figure 7. AD5321 Typical DNL Plot

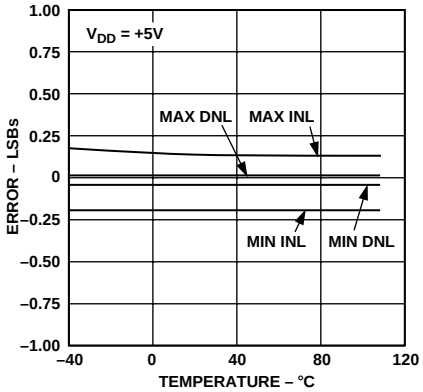


Figure 8. AD5301 INL Error and DNL Error vs. Temperature

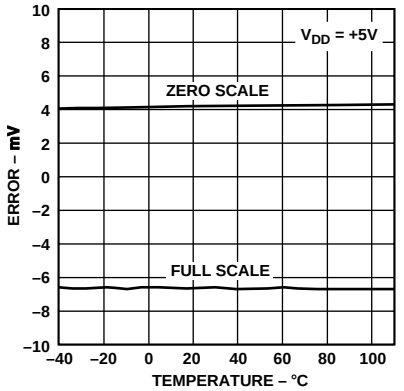


Figure 9. Zero-Code Error and Full-Scale Error vs. Temperature

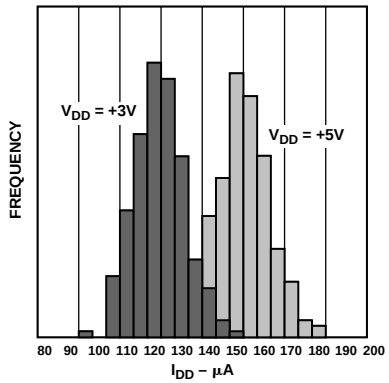


Figure 10. I_{DD} Histogram with V_{DD} = +3 V and V_{DD} = +5 V

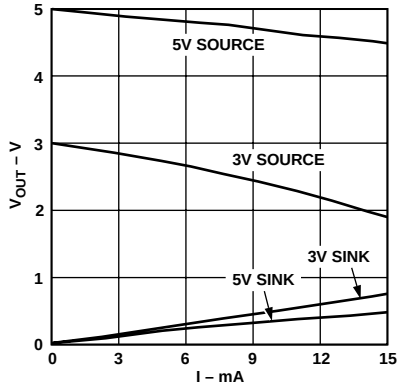


Figure 11. Source and Sink Current Capability

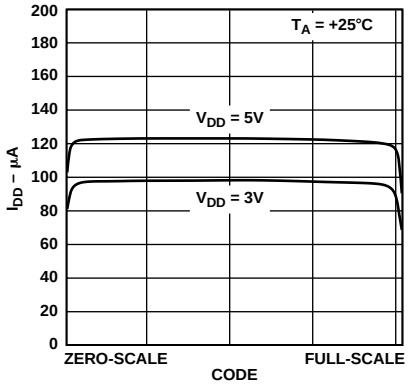


Figure 12. Supply Current vs. Code

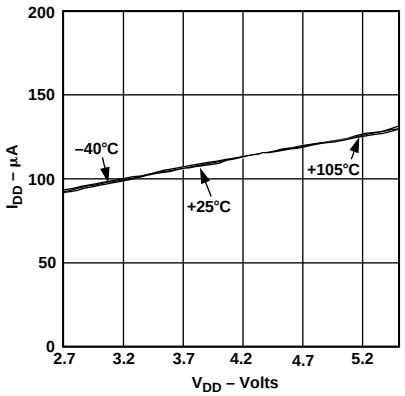


Figure 13. Supply Current vs. Supply Voltage

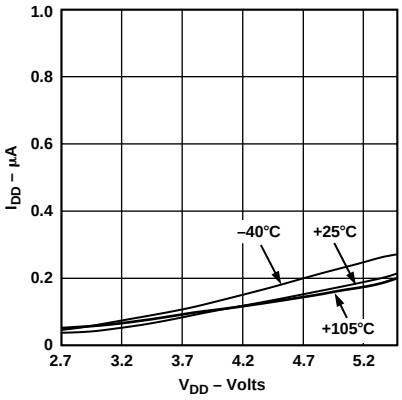


Figure 14. Power-Down Current vs. Supply Voltage

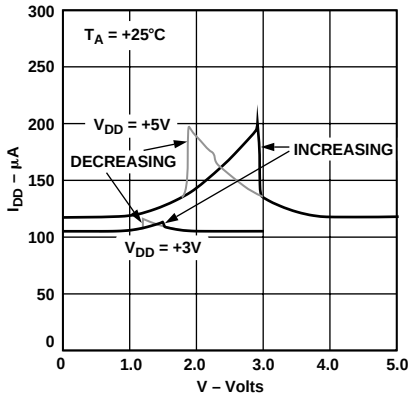


Figure 15. Supply Current vs. Logic Input Voltage for SDA and SCL Voltage Increasing and Decreasing

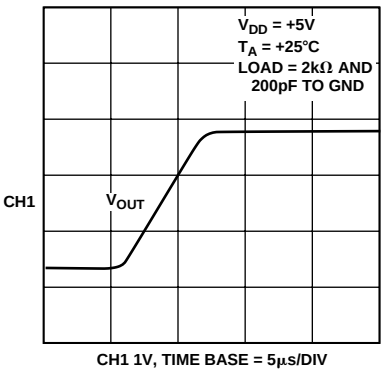


Figure 16. Half-Scale Settling (1/4 to 3/4 Scale Code Charge)

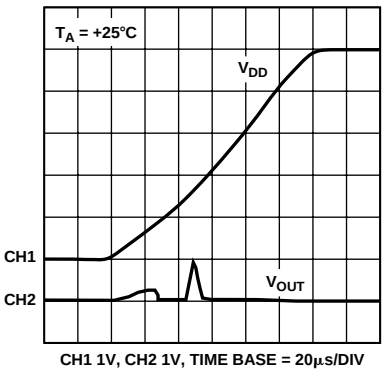


Figure 17. Power-On Reset to 0 V

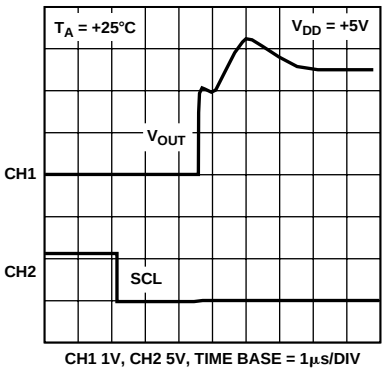


Figure 18. Exiting Power-Down to Midscale

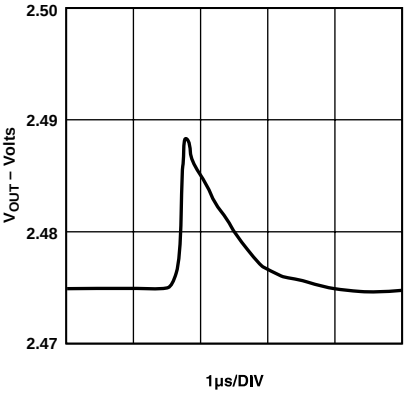


Figure 19. Major-Code Transition

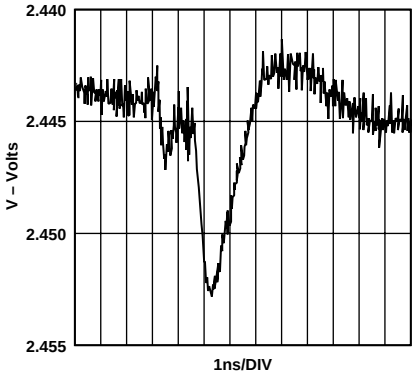


Figure 20. Digital Feedthrough

GENERAL DESCRIPTION

The AD5301/AD5311/AD5321 are single resistor-string DACs fabricated on a CMOS process with resolutions of 8, 10 and 12 bits respectively. Data is written via a 2-wire serial interface. They operate from single supplies of +2.5 V to +5.5 V and the output buffer amplifiers provide rail-to-rail output swing with a slew rate of 0.7 V/µs. The power-supply (V_{DD}) acts as the reference to the DAC. The devices have three programmable power-down modes, in which the DAC may be turned off completely with a high-impedance output, or the output may be pulled low by an on-chip resistor. See Power-Down section.

DIGITAL-TO-ANALOG SECTION

The architecture of the DAC channel consists of a resistor-string DAC followed by an output buffer amplifier. The voltage at the V_{DD} pin provides the reference voltage for the DAC. Figure 21 shows a block diagram of the DAC architecture. Since the input coding to the DAC is straight binary, the ideal output voltage is given by:

$$V_{OUT} = \frac{V_{DD} \times D}{2^N}$$

where:

N = DAC resolution
D = decimal equivalent of the binary code which is loaded to the DAC register:

0–255 for AD5301 (8 Bits)
0–1023 for AD5311 (10 Bits)
0–4095 for AD5321 (12 Bits)

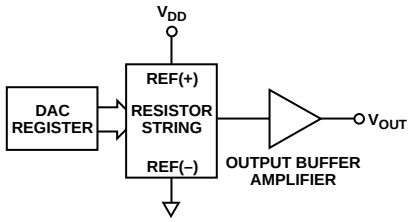


Figure 21. DAC Channel Architecture

RESISTOR STRING

The resistor string section is shown in Figure 22. It is simply a string of resistors, each of value R. The digital code loaded to the DAC register determines at what node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic over all codes.

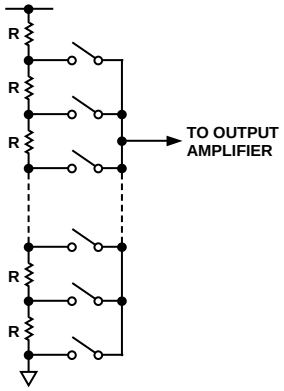


Figure 22. Resistor String

OUTPUT AMPLIFIER

The output buffer amplifier is capable of generating output voltages to within 1 mV from either rail, which gives an output range of 0.001 V to V_{DD} – 0.001 V. It is capable of driving a load of 2 kΩ to GND and V_{DD}, in parallel with 500 pF to GND. The source and sink capabilities of the output amplifier can be seen in Figure 11.

The slew rate is 0.7 V/µs with a half-scale settling time to ±0.5 LSB (at 8 bits) of 6 µs with the output unloaded.

POWER-ON RESET

The AD5301/AD5311/AD5321 are provided with a power-on reset function, ensuring that they power up in a defined state.

The DAC register is filled with zeros and remains so until a valid write sequence is made to the device. This is particularly useful in applications where it is important to know the state of the DAC output while the device is powering up.

SERIAL INTERFACE

2-WIRE SERIAL BUS

The AD5301/AD5311/AD5321 are controlled via an I^2C-compatible serial bus. The DACs are connected to this bus as slave devices (no clock is generated by the AD5301/AD5311/AD5321 DACs).

The AD5301/AD5311/AD5321 has a 7-bit slave address. In the case of the 6-pin device, the 6 MSBs are 000110 and the LSB is determined by the state of the A0 pin. In the case of the 8-pin device, the 5 MSBs are 00011 and the 2 LSBs are determined by the state of the A0 and A1 pins. A1 and A0 allow the user to use up to four of these DACs on one bus.

The 2-wire serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a START condition, which is when a high to low transition on the SDA line occurs while SCL is high. The following byte is the address byte which consists of the 7-bit slave address followed by an R/$\overline{W}$ bit (this bit determines whether data will be read from or written to the slave device).

   The slave whose address corresponds to the transmitted address responds by pulling the SDA line low during the ninth clock pulse (this is termed the Acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to or read from its serial register. If the R/$\overline{W}$ bit is high, the master will read from the slave device. However, if the R/$\overline{W}$ bit is low, the master will write to the slave device.

2. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an Acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL.

3. When all data bits have been read or written, a STOP condition is established by the master. A STOP condition is defined as a low-to-high transition on the SDA line while SCL is high. In Write mode, the master will pull the SDA line high during the 10th clock pulse to establish a STOP condition. In Read mode, the master will issue a No Acknowledge for the 9th clock pulse (i.e., the SDA line remains high). The master will then bring the SDA line low before the 10th clock pulse and then high during the 10th clock pulse to establish a STOP condition.

In the case of the AD5301/AD5311/AD5321, a write operation contains two bytes whereas a read operation may contain one or two bytes. See Figures 24 to 29 below for a graphical explanation of the serial interface.

A repeated write function gives the user flexibility to update the DAC output a number of times after addressing the part only once. During the write cycle, each multiple of two data bytes will update the DAC output. For example, after the DAC has acknowledged its address byte, and receives two data bytes, the DAC output will update after the two data bytes, if another two data bytes are written to the DAC while it is still the addressed slave device, these data bytes will also cause an output update. Repeat read of the DAC is also allowed.

INPUT SHIFT REGISTER

The input shift register is 16 bits wide. Figure 23 illustrates the contents of the input shift register for each part. Data is loaded into the device as a 16-bit word under the control of a serial clock input, SCL. The timing diagram for this operation is shown in Figure 1. The 16-bit word consists of four control bits followed by 8, 10 or 12 bits of data, depending on the device type. MSB (Bit 15) is loaded first. The first two bits are "don't cares." The next two are control bits that control the mode of operation of the device (normal mode or any one of three power-down modes). See Power Down Modes section for a complete description. The remaining bits are left-justified DAC data bits, starting with the MSB and ending with the LSB.

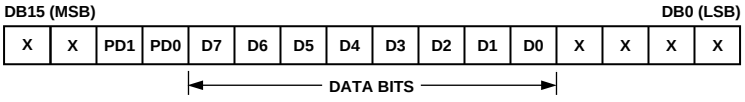


Figure 23a. AD5301 Input Shift Register Contents

Figure 23b. AD5311 Input Shift Register Contents

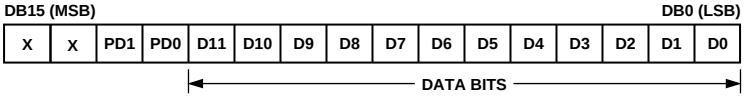


Figure 23c. AD5321 Input Shift Register Contents

WRITE OPERATION

When writing to the AD5301/AD5311/AD5321 DACs, the user must begin with an address byte, after which the DAC will acknowledge that it is prepared to receive data by pulling SDA low. This address byte is followed by the 16-bit word in the form of two control bytes. The write operations for the three DACs are shown in the figures below.

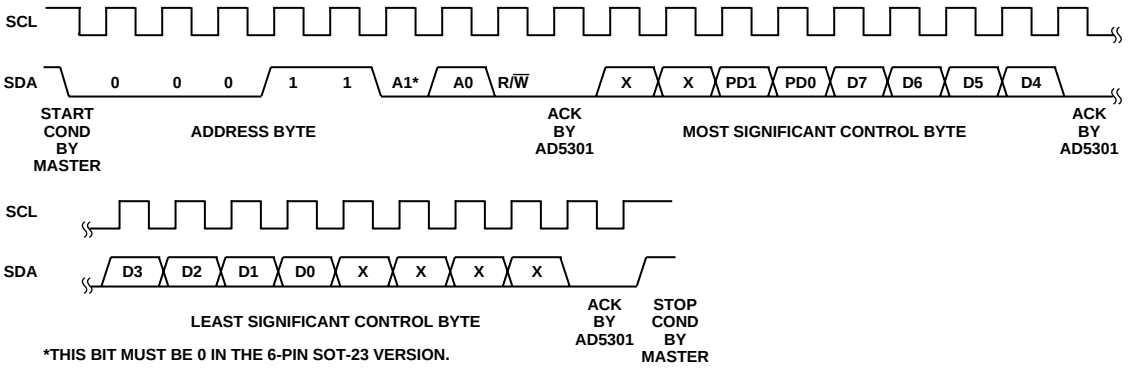


Figure 24. AD5301 Write Sequence

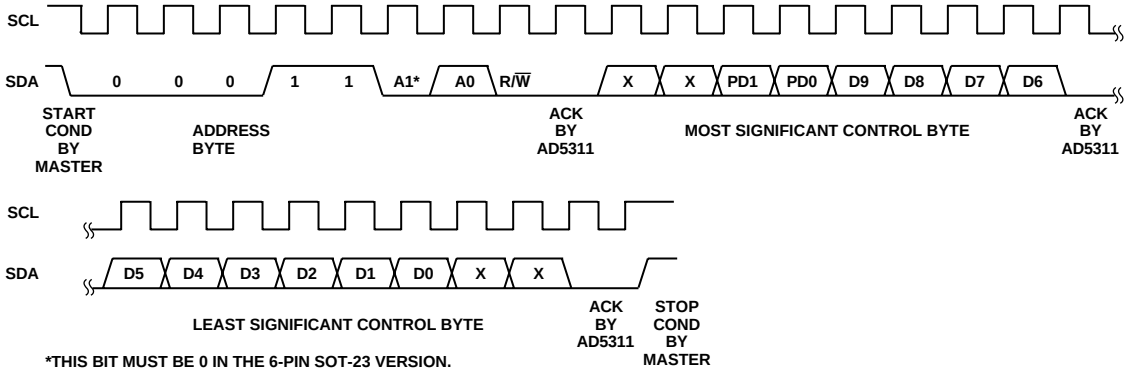


Figure 25. AD5311 Write Sequence

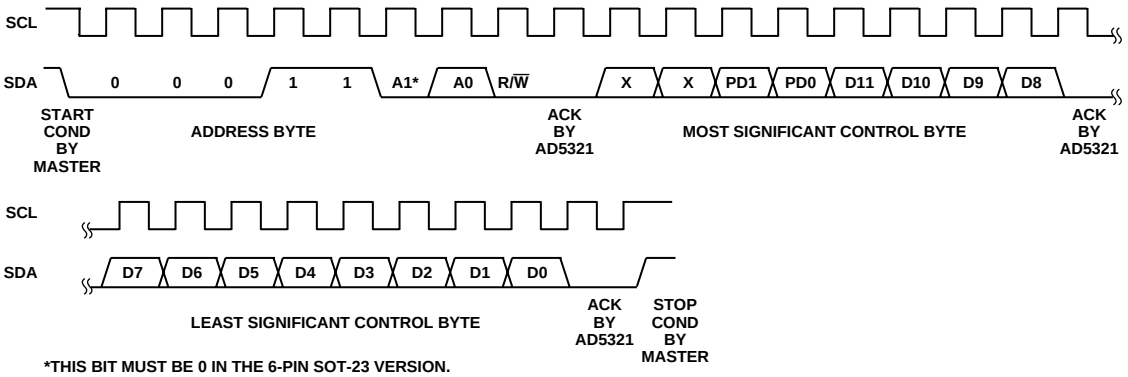


Figure 26. AD5321 Write Sequence

READ OPERATION

When reading data back from the AD5301/AD5311/AD5321 DACs, the user must begin with an address byte after which the DAC will acknowledge that it is prepared to transmit data by pulling SDA low. There are two different read operations. In the case of the AD5301, the readback is a single byte that consists of the eight data bits in the DAC register. However, in the case of the AD5311 and AD5321, the readback consists of two bytes that contain both the data and the power-down mode bits. The read operations for the three DACs are shown in the figures below.

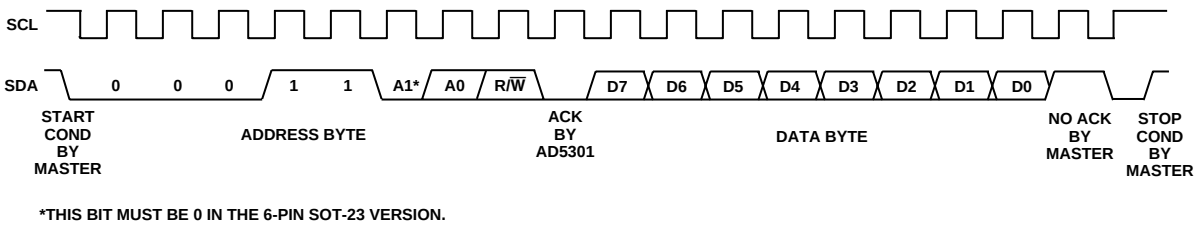


Figure 27. AD5301 Readback Sequence

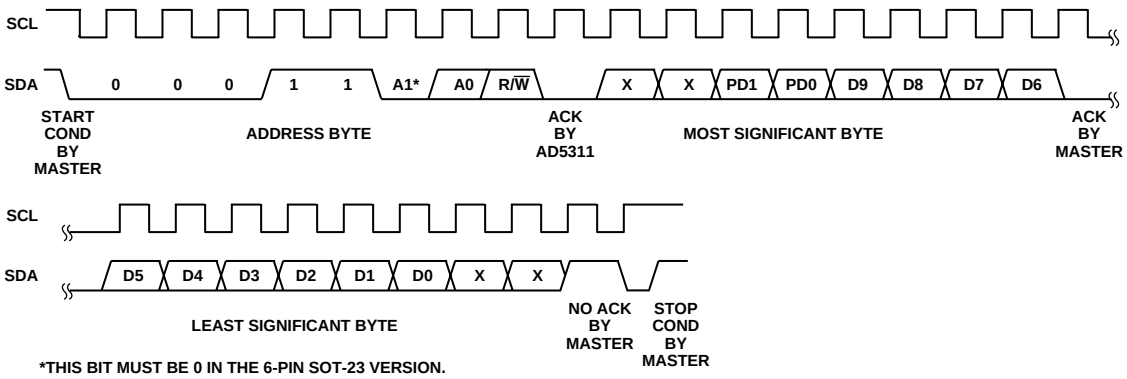


Figure 28. AD5311 Readback Sequence

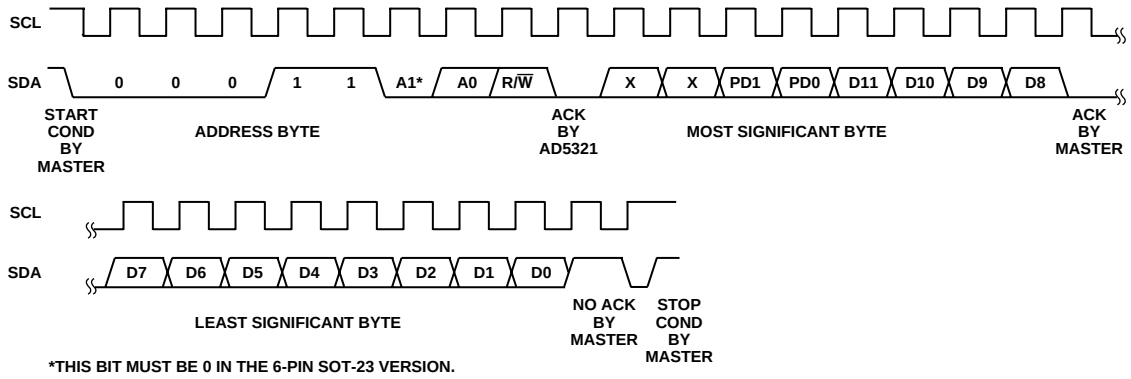


Figure 29. AD5321 Readback Sequence

POWER-DOWN MODES

The AD5301/AD5311/AD5321 have very low power consumption, dissipating typically 0.36 mW with a 3 V supply and 0.75 mW with a 5 V supply. Power consumption can be further reduced when the DAC is not in use by putting it into one of three power-down modes, which are selected by Bits 13 and 12 (PD1 and PD0) of the control word. Table I shows how the state of the bits corresponds to the mode of operation of the DAC.

Table I. PD1/PD0 Operating Modes

PD1	PD0	Operating Mode
0	0	Normal Operation
0	1	Power-Down (1 kΩ Load to GND)
1	0	Power-Down (100 kΩ Load to GND)
1	1	Power-Down (Three-State Output)

The software power-down modes programmed by PD0 and PD1 may be overridden by the $\overline{PD}$ pin on the 8-pin version. Taking this pin low puts the DAC into three-state power-down mode. If $\overline{PD}$ is not used it should be tied high.

When both bits are set to 0, the DAC works normally with its normal power consumption of 150 μA at 5 V, while for the three power-down modes, the supply current falls to 200 nA at 5 V (50 nA at 3 V). Not only does the supply current drop, but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This has the advantage that the output impedance of the part is known while the part is in power-down mode and provides a defined input condition for whatever is connected to the output of the DAC amplifier. There are three different options. The output is connected internally to GND through a 1 kΩ resistor, a 100 kΩ resistor or it is left open-circuited (Three-State). Resistor tolerance = ±20%. The output stage is illustrated in Figure 30.

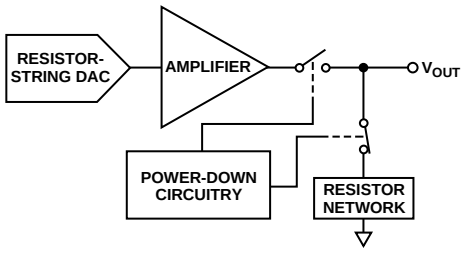


Figure 30. Output Stage During Power-Down

The bias generator, the output amplifier, the resistor string and all other associated linear circuitry are all shut down when the power-down mode is activated. However, the contents of the DAC register are unchanged when in power-Down. The time to exit power-down is typically 2.5 μs for V_{DD} = 5 V and 6 μs when V_{DD} = 3 V. See Figure 18 for a plot.

APPLICATIONS

USING REF19x AS A POWER SUPPLY

Because the supply current required by the AD5301/AD5311/AD5321 is extremely low, the user has an alternative option to use a REF19x voltage reference (REF195 for +5 V or REF193 for +3 V) to supply the required voltage to the part, see Figure 31.

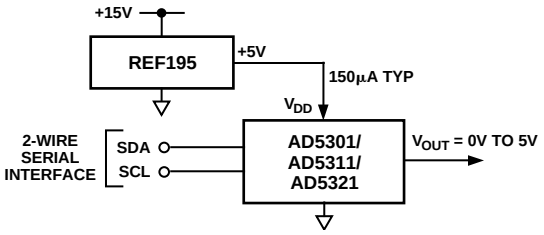


Figure 31. REF195 as Power Supply to AD5301/AD5311/AD5321

This is especially useful if the power supply is quite noisy or if the system supply voltages are at some value other than +5 V or +3 V (e.g., +15 V). The REF19x will output a steady supply voltage for the AD5301/AD5311/AD5321. If the low dropout REF195 is used, the current it needs to supply to the AD5301/AD5311/AD5321 is 150 μA. This is with no load on the output of the DAC. When the DAC output is loaded, the REF195 also needs to supply the current to the load.

The total current required (with a 2 kΩ load on the DAC output and full scale loaded to the DAC) is:

$$150\ \mu A + (5\ V/2\ k\Omega) = 2.65\ mA$$

The load regulation of the REF195 is typically 2 ppm/mA which results in an error of 5.3 ppm (26.5 μV) for the 2.65 mA current drawn from it. This corresponds to a 0.00136 LSB error.

BIPOLAR OPERATION USING THE AD5301/AD5311/AD5321

The AD5301/AD5311/AD5321 has been designed for single-supply operation but a bipolar output range is also possible using the circuit in Figure 32. The circuit below will give an output voltage range of ±5 V. Rail-to-rail operation at the amplifier output is achievable using an AD820 or an OP295 as the output amplifier.

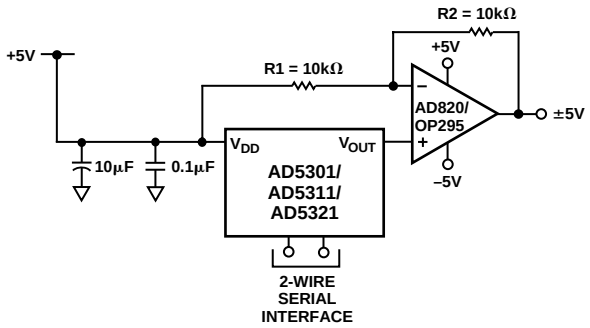


Figure 32. Bipolar Operation with the AD5301/AD5311/AD5321

The output voltage for any input code can be calculated as follows:

$$V_{OUT} = [(V_{DD} \times (D/2^N) \times (R1 + R2)/R1) - V_{DD} \times (R2/R1)]$$

where D is the decimal equivalent of the code loaded to the DAC.

N is the DAC resolution.

With V_{DD} = 5 V, R1 = R2 = 10 kΩ:

$$V_{OUT} = (10 \times D/2^N) - 5\ V$$

MULTIPLE DEVICES ON ONE BUS

Figure 33 shows four AD5301 devices on the same serial bus. Each has a different slave address since the state of their A0 and A1 pins is different. This allows each DAC to be written to or read from independently. The master device output bus line drivers are open-drain pull downs in a fully I²C-compatible interface.

CMOS DRIVEN SCL AND SDA LINES

For single or multisupply systems where the minimum SCL swing requirements allow it, a CMOS SCL driver may be used, the SCL pull-up resistor can be removed, making the SCL bus line fully CMOS compatible. This will reduce power consumption in both the SCL driver and receiver devices. The SDA line remains open-drain, I²C-compatible.

Further changes, in the SDA line driver, may be made to make the system more CMOS-compatible and save more power. As the SDA line is bidirectional, it cannot be made fully CMOS-compatible. A switched pull-up resistor can be combined with a CMOS device with an open-circuit (three-state) input such that the CMOS SDA driver is enabled during write cycles and I²C mode is enabled during shared cycles, i.e., readback, acknowledge bit cycles, start and stop conditions.

POWER SUPPLY DECOUPLING

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The AD5301/AD5311/AD5321 should be decoupled to GND with a 10 µF in parallel with 0.1 µF capacitor, located as close to the package as possible. The 10 µF capacitor should be the tantalum bead type, while a ceramic 0.1 µF capacitor will provide sufficient low impedance path to ground at high frequencies. The power supply lines of the AD5301/AD5311/AD5321 should use as large a trace as possible to provide low impedance paths. A ground line routed between the SDA and SCL lines will help reduce crosstalk between them (not required on a multilayer board as there will be a ground plane layer, but separating the lines will help).

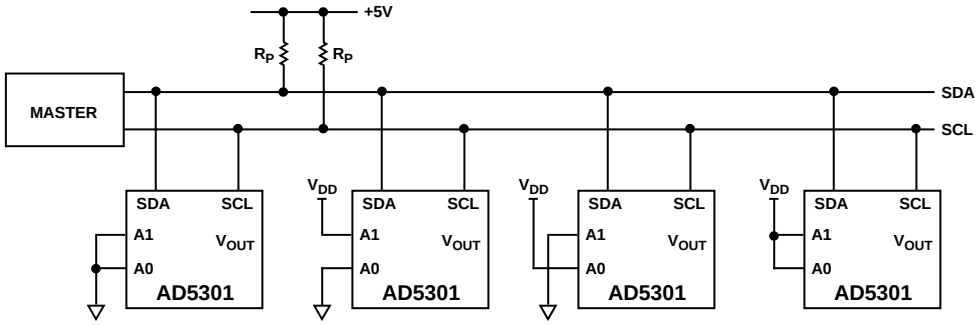
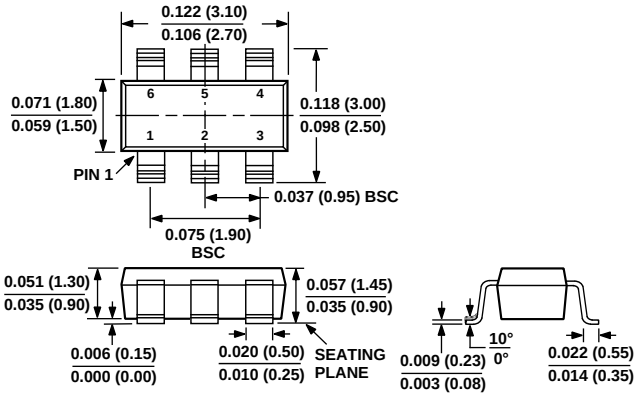


Figure 33. Multiple AD5301 Devices on One Bus

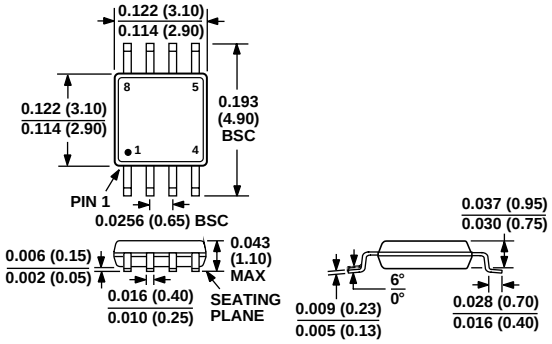
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

6-Lead SOT-23
(RT-6)



8-Lead μSOIC
(RM-8)



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