Single Supply, Rail-to-Rail, Low Cost Instrumentation Amplifier

AD623

FEATURES
Easy to Use
Higher Performance than Discrete Design
Single and Dual Supply Operation
Rail-to-Rail Output Swing
Input Voltage Range Extends 150 mV Below Ground (Single Supply)
Low Power, 575 μA Max Supply Current
Gain Set with One External Resistor
Gain Range 1 (No Resistor) to 1,000

HIGH ACCURACY DC PERFORMANCE
0.1% Gain Accuracy (G = 1)
0.35% Gain Accuracy (G > 1)
25 ppm Gain Drift (G = 1)
200 μV Max Input Offset Voltage (AD623A)
2 μV/°C Max Input Offset Drift (AD623A)
100 μV Max Input Offset Voltage (AD623B)
1 μV/°C Max Input Offset Drift (AD623B)
25 nA Max Input Bias Current

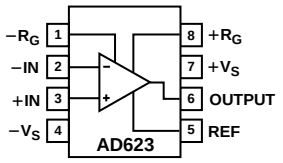
NOISE
35 nV/√Hz RTI Noise @ 1 kHz (G = 1)

EXCELLENT AC SPECIFICATIONS
90 dB Min CMRR (G = 10); 84 dB Min CMRR (G = 5) (@ 60 Hz, 1K Source Imbalance)
800 kHz Bandwidth (G = 1)
20 μs Settling Time to 0.01% (G = 10)

APPLICATIONS
Low Power Medical Instrumentation
Transducer Interface
Thermocouple Amplifier
Industrial Process Controls
Difference Amplifier
Low Power Data Acquisition

CONNECTION DIAGRAM

8-Lead Plastic DIP (N), SOIC (R) and μSOIC (RM) Packages



PRODUCT DESCRIPTION

The AD623 is an integrated single supply instrumentation amplifier that delivers rail-to-rail output swing on a single supply (+3 V to +12 V supplies). The AD623 offers superior user flexibility by allowing single gain set resistor programming, and conforming to the 8-lead industry standard pinout configuration. With no external resistor, the AD623 is configured for unity gain (G = 1) and with an external resistor, the AD623 can be programmed for gains up to 1,000.

The AD623 holds errors to a minimum by providing superior AC CMRR that increases with increasing gain. Line noise, as well as line harmonics, will be rejected since the CMRR remains constant up to 200 Hz. The AD623 has a wide input common-mode range and can amplify signals that have a common-mode voltage 150 mV below ground. Although the design of the AD623 has been optimized to operate from a single supply, the AD623 still provides superior performance when operated from a dual voltage supply (±2.5 V to ±6.0 V).

Low power consumption (1.5 mW at 3 V), wide supply voltage range, and rail-to-rail output swing make the AD623 ideal for battery powered applications. The rail-to-rail output stage maximizes the dynamic range when operating from low supply voltages. The AD623 replaces discrete instrumentation amplifier designs and offers superior linearity, temperature stability and reliability in a minimum of space. Until the AD623, this level of instrumentation amplifier performance has not been achieved.

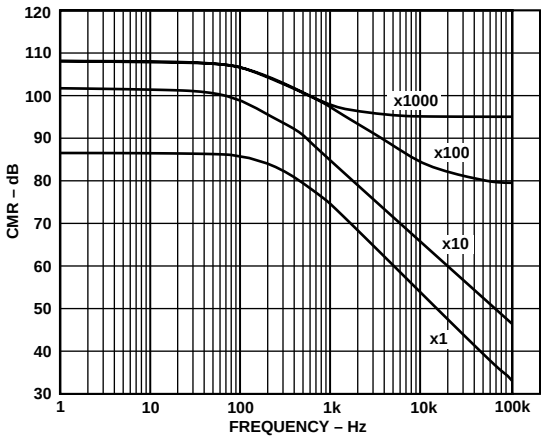


Figure 1. CMR vs. Frequency, +5 V_S, 0 V_S

REV. C

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AD623–SPECIFICATIONS

SINGLE SUPPLY (typical @ +25°C Single Supply, V_S = +5 V, and R_L = 10 kΩ, unless otherwise noted)

Model Specification	Conditions	AD623A Min	AD623A Typ	AD623A Max	AD623ARM Min	AD623ARM Typ	AD623ARM Max	AD623B Min	AD623B Typ	AD623B Max	Units
GAIN	G = 1 + (100 k/R_G)										
Gain Range		1		1000	1		1000	1		1000	
Gain Error[1]	G1 V_{OUT} = 0.05 V to 3.5 V G > 1 V_{OUT} = 0.05 V to 4.5 V										
G = 1			0.03	0.10		0.03	0.10		0.03	0.05	%
G = 10			0.10	0.35		0.10	0.35		0.10	0.35	%
G = 100			0.10	0.35		0.10	0.35		0.10	0.35	%
G = 1000			0.10	0.35		0.10	0.35		0.10	0.35	%
Nonlinearity,	G1 V_{OUT} = 0.05 V to 3.5 V G > 1 V_{OUT} = 0.05 V to 4.5 V										
G = 1–1000			50			50			50		ppm
Gain vs. Temperature											
G = 1			5	10		5	10		5	10	ppm/°C
G > 1[1]			50			50			50		ppm/°C
VOLTAGE OFFSET	Total RTI Error = V_{OSI} + V_{OSO}/G										
Input Offset, V_{OSI}			25	200		200	500		25	100	µV
Over Temperature				350			650			160	µV
Average TC			0.1	2		0.1	2		0.1	1	µV/°C
Output Offset, V_{OSO}			200	1000		500	2000		200	500	µV
Over Temperature				1500			2600			1100	µV
Average TC			2.5	10		2.5	10		2.5	10	µV/°C
Offset Referred to the Input vs. Supply (PSR)											
G = 1		80	100		80	100		80	100		dB
G = 10		100	120		100	120		100	120		dB
G = 100		120	140		120	140		120	140		dB
G = 1000		120	140		120	140		120	140		dB
INPUT CURRENT											
Input Bias Current			17	25		17	25		17	25	nA
Over Temperature				27.5			27.5			27.5	nA
Average TC			25			25			25		pA/°C
Input Offset Current			0.25	2		0.25	2		0.25	2	nA
Over Temperature				2.5			2.5			2.5	nA
Average TC			5			5			5		pA/°C
INPUT											
Input Impedance											
Differential			2‖2			2‖2			2‖2		GΩ‖pF
Common-Mode			2‖2			2‖2			2‖2		GΩ‖pF
Input Voltage Range[2]	V_S = +3 V to +12 V	(–V_S) – 0.15		(+V_S) – 1.5	(–V_S) – 0.15		(+V_S) – 1.5	(–V_S) – 0.15		(+V_S) – 1.5	V
Common-Mode Rejection at 60 Hz with 1 kΩ Source Imbalance											
G = 1	V_{CM} = 0 V to 3 V	70	80		70	80		77	86		dB
G = 10	V_{CM} = 0 V to 3 V	90	100		90	100		94	100		dB
G = 100	V_{CM} = 0 V to 3 V	105	110		105	110		105	110		dB
G = 1000	V_{CM} = 0 V to 3 V	105	110		105	110		105	110		dB
OUTPUT											
Output Swing	R_L = 10 kΩ	+0.01		(+V_S) – 0.5	+0.01		(+V_S) – 0.5	+0.01		(+V_S) – 0.5	V
	R_L = 100 kΩ	+0.01		(+V_S) – 0.15	+0.01		(+V_S) – 0.15	+0.01		(+V_S) – 0.15	V
DYNAMIC RESPONSE											
Small Signal –3 dB Bandwidth											
G = 1			800			800			800		kHz
G = 10			100			100			100		kHz
G = 100			10			10			10		kHz
G = 1000			2			2			2		kHz
Slew Rate			0.3			0.3			0.3		V/µs
Settling Time to 0.01%	V_S = +5 V										
G = 1	Step Size: 3.5 V		30			30			30		µs
G = 10	Step Size: 4 V, V_{CM} = 1.8 V		20			20			20		µs

DUAL SUPPLIES (typical @ +25°C Dual Supply, V_S = ±5 V, and R_L = 10 kΩ, unless otherwise noted)

Model Specification	Conditions	AD623A Min	AD623A Typ	AD623A Max	AD623ARM Min	AD623ARM Typ	AD623ARM Max	AD623B Min	AD623B Typ	AD623B Max	Units
GAIN	G = 1 + (100 k/R_G)										
Gain Range		1		1000	1		1000	1		1000	
Gain Error[1]	G1 V_{OUT} = −4.8 V to 3.5 V G > 1 V_{OUT} = 0.05 V to 4.5 V										
G = 1			0.03	0.10		0.03	0.10		0.03	0.05	%
G = 10			0.10	0.35		0.10	0.35		0.10	0.35	%
G = 100			0.10	0.35		0.10	0.35		0.10	0.35	%
G = 1000			0.10	0.35		0.10	0.35		0.10	0.35	%
Nonlinearity,	G1 V_{OUT} = −4.8 V to 3.5 V G > 1 V_{OUT} = −4.8 V to 4.5 V										
G = 1–1000			50			50			50		ppm
Gain vs. Temperature											
G = 1			5	10		5	10		5	10	ppm/°C
G > 1[1]			50			50			50		ppm/°C
VOLTAGE OFFSET	Total RTI Error = V_{OSI} + V_{OSO}/G										
Input Offset, V_{OSI}			25	200		200	500		25	100	µV
Over Temperature				350			650			160	µV
Average TC			0.1	2		0.1	2		0.1	1	µV/°C
Output Offset, V_{OSO}			200	1000		500	2000		200	500	µV
Over Temperature				1500			2600			1100	µV
Average TC			2.5	10		2.5	10		2.5	10	µV/°C
Offset Referred to the Input vs. Supply (PSR)											
G = 1		80	100		80	100		80	100		dB
G = 10		100	120		100	120		100	120		dB
G = 100		120	140		120	140		120	140		dB
G = 1000		120	140		120	140		120	140		dB
INPUT CURRENT											
Input Bias Current			17	25		17	25		17	25	nA
Over Temperature				27.5			27.5			27.5	nA
Average TC			25			25			25		pA/°C
Input Offset Current			0.25	2		0.25	2		0.25	2	nA
Over Temperature				2.5			2.5			2.5	nA
Average TC			5			5			5		pA/°C
INPUT											
Input Impedance											
Differential			2‖2			2‖2			2‖2		GΩ‖pF
Common-Mode			2‖2			2‖2			2‖2		GΩ‖pF
Input Voltage Range[2]	V_S = +2.5 V to ±6 V	(−V_S) − 0.15		(+V_S) − 1.5	(−V_S) −0.15		(+V_S) − 1.5	(−V_S) − 0.15		(+V_S) − 1.5	V
Common-Mode Rejection at 60 Hz with 1 kΩ Source Imbalance											
G = 1	V_{CM} = +3.5 V to −5.15 V	70	80		70	80		77	86		dB
G = 10	V_{CM} = +3.5 V to −5.15 V	90	100		90	100		94	100		dB
G = 100	V_{CM} = +3.5 V to −5.15 V	105	110		105	110		105	110		dB
G = 1000	V_{CM} = +3.5 V to −5.15 V	105	110		105	110		105	110		dB
OUTPUT											
Output Swing	R_L = 10 kΩ, V_S = ±5 V	(−V_S) +0. 2		(+V_S) − 0.5	(−V_S) + 0.2		(+V_S) − 0.5	(−V_S) + 0.2		(+V_S) − 0.5	V
	R_L = 100 kΩ	(−V_S) + 0.05		(+V_S) − 0.15	(−V_S) + 0.05		(+V_S) − 0.15	(−V_S) + 0.05		(+V_S) − 0.15	V
DYNAMIC RESPONSE											
Small Signal −3 dB Bandwidth											
G = 1			800			800			800		kHz
G = 10			100			100			100		kHz
G = 100			10			10			10		kHz
G = 1000			2			2			2		kHz
Slew Rate			0.3			0.3			0.3		V/µs
Settling Time to 0.01%	V_S = ±5 V, 5 V Step										
G = 1			30			30			30		µs
G = 10			20			20			20		µs

AD623–SPECIFICATIONS
BOTH DUAL AND SINGLE SUPPLIES

Model Specification	Conditions	AD623A Min	AD623A Typ	AD623A Max	AD623ARM Min	AD623ARM Typ	AD623ARM Max	AD623B Min	AD623B Typ	AD623B Max	Units
NOISE											
Voltage Noise, 1 kHz	Total RTI Noise = $\sqrt{\left(e_{ni}\right)^2 + \left(e_{no}/G\right)^2}$										
Input, Voltage Noise, e_{ni}			35			35			35		nV/√Hz
Output, Voltage Noise, e_{no}			50			50			50		nV/√Hz
RTI, 0.1 Hz to 10 Hz											
G = 1			3.0			3.0			3.0		µV p-p
G = 1000			1.5			1.5			1.5		µV p-p
Current Noise	f = 1 kHz		100			100			100		fA/√Hz
0.1 Hz to 10 Hz			1.5			1.5			1.5		pA p-p
REFERENCE INPUT											
R_{IN}			100	±20%		100	±20%		100	±20%	kΩ
I_{IN}	V_{IN+}, V_{REF} = 0		+50	+60		+50	+60		+50	+60	µA
Voltage Range		$-V_S$		$+V_S$	$-V_S$		$+V_S$	$-V_S$		$+V_S$	V
Gain to Output			1 ± 0.0002			1 ± 0.0002			1 ± 0.0002		V
POWER SUPPLY											
Operating Range	Dual Supply	±2.5		±6	±2.5		±6	±2.5		±6	V
	Single Supply	+2.7		+12	+2.7		+12	+2.7		+12	V
Quiescent Current	Dual Supply		375	550		375	550		375	550	µA
	Single Supply		305	480		305	480		305	480	µA
Over Temperature				625			625			625	µA
TEMPERATURE RANGE											
For Specified Performance			–40 to +85			–40 to +85			–40 to +85		°C

NOTES
[1]Does not include effects of external resistor R_G.
[2]One input grounded. G = 1.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±6 V
Internal Power Dissipation[2] . . . . . 650 mW
Differential Input Voltage . . . . . ±6 V
Output Short Circuit Duration . . . . . Indefinite
Storage Temperature Range
(N, R, RM) . . . . . –65°C to +125°C
Operating Temperature Range
(A) . . . . . –40°C to +85°C
Lead Temperature Range
(Soldering 10 seconds) . . . . . +300°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Specification is for device in free air:
8-Lead Plastic DIP Package: θ_{JA} = 95°C/W
8-Lead SOIC Package: θ_{JA} = 155°C/W
8-Lead µSOIC Package: θ_{JA} = 200°C/W

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Brand Code
AD623AN	–40°C to +85°C	8-Lead Plastic DIP	N-8	
AD623AR	–40°C to +85°C	8-Lead SOIC	SO-8	
AD623ARM	–40°C to +85°C	8-Lead µSOIC	RM-8	J0A
AD623AR-REEL	–40°C to +85°C	13" Tape and Reel	SO-8	
AD623AR-REEL7	–40°C to +85°C	7" Tape and Reel	SO-8	
AD623ARM-REEL	–40°C to +85°C	13" Tape and Reel	RM-8	J0A
AD623ARM-REEL7	–40°C to +85°C	7" Tape and Reel	RM-8	J0A
AD623BN	–40°C to +85°C	8-Lead Plastic DIP	N-8	
AD623BR	–40°C to +85°C	8-Lead SOIC	SO-8	
AD623BR-REEL	–40°C to +85°C	13" Tape and Reel	SO-8	
AD623BR-REEL7	–40°C to +85°C	7" Tape and Reel	SO-8	

ESD SUSCEPTIBILITY

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 volts, which readily accumulate on the human body and on test equipment, can discharge without detection. Although the AD623 features proprietary ESD protection circuitry, permanent damage may still occur on these devices if they are subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.

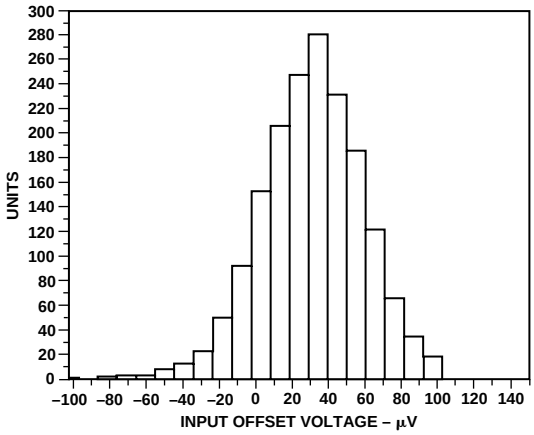


Figure 2. Typical Distribution of Input Offset Voltage; Package Option N-8, SO-8

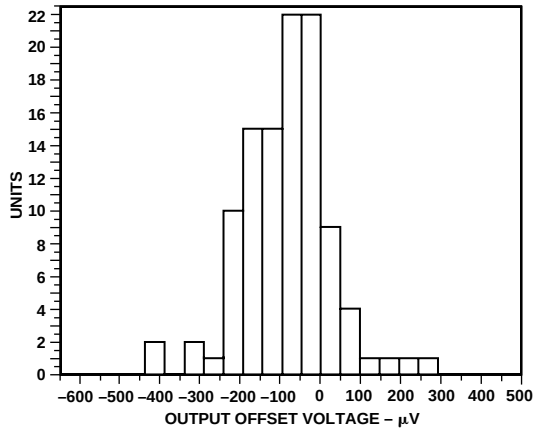


Figure 5. Typical Distribution of Output Offset Voltage, V_S = +5, Single Supply, V_{REF} = –0.125 V; Package Option N-8, SO-8

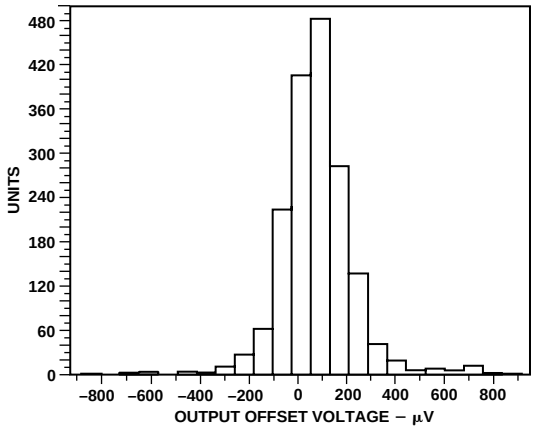


Figure 3. Typical Distribution of Output Offset Voltage; Package Option N-8, SO-8

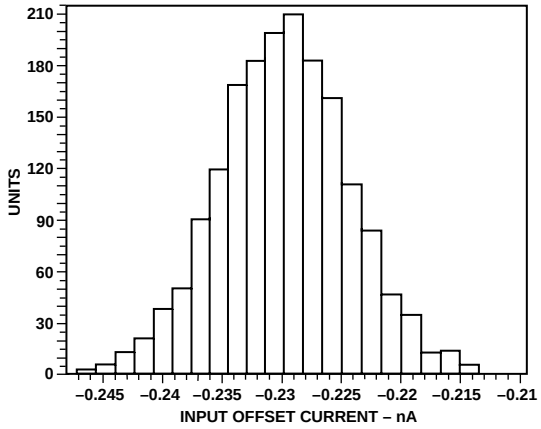


Figure 6. Typical Distribution for Input Offset Current; Package Option N-8, SO-8

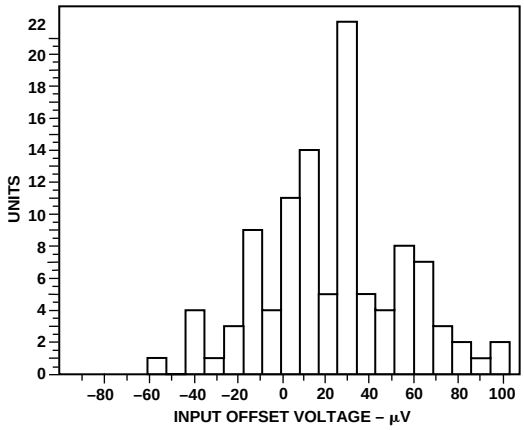


Figure 4. Typical Distribution of Input Offset Voltage, V_S = +5, Single Supply, V_{REF} = –0.125 V; Package Option N-8, SO-8

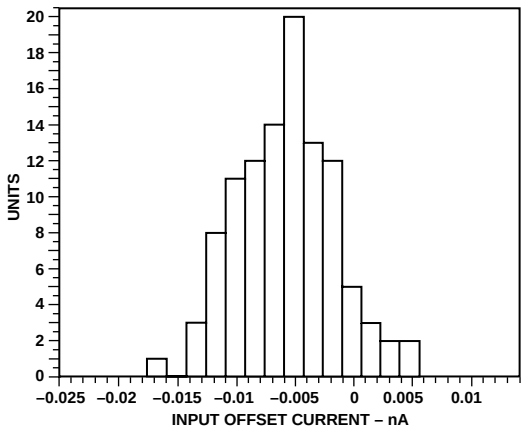


Figure 7. Typical Distribution for Input Offset Current, V_S = +5, Single Supply, V_{REF} = –0.125 V; Package Option N-8, SO-8

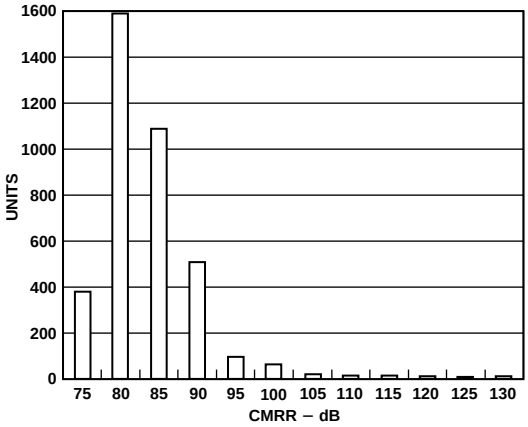


Figure 8. Typical Distribution for CMRR (G = 1)

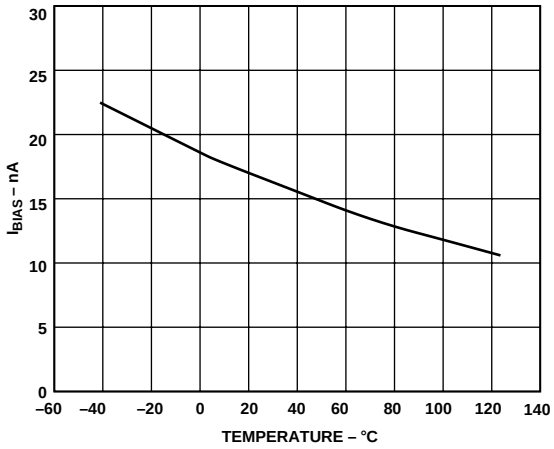


Figure 11. I_{BIAS} vs. Temp

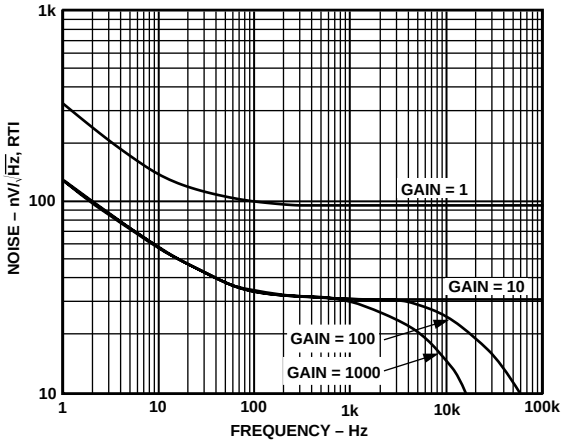


Figure 9. Voltage Noise Spectral Density vs. Frequency

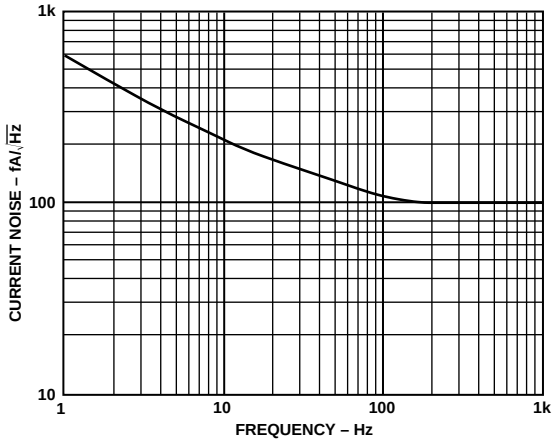


Figure 12. Current Noise Spectral Density vs. Frequency

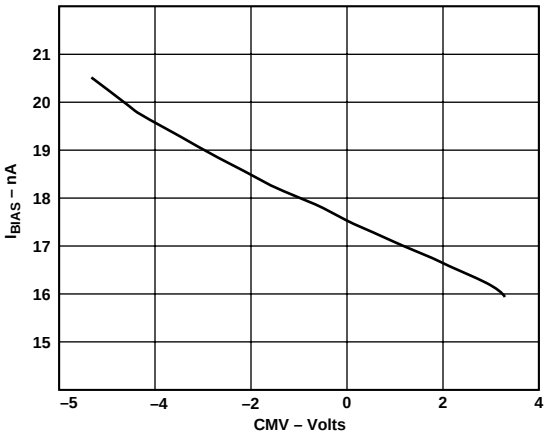


Figure 10. I_{BIAS} vs. CMV, $V_S = \pm 5$ V

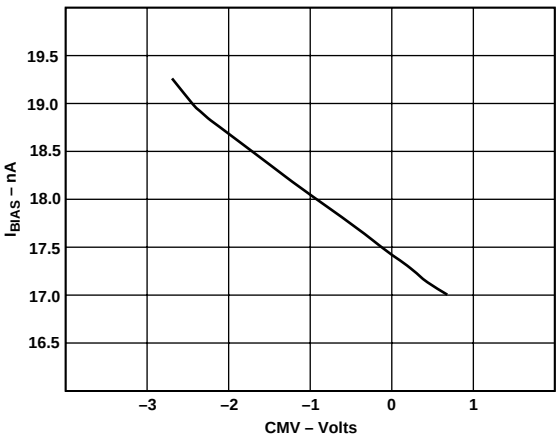


Figure 13. I_{BIAS} vs. CMV, $V_S = \pm 2.5$ V

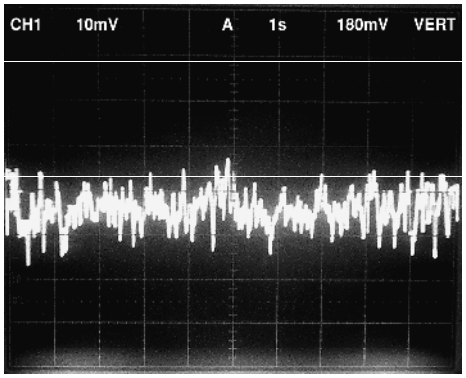


Figure 14. 0.1 Hz to 10 Hz Current Noise (0.71 pA/Div)

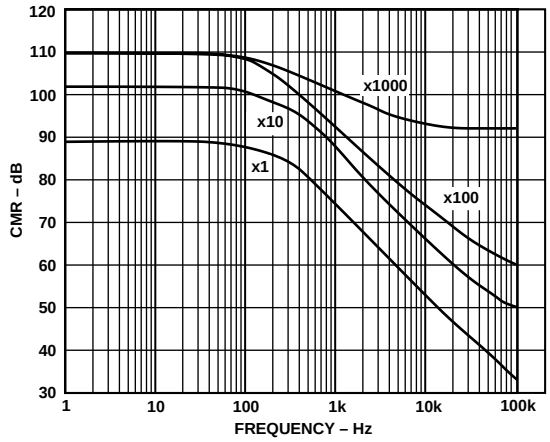


Figure 17. CMR vs. Frequency, ±5 V_S

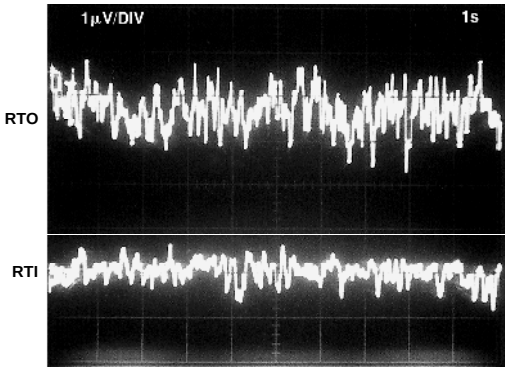


Figure 15. 0.1 Hz to 10 Hz RTI Voltage Noise (1 Div = 1 µV p-p)

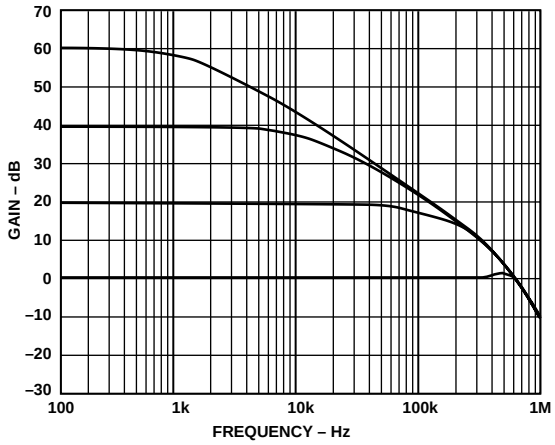


Figure 18. Gain vs. Frequency (V_S = +5 V, 0 V), V_{REF} = 2.5 V

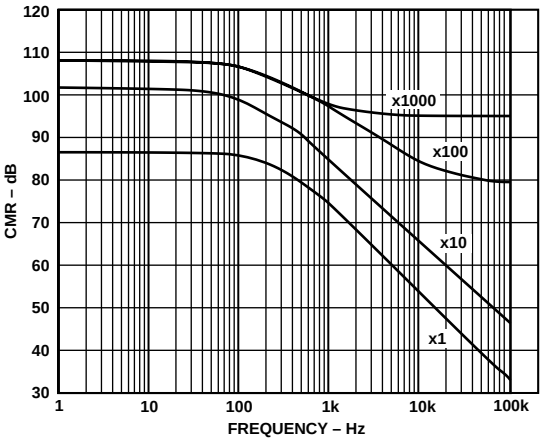


Figure 16. CMR vs. Frequency, +5, 0 V_S, V_{REF} = 2.5 V

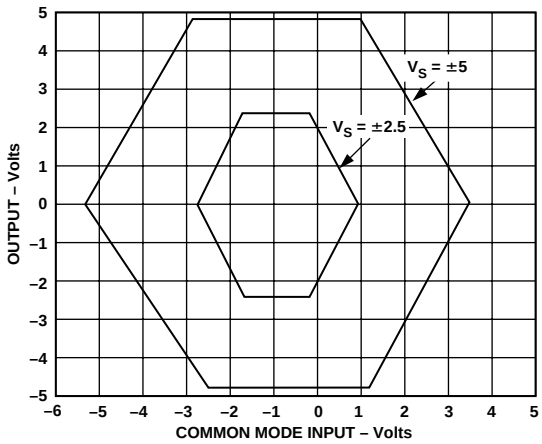


Figure 19. Maximum Output Voltage vs. Common Mode, G = 1, R_L = 100 kΩ

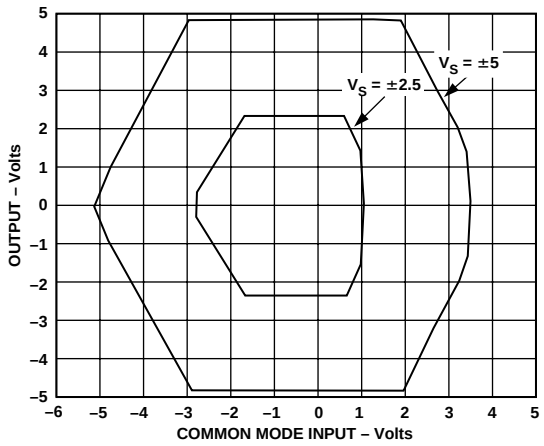


Figure 20. Maximum Output Voltage vs. Common Mode, G ≥ 10, R_L = 100 kΩ

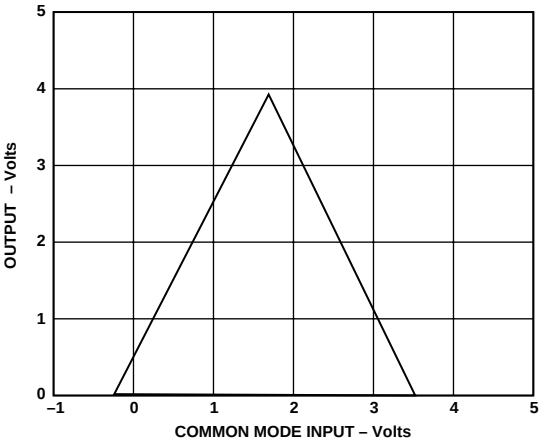


Figure 21. Maximum Output Voltage vs. Common Mode, G = 1, V_S = +5 V, R_L = 100 kΩ

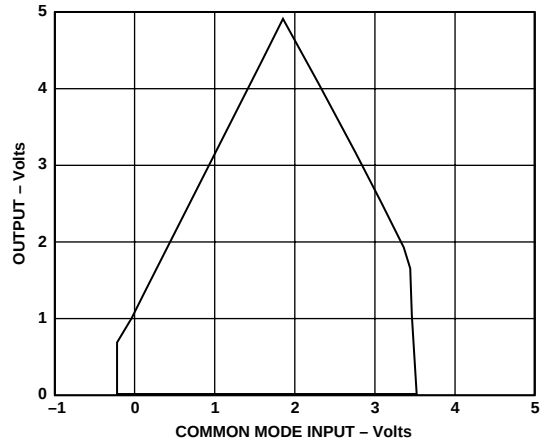


Figure 22. Maximum Output Voltage vs. Common Mode, G ≥ 10, V_S = +5 V, R_L = 100 kΩ

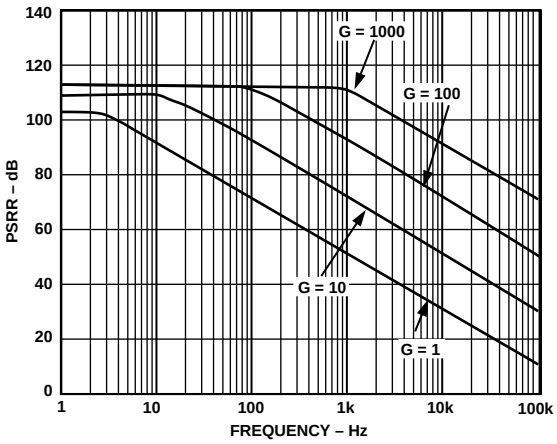


Figure 23. Positive PSRR vs. Frequency, ±5 V_S

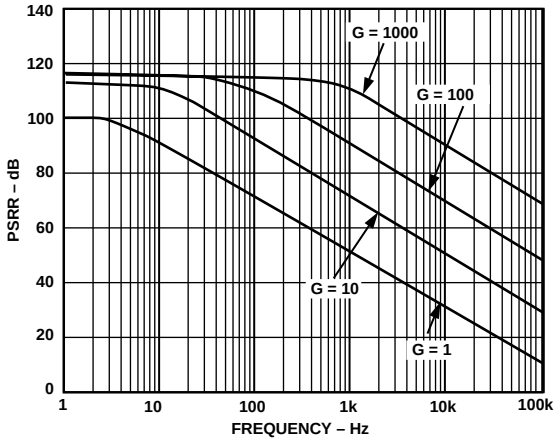


Figure 24. Positive PSRR vs. Frequency, +5 V_S, 0 V_S

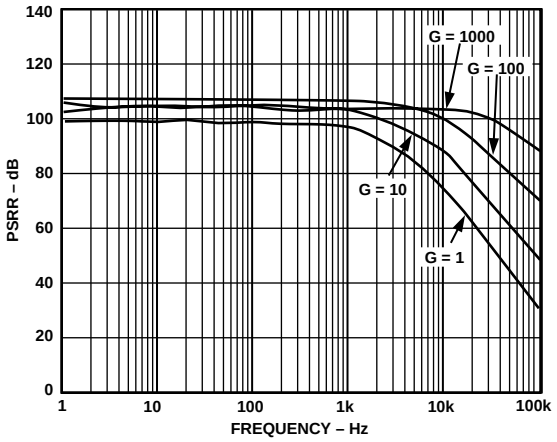


Figure 25. Negative PSRR vs. Frequency, ±5 V_S

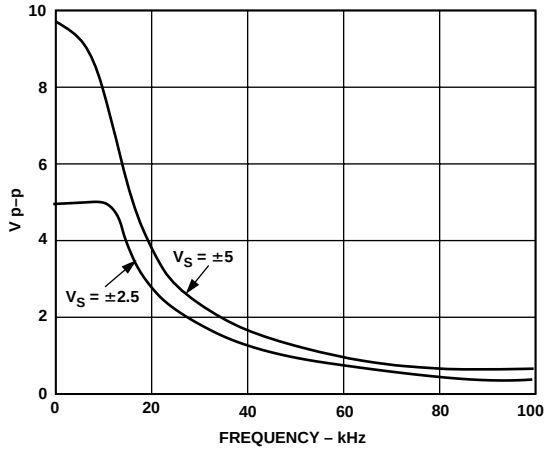


Figure 26. Large Signal Response, G ≤ 10

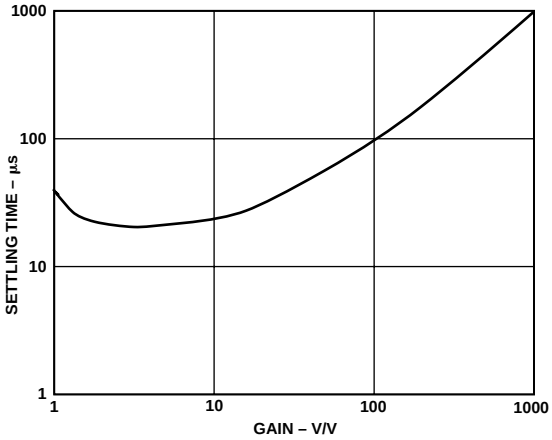


Figure 27. Settling Time to 0.01% vs. Gain, for a 5 V Step at Output, C_L = 100 pF, V_S = ±5 V

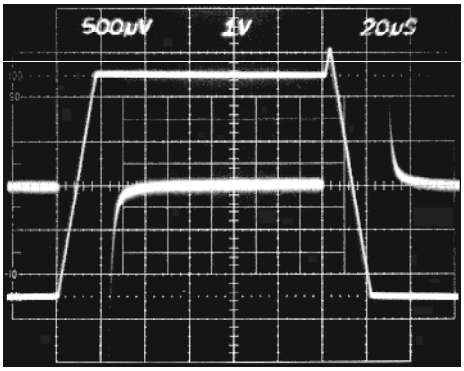


Figure 28. Large Signal Pulse Response and Settling Time, G = –1 (0.250 mV = 0.01%), C_L = 100 pF

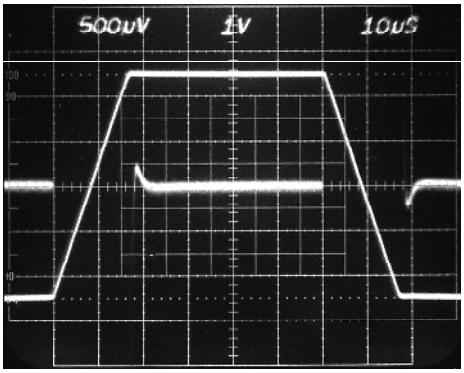


Figure 29. Large Signal Pulse Response and Settling Time, G = –10 (0.250 mV = 0.01%), C_L = 100 pF

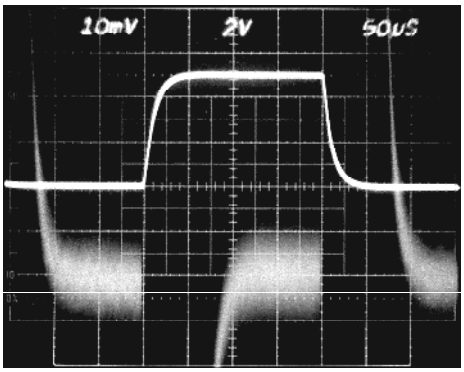


Figure 30. Large Signal Pulse Response and Settling Time, G = 100, C_L = 100 pF

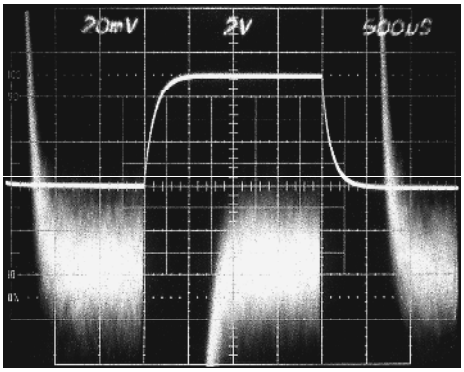


Figure 31. Large Signal Pulse Response and Settling Time, G = –1000 (5 mV = 0.01%), C_L = 100 pF

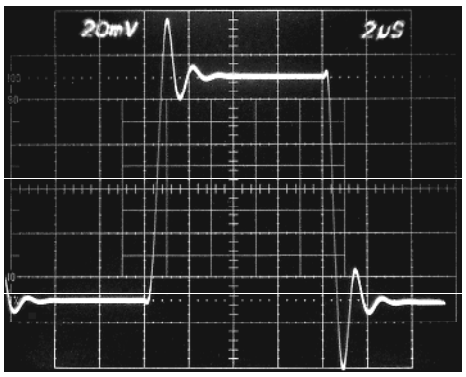


Figure 32. Small Signal Pulse Response, G = 1, R_L = 10 kΩ, C_L = 100 pF

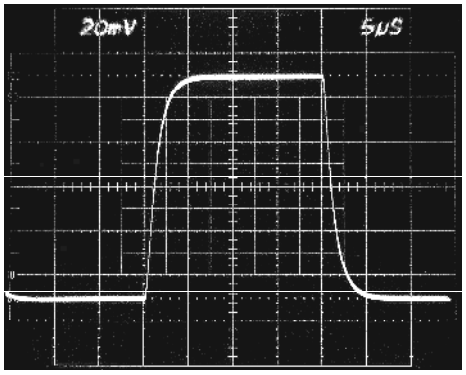


Figure 33. Small Signal Pulse Response, G = 10, R_L = 10 kΩ, C_L = 100 pF

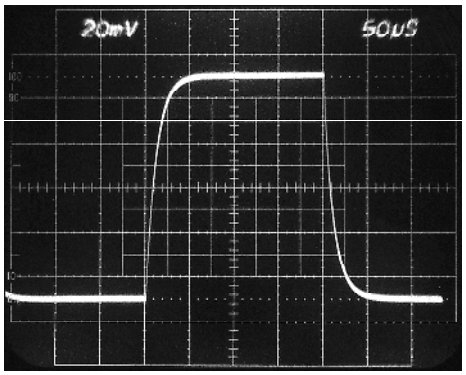


Figure 34. Small Signal Pulse Response G = 100, R_L = 10 kΩ, C_L = 100 pF

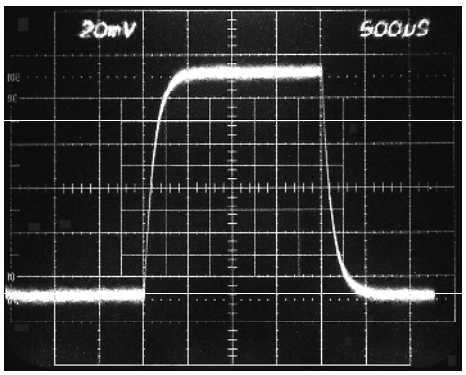


Figure 35. Small Signal Pulse Response, G = 1000, R_L = 10 kΩ, C_L = 100 pF

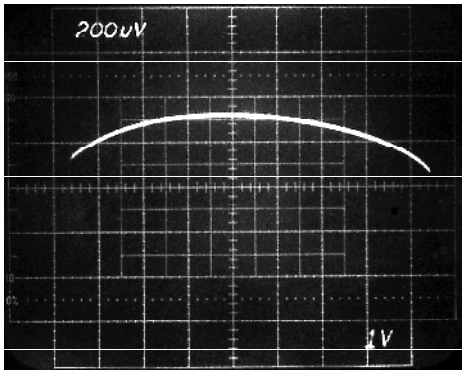


Figure 36. Gain Nonlinearity, G = –1 (50 ppm/Div)

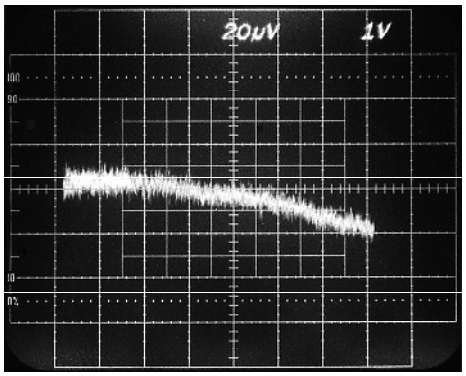


Figure 37. Gain Nonlinearity, G = –10 (6 ppm/Div)

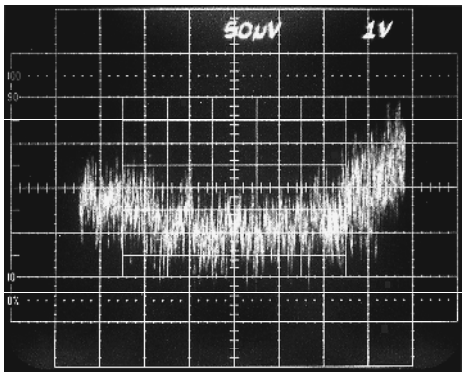


Figure 38. Gain Nonlinearity (G = –100, 15 ppm/Div)

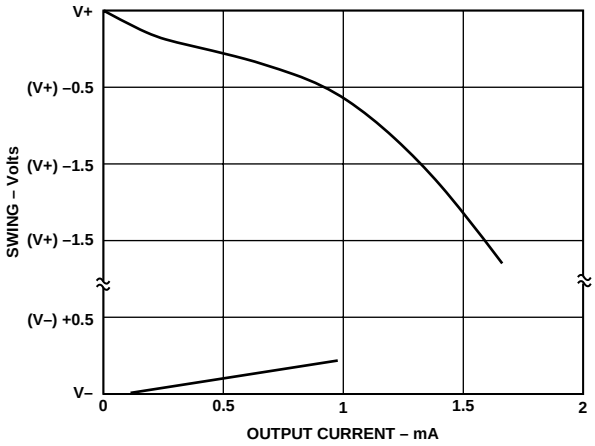


Figure 39. Output Voltage Swing vs. Output Current

THEORY OF OPERATION

The AD623 is an instrumentation amplifier based on a modified classic three op amp approach, to assure single or dual supply operation even at common-mode voltages at the negative supply rail. Low voltage offsets, input and output, as well as absolute gain accuracy, and one external resistor to set the gain, make the AD623 one of the most versatile instrumentation amplifiers in its class.

The input signal is applied to PNP transistors acting as voltage buffers and providing a common-mode signal to the input amplifiers (Figure 40). An absolute value 50 kΩ resistor in each of the amplifiers' feedback assures gain programmability.

The differential output is

$$V_O = \left(1 + \frac{100\ k\Omega}{R_G}\right) V_C$$

The differential voltage is then converted to a single-ended voltage using the output amplifier, which also rejects any common-mode signal at the output of the input amplifiers.

Since all the amplifiers can swing to either supply rails, as well as have their common-mode range extended to below the negative supply rail, the range over which the AD623 can operate is further enhanced (Figures 19 and 20).

The output voltage at Pin 6 is measured with respect to the potential at Pin 5. The impedance of the reference pin is 100 kΩ, so in applications requiring V/I conversion, a small resistor between Pins 5 and 6 is all that is needed.

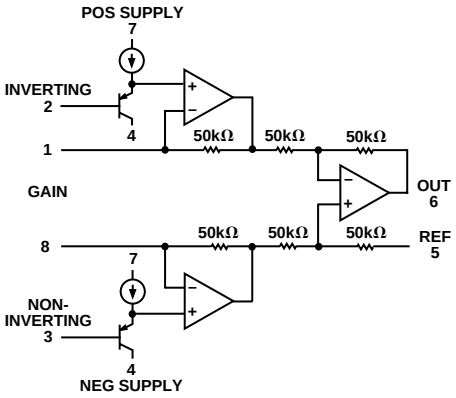


Figure 40. Simplified Schematic

The bandwidth of the AD623 is reduced as the gain is increased, since all the amplifiers are of voltage feedback type. At unity gain, it is the output amplifier that limits the bandwidth. Therefore even at higher gains the AD623 bandwidth does not roll off as quickly.

APPLICATIONS

Basic Connection

Figure 41 shows the basic connection circuit for the AD623. The $+V_S$ and $-V_S$ terminals are connected to the power supply. The supply can be either bipolar (V_S = ±2.5 V to ±6 V) or single supply ($-V_S$ = 0 V, $+V_S$ = 3.0 V to 12 V). Power supplies should be capacitively decoupled close to the devices power pins. For best results, use surface mount 0.1 µF ceramic chip capacitors and 10 µF electrolytic tantalum capacitors.

The input voltage, which can be either single-ended (tie either –IN or +IN to ground) or differential is amplified by the programmed gain. The output signal appears as the voltage difference between the Output pin and the externally applied voltage on the REF input. For a ground referenced output, REF should be grounded.

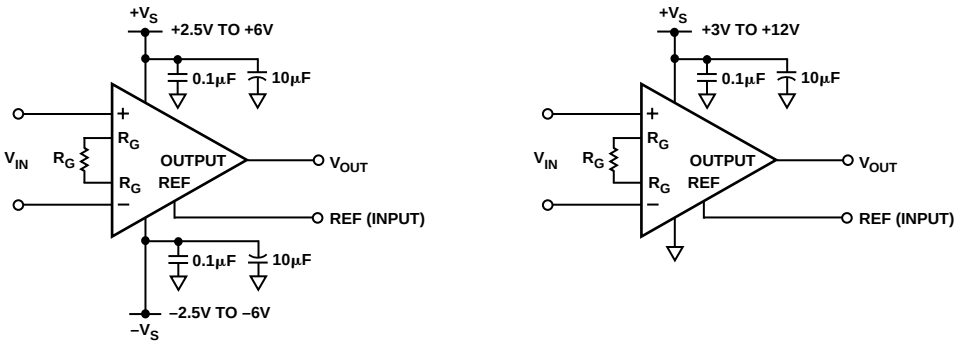
GAIN SELECTION

The AD623's gain is resistor programmed by R_G, or more precisely, by whatever impedance appears between Pins 1 and 8. The AD623 is designed to offer accurate gains using 0.1%–1% tolerance resistors. Table I shows required values of R_G for various gains. Note that for G = 1, the R_G terminals are unconnected ($R_G = \infty$). For any arbitrary gain, R_G can be calculated by using the formula

$$R_G = 100\ k\Omega/(G - 1)$$

REFERENCE TERMINAL

The reference terminal potential defines the zero output voltage and is especially useful when the load does not share a precise ground with the rest of the system. It provides a direct means of injecting a precise offset to the output. The reference terminal is also useful when bipolar signals are being amplified as it can be used to provide a virtual ground voltage. The voltage on the reference terminal can be varied from $-V_S$ to $+V_S$.



a. Dual Supply *b. Single Supply*

Figure 41. Basic Connections

Table I. Required Values of Gain Resistors

Desired Gain	1% Std Table Value of R_G, Ω	Calculated Gain Using 1% Resistors
2	100 k	2
5	24.9 k	5.02
10	11 k	10.09
20	5.23 k	20.12
33	3.09 k	33.36
40	2.55 k	40.21
50	2.05 k	49.78
65	1.58 k	64.29
100	1.02 k	99.04
200	499	201.4
500	200	501
1000	100	1001

INPUT AND OUTPUT OFFSET VOLTAGE

The low errors of the AD623 are attributed to two sources, input and output errors. The output error is divided by the programmed gain when referred to the input. In practice, the input errors dominate at high gains and the output errors dominate at low gains. The total V_{OS} for a given gain is calculated as:

Total Error RTI = Input Error + (Output Error/G)

Total Error RTO = (Input Error × G) + Output Error

RTI offset errors and noise voltages for different gains are shown below in Table II.

Table II. RTI Error Sources

Gain	Max Total Input Offset Error µV		Max Total Input Offset Drift µV/°C		Total Input Referred Noise (nV/√Hz)
	AD623A	AD623B	AD623A	AD623B	AD623A & AD623B
1	1200	600	12	11	62
2	700	350	7	6	45
5	400	200	4	3	38
10	300	150	3	2	35
20	250	125	2.5	1.5	35
50	220	110	2.2	1.2	35
100	210	105	2.1	1.1	35
1000	200	100	2	1	35

INPUT PROTECTION

Internal supply referenced clamping diodes allow the input, reference, output and gain terminals of the AD623 to safely withstand overvoltages of 0.3 V above or below the supplies. This is true for all gains, and for power on and off. This last case is particularly important since the signal source and amplifier may be powered separately.

If the overvoltage is expected to exceed this value, the current through these diodes should be limited to about 10 mA using external current limiting resistors. This is shown in Figure 42. The size of this resistor is defined by the supply voltage and the required overvoltage protection.

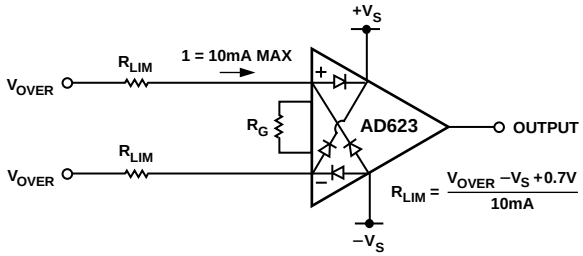


Figure 42. Input Protection

RF INTERFERENCE

All instrumentation amplifiers can rectify high frequency out-of-band signals. Once rectified, these signals appear as dc offset errors at the output. The circuit of Figure 43 provides good RFI suppression without reducing performance within the in amps pass band. Resistor R1 and capacitor C1 (and likewise, R2 and C2) form a low-pass RC filter that has a –3 dB BW equal to: $F = 1/(2\pi R1C1)$. Using the component values shown, this filter has a –3 dB bandwidth of approximately 40 kHz. Resistors R1 and R2 were selected to be large enough to isolate the circuit's input from the capacitors, but not large enough to significantly increase the circuit's noise. To preserve common-mode rejection in the amplifier's pass band, capacitors C1 and C2 need to be 5% or better units, or low cost 20% units can be tested and "binned" to provide closely matched devices.

Capacitor C3 is needed to maintain common-mode rejection at the low frequencies. R1/R2 and C1/C2 form a bridge circuit whose output appears across the in amp's input pins. Any mismatch between C1 and C2 will unbalance the bridge and reduce common-mode rejection. C3 ensures that any RF signals

are common mode (the same on both in amp inputs) and are not applied differentially. This second low pass network, R1+R2 and C3, has a –3 dB frequency equal to: 1/(2 π (R1+R2) (C3)). Using a C3 value of 0.047 µF as shown, the –3 dB signal BW of this circuit is approximately 400 Hz. The typical dc offset shift over frequency will be less than 1.5 µV and the circuit's RF signal rejection will be better than 71 dB. The 3 dB signal bandwidth of this circuit may be increased to 900 Hz by reducing resistors R1 and R2 to 2.2 kΩ. The performance is similar to that using 4 kΩ resistors, except that the circuitry preceding the in amp must drive a lower impedance load.

The circuit of Figure 43 should be built using a PC board with a ground plane on both sides. All component leads should be as short as possible. Resistors R1 and R2 can be common 1% metal film units but capacitors C1 and C2 need to be ±5% tolerance devices to avoid degrading the circuit's common-mode rejection. Either the traditional 5% silver mica units or Panasonic ±2% PPS film capacitors are recommended.

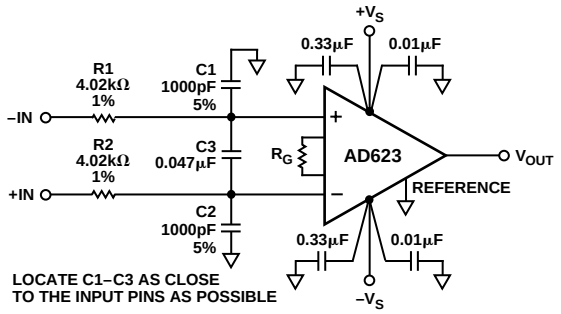


Figure 43. Circuit to Attenuate RF Interference

In many applications shielded cables are used to minimize noise; for best CMR over frequency the shield should be properly driven. Figure 44 shows an active guard drive that is configured to improve ac common-mode rejection by "bootstrapping" the capacitances of input cable shields, thus minimizing the capacitance mismatch between the inputs.

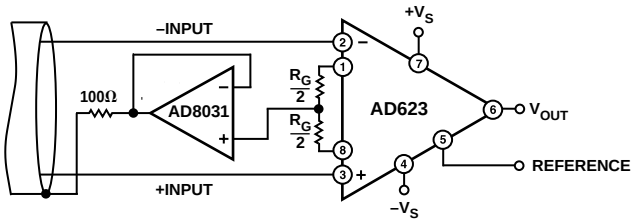


Figure 44. Common-Mode Shield Driver

GROUNDING

Since the AD623 output voltage is developed with respect to the potential on the reference terminal, many grounding problems can be solved by simply by tying the REF pin to the appropriate "local ground." The REF pin should, however, be tied to a low impedance point for optimal CMR.

The use of ground planes is recommended to minimize the impedance of ground returns (and hence the size of dc errors). In order to isolate low level analog signals from a noisy digital environment, many data-acquisition components have separate analog and digital ground returns (Figure 45). All ground pins from mixed signal components such as analog-to-digital converters should be returned through the "high quality" analog ground

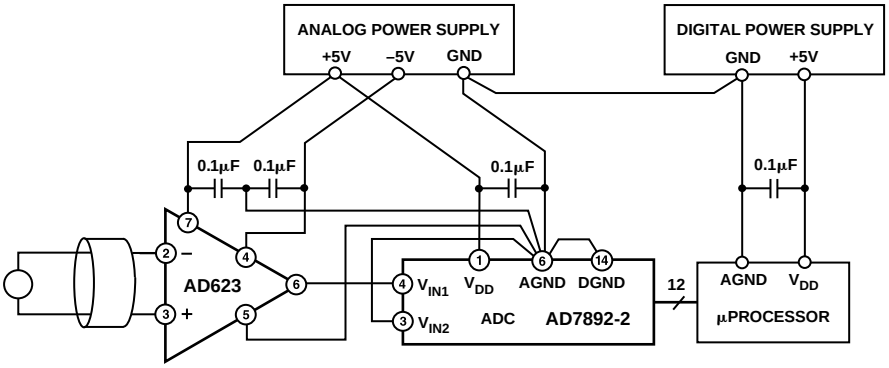


Figure 45. Optimal Grounding Practice for a Bipolar Supply Environment with Separate Analog and Digital Supplies

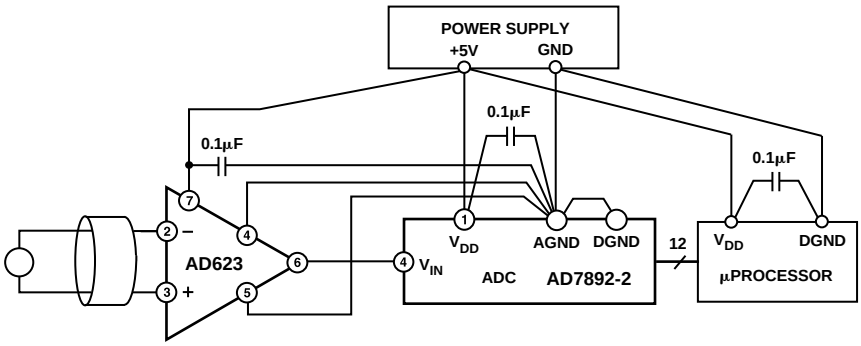


Figure 46. Optimal Ground Practice in a Single Supply Environment

plane. Maximum isolation between analog and digital is achieved by connecting the ground planes back at the supplies. The digital return currents from the ADC, which flow in the analog ground plane will, in general, have a negligible effect on noise performance.

If there is only a single power supply available, it must be shared by both digital and analog circuitry. Figure 46 shows how to minimize interference between the digital and analog circuitry. As in the previous case, separate analog and digital ground planes should be used (reasonably thick traces can be used as an alternative to a digital ground plane). These ground planes should be connected at the power supply's ground pin. Separate traces should be run from the power supply to the supply pins of the digital and analog circuits. Ideally, each device should have its own power supply trace, but these can be shared by a number of devices as long as a single trace is not used to route current to both digital and analog circuitry.

Ground Returns for Input Bias Currents

Input bias currents are those dc currents that must flow in order to bias the input transistors of an amplifier. These are usually transistor base currents. When amplifying "floating" input sources such as transformers or ac-coupled sources, there must be a direct dc path into each input in order that the bias current can flow. Figure 47 shows how a bias current path can be provided for the cases of transformer coupling, capacitive ac-coupling and for a thermocouple application. In dc-coupled resistive bridge applications, providing this path is generally not necessary as the bias current simply flows from the bridge supply through the bridge and into the amplifier. However, if the impedances that the two inputs see are large and differ by a large amount (>10 kΩ), the offset current of the input stage will cause dc errors proportional with the input offset voltage of the amplifier.

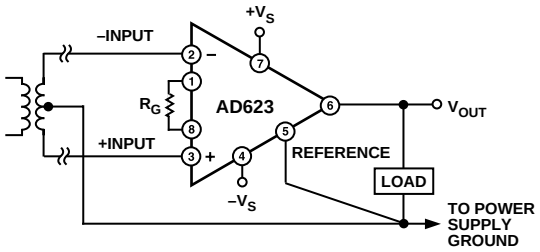


Figure 47a. Ground Returns for Bias Currents with Transformer Coupled Inputs

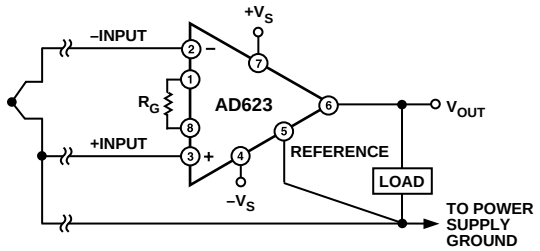


Figure 47b. Ground Returns for Bias Currents with Thermocouple Inputs

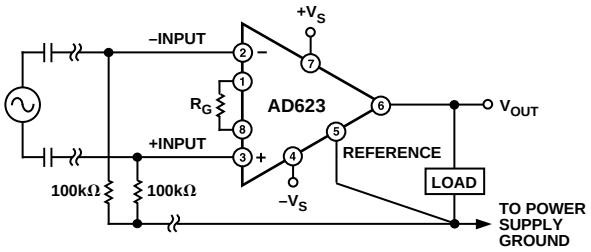


Figure 47c. Ground Returns for Bias Currents with AC Coupled Inputs

Output Buffering

The AD623 is designed to drive loads of 10 kΩ or greater. If the load is less that this value, the AD623's output should be buffered with a precision single supply op amp such as the OP113. This op amp can swing from 0 V to 4 V on its output while driving a load as small as 600 Ω. Table III summarizes the performance of some other buffer op amps.

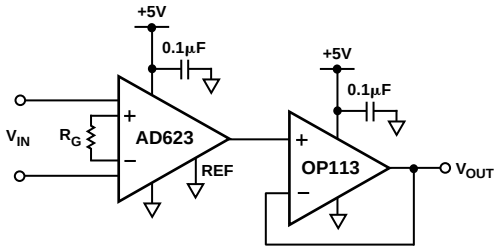


Figure 48. Output Buffering

Table III. Buffering Options

Op Amp	Comments
OP113	Single Supply, High Output Current
OP191	Rail-to-Rail Input and Output, Low Supply Current
OP150	Rail-to-Rail Input and Output, High Output Current

A Single Supply Data Acquisition System

Interfacing bipolar signals to single supply analog to digital converters (ADCs) presents a challenge. The bipolar signal must be "mapped" into the input range of the ADC. Figure 49 shows how this translation can be achieved.

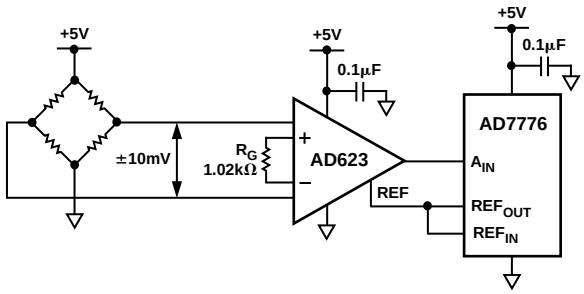


Figure 49. A Single Supply Data Acquisition System

The bridge circuit is excited by a +5 V supply. The full-scale output voltage from the bridge (±10 mV) therefore has a common-mode level of 2.5 V. The AD623 removes the common-mode component and amplifies the input signal by a factor of 100 (R_{GAIN} = 1.02 kΩ). This results in an output signal of ±1 V. In order to prevent this signal from running into the AD623's ground rail, the voltage on the REF pin has to be raised to at least 1 V. In this example, the 2 V reference voltage from the AD7776 ADC is used to bias the AD623's output voltage to 2 V ±1 V. This corresponds to the input range of the ADC.

Amplifying Signals with Low Common-Mode Voltage

Because the common-mode input range of the AD623 extends 0.1 V below ground, it is possible to measure small differential signals which have low, or no, common mode component. Figure 50 shows a thermocouple application where one side of the J-type thermocouple is grounded.

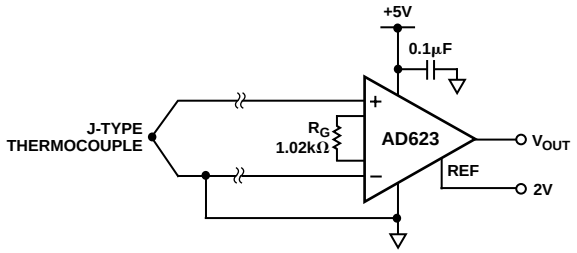


Figure 50. Amplifying Bipolar Signals with Low Common-Mode Voltage

Over a temperature range from –200°C to +200°C, the J-type thermocouple delivers a voltage ranging from –7.890 mV to 10.777 mV. A programmed gain on the AD623 of 100 (R_G = 1.02 kΩ) and a voltage on the AD623 REF pin of 2 V, results in the AD623's output voltage ranging from 1.110 V to 3.077 V relative to ground.

INPUT DIFFERENTIAL AND COMMON-MODE RANGE VS. SUPPLY AND GAIN

Figure 51 shows a simplified block diagram of the AD623. The voltages at the outputs of the amplifiers A1 and A2 are given by the equations

$$V_{A2} = V_{CM} + V_{DIFF}/2 + 0.6\ V + V_{DIFF} \times R_F/R_G$$
$$= V_{CM} + 0.6\ V + V_{DIFF} \times Gain/2$$

$$V_{A1} = V_{CM} - V_{DIFF}/2 + 0.6\ V - V_{DIFF} \times R_F/R_G$$
$$= V_{CM} + 0.6\ V - V_{DIFF} \times Gain/2$$

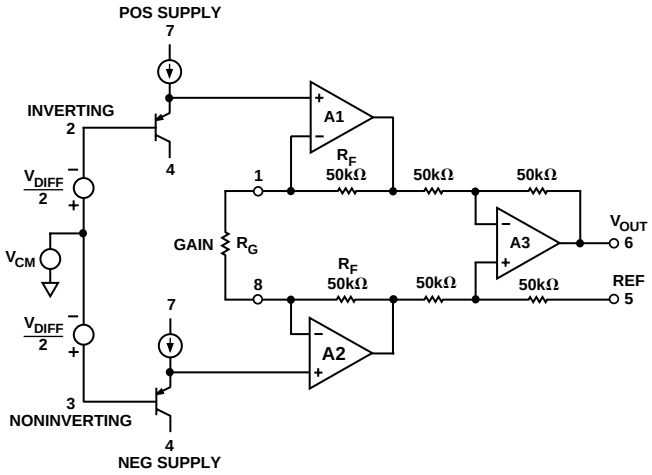


Figure 51. Simplified Block Diagram

The voltages on these internal nodes are critical in determining whether or not the output voltage will be clipped. The voltages V_{A1} and V_{A2} can swing from about 10 mV above the negative supply (V– or Ground) to within about 100 mV of the positive rail before clipping occurs. Based on this and from the above equations, the maximum and minimum input common-mode voltages are given by the equations

$$V_{CMMAX} = V+ - 0.7\ V - V_{DIFF} \times Gain/2$$

$$V_{CMMIN} = V- - 0.590\ V + V_{DIFF} \times Gain/2$$

These equations can be rearranged to give the maximum possible differential voltage (positive or negative) for a particular common-mode voltage, gain, and power supply. Because the signals on A1 and A2, can clip on either rail, the maximum differential voltage will be the lesser of the two equations.

$$|V_{DIFFMAX}| = 2\ (V+ - 0.7\ V - V_{CM})/Gain$$

$$|V_{DIFFMAX}| = 2\ (V_{CM} - V- + 0.590\ V)/Gain$$

However, the *range* on the differential input voltage range is also constrained by the output swing. So the range of V_{DIFF} may have to be lower according the equation.

$$Input\ Range \le Available\ Output\ Swing/Gain$$

For a bipolar input voltage with a common-mode voltage that is roughly half way between the rails, $V_{DIFFMAX}$ will be half the value that the above equations yield because the REF pin will be at midsupply. Note that the available output swing is given for different supply conditions in the Specifications section.

The equations can be rearranged to give the maximum gain for a fixed set of input conditions. Again, the maximum gain will be the lesser of the two equations.

$$Gain_{MAX} = 2\ (V+ - 0.7\ V - V_{CM})/V_{DIFF}$$
$$Gain_{MAX} = 2\ (V_{CM} - V- + 0.590\ V)/V_{DIFF}$$

Again, we must ensure that the resulting gain times the input range is less than the available output swing. If this is not the case, the maximum gain is given by,

$$Gain_{MAX} = Available\ Output\ Swing/Input\ Range$$

Also for bipolar inputs (i.e., input range = 2 V_{DIFF}), the maximum gain will be half the value yielded by the above equations because the REF pin must be at midsupply.

The maximum gain and resulting output swing for different input conditions is given in Table IV. Output voltages are referenced to the voltage on the REF pin.

For the purposes of computation, it is necessary to break down the input voltage into its differential and common-mode component. So when one of the inputs is grounded or at a fixed voltage, the common-mode voltage changes as the differential voltage changes. Take the case of the thermocouple amplifier in Figure 50. The inverting input on the AD623 is grounded. So when the input voltage is –10 mV, the voltage on the noninverting input is –10 mV. For the purposes of signal swing calculations, this input voltage should be considered to be composed of a common-mode voltage of –5 mV (i.e., (+IN + –IN)/2) and a differential input voltage of –10 mV (i.e., +IN – –IN).

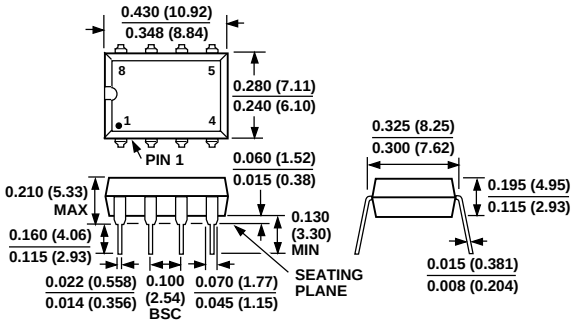
Table IV. Maximum Attainable Gain and Resulting Output Swing for Different Input Conditions

V_{CM}	V_{DIFF}	REF Pin	Supply Voltages	Max Gain	Closest 1% Gain Resistor, Ω	Resulting Gain	Output Swing
0 V	±10 mV	2.5 V	+5 V	118	866	116	±1.2 V
0 V	±100 mV	2.5 V	+5 V	11.8	9.31 k	11.7	±1.1 V
0 V	±10 mV	0 V	±5 V	490	205	488	±4.8 V
0 V	±100 mV	0 V	±5 V	49	2.1 k	48.61	±4.8 V
0 V	±1 V	0 V	±5 V	4.9	26.1 k	4.83	±4.8 V
2.5 V	±10 mV	2.5 V	+5 V	242	422	238	±2.3 V
2.5 V	±100 mV	2.5 V	+5 V	24.2	4.32 k	24.1	±2.4 V
2.5 V	±1 V	2.5 V	+5 V	2.42	71.5 k	2.4	±2.4 V
1.5 V	±10 mV	1.5 V	+3 V	142	715	141	±1.4 V
1.5 V	±100 mV	1.5 V	+3 V	14.2	7.68 k	14	±1.4 V
0 V	±10 mV	1.5 V	+3 V	118	866	116	±1.1 V
0 V	±100 mV	1.5 V	+3 V	11.8	9.31 k	11.74	±1.1 V

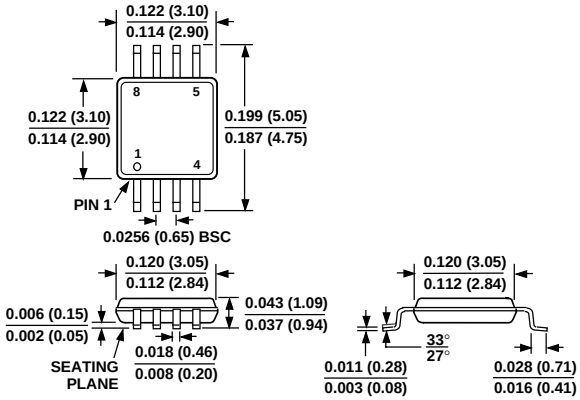
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

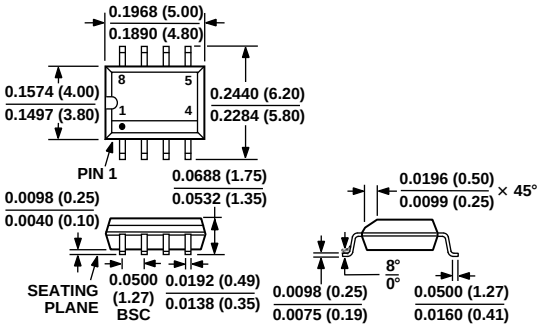
8-Lead Plastic DIP (N-8)



8-Lead μSOIC (RM-8)



8-Lead SOIC (SO-8)



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