Low Cost RGB to NTSC/PAL Encoder with Luma Trap Port

AD725

FEATURES

Composite Video Output: Both NTSC and PAL
Chrominance and Luminance (S-Video) Outputs
Luma Trap Port to Eliminate Cross Color Artifacts
TTL Logic Levels
Integrated Delay Line and Auto-Tuned Filters
Drives 75 Ω Reverse-Terminated Loads
Low Power +5 V Operation
Power-Down to <1 μA
Very Low Cost

APPLICATIONS

RGB/VGA to NTSC/PAL Encoding
Personal Computers/Network Computers
Video Games
Video Conference Cameras
Digital Still Cameras

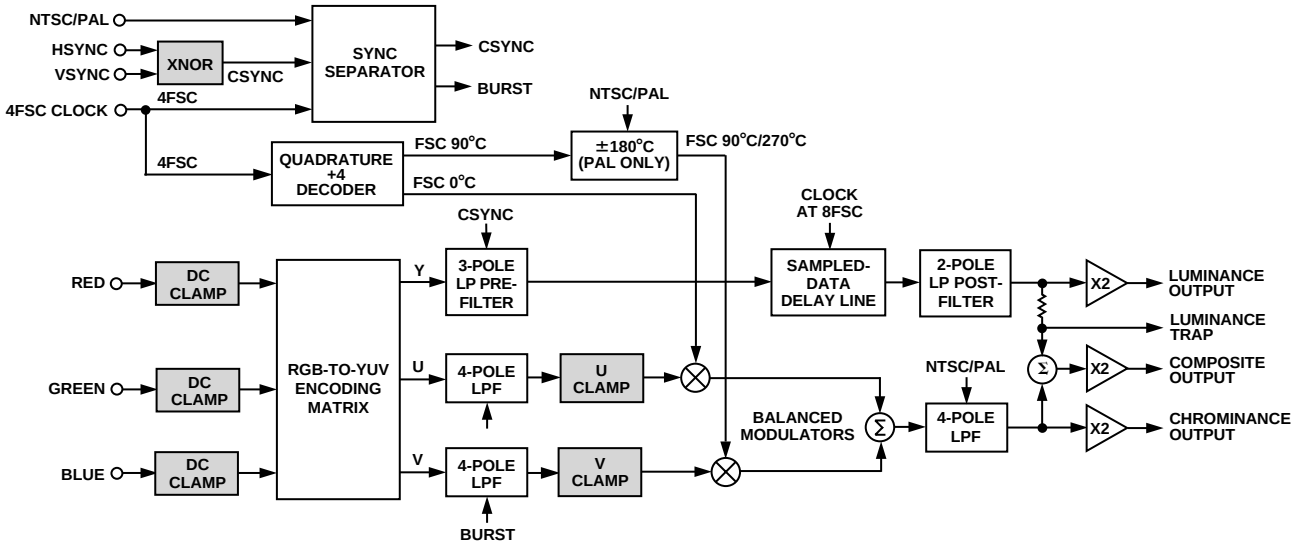
PRODUCT DESCRIPTION

The AD725 is a very low cost general purpose RGB to NTSC/PAL encoder that converts red, green and blue color component signals into their corresponding luminance (baseband amplitude) and chrominance (subcarrier amplitude and phase) signals in accordance with either NTSC or PAL standards. These two outputs are also combined on-chip to provide a composite video output. All three outputs are available separately at voltages of twice the standard signal levels as required for driving 75 Ω, reverse-terminated cables.

The AD725 features a luminance trap (YTRAP) pin that provides a means of reducing cross color generated by subcarrier frequency components found in the luminance signal. For portable or other power-sensitive applications, the device can be powered down to less than 1 μA of current consumption. All logic levels are TTL compatible thus supporting the logic requirements of 3 V CMOS systems.

The AD725 is packaged in a low cost 16-lead SOIC and operates from a +5 V supply.

FUNCTIONAL BLOCK DIAGRAM



REV. 0

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AD725—SPECIFICATIONS (Unless otherwise noted, V_S = +5, T_A = +25°C, using 4FSC synchronous clock. All loads are 150 Ω ± 5% at the IC pins. Outputs are measured at the 75 Ω reverse terminated load.)

Parameter	Conditions	Min	Typ	Max	Units
SIGNAL INPUTS (RIN, GIN, BIN)					
Input Amplitude	Full Scale			714	mV p-p
Black Level[1]			0.8		V
Input Resistance[2]	RIN, GIN, BIN	1			MΩ
Input Capacitance			5		pF
LOGIC INPUTS (HSYNC, VSYNC, 4FSC, CE, STND)	TTL Logic Levels				
Logic Low Input Voltage				1	V
Logic High Input Voltage		2			V
Logic Low Input Current (DC)				1	µA
Logic High Input Current (DC)				1	µA
VIDEO OUTPUTS[3]					
Luminance (LUMA)					
Bandwidth, –3 dB	NTSC		4.4		MHz
	PAL		5.2		MHz
Gain Error		–7	–2	+7	%
Nonlinearity	max p-p		0.3		%
Sync Level	NTSC	252	279	310	mV
	PAL	264	291	325	mV
DC Black Level			1.3		V
Luminance Trap (YTRAP)					
Output Resistance			1.0		kΩ
DC Black Level			1.0		V
Chrominance (CRMA)					
Bandwidth, –3 dB	NTSC		1.2		MHz
	PAL		1.5		MHz
Color Burst Amplitude	NTSC	206	255	305	mV p-p
	PAL	221	291	362	mV p-p
Color Burst Width	NTSC		2.51		µs
	PAL		2.28		µs
Chroma Level Error[4]			–4		%
Chroma Phase Error[5]			±3		Degrees
DC Black Level			2.0		V
Chroma Feedthrough	R, G, B = 0		15	40	mV p-p
Composite (COMP)					
Absolute Gain Error	With Respect to Luma	–5	–1	+3	%
Differential Gain	With Respect to Chroma		0.5		%
Differential Phase	With Respect to Chroma		1.5		Degrees
DC Black Level			1.4		V
Chroma/Luma Time Alignment	S-Video		20		ns
POWER SUPPLIES					
Recommended Supply Range	Single Supply	+4.75		+5.25	V
Quiescent Current—Encode Mode			30	36	mA
Quiescent Current—Power Down			<1		µA

NOTES
[1]R, G, and B signals are inputted via an external ac coupling capacitor.
[2]Except during dc restore period (back porch clamp).
[3]All outputs measured at a 75 Ω reverse-terminated load; ac voltages at the IC output pins are twice those specified here.
[4]Difference between ideal and actual color bar subcarrier amplitudes.
[5]Difference between ideal and actual color bar subcarrier phases.

Specifications are subject to change without notice.

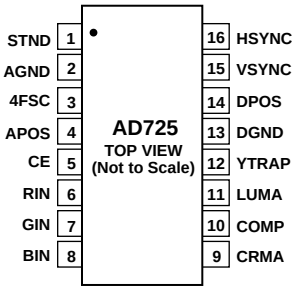
ABSOLUTE MAXIMUM RATINGS*

Supply Voltage, APOS to AGND . . . . . +6 V
Supply Voltage, DPOS to DGND . . . . . +6 V
AGND to DGND . . . . . –0.3 V to +0.3 V
Inputs . . . . . DGND – 0.3 to DPOS + 0.3 V
Internal Power Dissipation . . . . . 800 mW
Operating Temperature Range . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +125°C
Lead Temperature Range (Soldering 30 sec) . . . . . +230°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics: 16-Pin SOIC Package: θ_{JA} = 100°C/W.

PIN CONFIGURATION
16-Lead Wide Body (SOIC)
(R-16)



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD725AR	–40°C to +85°C	16-Lead SOIC	R-16
AD725AR-Reel	–40°C to +85°C	16-Lead SOIC	R-16
AD725AR-Reel7	–40°C to +85°C	16-Lead SOIC	R-16
AD725-EB		Evaluation Board	

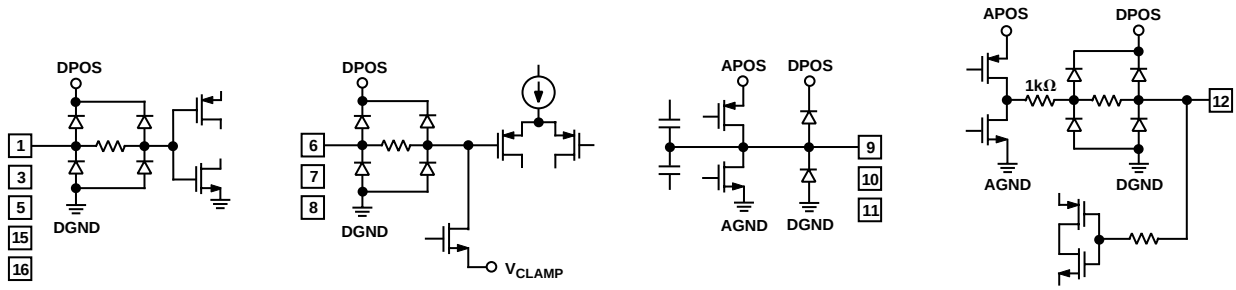
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD725 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN DESCRIPTIONS

Pin	Mnemonic	Description	Equivalent Circuit
1	STND	Encoding Standard Pin. A Logic HIGH input selects NTSC encoding. A Logic LOW input selects PAL encoding. TTL Logic Levels.	Circuit A
2	AGND	Analog Ground Connection.	
3	4FSC	4FSC Clock Input. For NTSC: 14.318 180 MHz. For PAL: 17.734 475 MHz. TTL Logic Levels.	Circuit A
4	APOS	Analog Positive Supply (+5 V ± 5%).	
5	CE	Chip Enable. A Logic HIGH input enables the encode function. A Logic LOW input powers down chip when not in use. TTL Logic Levels.	Circuit A
6	RIN	Red Component Video Input. 0 mV to 714 mV AC-Coupled.	Circuit B
7	GIN	Green Component Video Input. 0 mV to 714 mV AC-Coupled.	Circuit B
8	BIN	Blue Component Video Input. 0 mV to 714 mV AC-Coupled.	Circuit B
9	CRMA	Chrominance Output.* Approximately 1.8 V peak-to-peak for both NTSC and PAL.	Circuit C
10	COMP	Composite Video Output.* Approximately 2.5 V peak-to-peak for both NTSC and PAL.	Circuit C
11	LUMA	Luminance plus CSYNC Output.* Approximately 2 V peak-to-peak for both NTSC and PAL.	Circuit C
12	YTRAP	Luminance Trap Filter Tap. Attach L-C resonant network to reduce cross-color artifacts.	Circuit D
13	DGND	Digital Ground Connection.	
14	DPOS	Digital Positive Supply (+5 V ± 5%).	
15	VSYNC	Vertical Sync Signal (if using external CSYNC set at > +2 V). TTL Logic Levels.	Circuit A
16	HSYNC	Horizontal Sync Signal (or CSYNC signal). TTL Logic Levels.	Circuit A

*The Luminance, Chrominance and Composite Outputs are at twice normal levels for driving 75 Ω reverse-terminated lines.



Circuit A *Circuit B* *Circuit C* *Circuit D*

Figure 1. Equivalent Circuits

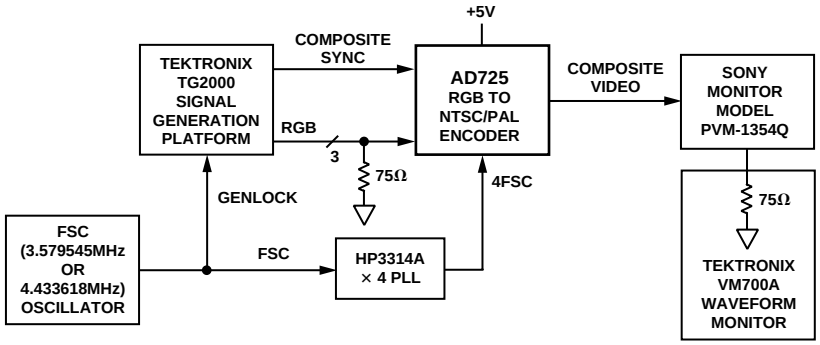


Figure 2. Evaluation Setup

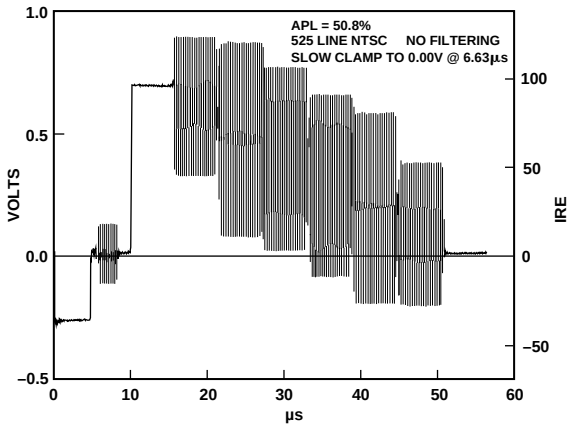


Figure 3. 100% Color Bars, NTSC

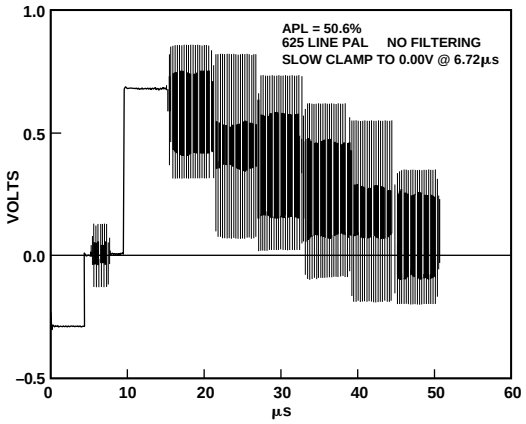


Figure 5. 100% Color Bars, PAL

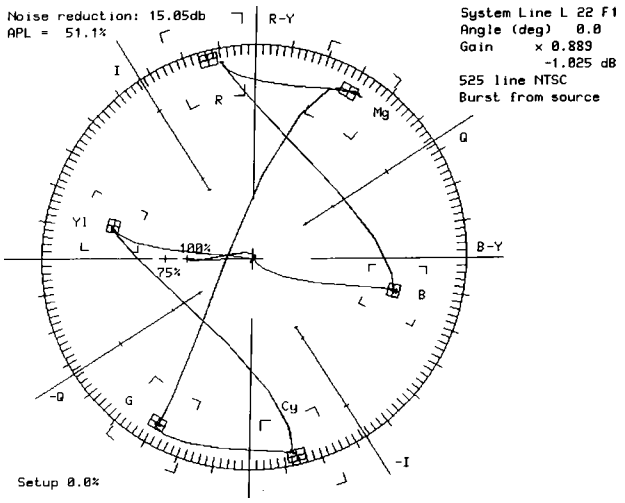


Figure 4. 100% Color Bars on Vector Scope, NTSC

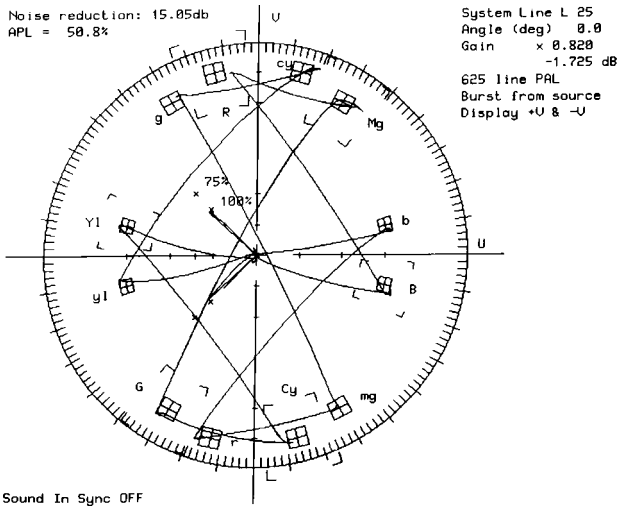


Figure 6. 100% Color Bars on Vector Scope, PAL

AD725–Typical Characteristics

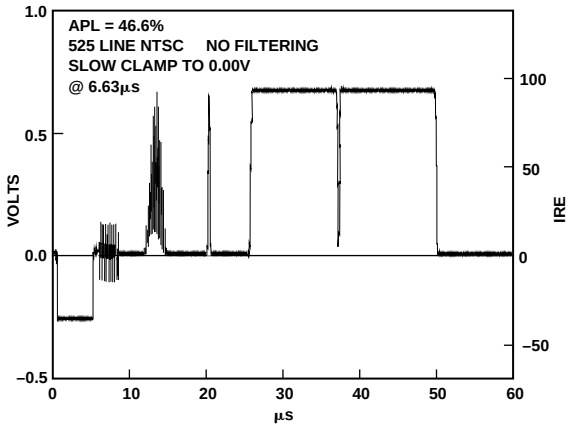


Figure 7. Modulated Pulse and Bar, NTSC

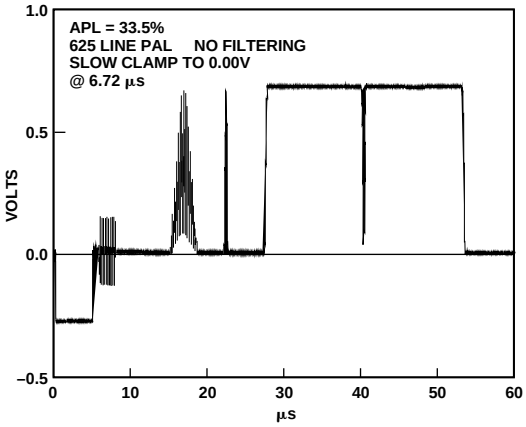


Figure 9. Modulated Pulse and Bar, PAL

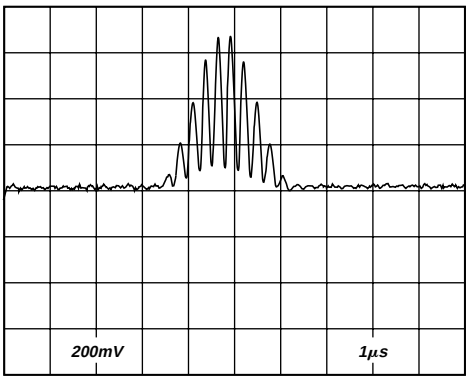


Figure 8. Zoom on Modulated Pulse, NTSC

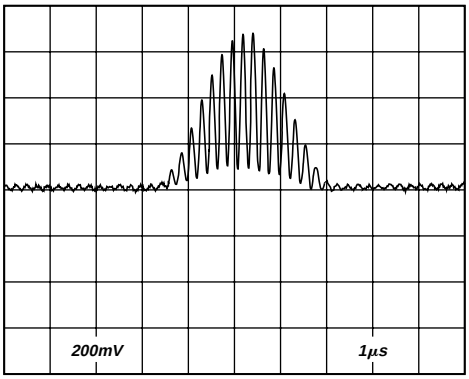


Figure 10. Zoom on Modulated Pulse, PAL

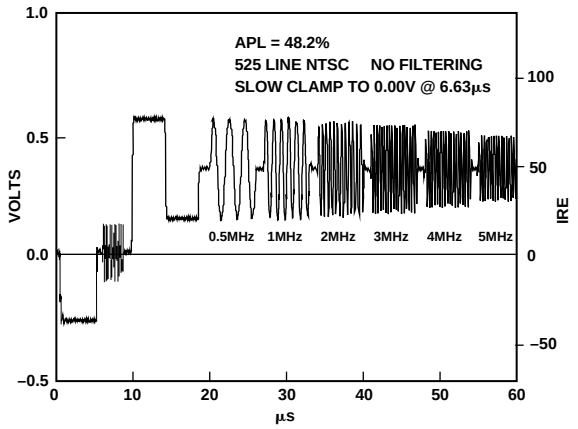


Figure 11. Multiburst, NTSC

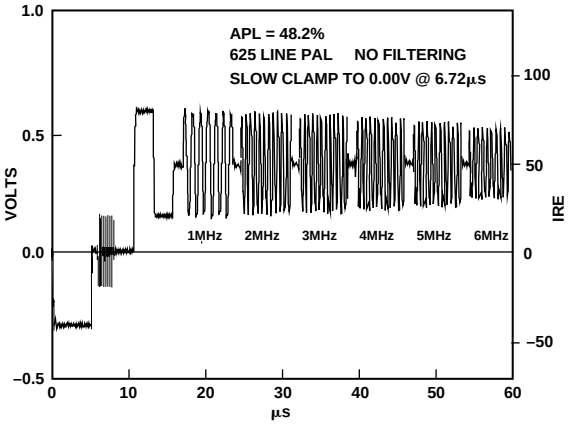


Figure 14. Multiburst, PAL

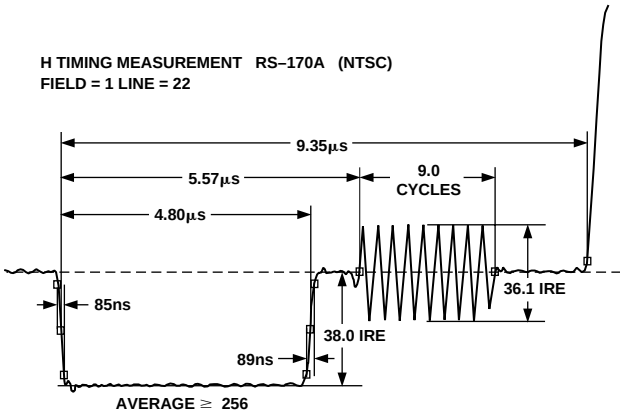


Figure 12. Horizontal Timing, NTSC

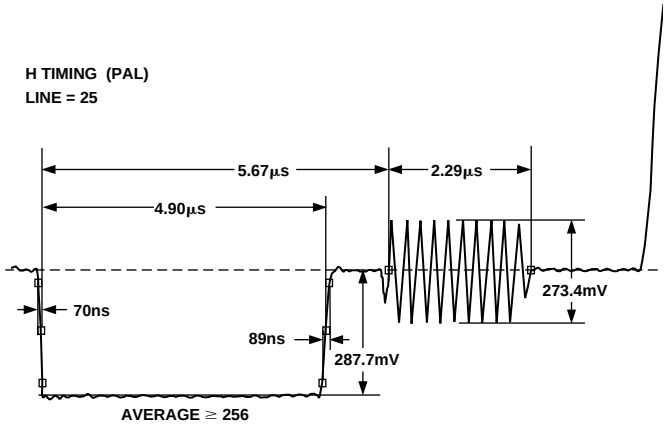


Figure 15. Horizontal Timing, PAL

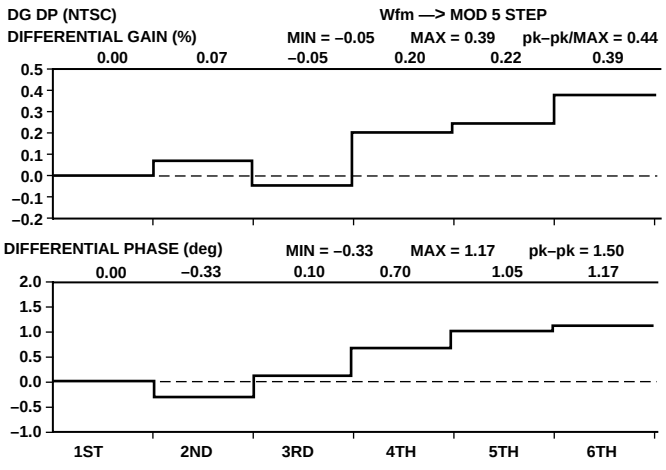


Figure 13. Composite Output Differential Phase and Gain, NTSC

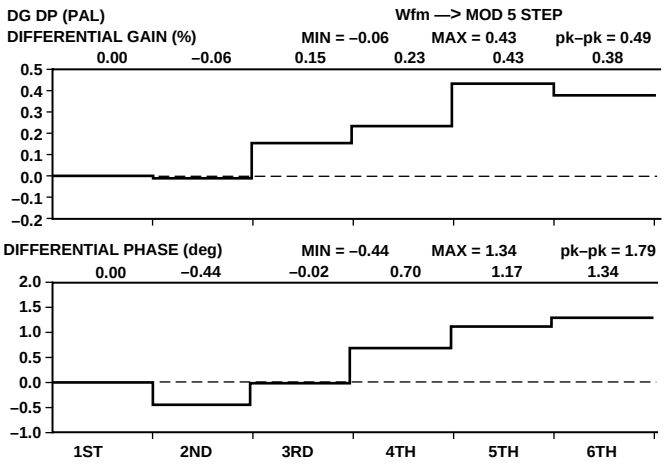


Figure 16. Composite Output Differential Phase and Gain, PAL

THEORY OF OPERATION

The AD725 is a predominantly analog design, with digital logic control of timing. This timing logic is driven by a external frequency reference at four times the color subcarrier frequency, input into the 4FSC pin of the AD725. This frequency should be 14.318 180 MHz for NTSC encoding, and 17.734 475 MHz for PAL encoding. The 4FSC input accepts standard TTL logic levels. The duty cycle of this input clock is not critical, but a fast-edged clock should be used to prevent excessive jitter in the timing.

The AD725 accepts two common sync standards, composite sync or separate horizontal and vertical syncs. To use an external composite sync, a logic high signal is input to the VSYNC pin and the composite sync is input to the HSYNC pin. If separate horizontal and vertical syncs are available, the horizontal sync can be input to the HSYNC pin and vertical sync to the VSYNC pin. Internally, the device XNORs the two sync inputs to combine them into one negative-going composite sync.

The AD725 detects the falling sync pulse edges, and times their width. A sync pulse of standard horizontal width will cause the insertion of a colorburst vector into the chroma modulators at the proper time. A sync pulse outside the detection range will cause suppression of the color burst, and the device will enter its vertical blanking mode. During this mode, the on-chip RC time constants are verified using the input frequency reference, and the filter cutoff frequencies are retuned as needed.

The component color inputs, RIN, GIN and BIN, receive analog signals specifying the desired active video output. The full-scale range of the inputs is 0.714 mV (for either NTSC or PAL operation). External black level is not important as these inputs are terminated externally, and then ac coupled to the AD725.

The AD725 contains on-chip RGB input clamps to restore the dc level on-chip to match its single supply signal path. This dc restore timing is coincident with the burst flag, starting approximately 5.5 µs after the falling sync edge and lasting for 2.5 µs. During this time, the device should be driven with a black input.

Following the dc clamps, the RGB inputs are buffered and split into two signal paths for constructing the luminance and chrominance outputs.

Luminance Signal Path

The luminance path begins with the luma (Y) matrix. This matrix combines the RGB inputs to form the brightness information in the output video. The inputs are combined by the standard transformation

$$Y = 0.299 \times R + 0.587 \times G + 0.114 \times B$$

This equation describes the sensitivity of the human eye to the individual component colors, combining them into one value of brightness. The equation is balanced so that full-scale RGB inputs give a full-scale Y output.

Following the luma matrix, the composite sync is added. The user-supplied sync (from the HSYNC and VSYNC inputs) is latched into the AD725 at half the master clock rate, gating a sync pulse into the luminance signal. With the exception of transitioning on the clock edges, the output sync timing will be in the same format as the input sync timing. The output sync level will depend on the encoding standard, 286 mV (40 IRE) for NTSC and 300 mV for PAL (voltages at the pin will be twice these levels).

In order to be time-aligned with the filtered chrominance signal path, the luma signal must be delayed before it is output. The AD725 uses a sampled delay line to achieve this delay.

Following the luma matrix and prior to this delay line, a prefilter removes higher frequencies from the luma signal to prevent aliasing by the sampled delay line. This three-pole Bessel low-pass filter has a –3 dB frequency of 4.85 MHz for NTSC, 6 MHz for PAL.

After the luma prefilter, the bandlimited luma signal is sampled onto a set of capacitors at twice the master reference clock rate. After an appropriate delay, the data is read off the delay line, reconstructing the luma signal. The 8FSC oversampling of this delay line limits the amount of jitter in the reconstructed sync output. The clocks driving the delay line are reset once per video line during the burst flag. The output of the luma path will remain unchanged during this period and will not respond to changing RGB inputs.

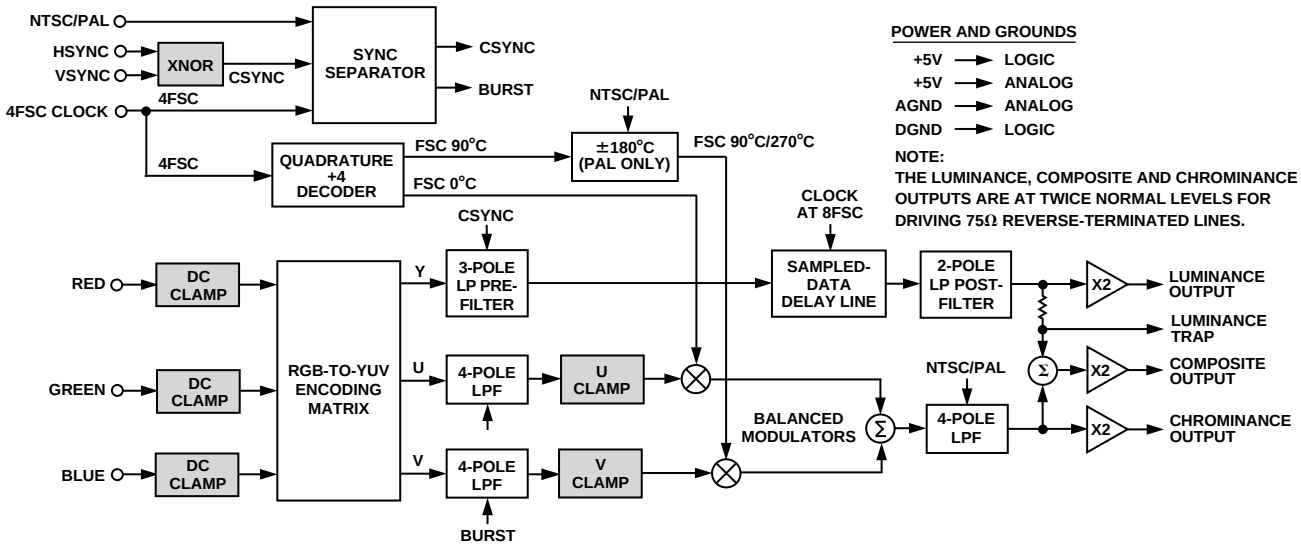


Figure 17. Functional Block Diagram

The reconstructed luma signal is then smoothed with a two pole Bessel low-pass filter. This filter has a –3 dB bandwidth of 5.25 MHz for NTSC, 6.5 MHz for PAL. A final buffer provides current drive for the LUMA output pin.

Chrominance Signal Path

The chrominance path begins with the U and V color-difference matrices. The AD725 uses U and V modulation vectors for NTSC and PAL (+U being defined as 0 degrees phase), simplifying the design compared to I and Q designs. The U and V matrices combine the RGB inputs by the standard transformations:

$$U = 0.493 \times (B - Y)$$
$$V = 0.877 \times (R - Y)$$

The Y signal in these transformations is provided by the luminance matrix.

Before modulation, the U and V signals are prefiltered to prevent aliasing. These four-pole modified Bessel low-pass filters have a –3 dB bandwidth of 1.2 MHz for NTSC and 1.5 MHz for PAL.

Between the prefilters and the modulators, the colorburst vectors are added to the U and V signals. The colorburst levels are defined according to the encoding standard. For NTSC, the colorburst is in the –U direction (with no V component) with a resultant amplitude of 286 mV (40 IRE) at 180 degrees phase. For PAL, the colorburst has equal parts of –U and ±V vectors (changing V phase every line) for a resultant amplitude of 300 mV alternating between 135 and 225 degrees phase (voltages at the pin will be twice these levels).

The burst gate timing is generated by waiting for a certain number of reference clock cycles following the falling sync edge. If the sync pulse width is measured to be outside the standard horizontal width, it is assumed that the device is in an h/2 period (vertical blanking interval) and the burst is suppressed.

The U and V signals are used to modulate a pair of quadrature clocks (sine and cosine) at one-fourth the reference frequency input (3.579 545 MHz for NTSC, 4.433618 MHz for PAL). For PAL operation, the phase of the cosine (V) clock is changed after each falling sync edge is detected. This will change the V-vector phase in PAL mode every horizontal line. By driving the AD725 with an odd number of sync edges per field, any individual line will flip phase each field as required by the standard.

In order to suppress the carriers in the chrominance signal, the U and V modulators are balanced. Once per horizontal line the offsets in the modulators are cancelled in order to minimize residual subcarrier when the RGB inputs are equal. This offset cancellation also provides a dc restore for the U and V signal paths, so it is important that the RGB inputs be held at black level during this time. The offset cancellation occurs after each falling sync edge, approximately 350 ns after the falling sync edge, lasting for a period of 140 ns. If the inputs are unbalanced during this time (for example, if a sync-on-green RGB input were used), there will be an offset in this chrominance response of the inputs during the remainder of the horizontal line, including the colorburst.

The U signal is sampled by the sine clock and the V signal is sampled by the cosine clock in the modulators, after which they are summed to form the chrominance (C) signal.

The chrominance signal then passes through a final four-pole modified Bessel low-pass filter to remove the harmonics of the switching modulation. This filter has a –3 dB frequency of 4.4 MHz for NTSC and 5.9 MHz for PAL. A final buffer provides current drive for the CRMA output pin.

Composite Output

To provide a composite video output, the separate (S-Video) luminance and chrominance signal paths are summed. Prior to summing, however, a filter tap for removing cross-color artifacts in the receiver is provided.

The luminance path contains a resistor, output pin (YTRAP), and buffer prior to entering the composite summer. By connecting an inductor and capacitor on this pin, an R-L-C series-resonant circuit can be tuned to null out the luminance frequency response at the chrominance subcarrier frequency (3.579 545 MHz for NTSC, 4.433 618 MHz for PAL). The center frequency (f_C) of this filter will be determined by the external inductor and capacitor by the equation:

$$f_C = \frac{1}{2\pi\sqrt{LC}}$$

It can be seen from this equation that the center frequency of the trap is entirely dependent on external components.

The ratio of center frequency to bandwidth of the notch (Q = f_C/BW) can be described by the equation:

$$Q = \frac{1}{1000}\sqrt{\frac{L}{C}}$$

When choosing the Q of the filter, it should be kept in mind that the sharper the notch, the more critical the tolerance of the components must be in order to target the subcarrier frequency. Additionally, higher Q notches will exhibit a transient response with more ringing after a luminance step. The magnitude of this ringing can be large enough to cause visible shadowing for Q values much greater than 1.5.

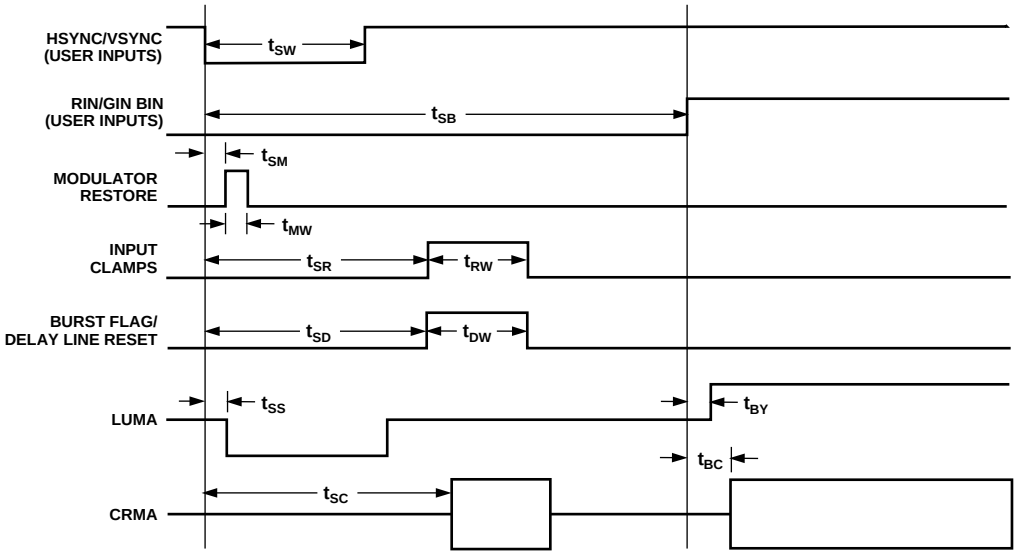


Figure 18. Timing Diagram (Not to Scale)

Table I. Timing Description (See Figure 18)

Symbol	Name	Description	NTSC[1]		PAL[2]	
t_{SW}	Sync Width	Input valid sync width for burst insertion (user-controlled).	Min Max	2.8 µs 5.3 µs	Min Max	3.3 µs 5.4 µs
t_{SB}	Sync to Blanking End	Minimum sync to color delay (user-controlled).	Min	8.2 µs	Min	8.1 µs
t_{SM}	Sync to Modulator Restore	Delay to modulator clamp start.		392 ns		298 ns
t_{MW}	Modulator Restore Width	Length of modulator offset clamp (no chroma during this period).		140 ns		113 ns
t_{SR}	Sync to RGB DC Restore	Delay to input clamping start.		5.4 µs		5.6 µs
t_{RW}	DC Restore Width	Length of input clamp (no RGB response during this period).		2.5 µs		2.3 µs
t_{SD}	Sync to Delay Line Reset	Delay to start of delay line clock reset.		5.7 µs		5.8 µs
t_{DW}	Delay Line Reset Width	Length of delay line clock reset (no luma response during this period), also burst gate.		2.5 µs		2.3 µs
t_{SS}	Sync Input to Luma Sync Output	Delay from sync input assertion to sync in LUMA output.	typ	310 ns	typ	265 ns
t_{BY}	Blanking End to LUMA Start	Delay from RGB input assertion to LUMA output response.	typ	340 ns	typ	280 ns
t_{SC}	Sync to Colorburst	Delay from valid horizontal sync start to CRMA colorburst output.	typ	5.8 µs	typ	5.9 µs
t_{BC}	Blanking End to CRMA Start	Delay from RGB input assertion to CRMA output response.	typ	360 ns	typ	300 ns

NOTES
[1]Input clock = 14.318180 MHz, STND pin = logic high.
[2]Input cock = 17.734475 MHz, STND pin = logic low.

APPLYING THE AD725

Inputs

RIN, BIN, GIN are analog inputs that should be terminated to ground with 75 Ω in close proximity to the IC. When properly terminated the peak-to-peak voltage for a maximum input level should be 714 mV p-p. The horizontal blanking interval should be the most negative part of each signal.

The inputs should be held at the input signal's black level during the horizontal blanking interval. The internal dc clamps will clamp this level during color burst to a reference that is used internally as the black level. Any noise present on the RIN, GIN, BIN or AGND pins during this interval will be sampled onto the input capacitors. This can result in varying dc levels from line to line in all outputs, or if imbalanced, subcarrier feedthrough in the COMP and CRMA outputs.

For increased noise rejection, larger input capacitors are desired. A capacitor of 0.1 μF is usually adequate.

Similarly, the U and V clamps balance the modulators during an interval shortly after the falling CSYNC input. Noise present during this interval will be sampled in the modulators, resulting in residual subcarrier in the COMP and CRMA outputs.

HSYNC and VSYNC are two logic level inputs that are combined internally to produce a composite sync signal. If a composite sync signal is to be used, it can be input to HSYNC while VSYNC is pulled to logic HI (> +2 V).

The form of the input sync signal(s) will determine the form of the composite sync on the composite video (COMP) and luminance (LUMA) outputs. If no equalization or serration pulses are included in the HSYNC input there won't be any in the outputs. Although sync signals without equalization and serration pulses do not technically meet the video standards' specifications, many monitors do not require these pulses in order to display good pictures. The decision whether to include these signals is a system trade-off between cost and complexity and adhering strictly to the video standards.

The HSYNC and VSYNC logic inputs have a small amount of built-in hysteresis to avoid interpreting noisy input edges as multiple sync edges. This is critical to proper device operation, as the sync pulses are timed for vertical blanking interval detection.

The logic inputs have been designed for VIL < 1.0 V and VIH > 2.0 V for the entire temperature and supply range of operation. This allows the AD725 to directly interface to TTL or 3 V CMOS compatible outputs, as well as 5 V CMOS outputs where VOL is less than 1.0 V.

The NTSC specification calls for a frequency accuracy of ±10 Hz from the nominal subcarrier frequency of 3.579545 MHz. While maintaining this accuracy in a broadcast studio might not be a severe hardship, it can be quite expensive in a low cost consumer application.

The AD725 will operate with subcarrier frequencies that deviate quite far from those specified by the TV standards. However, the monitor will in general not be quite so forgiving. Most monitors can tolerate a subcarrier frequency that deviates several hundred Hz from the nominal standard without any degradation in picture quality. These conditions imply that the subcarrier frequency accuracy is a system specification and not a specification of the AD725 itself.

The STND pin is used to select between NTSC and PAL operation. Various blocks inside the AD725 use this input to program their operation. Most of the more common variants of NTSC and PAL are supported. There are, however, two known specific standards which are not supported by the standard AD725. These are NTSC 4.43 and M-PAL.

Basically these two standards use most of the features of the standard that their names imply, but use the subcarrier that is equal to or approximately equal to the frequency of the other standard. Because of the automatic programming of the filters in the chrominance path and other timing considerations, a factory-programmed special version of the AD725 is necessary to support these standards.

Layout Considerations

The AD725 is an all CMOS mixed signal part. It has separate pins for the analog and digital +5 V and ground power supplies. Both the analog and digital ground pins should be tied to the ground plane by a short, low inductance path. Each power supply pin should be bypassed to ground by a low inductance 0.1 μF capacitor and a larger tantalum capacitor of about 10 μF.

The three analog inputs (RIN, GIN, BIN) should be terminated with 75 Ω to ground close to the respective pins. However, as these are high impedance inputs, they can be in a loop-through configuration. This technique is used to drive two or more devices with high frequency signals that are separated by some distance. A connection is made to the AD725 with no local termination, and the signals are run to another distant device where the termination for these signals is provided.

The output amplitudes of the AD725 are double that required by the devices that it drives. This compensates for the halving of the signal levels by the required terminations. A 75 Ω series resistor is required close to each AD725 output, while 75 Ω to ground should terminate the far end of each line.

The outputs have a dc bias and must be ac coupled for proper operation. The COMP and LUMA outputs have information down to 30 Hz for NTSC (25 MHz for PAL) that must be transmitted. Each output requires a 220 μF series capacitor to work with the 75 Ω resistance to pass these low frequencies. The CRMA signal has information mostly up at the chroma frequency and can use a smaller capacitor if desired, but 220 μF can be used to minimize the number of different components used in the design.

Displaying VGA Output on a TV

The AD725 can be used to convert the analog RGB output from a personal computer's VGA card to the NTSC or PAL television standards. To accomplish this it is important to understand that the AD725 requires interlaced RGB video and clock rates that are consistent with those required by the television standards. In most computers the default output is a noninterlaced RGB signal at a frame rate higher than used by either NTSC or PAL.

Most VGA controllers support a wide variety of output modes that are controlled by altering the contents of internal registers. It is best to consult with the VGA controller manufacturer to determine the exact configuration required to provide an interlaced output at 60 Hz (50 Hz for PAL).

Figure 19 shows a circuit for connection to the VGA port of a PC. The RGB outputs are ac coupled to the respective inputs of the AD725. These signals should each be terminated to ground with 75 Ω.

The standard 15-pin VGA connector has HSYNC on Pin 13 and VSYNC on Pin 14. These signals also connect directly to the same name signals on the AD725. For a synchronous NTSC system, the internal 4FSC (14.318 180 MHz) clock that drives the VGA controller can be used for 4FSC on the AD725. This signal is not directly accessible from outside the computer, but it does appear on the VGA card. (A 1FSC-input encoder, the AD724, is also available.)

If a separate RGB monitor is also to be used, it is not possible to simply connect it to the R, G and B signals. The monitor provides a termination that would double terminate these signals. The R, G, and B signals should be buffered by three amplifiers with high input impedances. These should be configured for a gain of two, which is normalized by the divide by two termination scheme used for the RGB monitor.

The AD8073 is a low cost triple video amplifier that can provide the buffering required in this application. However, since the R, G and B signals go all the way to ground during horizontal sync, the AD8073 will require a –5 V supply to handle these signals. To be able to buffer the R, G and B signals using a single supply, a rail-to-rail amplifier is required. In this application, the AD8051 (single) and AD8052 (dual) can be used to provide the three required channels. These can be operated on a single supply of 3 V to 5 V.

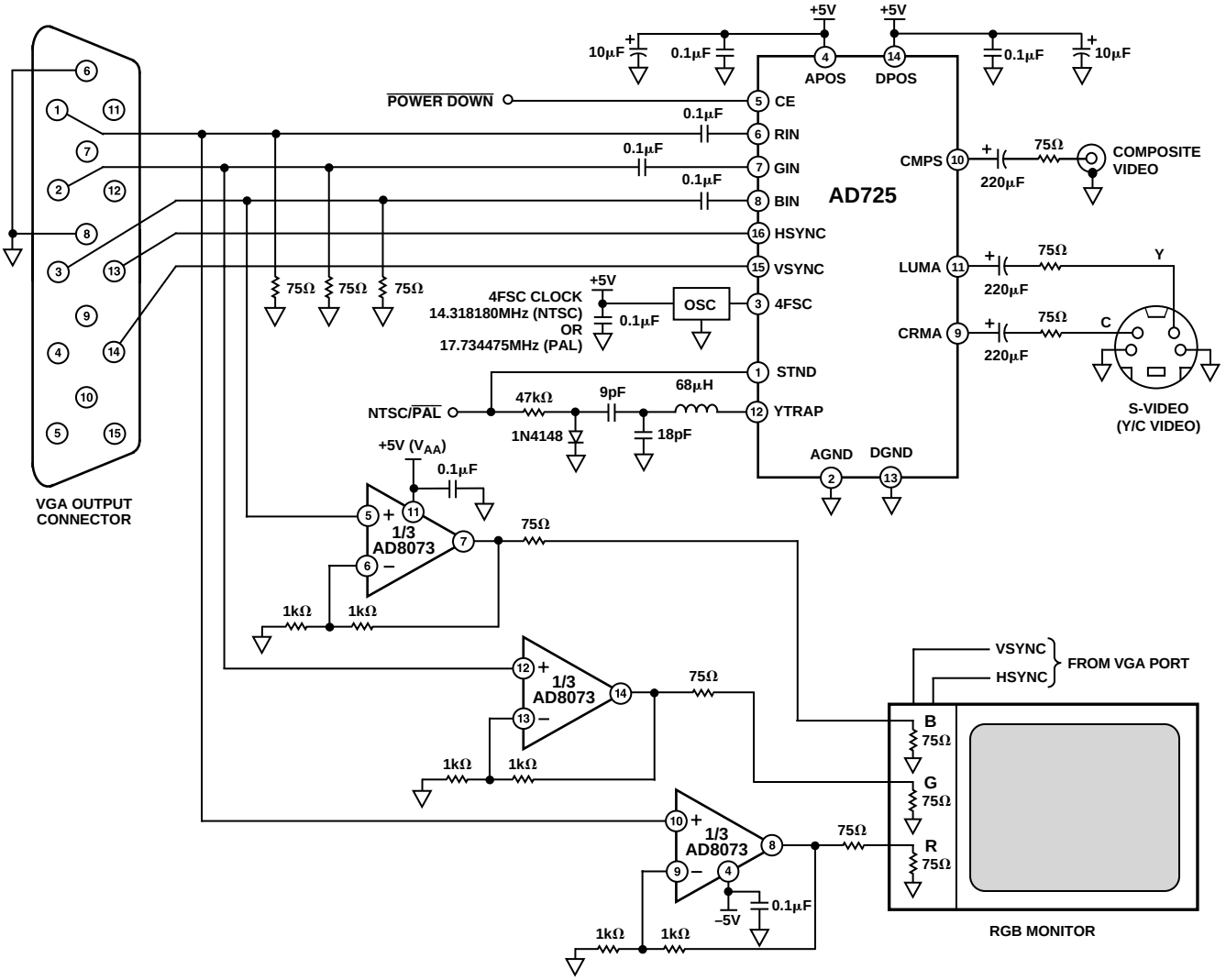


Figure 19. Interfacing the AD725 to the (Interlaced) VGA Port of a PC

Low Cost Crystal Oscillator

A low cost oscillator can be made that provides a CW clock that can be used to drive both the AD725 4FSC and other devices in the system that require a clock at this frequency. Figure 20 shows a circuit that uses one inverter of a 74HC04 package to create a crystal oscillator and another inverter to buffer the oscillator and drive other loads. The logic family must be a CMOS type that can support the frequency of operation, and it must NOT be a Schmitt trigger type of inverter. Resistor R1 from input to output of U1A linearizes the inverter's gain such that it provides useful gain and a 180 degree phase shift to drive the oscillator.

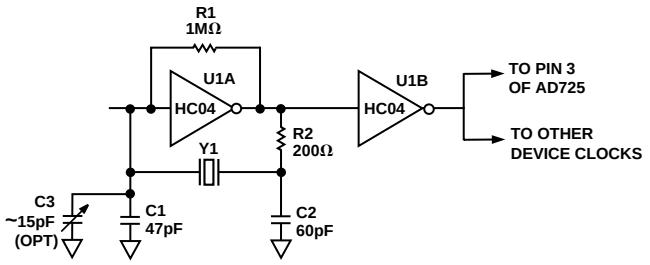


Figure 20. Low Cost Crystal Oscillator

The crystal should be a parallel resonant type at the appropriate frequency (NTSC/PAL, 4FSC). The series combination of C1 and C2 should approximately equal to the crystal manufacturer's specification for the parallel capacitance required for the crystal to operate at its specified frequency. C1 will usually want to be a somewhat smaller value because of the input parasitic capacitance of the inverter. If it is desired to tune the frequency to greater accuracy, C1 can be made still smaller and a parallel adjustable capacitor can be used to adjust the frequency to the desired accuracy.

Resistor R2 serves to provide the additional phase shift required by the circuit to sustain oscillation. It can be sized by $R2 = 1/(2 \times \pi \times f \times C2)$. Other functions of R2 are to provide a low pass filter that suppresses oscillations at harmonics of the fundamental of the crystal and to isolate the output of the inverter from the resonant load that the crystal network presents.

The basic oscillator described above is buffered by U1B to drive the AD725 4FSC pin and other devices in the system. For a system that requires both an NTSC and PAL oscillator, the circuit can be duplicated by using a different pair of inverters from the same package.

Dot Crawl

There are numerous distortions that are apparent in the presentation of composite signals on TV monitors. These effects will vary in degree depending on the circuitry used by the monitor to process the signal and on the nature of the image being displayed. It is generally not possible to produce pictures on a composite monitor that are as high quality as those produced by standard quality RGB, VGA monitors.

One well known distortion of composite video images is called dot crawl. It shows up as a moving dot pattern at the interface between two areas of different color. It is caused by the inability of the monitor circuitry to adequately separate the luminance and chrominance signals.

One way to prevent dot crawl is to use a video signal that has separate luminance and chrominance. Such a signal is referred to as S-video or Y/C video. Since the luminance and chrominance are already separated, the monitor does not have to perform this function. The S-video outputs of the AD725 can be used to create higher quality pictures when there is an S-video input available on the monitor.

Flicker

In a VGA conversion application, where the software controlled registers are correctly set, there are two techniques that are commonly used by VGA controller manufacturers to generate the interlaced signal. Each of these techniques introduces a unique characteristic into the display created by the AD725. The artifacts described below are not due to the encoder or its encoding algorithm as all encoders will generate the same display when presented with these inputs. They are due to the method used by the controller display chip to convert a noninterlaced output to an interlaced signal.

The first interlacing technique outputs a true interlaced signal with odd and even fields (one each to a frame Figure 21a). This provides the best picture quality when displaying photography, CD video and animation (games, etc.). However, it will introduce a defect commonly referred to as flicker into the display. Flicker is a fundamental defect of all interlaced displays and is caused by the alternating field characteristic of the interlace technique. Consider a one pixel high black line which extends horizontally across a white screen. This line will exist in only one field and will be refreshed at a rate of 30 Hz (25 Hz for PAL). During the time that the other field is being displayed the line will not be displayed. The human eye is capable of detecting this, and the display will be perceived to have a pulsating or flickering black line. This effect is highly content sensitive and is most pronounced in applications in which text and thin horizontal lines are present. In applications such as CD video, photography and animation, portions of objects naturally occur in both odd and even fields and the effect of flicker is imperceptible.

The second commonly used technique is to output an odd and even field that are identical (Figure 21b). This ignores the data that naturally occurs in one of the fields. In this case the same one pixel high line mentioned above would either appear as a two pixel high line, (one pixel high in both the odd and even field) or not appear at all if it is in the data that is ignored by the controller. Which of these cases occurs is dependent on the placement of the line on the screen. This technique provides a stable (i.e., nonflickering) display for all applications, but small text can be difficult to read and lines in drawings (or spreadsheets) can disappear. As above, graphics and animation are not particularly affected although some resolution is lost.

There are methods to dramatically reduce the effect of flicker and maintain high resolution. The most common is to ensure that display data never exists solely in a single line. This can be accomplished by averaging/weighting the contents of successive/multiple noninterlaced lines prior to creating a true interlaced output (Figure 21c). In a sense, this provides an output that will lie between the two extremes described above. The weight or percentage of one line that appears in another, and the number of lines used, are variables that must be considered in developing a system of this type. If this type of signal processing is performed, it must be completed prior to the data being presented to the AD725 for encoding.

Vertical Scaling

In addition to converting the computer generated image from noninterlaced to interlaced format, it is also necessary to scale the image down to fit into NTSC or PAL format. The most common vertical lines/screen for VGA display are 480 and 600 lines. NTSC can only accommodate approximately 400 visible lines/frame (200 per field), PAL can accommodate 576 lines/ frame (288 per field). If scaling is not performed, portions of the original image will not appear in the television display.

This line reduction can be performed by merely eliminating every Nth (6th line in converting 480 lines to NSTC or every 25th line in converting 600 lines to PAL). This risks generation of jagged edges and jerky movement. It is best to combine the scaling with the interpolation/averaging technique discussed above to ensure that valuable data is not arbitrarily discarded in the scaling process. Like the flicker reduction technique mentioned above, the line reduction must be accomplished prior to the AD725 encoding operation.

There is a new generation of VGA controllers on the market specifically designed to utilize these techniques to provide a crisp and stable display for both text and graphics oriented applications. In addition these chips rescale the output from the computer to fit correctly on the screen of a television. A list of known devices is available through Analog Devices' Applications group, but the most complete and current information will be available from the manufacturers of graphics controller ICs.

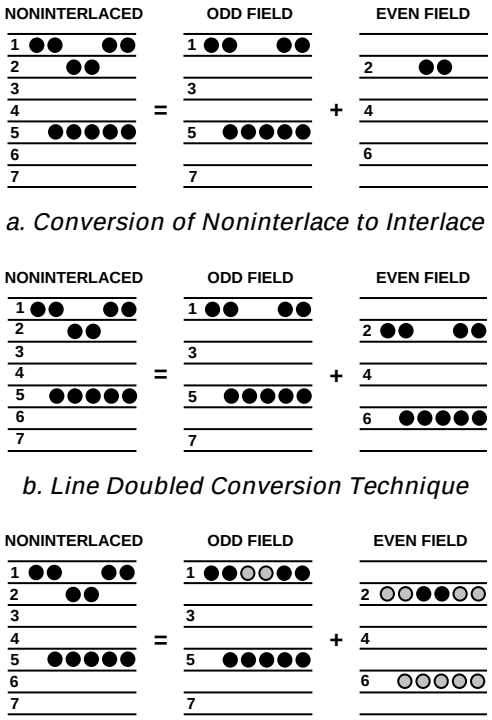
Synchronous vs. Asynchronous Operation

The source of RGB video and synchronization used as an input to the AD725 in some systems is derived from the same clock signal as used for the AD725 subcarrier input (4FSC). These systems are said to be operating synchronously. In systems where two different clock sources are used for these signals, the operation is called asynchronous.

The AD725 supports both synchronous and asynchronous operation, but some minor differences might be noticed between them. These can be caused by some details of the internal circuitry of the AD725.

There is an attempt to process all of the video and synchronization signals totally asynchronous with respect to the subcarrier signal. This was achieved everywhere except for the sampled delay line used in the luminance channel to time align the luminance and chrominance. This delay line uses a signal at eight times the subcarrier frequency as its clock.

The phasing between the delay line clock and the luminance signal (with inserted composite sync) will be constant during synchronous operation, while the phasing will demonstrate a periodic variation during asynchronous operation. The jitter of the asynchronous video output will be slightly greater due to these periodic phase variations.



a. Conversion of Noninterlace to Interlace

b. Line Doubled Conversion Technique

c. Line Averaging Technique

Figure 21.

LUMA TRAP-THEORY

The composite video output of the AD725 can be improved for some types of images by incorporating a luma trap (or Y-Trap) in the encoder circuit. The basic configuration for such a circuit is a notch or band elimination filter that is centered at the subcarrier frequency. The luma trap is only functional for the composite video output of the AD725; it has no influence on the S-Video (or Y/C-Video) output.

The need for a luma trap arises from the method used by composite video to encode the color part (chrominance or chroma) of the video signal. This is performed by amplitude and phase modulation of a subcarrier. The saturation (or lack of dilution of a color with white) is represented in the subcarrier's amplitude modulation, while the hue (or color as thought of as the sections of a rainbow) information is contained in the subcarrier's phase modulation. The modulated subcarrier occupies a bandwidth somewhat greater than 1 MHz depending on the video standard.

For a composite signal, the chroma is linearly added to the luminance (luma or brightness) plus sync signal to form a single composite signal with all of the picture information. Once this addition is performed, it is no longer possible to ascertain which component contributed which part of the composite signal.

At the receiver, this single composite signal must be separated into its various parts to be properly processed. In particular, the chroma must be separated and then demodulated into its orthogonal components, U and V. Then, along with the luma signal, the U and V signals generate the RGB signals that control the three video guns in the monitor.

A basic problem arises when the luma signal (which contains no color information) contains frequency components that fall

within the chroma band. All signals in this band are processed as chroma information since the chroma processing circuit has no knowledge as to where these signals originated. Therefore, the color that results from the luma signals in the chroma band is a false color. This effect is referred to as cross chrominance.

The cross chrominance effect is sometimes evident in white text on a black background as a moving rainbow pattern around the characters. The sharp transitions from black to white (and vice versa) that comprise the text dots contain frequency components across the whole video band, and those in the chroma band create cross chrominance. This is especially pronounced when the dot clock used to generate the characters is an integer multiple of the chroma subcarrier frequency.

Another common contributor to cross chrominance effects is certain striped clothing patterns that are televised. At a specific amount of zoom, the spatial frequency of vertical stripe patterns will generate luma frequencies in the chroma band. These frequency components will ultimately get turned into color by the video monitor. Since the phase of these signals is not coherent with the subcarrier, the effect shows up as random colors. If the zoom of a TV camera is modified or there is motion of the striped pattern, the false colors can vary quite radically and produce a quite objectionable "moving rainbow" effect. Most TV-savvy people have learned to adapt by just not wearing certain patterns when appearing on TV.

An excellent way to eliminate virtually all cross chrominance effects is to use S-video. Since the luma and chroma are carried on two separate circuits, there is no confusion as to which circuit should process which signals. Unfortunately, not all TVs that exist today, and probably still not even half of those being sold, have a provision for S-video input.

To ensure compatibility with the input capabilities of the majority of TVs in existence, composite video must be supplied. Many more TVs have a composite baseband video input port than have an S-video port to connect cameras and VCRs.

However, still the only common denominator for virtually all TVs is an RF input. This requires modulating the baseband video onto an RF carrier that is usually tuned to either Channel 3 or 4 (for NTSC). Most video games that can afford only a single output use an RF interface because of its universality. Sound can also be carried on this channel.

Since it is not practical to rely exclusively on S-video to improve the picture quality by eliminating cross chrominance, a luma trap can be used to minimize this effect for systems that use composite video. The luma trap notches out or "traps" the offending frequencies from the luma signal before it is added to the chroma. The cross chrominance that would be generated by these frequencies is thereby significantly attenuated.

The only sacrifice that results is that the luma response has a "hole" in it at the chroma frequency. This will lower the luminance resolution of details whose spatial frequency causes frequency components in the chroma band. However, the attenuation of cross chrominance outweighs this in the picture quality. S-video will not just eliminate cross chrominance, but will also not have this notch in the luma response.

Implementing a Luma Trap

The AD725 implementation of a luma trap uses an on-chip resistor along with an off-chip inductor and capacitor to create an RLC notch filter. The filter must be tuned to the center frequency of the video standard being output by the AD725, 3.58 MHz for NTSC or 4.43 MHz for PAL.

The circuit is shown in Figure 22. The 1 kΩ series resistor in the composite video luma path on the AD725 works against the impedance of the off-chip series LC to form a notch filter. The frequency of the filter is given by:

$$f = \frac{1}{2\pi\sqrt{LC}}$$

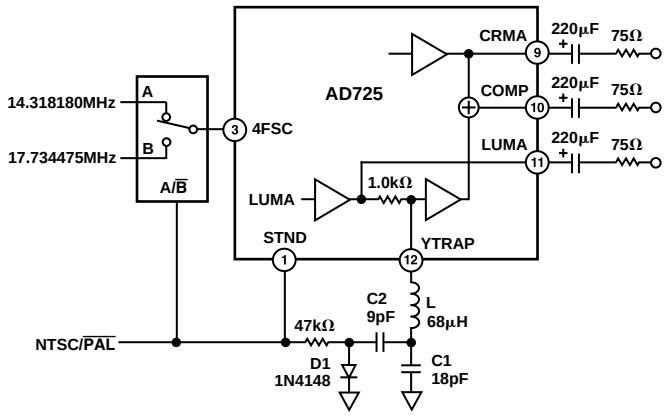


Figure 22. Luma Trap Circuit for NTSC and PAL Video

Dual-Standard Luma Trap

For a filter that will work for both PAL and NTSC a means is required to switch the tuning of the filter between the two subcarrier frequencies. The PAL standard requires a higher frequency than NTSC. A basic filter can be made that is tuned to the PAL subcarrier and a simple diode circuit can then be used to switch in an extra parallel capacitor that will lower the filter's frequency for NTSC operation.

Figure 22 shows how the logic signal that drives STND (Pin 1) can also be used to drive the circuit that selects the tuning of the luma trap circuit. When the signal applied to STND (Pin 1) is low (ground), the PAL mode is selected. This results in a bias of 0 V across D1, which is an off condition. As a result, C2 is out of the filter circuit and only C1 tunes the notch filter to the PAL subcarrier frequency, 4.43 MHz.

On the other hand, when STND is high (+5 V), NTSC is selected and there is a forward bias across D1. This turns the diode on and adds C2 in parallel with C1. The notch filter is now tuned to the NTSC subcarrier frequency, 3.58 MHz.

Measuring the Luma Trap Frequency Response

The frequency response of the luma trap can be measured in two different ways. The first involves using an RGB frequency sweep input pattern into the AD725 and observing the composite output on a TV monitor, a TV waveform monitor or on an oscilloscope.

On a TV monitor, the composite video display will look like vertical black and white lines that are coarsely spaced (low frequency) on the left side and progress to tightly spaced (high frequency) on the right side. Somewhere to the right of center, there will not be discernible stripes, but rather only a gray vertical area. This is the effect of the luma trap, which filters out luminance detail at a band of frequencies.

At the bottom of the display are markings at each megahertz that establish a scale of frequency vs. horizontal position. The location of the center of the gray area along the frequency marker scale indicates the range of frequencies that are being filtered out. The gray area should be about halfway between the 3 MHz and 4 MHz markers for NTSC, and about halfway between the 4 MHz and 5 MHz markers for PAL.

When a horizontal line is viewed on an oscilloscope or video waveform monitor, the notch in the response will be apparent. The frequency will have to be interpolated from the location of the notch position along the H-line.

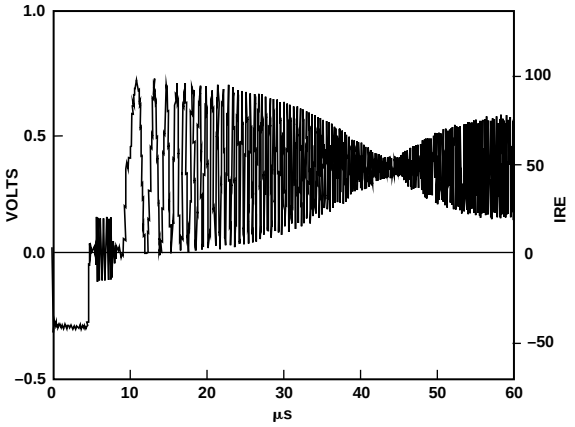


Figure 23. Luminance Sweep with Trap, COMP Pin

The second method involves using a network analyzer to measure the frequency response of the composite signal. In order to perform this successfully, the AD725 must be given the appropriate signals so that it will pass video signals through it. Figure 24 illustrates the setup used for these measurements.

The first requirement is that the part must receive a subcarrier clock. This will provide clocking to the internal delay line and enable it to pass the video signal. The subcarrier clock should be at the 4FSC frequency for either NTSC or PAL.

The second requirement is that the RGB inputs are properly biased for linear operation, and the timing logic is properly reset. It is acceptable to ac-couple the RGB inputs and momentarily apply an HSYNC signal to reset the timing and perform the dc restore. Because the inputs are high-impedance, the droop during testing will be minimal. It is not desirable to apply a steady pulse train of HSYNC inputs because the spectrum of these pulses will show up in the output response.

A more stable, low noise method is shown in Figure 23. The RGB inputs are biased using a power supply and the source port bias input of the network analyzer. A momentary sync input is still applied to the device to reset its internal timing, but droop during testing will no longer be an issue.

The signal source is applied to the GIN input for largest output response. This input should be terminated through the appropriate termination resistor (matching the output impedance of the network analyzer). If necessary, calibration inaccuracies can be flattened out by reading back the input reference using a FET probe.

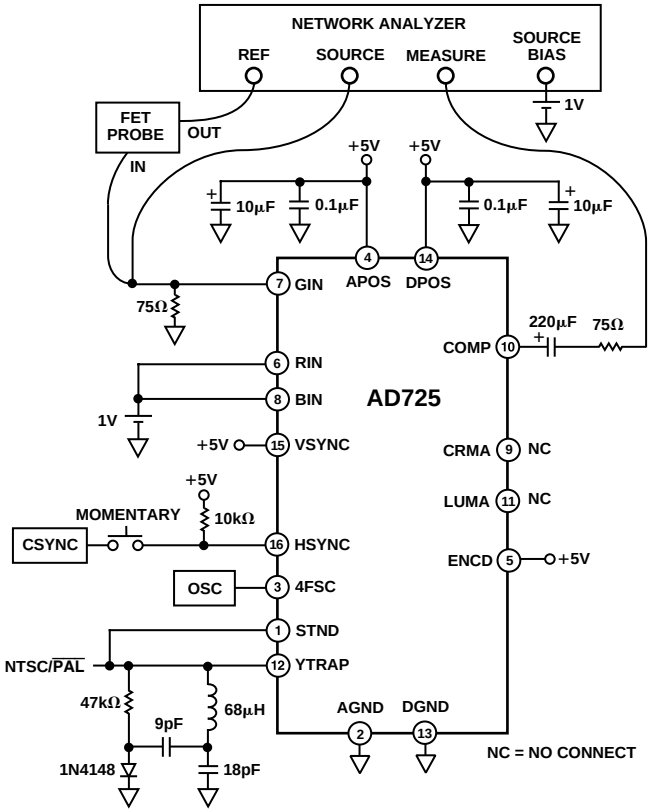


Figure 24. Measurement Setup for Determining Luma Trap Frequency

The composite output is reverse terminated with a 50 Ω or 75 Ω resistor and input to the measuring channel of a network analyzer.

Since only the green input is driven, this method does not yield an absolute measurement of composite signal levels, but the notch in the composite output will be readily discernible. The frequency measuring functions of the network analyzer can then be use to accurately measure the frequency of the luma notch filter (luma trap).

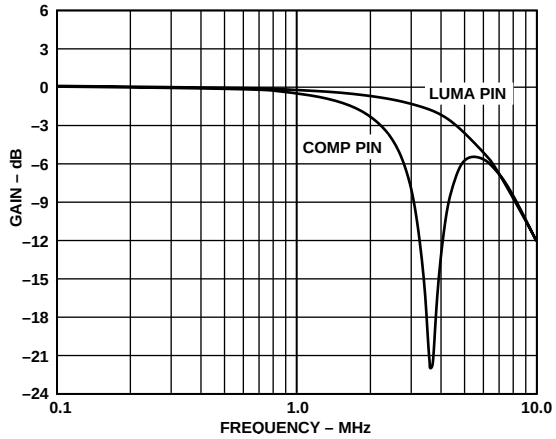


Figure 25. Luminance Frequency Response with NTSC Trap

SYNCHRONIZING SIGNALS

The AD725 requires explicit horizontal and vertical synchronizing signals for proper operation. This information cannot and should not be incorporated in any of the RGB signals. However, the synchronizing information can be provided as either separate horizontal (HSYNC) and vertical (VSYNC) signals or as a single composite sync (CSYNC) signal.

Internally the AD725 requires a composite sync logic signal that is mostly high and goes low during horizontal sync time. The vertical interval will have an inverted duty cycle from this. This signal should occur at the output of an on-chip XNOR gate on the AD725 whose two inputs are HSYNC (Pin 16) and VSYNC (Pin 15). There are several options for meeting these conditions.

The first is to have separate signals for HSYNC and VSYNC. Each should be mostly low and then high going during their respective time of assertion. This is the convention used by RGB monitors for most PCs. The proper composite sync signal will be produced by the on-chip XNOR gate when using these inputs.

If a composite sync signal is already available, it can be input into HSYNC (Pin 16), while VSYNC (Pin 15) can be used to change the polarity. (In actuality, HSYNC and VSYNC are interchangeable since they are symmetric inputs to a two-input gate).

If the composite sync input is mostly high and then low going for active HSYNC time (and inverted duty cycle during VSYNC), then it is already of the proper polarity. Pulling VSYNC high, while inputting the composite sync signal to HSYNC will pass this signal though the XNOR gate without inversion.

On the other hand, if the composite sync signal is the opposite polarity as described above, pulling VSYNC low will cause the XNOR gate to invert the signal. This will make it the proper polarity for use inside the AD725. These logic conditions are illustrated in Figure 26.

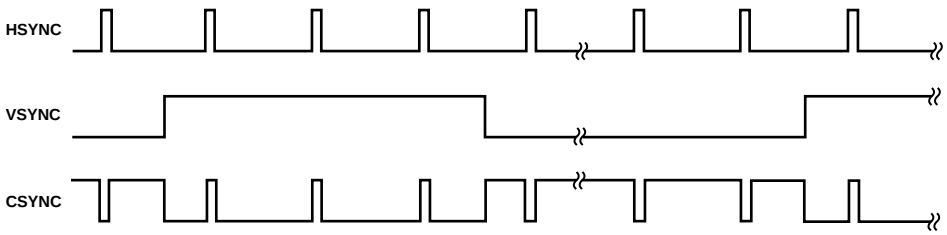
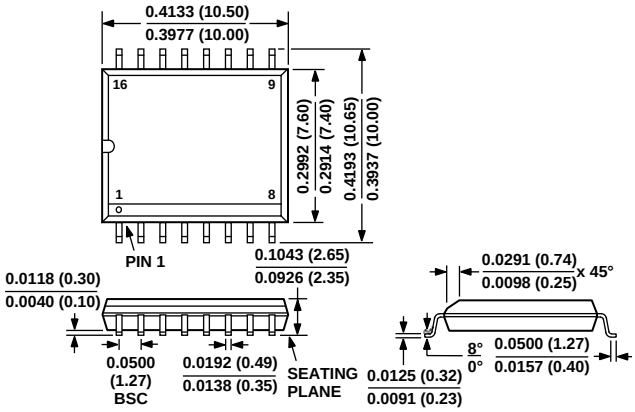


Figure 26. Sync Logic Levels (Equalization and Serration Pulses Not Shown)

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-Lead Wide Body SOIC
(R-16)



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