



Dual 6-Bit, 60 MSPS Monolithic A/D Converter

AD9066

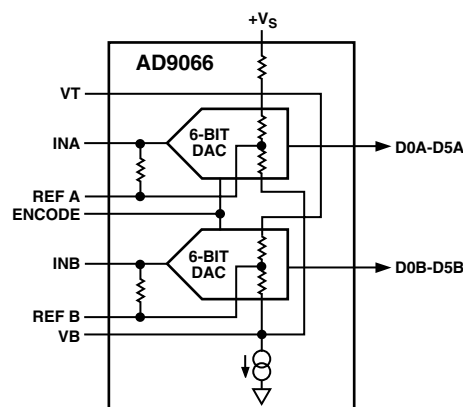
FEATURES

- Two Matched ADCs on Single Chip
- CMOS-Compatible I/O
- Low-Power (400 mW) Dissipation
- Single +5 V Supply
- On-Chip Voltage Reference
- Self-Biased for AC-Coupled Inputs
- 28-Lead SOIC and SSOP Packages

APPLICATIONS

- Direct Broadcast Satellite (DBS) Receivers
- QAM Demodulators
- Wireless LANs
- VSAT Receivers

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

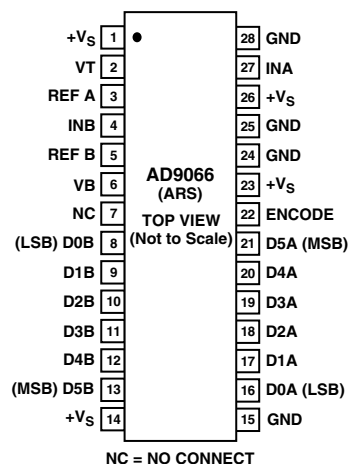
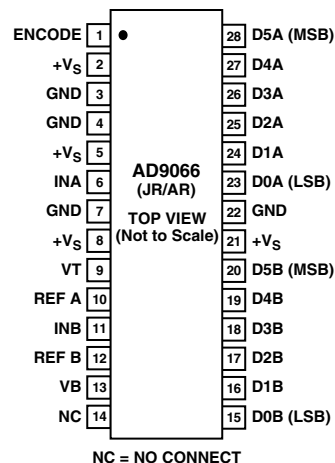
The AD9066 is a dual 6-bit ADC that has been optimized for low-cost in-phase and quadrature (I and Q) demodulators. Primary applications include digital direct broadcast satellite applications where broadband quadrature phase shift keying (QPSK) modulation is used. In these receivers the recovered signal is separated into I and Q vector components and digitized.

To reduce total system cost and power dissipation, the AD9066 provides an internal voltage reference and operates from a single +5 volt power supply. Digital outputs are CMOS compatible and rated to 60 MSPS conversion rates. The digital input (ENCODE) utilizes a CMOS input stage with a TTL compatible (1.4 V) threshold.

The AD9066 is housed in a 28-lead SOIC and a 28-lead SSOP package and is available in two temperature grades. The AD9066JR is rated for operation over the 0°C to 70°C commercial temperature range. The AD9066AR/ARS is rated for the -40°C to +85°C industrial temperature range.

The internal voltage reference insures that the analog input is biased to midscale with low offset when driven from an ac-coupled source. In dc-coupled applications, the midscale voltage reference can be used to control external biasing amplifiers to minimize offsets due to variations in temperature or supply voltage.

PIN CONFIGURATIONS



REV. A

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AD9066—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (+V_S = +5 V, AIN = 15.5 MHz, Encode Rate = 60 MSPS, T_C = T_A)

| Parameter | Test Level | Temp | AD9066JR | | | AD9066AR/ARS | | | Unit |
|--|------------|-------|----------|-----------------------|------|--------------|-----------------------|------|--------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| ANALOG INPUT | | | | | | | | | |
| Full-Scale Input Range | VI | Full | 475 | 500 | 525 | 450 | 500 | 530 | mV |
| Gain Matching (FS Range) | IV | Full | | | 16 | | | 16 | mV |
| DC Input (Midscale) ¹ | V | +25°C | | +V _S – 1.1 | | | +V _S – 1.1 | | V |
| Input Offset ¹ | VI | Full | –1.0 | | +1.0 | –1.0 | | +1.0 | LSBs |
| Input Capacitance | IV | Full | | 10 | 15 | | 10 | 15 | pF |
| Input Resistance (DC) | VI | Full | 25 | 45 | 55 | 22 | 45 | 57 | kΩ |
| Input Bandwidth (3 dB) | V | +25°C | | 100 | | | 100 | | MHz |
| Gain Flatness (to 15 MHz) | V | +25°C | | 0.25 | | | 0.25 | | dB |
| Integral Linearity | VI | Full | –1.0 | | +1.0 | –1.0 | | +1.0 | LSBs |
| Differential Linearity | VI | Full | –0.5 | | +0.5 | –0.5 | | +0.5 | LSBs |
| Monotonicity | VI | Full | | Guaranteed | | | Guaranteed | | |
| SWITCHING PERFORMANCE | | | | | | | | | |
| Max Conversion Rate | VI | Full | 60 | | | 60 | | | MSPS |
| Output Delay (t _V) ² | IV | Full | 4 | | | 4 | | | ns |
| Output Delay (t _{PD}) ² | IV | Full | | | 11 | | | 12 | ns |
| Aperture Uncertainty (Jitter) | V | +25°C | | 10 | | | 10 | | ps rms |
| Aperture Time (t _A) | V | +25°C | | 1.0 | | | 1.0 | | ns |
| DYNAMIC PERFORMANCE ³ | | | | | | | | | |
| Effective Number of Bits | VI | +25°C | 5.3 | 5.7 | | 5.2 | 5.7 | | Bits |
| SINAD | VI | +25°C | 34 | 36 | | 33 | 36 | | dB |
| Harmonic Distortion (THD) | VI | +25°C | 40 | 50 | | 40 | 50 | | dB |
| Crosstalk Rejection | IV | +25°C | 40 | 50 | | 40 | 50 | | dBc |
| ENCODE INPUT | | | | | | | | | |
| Logic High Voltage | VI | Full | 2.0 | | | 2.0 | | | V |
| Logic Low Voltage | VI | Full | | | 0.8 | | | 0.8 | V |
| Input High Current | VI | Full | | | 500 | | | 500 | μA |
| Input Low Current | VI | Full | | | 500 | | | 500 | μA |
| Pulsewidth High | IV | Full | 7.0 | | | 7.0 | | | ns |
| Pulsewidth Low | IV | Full | 7.0 | | | 7.0 | | | ns |
| DIGITAL OUTPUTS | | | | | | | | | |
| Output Coding | | Full | | Offset Binary | | | Offset Binary | | |
| Logic High Voltage (I _{OH} = 1 mA) | VI | Full | 3.8 | | | 3.8 | | | V |
| Logic Low Voltage (I _{OL} = 1 mA) | VI | Full | | | 0.4 | | | 0.4 | V |
| POWER SUPPLY | | | | | | | | | |
| +V _S Supply Voltage | VI | Full | 4.75 | | 5.25 | 4.75 | | 5.25 | V |
| Power Supply Rejection Ratio ¹ | IV | Full | | 110 | 130 | | 110 | 130 | mV/V |
| +V _S Supply Current | VI | Full | | 80 | 120 | | 80 | 120 | mA |
| Power Dissipation ⁴ | VI | Full | | 400 | 600 | | 400 | 600 | mW |

NOTES

¹For ac coupled applications, the ADC is internally biased to insure that the midpoint transition of the ADC is within the limits specified with no signal applied. For dc coupled applications, the dc value of the midpoint transition voltage will track the supply voltage within the limits shown for dc input (midscale) plus the dc offset. Power Supply Rejection Ratio (PSRR) refers to the variation of the input signal range (gain) to supply voltage.

²t_V and t_{PD} are measured from the 1.4 V level of the Clock and the 50% level between V_{OH} and V_{OL}. The ac load on all the digital outputs during test is 10 pF (max), the dc load will not exceed ±40 μA.

³Effective number of bits (ENOB) and THD are measured using a FFT with a pure sine wave analog input @ 15.5 MHz, 1 dB below full scale. ENOB is calculated by ENOB = (SNR – 1.76 dB)/6.02; THD is measured from full scale to the sum of the second through seventh harmonic of the input.

⁴Typical thermal impedance for the “R” style (SOIC) 28-lead package is: θ_{JC} = 4°C/W, θ_{CA} = 41°C/W, θ_{JA} = 45°C/W, and the “RS” style (SSOP) 28-lead package is: θ_{JC} = 26.97°C/W, θ_{CA} = 51.61°C/W, θ_{JA} = 78.58°C/W.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

| Pin | Min | Max | Unit |
|-------------------|------|-----------------|------|
| ENCODE | -0.5 | +V _S | V |
| +V _S | | 7.0 | V |
| INA, INB | -0.5 | +V _S | V |
| VT | 2.5 | +V _S | V |
| REF A, REF B | -0.5 | +V _S | V |
| VB | 0.0 | +V _S | V |
| D0-D5 Current OUT | | 20 | mA |

EXPLANATION OF TEST LEVELS

| Test Level | Description |
|------------|--|
| I | 100% Production Tested |
| II | 100% Production Tested at +25°C, and Sample Tested at Specified Temperatures |
| III | Sample Tested Only |
| IV | Parameter Is Guaranteed by Design |
| V | Parameter Is Typical Value Only |
| VI | 100% Tested at +25°C |

DIE LAYOUT AND MECHANICAL INFORMATION

| | |
|---------------------|-------------------------|
| Die Dimensions | 132 × 68 × 21 (±1) mils |
| Pad Dimensions | 4 × 4 mils |
| Metalization | Aluminum |
| Backing | None |
| Substrate Potential | Ground |
| Transistor Count | 5,810 |
| Passivation | Silicon Nitride |
| Die Attach | Silver Filled |
| Bond Wire | Gold |

ORDERING GUIDE

| Model | Temperature Range | Package Option* |
|-----------|-------------------|-----------------|
| AD9066AR | -40°C to +85°C | R-28 |
| AD9066JR | 0°C to +70°C | R-28 |
| AD9066ARS | -40°C to +85°C | RS-28 |

*R = "SO" Small Outline Package; RS = SSOP.

PIN DESCRIPTIONS

| AR:JR Pin No. | ARS Pin No. | Name | Function |
|---------------|-------------|-----------------|--|
| 1 | 22 | ENCODE | TTL Compatible CMOS Clock, Samples on Rising Edge. |
| 2 | 23 | +V _S | +5 V Supply for Digital Input. |
| 3 | 24 | GND | Ground. |
| 4 | 25 | GND | Ground. |
| 5 | 26 | +V _S | +5 V Supply (Analog). |
| 6 | 27 | INA | Channel A Analog Input. |
| 7 | 28 | GND | Ground. |
| 8 | 1 | +V _S | +5 V Supply (Analog). |
| 9 | 2 | VT | Top of Voltage Reference, Bypass to GND. |
| 10 | 3 | REF A | Mid Reference to ADC A, Bypass to GND. |
| 11 | 4 | INB | Channel B Analog Input. |
| 12 | 5 | REF B | Mid Reference to ADC B, Bypass to GND. |
| 13 | 6 | VB | Bottom of Reference Ladder, Bypass to GND. |
| 14 | 7 | NC | No Connect. |
| 15 | 8 | D0B (LSB) | Digital Outputs Channel B, CMOS Compatible. |
| 16 | 9 | D1B | |
| 17 | 10 | D2B | |
| 18 | 11 | D3B | |
| 19 | 12 | D4B | |
| 20 | 13 | D5B (MSB) | |
| 21 | 14 | +V _S | +5 V Supply for Digital Outputs. |
| 22 | 15 | GND | Ground. |
| 23 | 16 | D0A (LSB) | Digital Outputs Channel A, CMOS Compatible. |
| 24 | 17 | D1A | |
| 25 | 18 | D2A | |
| 26 | 19 | D3A | |
| 27 | 20 | D4A | |
| 28 | 21 | D5A (MSB) | |

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9066 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



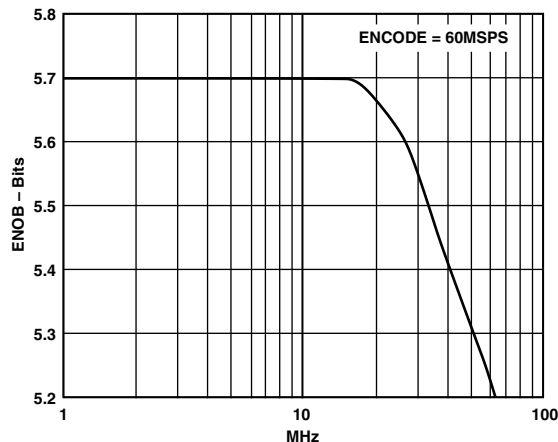


Figure 1. ENOB vs. Analog Input Frequency

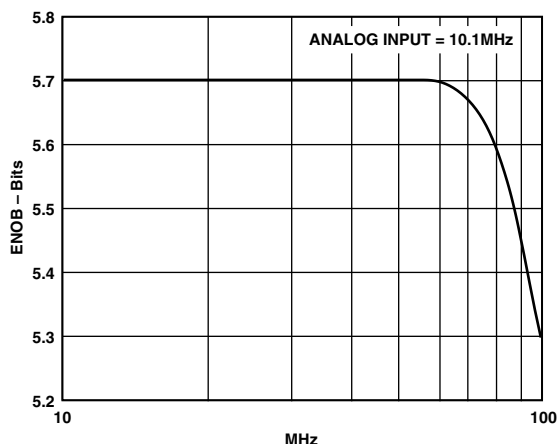


Figure 2. ENOB vs. Encode Rate

USING THE AD9066

Analog Input and Voltage References

The AD9066 is optimized to allow ac coupled inputs with a full-scale input range of $500 \text{ mV} \pm 5\%$. An LSB weight is approximately 8 mV. The full-scale input range is defined as the voltage range that accommodates $2^n - 2$ codes of equally weighted LSBs (between the first and last code transitions). For the AD9066 there are 32 codes above and below the midscale voltage of the A see Figure 3).

The full-scale input range of the AD9066 is equal to $500/620 \times (V_T - V_B)$, or nominally 500 mV. For dc coupled applications, the REF A and REF B voltages can be used to feed back offset compensation signals. This will allow the midscale transition voltage of the ADCs to track supply and temperature variations.

In the event that offset correction signals are generated digitally, the REF pins would not be required. Figure 4a shows the equivalent circuit for the internal references. All component tolerances are $\pm 25\%$.

Gain Variation

The full-scale input range is established by the current through the two matched resistor ladders (620 ohms each nominal). Therefore the gain of the ADC may be modified by forcing different voltages across the top and bottom voltage taps (V_T and V_B).

The easiest way to increase the input range will be to force V_B to a lower voltage. Using an external amplifier, the voltage at V_B may be forced as low as 3.0 V (3.58 nominal). Using the previously described relationship for full scale and the internal resistor ladder values, 3.0 V at V_B will result in a nominal full-scale input range of 705 mV.

A larger input range can be established by taking the V_T voltage all the way to the supply voltage level while pulling V_B to 3.0 V. This would force a 2 V potential across the ladder and create a full-scale input range of 1.6 V.

Greater flexibility and improved power supply rejection can be achieved by forcing external voltage references at both the top and bottom of the resistor ladder.

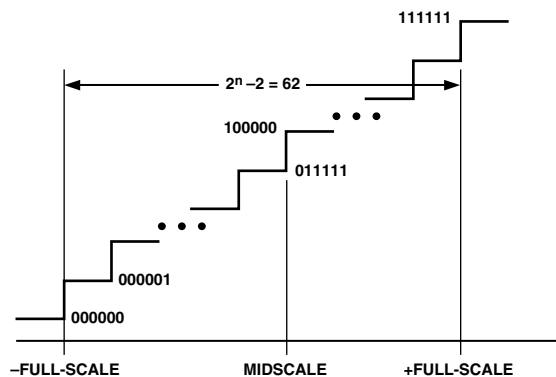


Figure 3.

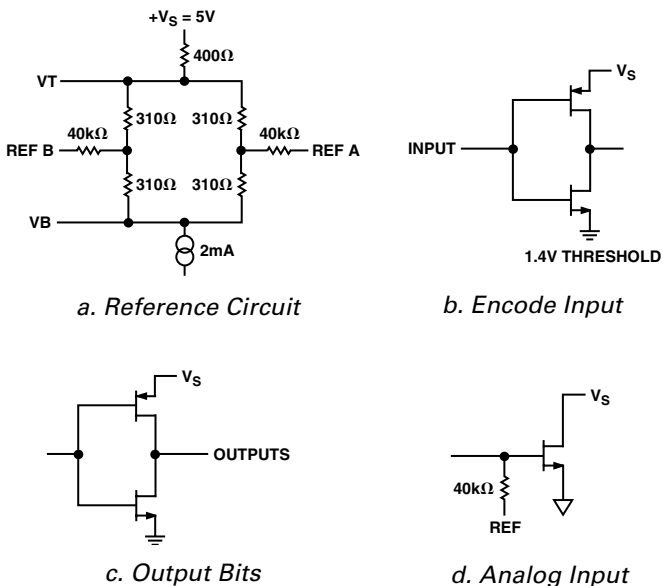


Figure 4. Equivalent Circuits

Timing

The duty cycle of the encode clock for the AD9066 is critical in obtaining rated performance of the ADC. Rated maximum and minimum pulse widths should be maintained, especially for sample rates greater than 40 MSPS.

The AD9066 provides latched data outputs with three pipeline delays. The length and load on the output data lines should be minimized to reduce power supply transients inside the AD9066 which might diminish dynamic performance.

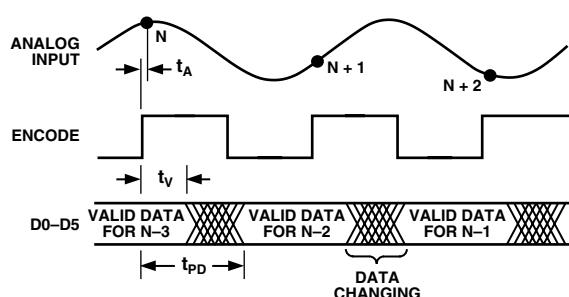


Figure 5. Timing Diagram

The data is invalid during the period between t_V and t_{PD} . This period refers to the time required for the AD9066 to fully switch between valid CMOS logic levels. When latching the output data, be careful to observe latch setup and hold time restrictions as well as this data invalid period when designing the system timing.

Layout and Signal Care

To insure optimum performance, a single low impedance ground plane is recommended. Analog and digital grounds should be connected together at the AD9066. Analog and digital power supplies should be bypassed, at the device, to ground through 0.1 μF ceramic capacitors.

The use of sockets may limit the dynamic performance of the part and is not recommended except for prototype or evaluation purposes.

Driving the AD9066 with a Bipolar Input

The analog input range of the AD9066 is between 3.7 V and 4.2 V. Because the input is offset, the normal method of driving the analog input is to use a blocking capacitor between the analog source and the AD9066 analog input pins. In applications where DC coupling must be employed, the simple circuit shown in Figure 6 will take a bipolar input and offset it to the operating range of the AD9066.

To offset the input, the midpoint voltage of the AD9066 is buffered off chip and then inverted with an AD712, a low input bias current dual op amp. This inverted midpoint is then fed to a summation amplifier that combines the bipolar input with the inverted offset voltage. The summation amplifier is an AD812, a wideband current feedback amplifier that provides good bandwidth and low distortion.

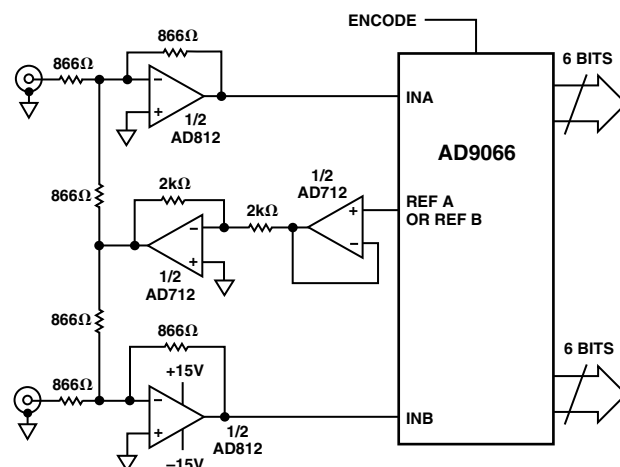


Figure 6. Bipolar Input Using AD812 Drive for AD9066

Layout should follow high frequency/high speed design guidelines. In addition the capacitance around the inverting input to the AD812 should be minimized through a tight layout and the use of low capacitance chip resistors for gain setting.

Quadrature Receiver Using the AD9066

Although any type of input signal may be applied, the AD9066 has been optimized for low cost in-phase and quadrature (I and Q) demodulators. Primary applications include digital direct broadcast satellite applications where broadband quadrature phase shift keying (QPSK) modulation is used. In these receivers the recovered signal is separated into I and Q vector components and digitized.

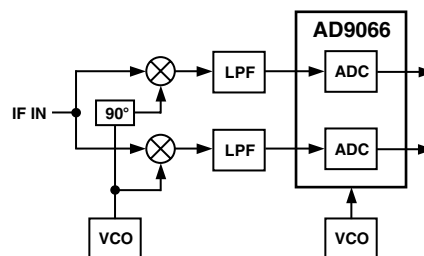


Figure 7. Simplified Block Diagram

For data symbol rates less than 10 Mbaud, the AD607 IF/RF receiver subsystem provides an ideal solution for the second conversion stage of a complete receiver system. Figure 8 shows the AD9066 and AD607 used together.

The AD607 accepts inputs as high as 500 MHz which may be the output of the first IF stage or RF signals directly. The IF/RF signal is mixed with the local oscillator to provide an IF frequency of 400 kHz to 22 MHz. This signal is filtered externally and then amplified with an on-chip AGC before being synchronously demodulated with an on-chip PLL carrier recovery circuit. The outputs are digitized with the AD9066. The digital outputs may be processed with a DSP chip such as the ADSP-2171, ADSP-21062, general purpose DSP or ASIC.

AD9066

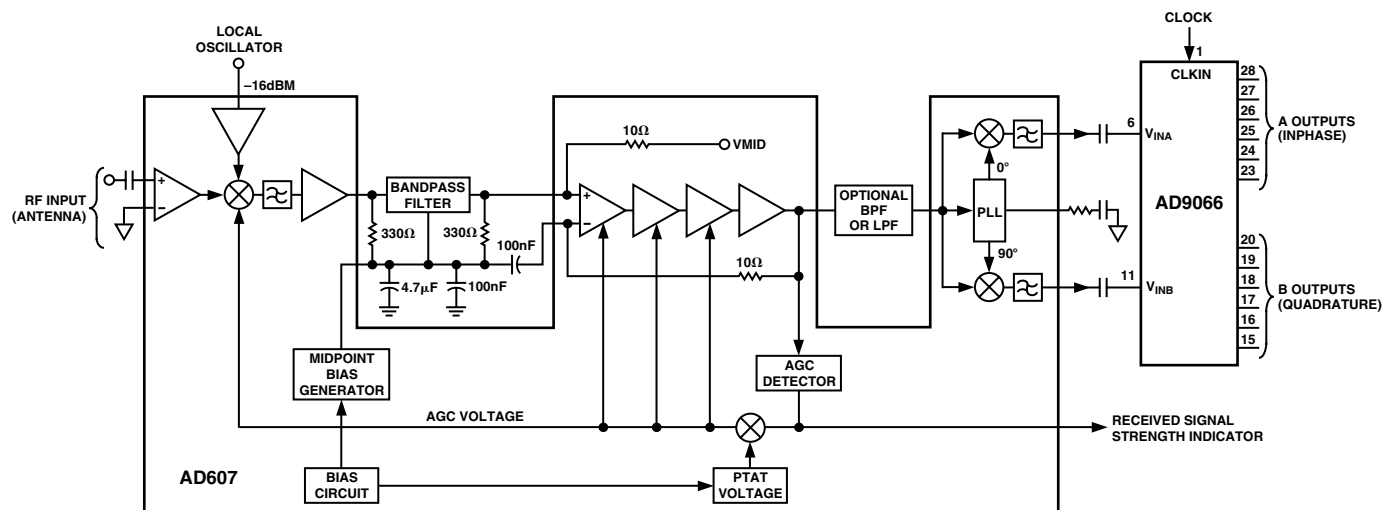


Figure 8. Digitizer with AD607 Receiver Circuit

Theory of Operation

The AD9066 dual ADC employs a patented interpolated flash architecture. This architecture enables 64 possible quantization levels with only 32 comparator preamplifiers. This keeps input capacitance to a minimum. The midpoint of the reference ladder is fed back to the analog input, allowing easy biasing of the ADC to midscale for ac coupled applications.

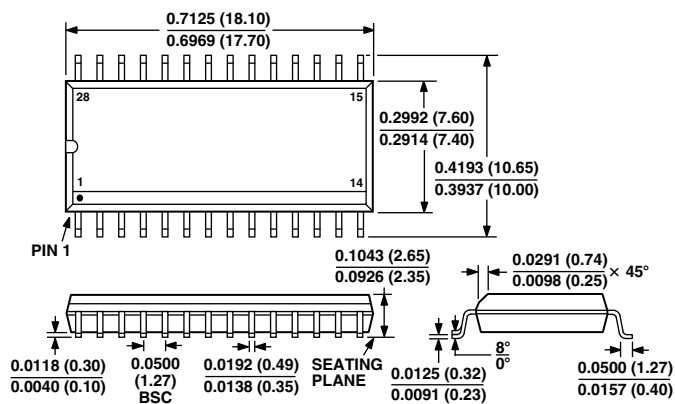
As shown in Figure 4d, a simple resistor is used to provide the reference ladder midpoint to the analog input. The high impedance MOS inputs of the comparators insure no static voltage drop across the resistor. This eliminates the need for an active buffer (and its inherent offsets) to set the reference midpoint at the analog input.

The outputs of the comparators are converted to a 6-bit word and converted to CMOS levels. The digital signals are latched at six stages (two pipeline delays) in the signal path. The digital outputs are CMOS with approximately equal rise and fall times.

The encode clock utilizes a CMOS input stage with TTL-compatible (1.4 V) thresholds. Internal clock buffers minimize external clock drive requirements.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

28-Lead Small Outline Package
(R-28)28-Lead SSOP
(RS-28)