a

12-Bit, 170 MSPS 3.3V A/D Converter

Preliminary Technical Data AD9430

FEATURES

SNR = 65dB @ Fin up to 65MHz at 170Msps
ENOB of 10.3 @ Fin up to 65MHz at 170 Msps (-1dBFs)
SFDR = -80dBc @ Fin up to 65MHz at 170Msps (-1dBFs)
Excellent Linearity:
- **DNL = +/- 1 lsb (typ)**
- **INL = +/- 1.5 lsb (typ)**

Two Output Data options
- **Demultiplexed 3.3V CMOS outputs each at 85 Msps**
- **LVDS at 170Msps**

700 MHz Full Power Analog Bandwidth
On–chip reference and track/hold
Power dissipation = 1.25W typical at 170Msps
1.5V Input voltage range
+3.3V Supply Operation
Output data format option
Data Sync input and Data Clock output provided
Interleaved or parallel data output option (CMOS)
Clock Duty Cycle Stabilizer.

APPLICATIONS

Wireless and Wired Broadband Communications
- **Wideband carrier frequency systems**
- **Cable Reverse Path**

Communications Test Equipment
Radar and Satellite sub-systems
Power Amplifier Linearization

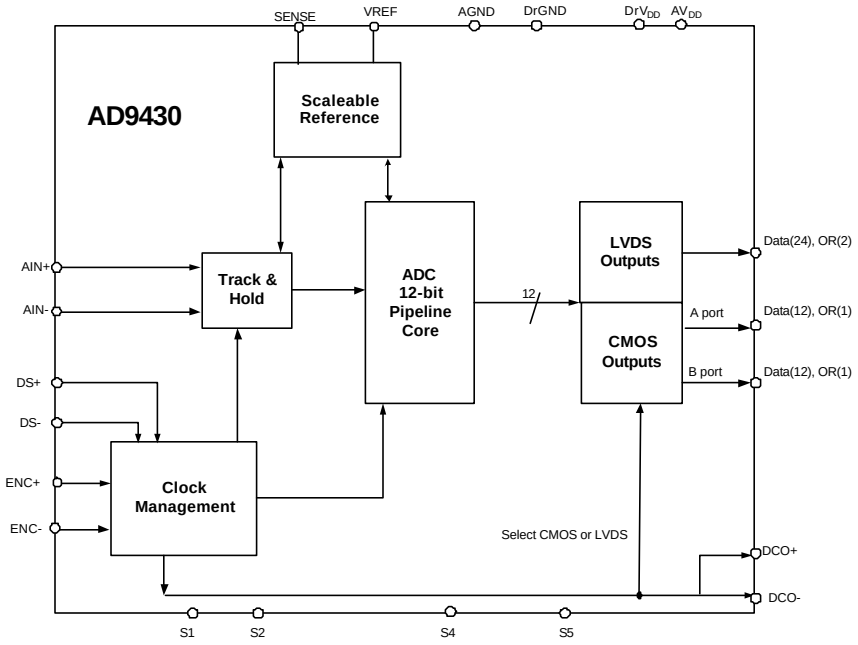
PRODUCT DESCRIPTION

The AD9430 is a 12-bit monolithic sampling analog–to–digital converter with an on–chip track–and–hold circuit and is optimized for low cost, low power, small size and ease of use. The product operates up to 170 Msps conversion rate and is optimized for outstanding dynamic performance in wideband carrier systems.

The ADC requires a +3.3V power supply and a differential encode clock for full performance operation. No external reference or driver components are required for many applications. The digital outputs are TTL/CMOS or LVDS compatible. Separate output power supply pins support interfacing with 3.3V CMOS logic.

An output data format select option of two's complement or offset binary is supported. In CMOS mode two output buses support demultiplexed data up to 85 Msps rates. A data sync input is supported for proper output data port alignment and a data clock output is available for proper output data timing.

Fabricated on an advanced BiCMOS process, the AD9430 is available in a 100 pin surface mount plastic package (100 TQFP ePAD) specified over the industrial temperature range (–40°C to +85°C).



AD9430 FUNCTIONAL BLOCK DIAGRAM

REV. PrG 4/01/2002

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AD9430

DC SPECIFICATIONS (AV_{DD}= DrV_{DD} = 3.3V; T_{MIN} = -40°C, T_{MAX} = +85°C, Fin = -0.5dBFS, 1.235V External reference, LVDS Output Mode)

Parameter	Temp	Test Level	AD9430BSV-170 Min	Typ	Max	Units
RESOLUTION				12		Bits
ACCURACY						
No Missing Codes	Full	I		Guaranteed		
Offset Error	25°C	I		tbd		mV
Gain Error	25°C	I		tbd		% FS
Differential Nonlinearity (DNL)	25°C	I		+/- .3		LSB
Integral Nonlinearity (INL)	25°C	I		+/- .5		LSB
TEMPERATURE DRIFT						
Offset Error	Full	V		tbd		ppm/°C
Gain Error	Full	V		tbd		ppm/°C
POWER SUPPLY REJECTION	Full	V		± tbd		mV/V
REFERENCE OUT (V_{REF})	Full	V		1.235		V
ANALOG INPUTS (AIN, $\overline{AIN}$)						
Input Voltage Range (AIN– $\overline{AIN}$)[1]	Full	V		± .768		V
Input Common Mode Voltage	Full	V		2.8		V
Input Resistance	Full	V		3		kΩ
Input Capacitance	Full	V		5		pF
POWER SUPPLY						
Supply Voltages						
AV_{DD}	Full	V	3.0	3.3	3.6	V
DrV_{DD}	Full	V	3.0	3.3	3.6	V
Supply Current						
I_{ANALOG} (AV_{DD}= 3.3V)[2]	Full	V		335		mA
$I_{DIGITAL}$ (DrVDD = 3.3V)[2]	Full	V		55		mA
POWER CONSUMPTION[3]	Full	V		1.29		W

NOTES

[1] Nominal Differential Full Scale = .766 V * 2 = 1.53 $V_{p\text{-}p\ differential}$ for S5 = 0; Nominal Differential Full Scale = .766 $V_{p\text{-}p\ differential}$ for S5 = 1 (see Fig. X)

2 I_{AVDD} and I_{DrVDD} are measured with an analog input of 10.3MHz, -0.5dBFs, sine wave, rated Encode rate and in LVDS output mode. See Typical Performance Characteristics and Applications section for I_{DrVDD}. 3 Power Consumption is measured with a DC input at rated Encode rate in LVDS output mode

DIGITAL SPECIFICATIONS (AV_{DD}= 3.3V, DrV_{DD} = 3.3V; T_{MIN} = -40°C, T_{MAX} = +85°C)

Parameter (Conditions)	Temp	Test Level	AD9430BSV-170 Min	Typ	Max	Units
ENCODE AND DATA SYNC INPUTS (ENC, $\overline{ENC}$, DS, DS/)						
Differential Input Voltage[1]	Full	IV	0.2			V
Encode Common Mode Voltage	Full	IV		1.5		V
Input Resistance	Full	IV		5.5		kΩ
Input Capacitance	Full	IV		4		pF
LOGIC INPUTS (S1,S2,S4,S5)						
Logic '1' Voltage	Full	IV	2.0			V
Logic '0' Voltage	Full	IV			.8	V
Input Resistance	Full	IV		30		kΩ
Input Capacitance	Full	IV		4		pF
LOGIC OUTPUTS (Demux Mode)						
Logic "1" Voltage[2]	Full	IV	DrV_{DD}-0.05			V
Logic "0" Voltage[2]	Full	IV			0.05	V
LOGIC OUTPUTS (LVDS Mode)[2,3]						
V_{OD} Differential Output Voltage	Full	IV	247		454	mV
V_{OS} Output Offset Voltage	Full	IV	1.125		1.375	V
Output Coding	Full	IV	Two's Comp or Binary			

NOTES [1]All AC specifications tested by driving ENCODE and $\overline{ENCODE}$ differentially | ENCODE - $\overline{ENCODE}$ | > 200mV

[2]Digital Output Logic Levels: DrV_{DD}= 3.3V, C_{LOAD} = 5pF. [3] LVDS Rl=100 ohms, LVDS Output Swing Set Resistor = 3.7K

AC SPECIFICATIONS[1] (AV_{DD}= 3.3 V, DrV_{DD} = 3.3V; ENCODE = Maximum Conversion Rate ; T_{MIN} = -40°C, T_{MAX} = +85°C, Internal voltage reference, LVDS Output Mode)

Parameter (Conditions)	Temp	Test Level	AD9430BSV-170 Min	Typ	Max	Units
SNR						
Analog Input 10 MHz	25°C	I		65		dB
@ -0.5dBFS 65 MHz	25°C	I		65		dB
100 MHz	25°C	V		65		dB
240 MHz	25°C	V		64		dB
SINAD						
Analog Input 10 MHz	25°C	I		65		dB
@ -0.5dBFS 65 MHz	25°C	I		65		dB
100 MHz	25°C	V		64.5		dB
240 MHz	25°C	V		60		dB
Worst Harmonic (2^{nd} or 3^{rd})						
Analog Input 10 MHz	25°C	I		-85		dBc
@ -0.5dBFS 65 MHz	25°C	I		-80		dBc
100 MHz	25°C	V		-77		dBc
240 MHz	25°C	V		-63		dBc
Worst Harmonic (4^{th} or higher)						
Analog Input 10 MHz	25°C	I		-87		dBc
@ -0.5dBFS 65 MHz	25°C	I		-87		dBc
100 MHz	25°C	V		-77		dBc
240 MHz	25°C	V		-63		dBc
Two-tone IMD[2]						
F1, F2 @ -7 dBFS	Full	V		-75		dBc
Analog Input Bandwidth	25°C	V		700		MHz

NOTES
[1] All AC specifications tested by driving ENCODE and $\overline{\text{ENCODE}}$ differentially.
2 F1 = 31.5 MHz, F2 = 32.5 MHz

SWITCHING SPECIFICATIONS (AV_{DD}= 3.3 V, DrV_{DD} = 3.3V; ENCODE = Maximum Conversion Rate ; T_{MIN} = -40°C, T_{MAX} = +85°C)

Parameter (Conditions)	Temp	Test Level	AD9430BSV-170 Min	Typ	Max	Units
Maximum Conversion Rate[1]	Full	I		170		MSPS
Minimum Conversion Rate[1]	Full	V		40		MSPS
Encode Pulse Width High (t_{EH})[1]	Full	V		2		nS
Encode Pulse Width Low (t_{EL})[1]	Full	V		2		nS
DS Input Setup Time (t_{SDS})[2]	Full	IV		.5		nS
DS Input Hold Time (t_{HDS})[2]	Full	IV		1.5		nS

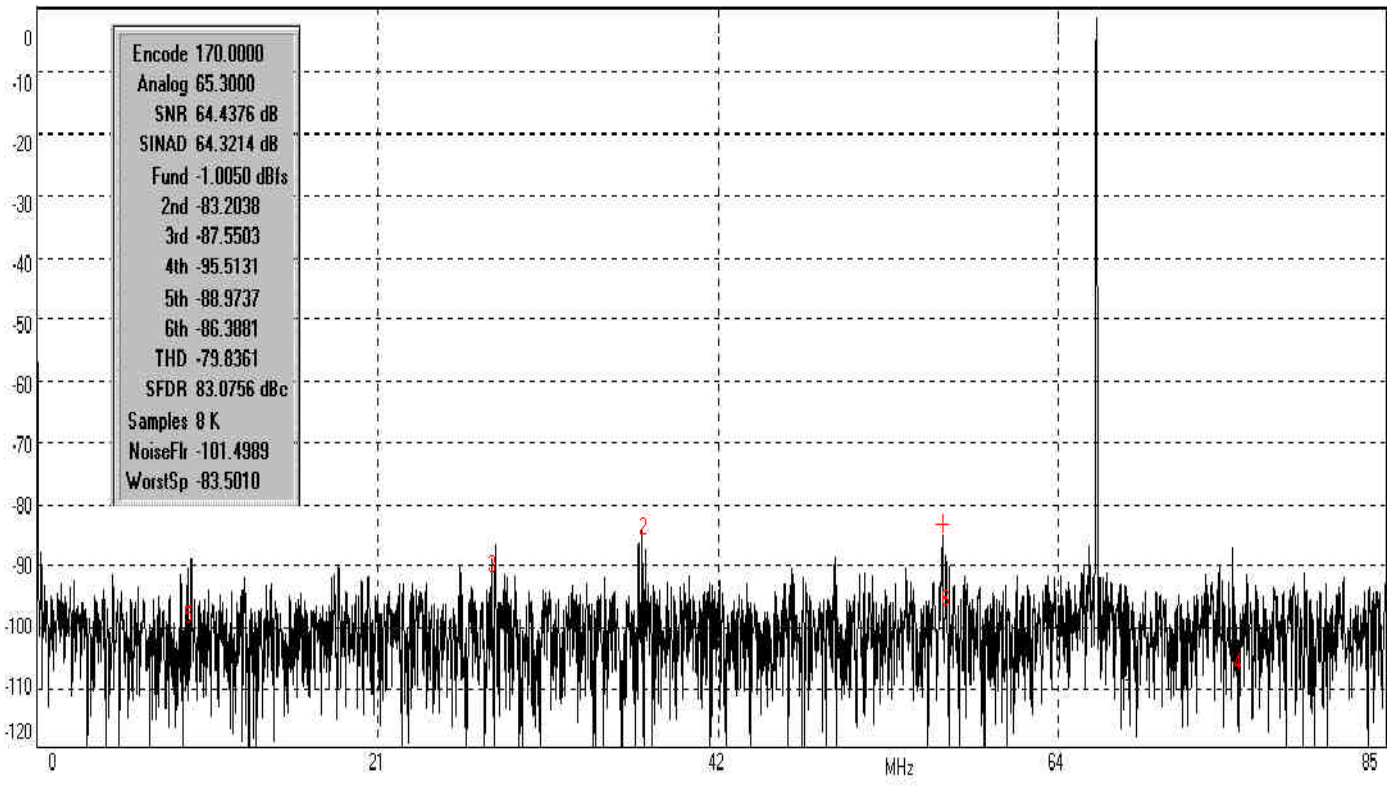
NOTES
[1] All AC specifications tested by driving ENCODE and $\overline{\text{ENCODE}}$ differentially, LVDS Mode.
2 DS inputs used in CMOS Mode only.

AD9430

SWITCHING SPECIFICATIONS (cont'd)

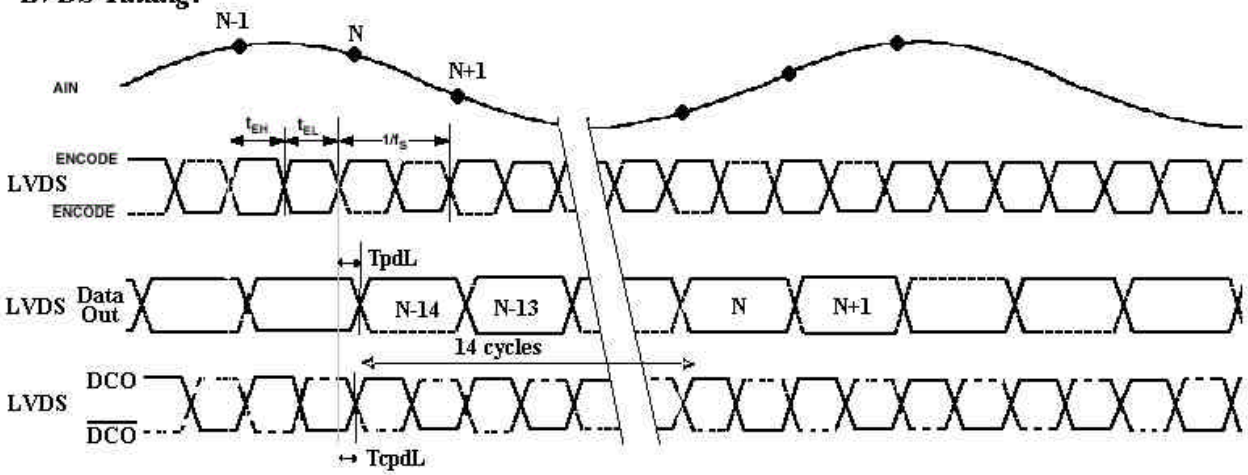
Parameter	Temp	Test Level	AD9430BSV-170 Min	Typ	Max	Units
OUTPUT Parameters in Demux Mode						
Valid Time (t_V)	Full	IV		tbd		ns
Propagation Delay (t_{PD})	Full	IV		3.8		ns
Rise Time (t_R) (20% to 80%)	25°C	V		1		ns
Fall Time (t_F) (20% to 80%)	25°C	V		1		ns
DCO Propagation Delay (t_{CPD})	Full	VI		3.8		ns
Data to DCO Skew ($t_{PD} - t_{CPD}$)	Full	IV		0		ns
Interleaved Mode (A, B Latency)	Full	VI		14/14		Cycles
Parallel Mode (A, B Latency)	Full	VI		14/15		Cycles
OUTPUT Parameters in LVDS Mode						
Valid Time (t_V)	Full	IV	2.0			ns
Propagation Delay (t_{PD})	Full	I		3.2	4.3	ns
Rise Time (t_R) (20% to 80%)	25°C	V		.5		ns
Fall Time (t_F) (20% to 80%)	25°C	V		.5		ns
DCO Propagation Delay (t_{CPD})	Full	VI	1.8	2.7	3.8	ns
Data to DCO Skew ($t_{PD} - t_{CPD}$)	Full	IV		.5		ns
Pipeline Latency	Full	VI		14		Cycles
Aperture Delay (t_A)	25°C	V		1.2		ps
Aperture Uncertainty (Jitter, t_J)	25°C	V		0.25		ps rms

Measured Preliminary Performance : FFT 65MHz Ain at 170MSPS

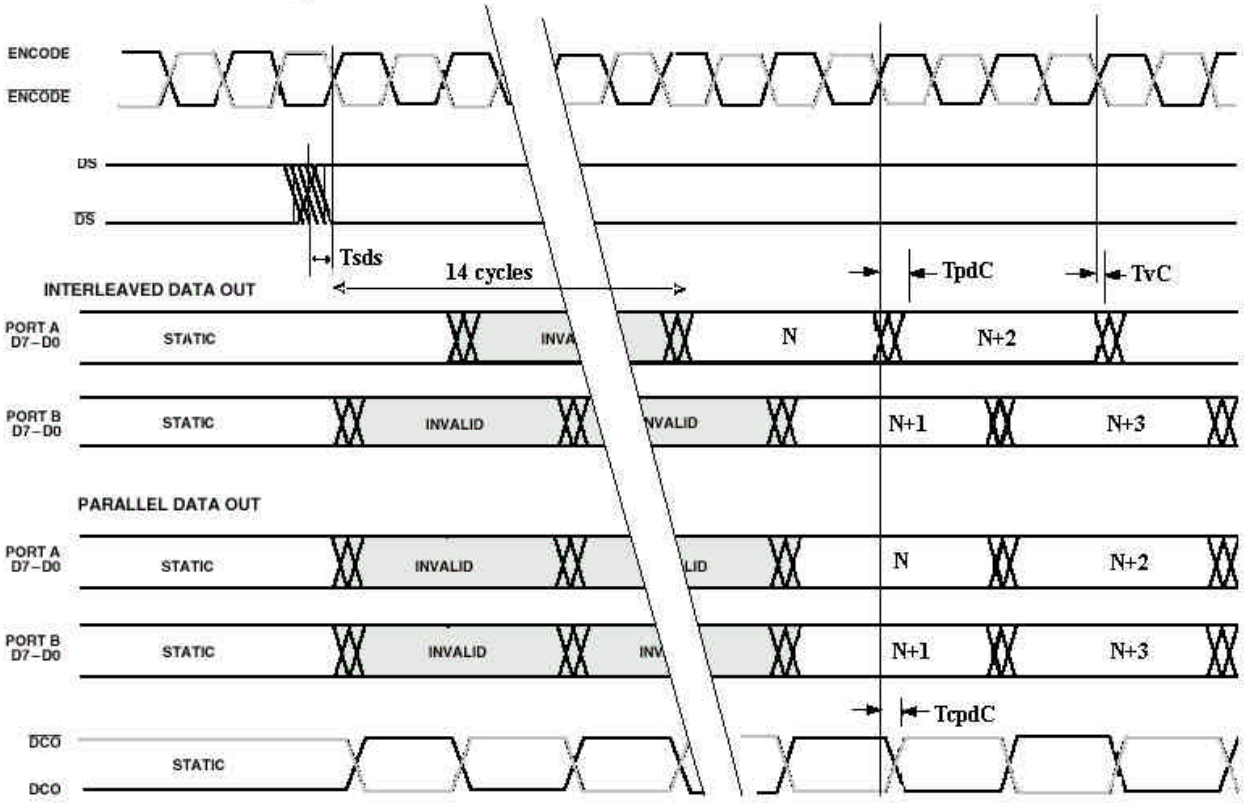


AD9430 Timing Diagram

LVDS Timing:



Dual Port CMOS Timing:



AD9430

ABSOLUTE MAXIMUM RATINGS

AVDD, DRVDD.. .. . . . . 4 V
Analog Inputs . . . . –0.5 V to AVDD + 0.5 V
Digital Inputs . . .. –0.5 V to DRVDD + 0.5 V
REFIN Inputs . . . . . .–0.5 V to AVDD + 0.5 V
Digital Output Current . . . . . 20 mA
Operating Temperature . . . . –55C to +125C
Storage Temperature . . . . –65C to +150C
Maximum Junction Temperature 150C
Maximum Case Temperature 150C
θ_{JA}[2] 25C/W, 32C/W

NOTES

1 Stresses above those listed under Absolute Maximum Ratings may cause
permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

2 Typical θ_{JA} = 32C/W (heat slug not soldered), Typical θ_{JA} = 25C/W (heat slug soldered), for multilayer board in still air.

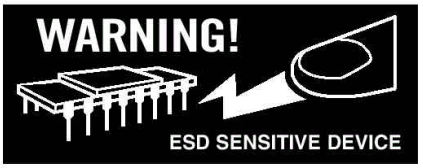
EXPLANATION OF TEST LEVELS

Test Level

I 100% production tested.
II 100% production tested at 25C and sample tested at specified temperatures.
III Sample tested only.
IV Parameter is guaranteed by design and characterization testing.
V Parameter is a typical value only.
VI 100% production tested at 25C; guaranteed by design and characterization testing for industrial temperature range; 100% production tested at temperature extremes for military devices.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9430 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



ORDERING GUIDE

Model	Temperature Range	Package Option
AD9430BSV-170	–40°C to +85°C	TQFP–100
AD9430/PCB-CMOS	+25°C	Evaluation Board (CMOS Mode)

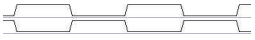
Table 1. AD9430 Output Select Coding

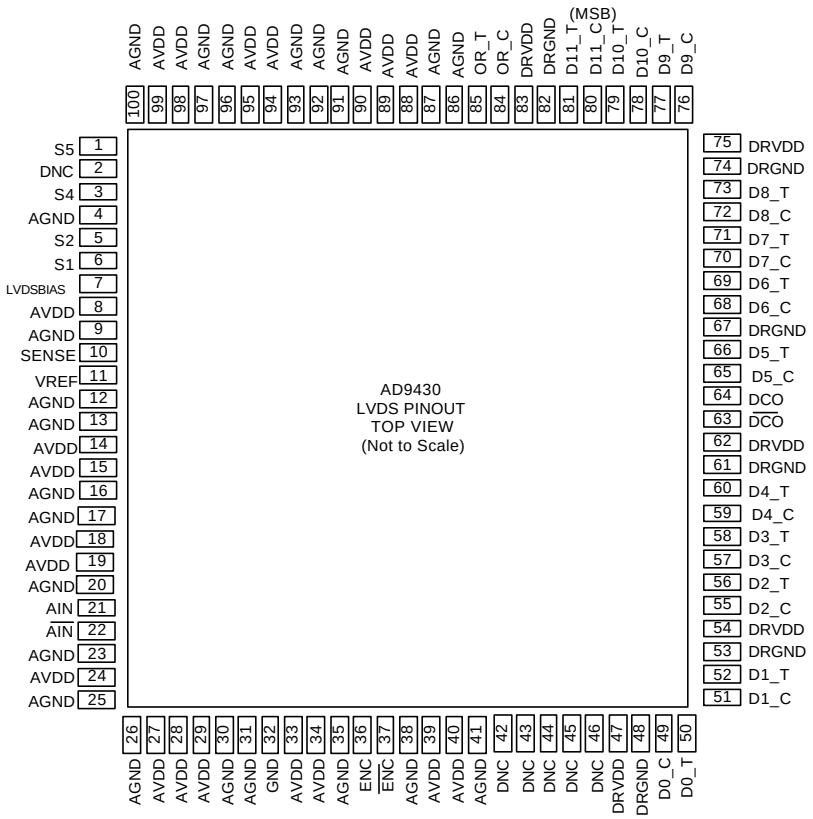
S1 (Data Format Select)[1]	S2 (LVDS/CMOS Output Mode Select)	S4 (Select Interleaved or Parallel Mode)[2]	S5 (Full Scale Adjust)	Mode
1	X	X	X	2's Complement
0	X	X	X	Offset Binary
X	0	1	X	Dual Mode CMOS Interleaved
X	0	0	X	Dual Mode CMOS Parallel
X	1	X	X	LVDS Mode
X	X	X	1	Full Scale -> .766 $V_{pp\ differential}$ 1.533 V_{pp} Single- Ended
X	X	X	0	Full Scale -> 1.533 $V_{pp\ differential}$

Notes:

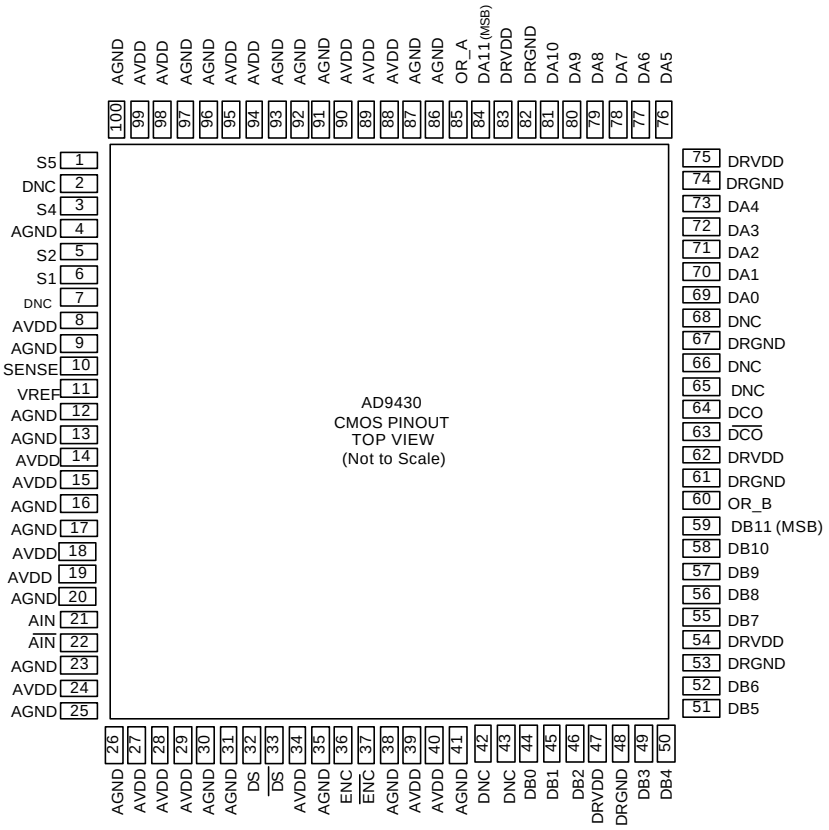
[1] *X = Don't Care*
S1-S5 all have 30K resistive pulldowns on chip

[2] *In interleaved mode output data on port A is offset from output data changes on port B by ½output clock cycle.*

Interleaved mode  *Parallel Mode* 



AD9430 LVDS Mode Pinout



AD9430 CMOS Dual Mode Pinout

PIN FUNCTION DESCRIPTIONS (CMOS mode)

CMOS Mode Pin Number	Name	Function in CMOS Mode
2,7,42,43,65,66,68	DNC	Do not connect
1	S5	Full Scale Adjust pin : '1' sets FS =.766 $V_{pp\ differential}$, '0' sets FS = 1.533 $V_{pp\ differential}$
3	S4	Interlaced or parallel output mode. (only in Dual Port mode operation) HIGH = data arrives in channel A at falling edge of clock and data arrives in channel A at rising edge of clock. LOW = data arrives in channels A and B at rising edge of clock.
5	S2	Output Mode select. Low = Dual Port, CMOS; High = LVDS
6	S1	Data format select. Low = Binary, High = Two's compliment
8,14,15,18,19,24,27,28,29,34, 39,40,88,89,90,94,95,98,99	AV_{DD}	3.3V analog supply. (3.0V to 3.6V)
4,9,12,13,16,17,20,23,25,26,3 0,31,35,38,41,86,87,91,92,93, 96,97,100	AGND	Analog Ground
10	SENSE	Control Pin for Reference , Full Scale
11	VREF	1.235 Reference I/O - function dependent on REFSENSE
21	VIN+	Analog input – true.
22	VIN-	Analog input – compliment.
32	DS+	Data sync (input) – true. Aligns output channels so that data from channel A represents a sample that is prior from data in channel B, taking into account the pipeline delay. (See timing diagram). Tie LOW if not used.
33	DS-	Data sync (input) – compliment. Tie HIGH if not used.
36	ENC+	Clock input – true.
37	ENC-	Clock input – compliment.
44	DB0	B Port Output Data Bit (LSB)
45	DB1	B Port Output Data Bit
46	DB2	B Port Output Data Bit
49	DB3	B Port Output Data Bit
50	DB4	B Port Output Data Bit
51	DB5	B Port Output Data Bit
52	DB6	B Port Output Data Bit
55	DB7	B Port Output Data Bit
56	DB8	B Port Output Data Bit
57	DB9	B Port Output Data Bit
58	DB10	B Port Output Data Bit
59	DB11	B Port Output Data Bit (MSB)
60	OR_B	B Port Overrange
48,53,61,67,74,82	DrGND	Digital ground.
47,54,62,75,83	DrV_{DD}	3.3V digital output supply. (3.0V to 3.6V)
63	DCO-	Data Clock output – compliment.
64	DCO+	Data Clock output – true.
69	DA0	A port Output Data Bit (LSB)
70	DA1	A port Output Data Bit
71	DA2	A port Output Data Bit
72	DA3	A port Output Data Bit
73	DA4	A port Output Data Bit
76	DA5	A port Output Data Bit
77	DA6	A port Output Data Bit
78	DA7	A port Output Data Bit
79	DA8	A port Output Data Bit
80	DA9	A port Output Data Bit
81	DA10	A port Output Data Bit
84	DA11	A port Output Data Bit (MSB)
85	OR_A	A port Overrange

PIN FUNCTION DESCRIPTIONS (LVDS mode)

LVDS Mode Pin Number	Name	Function in LVDS Mode
2,42,43,44,45,46	DNC	Do not connect
1	S5	Full Scale Adjust pin : '1' sets FS =.766 $V_{pp\ differential}$, '0' sets FS = 1.533 $V_{pp\ differential}$
3	S4	Interlaced or parallel output mode. (only in Dual Port mode operation) HIGH = data arrives in channel A at falling edge of clock and data arrives in channel A at rising edge of clock. LOW = data arrives in channels A and B at rising edge of clock.
5	S2	Output Mode select. Low = Dual Port, CMOS; High = LVDS
6	S1	Data format select. Low = Binary, High = Two's compliment
7	LVDSBIAS	Sets LVDS Output Current = 3.5mA (Place 3.7K RSET resistor from LVDSBIAS to ground)
8,14,15,18,19,24,27,28,29,34, 39,40,88,89,90,94,95,98,99	AV_{DD}	3.3V analog supply. (3.0V to 3.6V)
4,9,12,13,16,17,20,23,25,26,3 0,31,35,38,41,86,87,91,92,93, 96,97,100	AGND	Analog Ground
10	SENSE	Control Pin for Reference , Full Scale
11	VREF	1.235 Reference I/O - function dependent on REFSENSE
21	VIN+	Analog input – true.
22	VIN-	Analog input – compliment.
32	DS+	Data sync (input) – Not used in LVDS mode.Tie LOW .
33	DS-	Data sync (input) – compliment. Not used in LVDS mode.Tie HIGH.
36	ENC+	Clock input – true. (LVPECL levels)
37	ENC-	Clock input – compliment. (LVPECL levels)
47,54,62,75,83	DrV_{DD}	3.3V digital output supply.
48,53,61,67,74,82	DrGND	Digital ground.
49	D0_C	D0 complement output bit (LSB) (LVDS Levels)
50	D0_T	D0 true output bit (LSB) (LVDS Levels)
51	D1_C	D1 complement output bit (LVDS Levels)
52	D1_T	D1 true output bit (LVDS Levels)
55	D2_C	D2 complement output bit (LVDS Levels)
56	D2_T	D2 true output bit (LVDS Levels)
57	D3_C	D3 complement output bit (LVDS Levels)
58	D3_T	D3 true output bit (LVDS Levels)
59	D4_C	D4 complement output bit (LVDS Levels)
60	D4_T	D4 true output bit (LVDS Levels)
63	DCO-	Data Clock output – compliment. (LVDS Levels)
64	DCO+	Data Clock output – true. (LVDS Levels)
65	D5_C	D5 complement output bit (LVDS Levels)
66	D5_T	D5 true output bit (LVDS Levels)
68	D6_C	D6 complement output bit (LVDS Levels)
69	D6_T	D6 true output bit (LVDS Levels)
70	D7_C	D7 complement output bit (LVDS Levels)
71	D7_T	D7 true output bit (LVDS Levels)
72	D8_C	D8 complement output bit (LVDS Levels)
73	D8_T	D8 true output bit (LVDS Levels)
76	D9_C	D9 complement output bit (LVDS Levels)
77	D9_T	D9 true output bit (LVDS Levels)
78	D10_C	D10 complement output bit (LVDS Levels)
79	D10_T	D10 true output bit (LVDS Levels)
80	D11_C	D11 complement output bit (LVDS Levels) MSB
81	D11_T	D11 true output bit (LVDS Levels) MSB
84	OR_C	Overrange complement output bit (LVDS Levels)
85	OR_T	Overrange true output bit (LVDS Levels)

AD9430

TERMINOLOGY

Analog Bandwidth
The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Aperture Delay
The delay between the 50% point of the rising edge of the ENCODE command and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)
The sample-to-sample variation in aperture delay.

Crosstalk
Coupling onto one channel being driven by a low level (–40 dBFS) signal when the adjacent interfering channel is driven by a full-scale signal.

Differential Analog Input Resistance, Differential Analog Input Capacitance and Differential Analog Input Impedance
The real and complex impedances measured at each analog input port. The resistance is measured statically and the capacitance and differential input impedances are measured with a network analyzer.

Differential Analog Input Voltage Range
The peak-to-peak differential voltage that must be applied to the converter to generate a full-scale response. Peak differential voltage is computed by observing the voltage on a single pin and subtracting the voltage from the other pin, which is 180 degrees out of phase. Peak-to-peak differential is computed by rotating the inputs phase 180 degrees and again taking the peak measurement. The difference is then computed between both peak measurements.

Differential Nonlinearity
The deviation of any code width from an ideal 1 LSB step.

Effective Number of Bits
The effective number of bits (ENOB) is calculated from the measured SNR based on the equation:

$$ENOB = \frac{SNR_{MEASURED} - 1.76dB}{6.02}$$

ENCODE Pulsewidth / Duty Cycle
Pulsewidth high is the minimum amount of time that the ENCODE pulse should be left in Logic 1 state to achieve rated performance; pulsewidth low is the minimum time ENCODE pulse should be left in low state. See timing implications of changing t_{ENCH} in text. At a given clock rate, these specifica-tions define an acceptable ENCODE duty cycle.

Full-Scale Input Power
Expressed in dBm. Computed using the following equation:

$$Power_{Fullscale} = 10\log\left(\frac{\frac{V^2_{Fullscale_{rms}}}{Z_{Input}}}{.001}\right)$$

Gain Error
Gain error is the difference between the measured and ideal full scale input voltage range of the ADC.

Harmonic Distortion, Second
The ratio of the rms signal amplitude to the rms value of the second harmonic component, repo rted in dBc.

Harmonic Distortion, Third
The ratio of the rms signal amplitude to the rms value of the third harmonic component, reported in dBc.

Integral Nonlinearity
The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a “best straight line” determined by a least square curve fit.

Minimum Conversion Rate
The encode rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

Maximum Conversion Rate
The encode rate at which parametric testing is performed.

Output Propagation Delay
The delay between a differential crossing of ENCODE and ENCODE and the time when all output data bits are within valid logic levels.

Noise (for Any Range within the ADC)

$$V_{noise} = \sqrt{Z * .001 * 10^{\left(\frac{FS_{dBm} - SNR_{dBc} - Signal_{dBFS}}{10}\right)}}$$

Where *Z* is the input impedance, *FS* is the full scale of the device for the frequency in question, *SNR* is the value for the particular input level, and *Signal* is the signal level within the ADC reported in dB below full scale. This value includes both thermal and quantization noise.

Power Supply Rejection Ratio
The ratio of a change in input offset voltage to a change in power supply voltage.

Signal-to-Noise-and-Distortion (SINAD)
The ratio of the rms signal amplitude (set 1 dB below full scale) to the rms value of the sum of all other spectral components, including harmonics but excluding dc.

Signal -to-Noise Ratio (without Harmonics)
The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, excluding the first five harmonics and dc.

Spurious-Free Dynamic Range (SFDR)
The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic. May be reported in dBc (i.e., degrades as signal level is lowered), or dBFS (always related back to converter full scale).

Two-Tone Intermodulation Distortion Rejection
The ratio of the rms value of either input tone to the rms value of the worst third order intermodulation product; reported in dBc.

Two-Tone SFDR
The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product. May be reported in dBc (i.e., degrades as signal level is lowered), or in dBFS (always related back to converter full scale).

Worst Other Spur
The ratio of the rms signal amplitude to the rms value of the worst spurious component (excluding the second and third harmonic) reported in dBc.

Transient Response Time
Transient response is defined as the time it takes for the ADC to reacquire the analog input after a transient from 10% above negative full scale to 10% below positive full scale.

Out-of-Range Recovery Time
Out of range recovery time is the time it takes for the ADC to reacquire the analog input after a transient from 10% above positive full scale to 10% above negative full scale, or from 10% below negative full scale to 10% below positive full scale.

EQUIVALENT CIRCUITS

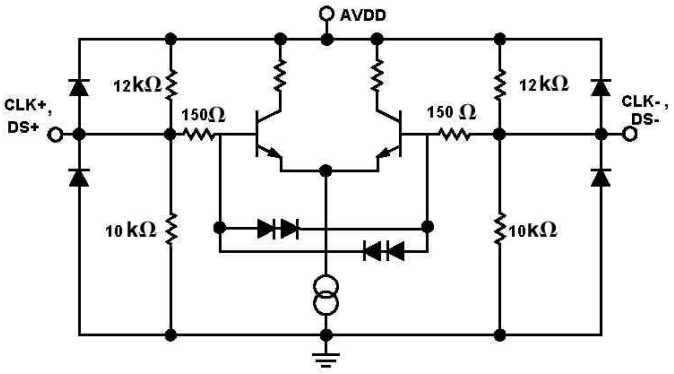


Figure X *Encode and DS Inputs*

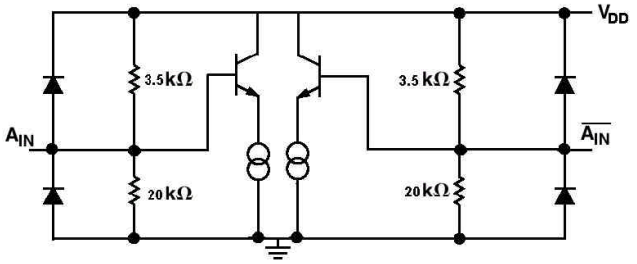


Figure X *Analog Inputs*

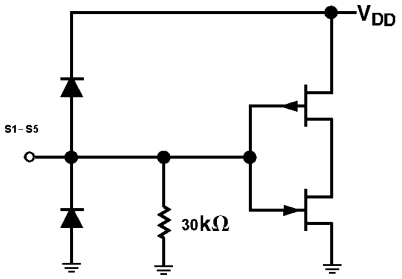


Figure X *S1-S5 Inputs*

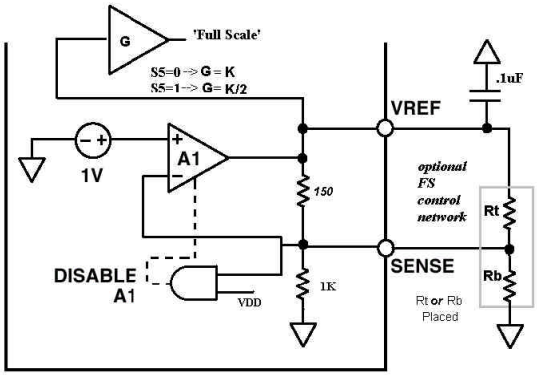


Figure X *VREF, SENSE I/O*

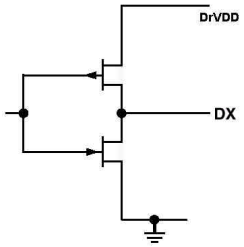


Figure X *Data Outputs (CMOS Mode)*

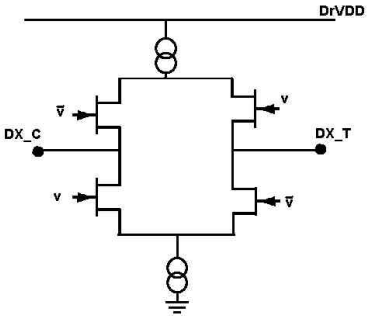


Figure X *Data Outputs (LVDS Mode)*

AD9430

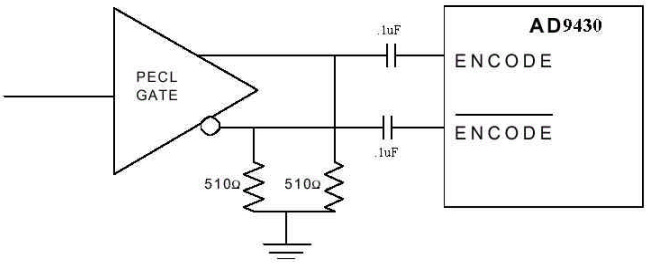
APPLICATION NOTES
THEORY OF OPERATION

The AD9430 architecture is optimized for high speed and ease of use. The analog inputs drive an integrated high bandwidth track-and-hold circuit that samples the signal prior to quantization by the 12-bit core. For ease of use the part includes an onboard reference and input logic that accepts TTL, CMOS, or LVPECL levels. The digital outputs logic levels are user selectable as standard 3V CMOS or LVDS (ANSI-644 compatible) via pin S2.

USING THE AD9430
ENCODE Input

Any high speed A/D converter is extremely sensitive to the quality of the sampling clock provided by the user. A track/hold circuit is essentially a mixer, and any noise, distortion, or timing jitter on the clock will be combined with the desired signal at the A/D output. For that reason, considerable care has been taken in the design of the ENCODE input of the AD9430, and the user is advised to give commensurate thought to the clock source.

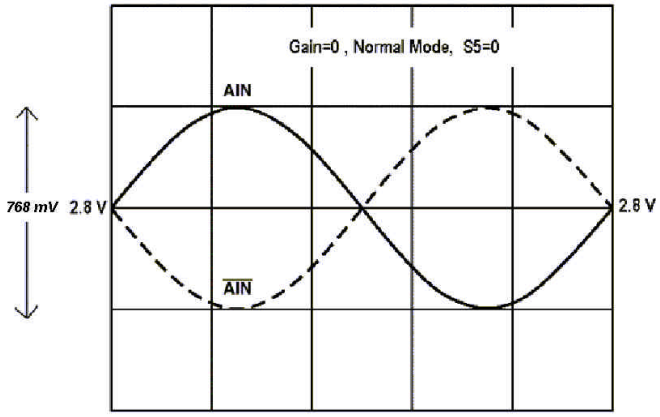
The AD9430 has an internal clock duty cycle stabilization circuit that locks to the rising edge of ENCODE (falling edge of ENCODE if driven differentially), and optimizes timing internally. This allows for a wide range of input duty cycles at the input without degrading performance. Jitter in the rising edge of the input is still of paramount concern, and is not reduced by the internal stabilization circuit. This circuit is always on, and cannot be disabled by the user. The ENCODE and ENCODE inputs are internally biased to 1.5V (nominal), and support either differential or single–ended signals. For best dynamic performance, a differential signal is recommended. Good performance is obtained using an MC10EL16 in the circuit to drive the encode inputs , as illustrated in figure below.



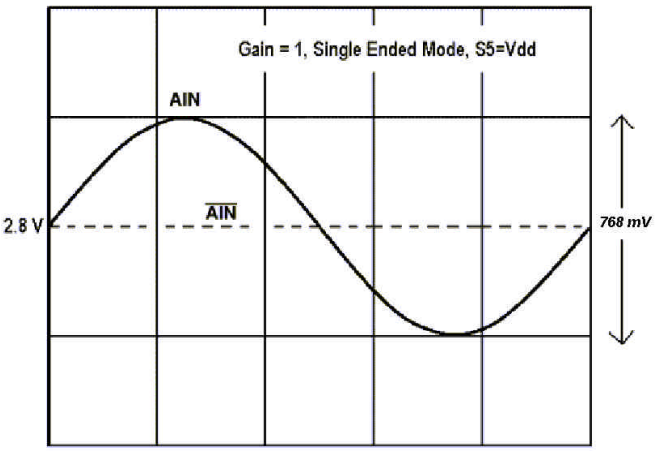
Driving Encode with EL16

Analog Input

The analog input to the AD9430 is a differential buffer. For best dynamic performance, impedances at AIN and $\overline{AIN}$ should match. The analog input has been optimized to provide superior wideband performance and requires that the analog inputs be driven differentially. SNR and SINAD performance will degrade significantly (~6dB) if the analog input is driven with a single-ended signal. A wideband transformer such as Minicircuits ADT1-1WT can be used to provide the differential analog inputs for applications that require a single-ended-to-differential conversion. Both analog inputs are self-biased by an on-chip resistor divider to a nominal 2.8 V. (See Equivalent Circuits section TBD.)
Special care was taken in the design of the Analog Input section of the AD9430 to prevent damage and corruption of data when the input is overdriven. The nominal input range is 1.5 V diff p-p. The nominal differential input range is 768 mV p-p × 2.



Differential Analog Input Range



Single Ended Analog Input Range

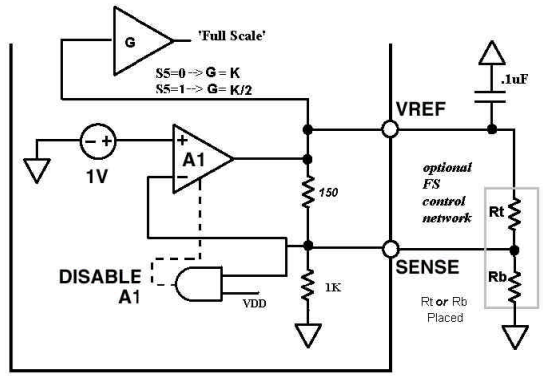
Digital Outputs
The off chip drivers on the chip can be configured by the user to provide CMOS or LVDS compatible output levels via pin S2.

The CMOS digital outputs (*S2=0*) are TTL/CMOS-compatible for lower power consumption. The outputs are biased from a separate supply (VDD), allowing easy interface to external logic. The outputs are CMOS devices which will swing from ground to VDD (with no dc load). It is recommended to minimize the capacitive load the ADC drives by keeping the output traces short (<1 inch, for a total C_{LOAD} < 5 pF). When operating in cmos mode it is also recommended to place low value (220 ohm) series damping resistors on the data lines to reduce switching transient effects on performance.

LVDS outputs are available when S2=VDD and a 3.7K RSET resistor is placed at pin 7 (*LVDSBIAS*) to ground . This resistor sets the output current at each output equal to a nominal 3.5mA (10* I_{RSET}) . A 100 ohm differential termination resistor placed at the lvds receiver inputs results in a nominal 350mV voltage swing at the receiver. Note that when operating in LVDS mode the output supply must be at a dc potential greater than or equal to the analog supply level (AVDD). This can be accomplished simply by biasing the two supplies from the same power plane or by tying the two supplies on the pcb through an inductor. When operating in CMOS mode this is not required and separate supplies are recommended.

Clock Outputs (DCO+, DCO-)
The input ENCODE is divided by two (in CMOS mode) and available off-chip at DCO+ and DCO-. These clocks can facilitate latching off-chip, providing a low skew clocking solution (see timing diagram). The on-chip clock buffers should not drive more than 5 pF of capacitance to limit switching transient effects on performance.
Note that the Outputs clocks are CMOS levels when CMOS mode is selected(S2=0) and are LVDS levels when in LVDS mode(S2=VDD). (Requiring a 100ohm differential termination at receiver in LVDS mode). The output clock in LVDS mode switches at the encode rate.

Voltage Reference
A stable and accurate 1.25 V voltage reference is built into the AD9430 (VREF). The analog input Full Scale Range is linearly proportional to the voltage at VREF. VREF (*and in turn input full scale*) can be varied by adding an external resistor network at VREF, SENSE and GROUND. (See figure X) . No appreciable degradation in performance occurs when VREF is adjusted ±5%. Note that an external reference can be used by connecting the SENSE pin to VDD (disabling internal reference) and driving VREF with the external reference source. A .1uF capacitor to ground is recommended at VREF pin in internal and external reference applications.



Simplified Voltage Reference Equivalent Circuit

AD9430 EVALUATION BOARD

The AD9430 evaluation board offers an easy way to test the AD9430. It requires a clock source, an analog input signal, and a 3.3 V power supply. The clock source is buffered on the board to provide the clocks for the ADC, an on-board DAC, latches, and a data ready signal. The digital outputs and output clocks are available at two 40-pin connectors, P3 and P4. The board has several different modes of operation, and is shipped in the following configuration:

- Offset Binary
- Internal Voltage Reference
- CMOS Parallel Timing
- Full-Scale Adjust = Low

Power Connector

Power is supplied to the board via a detachable 12-lead power strip (three 4-pin blocks).

Table II. Power Connector

AVDD 3.3 V	Analog Supply for ADC (~ 350 mA)
DRVDD 3.3 V	Output Supply for ADC (~ 28 mA)
VDL 3.3 V	Supply for Support Logic and DAC (~350 mA)
EXT_VREF*	Optional External Reference Input
VCLK/V_XTAL	Supply for Clock Buffer/Optional XTAL
VAMP	Supply for Optional Amp

*LVEL16 clock buffer can be powered from AVDD or VCLK at E47 jumper (AVDD, DrVDD,VDL are the minimum required power connections).

Analog Inputs

The evaluation board accepts a 1.3 V p-p analog input signal centered at ground at SMB connector J4. This signal is terminated to ground through 50 Ω by R16. The input can be alternatively terminated at T1 transformer secondary by R13, R14. T1 is a wideband RF transformer providing the single-ended to differential conversion allowing the ADC to be driven differentially, minimizing even order harmonics. An optional second transformer T2 can be placed following T1 if desired. This would provide some performance advantage (~1–2 dB) for high analog input frequencies (>100 MHz). If T2 is placed, two shorting traces at the pads would need to be cut. The analog signal is low pass filtered by R41, C12, and R42, C13 at the ADC input.

Gain

Full scale is set at E17–E19, E17–E18 sets S5 low, full scale = 1.5 V differential; E17–E19 sets S5 high, full scale = 0.75 V differential.

Encode

The encode clock is terminated to ground through 50 Ω at SMB connector J5. The input is ac-coupled to a high-speed differential receiver (LVEL16) which provides the required low-jitter, fast edge rates needed for optimum performance. J5 input should be > 0.5 V p-p. Power to the EL16 is set at jumper E47. E47–E45 powers the buffer from AVDD, E47–E46 powers the buffer from VCLK/V_XTAL.

Voltage Reference

The AD9430 has an internal 1.23 V voltage reference. The ADC uses the internal reference as the default when jumpers E24–E27 and E25–E26 are left open. The full scale can be increased by placing optional resistor R3. The required value would vary with process and needs to be tuned for the specific application. Full scale can similarly be reduced by placing R4; tuning would be required here as well. An external reference can be used by shorting the SENSE pin to 3.3 V (place jumper E26–E25). E27–E24 jumper connects the ADC VREF pin to EXT_VREF pin at the power connector.

Data Format Select

Data Format Select sets the output data format of the ADC. Setting DFS (E1–E2) low sets the output format to be offset binary; setting DFS high (E1–E3) sets the output to two's complement.

I/P

Output timing is set at E11–E13. E12–E11 sets S4 low for parallel output timing mode. E11–E13 sets S4 high for interleaved timing mode.

Timing Controls

Flexibility in latch clocking and output timing is accomplished by allowing for clock inversion at the timing controls section of the PCB. Each buffered clock is buffered by an XOR and can be inverted by moving the appropriate jumper for that clock.

Data Outputs

The ADC digital outputs are latched on the board by four LVT574s; the latch outputs are available at the two 40-pin connectors at pins 11–33 on P23 (channel A) and pins 11–33 on P3 (channel B). The latch output clocks (data ready) are available at Pin 37 on P23 (channel A) and Pin 37 on P3 (channel B). The data ready clocks can be inverted at the timing controls section if needed.

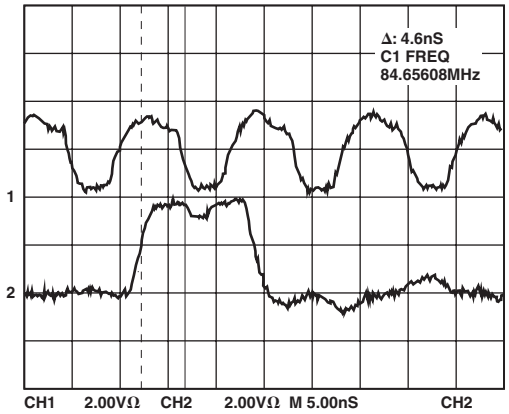


Figure 13. Data Output and Clock @ 80-Pin Connector

DAC Outputs

Each channel is reconstructed by an on-board dual-channel DAC, an AD9753. This DAC is intended to assist in debug—it should not be used to measure the performance of the ADC. It is a current output DAC with on-board 50 Ω termination resistors. The figure below is representative of the DAC output with a full-scale analog input. The scope setting is low bandwidth.

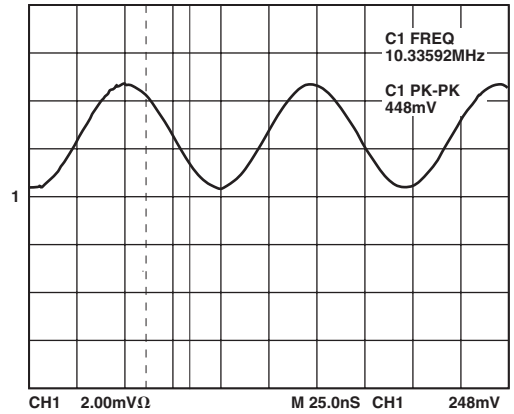


Figure 14. DAC Output

Encode Xtal

An optional xtal oscillator can be placed on the board to serve as a clock source for the PCB. Power to the xtal is through the VCLK/VXTAL pin at the power connector. If an oscillator is used, ensure proper termination for best results. The board has been tested with a Valpey Fisher VF561 and a Vectron JN00158-163.84. Test results for the VF561 are shown below.

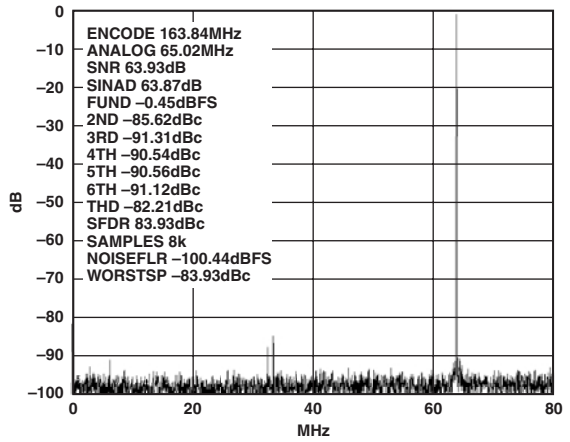


Figure 15. FFT—Using VF561 XTAL as Clock Source

Optional Amplifier

The footprint for transformer T2 can be modified to accept a wideband differential amplifier (AD8350) for low frequency applications where gain is required. Note that Pin 2 would need to be lifted and left floating for operation. Input transformer T1 would need to be modified to a 4:1 for impedance matching and ADC input filtering would enhance performance (see AD8350 data sheet). SNR/SINAD Performance of 61 dB/60 dB is possible and would start to degrade at about 30 MHz.

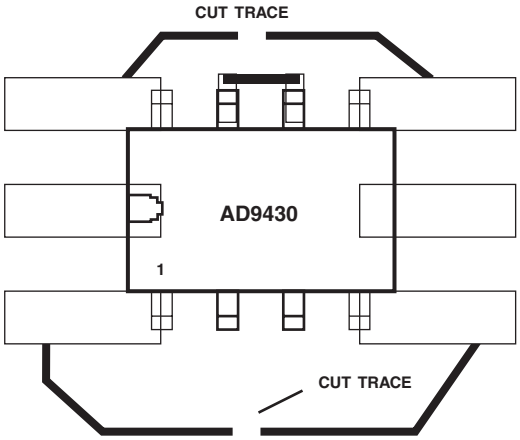


Figure 16. Using the AD8350 on the AD9430 PCB

Table III. Evaluation Board Bill of Materials

No.	Qty.	Reference Designator	Device	Package	Value	Comments
1	45	C1, C3–C11, C15–C17, C19–C29, C31–C48, C58–C62	Capacitor	0603	0.1 µF	C43, C47 Not Placed
2	0	C2	Capacitor	0603	10 pF	Not Placed
3	0	C12, C13	Capacitor	0603	20 pF	Not Placed
4	1	C14	Capacitor	0603	0.01 µF	
5	0	C18	Capacitor	0603	1 µF	
6	7	C30, C49, C63–C67	Capacitor	CAPL	10 µF	C30 Not Placed
7	9	E3–E1–E2 E19–E17–E18 E13–E11–E12 E26–E25–E27–E24 E46–E47–E45 E35–E33–E34 E32–E30–E31 E29–E23–E28 E22–E16–E21	3-Pin Header/Jumper 3-Pin Header/Jumper 3-Pin Header/Jumper 4-Pin Header 3-Pin Header/Jumper 3-Pin Header/Jumper 3-Pin Header/Jumper 3-Pin Header/Jumper 3-Pin Header/Jumper			
8	5	J1, J2, J3, J4, J5, J6	SMB	SMB		J1 Not Placed
9	2	P3, P23	40-Pin Header			
10	3	P4, P21, P22	4-Pin Power Connector	Post Detachable Connector	25.531.3425.0 25.602.5453.0	Wieland Wieland
11	8	R1, R5, R13, R14, R16, R25, R27, R28, R41, R42	Resistor	0603	50 Ω	R1, R13, R14 Not Placed
12	1	R2, R3, R4	Resistor	0603	3.9 kΩ	R3, R4 Not Placed
13	8	R6–R8, R10, R15, R21–R24, R33–R36, R38	Resistor	0603	100 Ω	R15, R21–R24, R38 Not Placed
14	5	R12, R30, R37	Resistor	0603	0 Ω	
15	4	R17, R18, R19, R20	Resistor	0603	510 Ω	
16	1	R26	Resistor	0603	2 kΩ	
17	1	R29	Resistor	0603	390 Ω	
18	7	R31, R32, R39, R40, R43, R44, R45	Resistor	0603	1 kΩ	
19	4	RZ1, RZ2, RZ3, RZ4	Resistor Pack 220 Ω	SO16RES	742C163221JTR	CTS
20	8	RZ5, RZ6, RZ7, RZ8, RZ9, RZ10, RZ11, RZ12	Resistor Pack 22 Ω	SO16RES	742C163220JTR	CTS
21	1	T1, T2	Transformer	CD542	Minicircuits ADT1–1WT	T2 Not Placed
22	1	U1	AD9430BSV	TQFP100	ADC	
23	1	U2	MC100LVEL16D	SO8NB	Clock Buffer	
24	1	U3	74LCX86	SO14NB	Xor/Buffer	
25	4	U4, U5, U6, U7	74LVT574	SO20	Latch	
26	1	U9	AD9753AST	LQFP48	DAC	

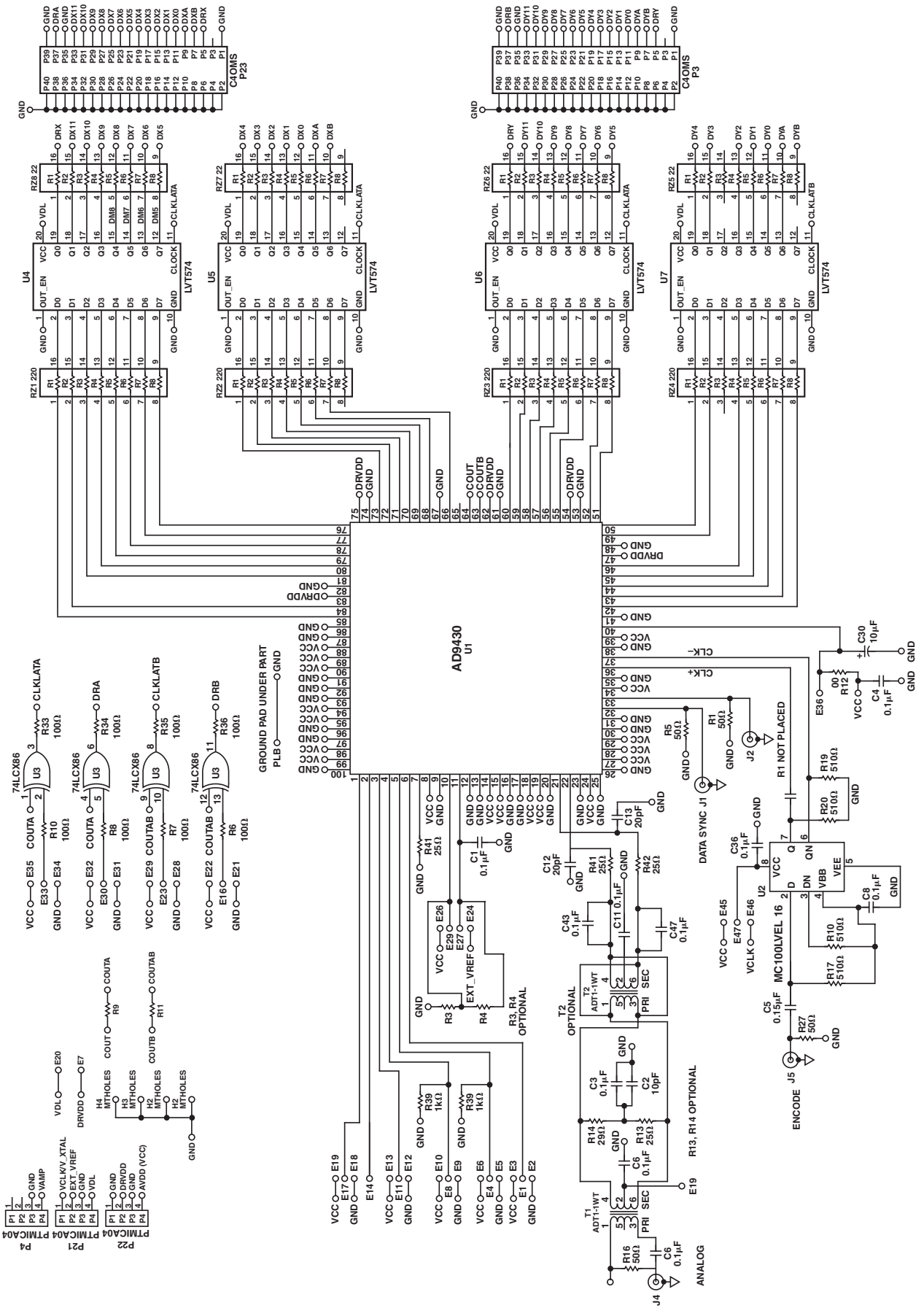


Figure 17a. Evaluation Board Schematic

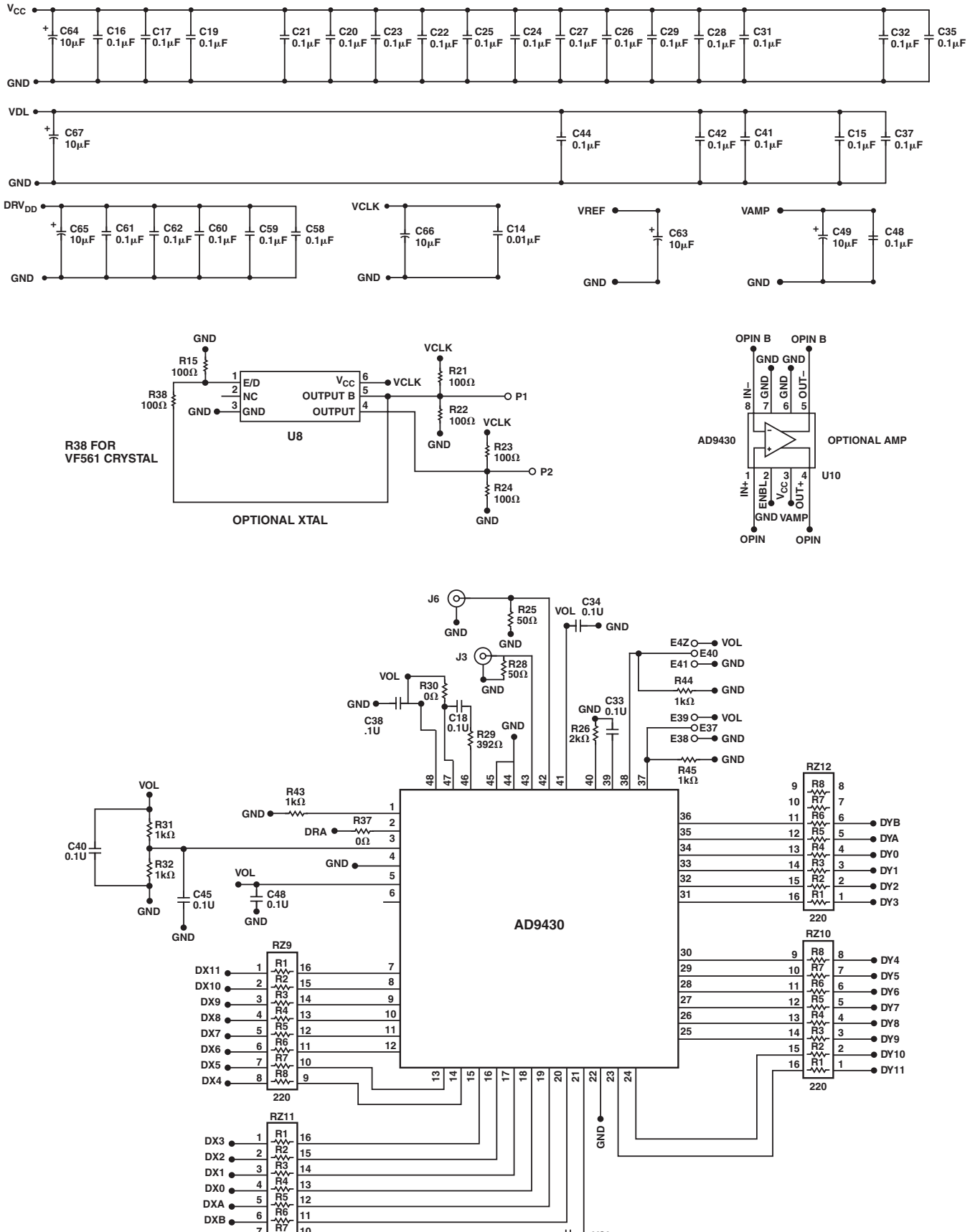


Figure 17b. Evaluation Board Schematic

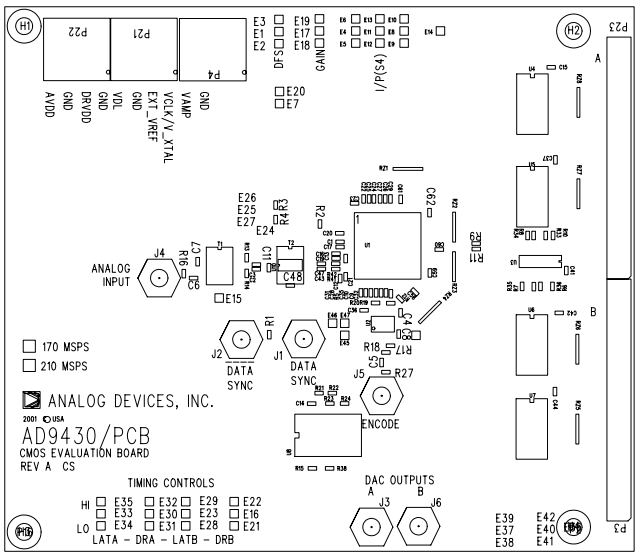


Figure 18. PCB Top Side Silkscreen

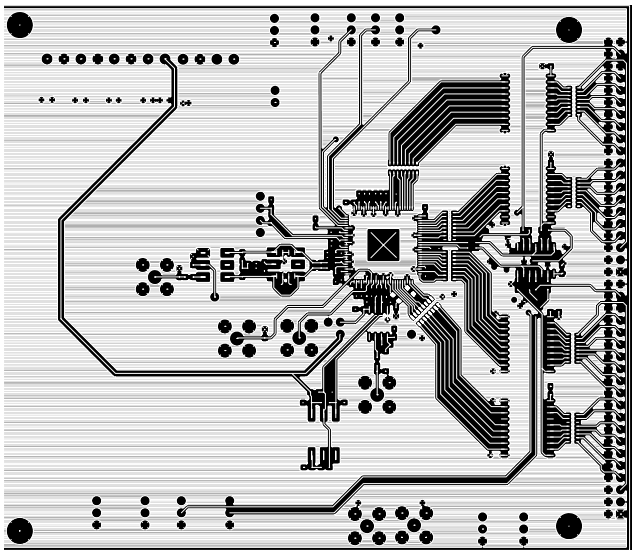


Figure 19. PCB Top Side Copper

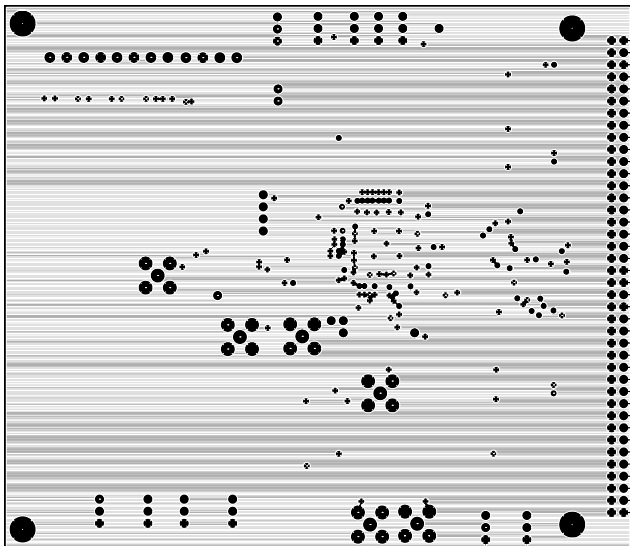


Figure 20. PCB Ground Layer

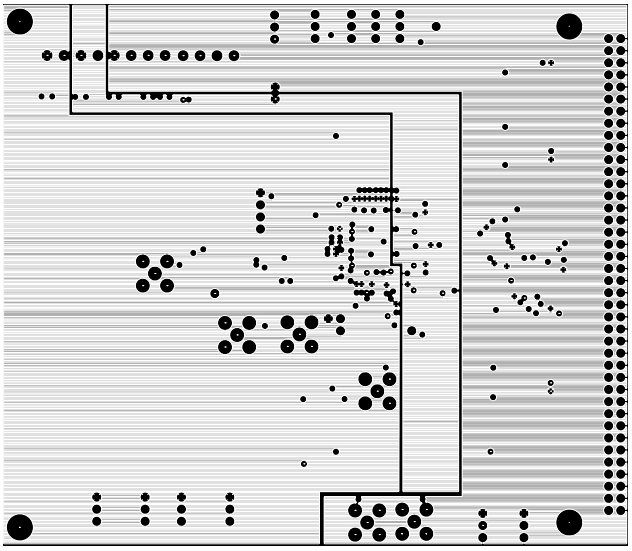


Figure 21. PCB Split Power Plane

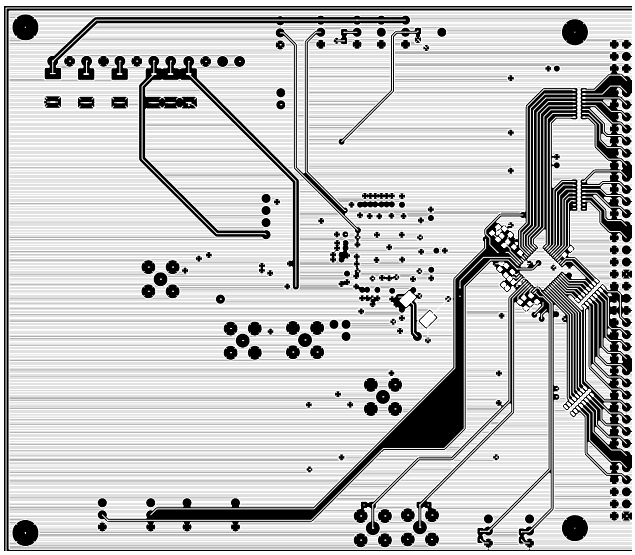


Figure 22. PCB Bottom Side Copper

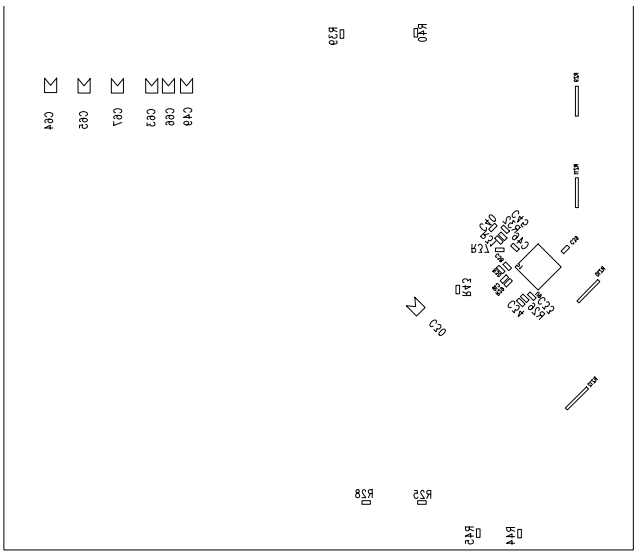


Figure 23. PCB Bottom Side Silkscreen

Troubleshooting

If the board does not seem to be working correctly, try the following:

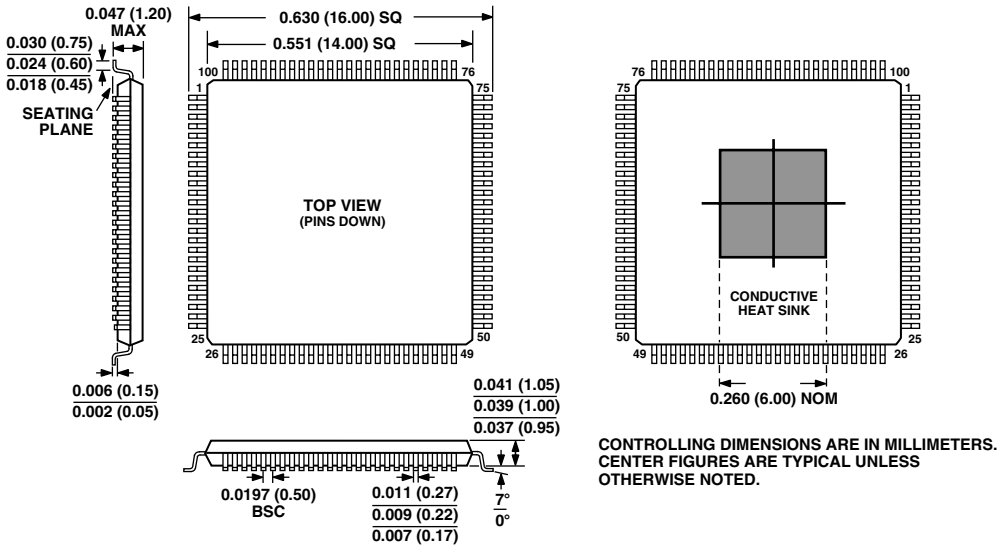
- Verify power at IC pins.
- Check that all jumpers are in the correct position for the desired mode of operation.
- Verify VREF is at 1.23 V.
- Try running Encode Clock and Analog Inputs at low speeds (10 MSPS/1 MHz) and monitor 574, DAC, and ADC outputs for toggling.

The AD9430 Evaluation Board is provided as a design example for customers of Analog Devices, Inc. ADI makes no warranties, express, statutory, or implied, regarding merchantability or fitness for a particular purpose.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

100-Lead TQFP (with Exposed Heat Sink) (TQFP-100)



CONTROLLING DIMENSIONS ARE IN MILLIMETERS. CENTER FIGURES ARE TYPICAL UNLESS OTHERWISE NOTED.

NOTE:
THE AD9430 HAS A CONDUCTIVE HEAT SLUG TO HELP DISSIPATE HEAT AND ENSURE RELIABLE OPERATION OF THE DEVICE OVER THE FULL INDUSTRIAL TEMPERATURE RANGE. THE SLUG IS EXPOSED ON THE BOTTOM OF THE PACKAGE AND ELECTRICALLY CONNECTED TO CHIP GROUND. IT IS RECOMMENDED THAT NO PCB SIGNAL TRACES OR VIAS BE LOCATED UNDER THE PACKAGE THAT COULD COME IN CONTACT WITH THE CONDUCTIVE SLUG. ATTACHING THE SLUG TO A GROUND PLANE WILL REDUCE THE JUNCTION TEMPERATURE OF THE DEVICE WHICH MAY BE BENEFICIAL IN HIGH TEMPERATURE ENVIRONMENTS.