a

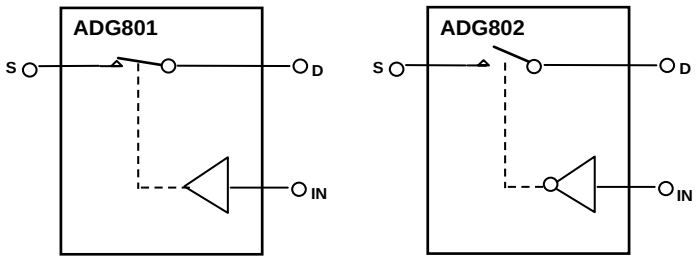
<0.5 Ω CMOS, Low Voltage, SPST Switches

ADG801/ADG802

FEATURES
Low On Resistance < 0.5 Ω max at 5 V supply
0.1 Ω On Resistance Flatness
+1.8 V to +5.5 V Single Supply
100pA Leakage Currents
14ns Switching Times
Extended Temperature Range -40°C to +125°C
High Current Carrying Capability
Tiny 6 lead SOT23 and 8 Lead µSOIC Packages
Low Power Consumption
TTL/CMOS Compatible Inputs
Pin Compatible with ADG701/ADG702

APPLICATIONS
Power Routing
Audio and Video Signal Routing
Cellular Phones
Modems
PCMCIA Cards
Hard Drives
Data Acquisition Systems
Communication Systems
Relay replacement
Audio and Video Switching
Battery Powered Systems

FUNCTIONAL BLOCK DIAGRAMS



SWITCHES SHOWN FOR A LOGIC "1" INPUT

GENERAL DESCRIPTION

The ADG801/ADG802 are monolithic CMOS SPST (Single Pole, Single Throw) switches with On Resistance of less than 0.5Ω. These switches are designed on an advanced submicron process that provides extremely low on resistance, high switching speed and low leakage currents.

The low On Resistance of <0.5Ω means these parts are ideal for applications where low on resistance switching is critical.

The ADG801 is a normally open (NO) switch, while the ADG802 is normally closed (NC). Each switch conducts equally well in both directions when ON.

The ADG801 and ADG802 are available in 6-lead SOT-23 and 8 Lead µSOIC packages.

PRODUCT HIGHLIGHTS

1. Low On Resistance (0.25 Ω typical).
2. +1.8V to +5.5V Single Supply Operation.
3. Tiny 6 Lead SOT23 and 8 Lead µSOIC Packages.
4. Pin Compatible with ADG701 (ADG801)
   Pin Compatible with ADG702 (ADG802).

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ADG801/ADG802–SPECIFICATIONS[1]

(V_{DD} = 5 V ±10%, V_{SS} = GND = 0 V. All specifications –40°C to +125°C unless otherwise noted.)

Parameter	+25°C	–40°C to +85°C	–40°C to +125°C	Units	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance (R_{ON})	0.25			Ω typ	V_S = 0 V to V_{DD}, I_S = –10 mA;
	0.4	0.5	0.75	Ω max	Test Circuit 1
On-Resistance Flatness ($R_{FLAT(ON)}$)	0.05			Ω typ	V_S = 0 V to V_{DD}, I_S = –10 mA
		0.1	0.2	Ω max	
LEAKAGE CURRENTS					V_{DD} = +5.5 V
Source OFF Leakage I_S (OFF)	±0.01			nA typ	V_S = 4.5 V/1 V, V_D = 1 V/4.5 V;
	±0.5	±1	tbd	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.01			nA typ	V_S = 4.5 V/1 V, V_D = 1 V/4.5 V;
	±0.5	±1	tbd	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.01			nA typ	V_S = V_D = 1 V, or 4.5 V;
	±0.5	±1	tbd	nA max	Test Circuit 3
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.4	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current					
I_{INL} or I_{INH}	0.005			µA typ	V_{IN} = V_{INL} or V_{INH}
			±0.1	µA max	
C_{IN}, Digital Input Capacitance	5			pF typ	
DYNAMIC CHARACTERISTICS[2]					
t_{ON}	30			ns typ	R_L = 50 Ω, C_L = 35 pF
	TBD		TBD	ns max	V_S = 3 V; Test Circuit 4
t_{OFF}	20			ns typ	R_L = 50 Ω, C_L = 35 pF
	TBD		TBD	ns max	V_S = 3 V; Test Circuit 4
Charge Injection	±20			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF, Test Circuit 5
Off Isolation	–65			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, Test Circuit 6
Bandwidth –3 dB	30			MHz typ	R_L = 50 Ω, C_L = 5 pF, Test Circuit 7
C_S (OFF)	55			pF typ	f = 1 MHz
C_D (OFF)	55			pF typ	f = 1 MHz
C_D, C_S (ON)	110			pF typ	f = 1 MHz
POWER REQUIREMENTS					V_{DD} = +5.5 V
I_{DD}	0.001			µA typ	Digital Inputs = 0 V or 5.5 V
			1.0	µA max	

NOTES

[1]Temperature ranges are as follows: Extended Temperature Range: –40°C to +125°C.

[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

SPECIFICATIONS[1] (V_{DD} = 2.7 V to 3.6 V, V_{SS} = GND = 0 V. All specifications –40°C to +125°C unless otherwise noted.)

Parameter	+25°C	–40°C to +85°C	–40°C to +125°C	Units	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance (R_{ON})	0.3		1	Ω typ	V_S = 0 V to V_{DD}, I_S = –10 mA;
	0.7	0.8		Ω max	Test Circuit 1
On-Resistance Flatness($R_{FLAT(ON)}$)	0.1		0.3	Ω typ	V_S = 0 V to V_{DD}, I_S = –10 mA
LEAKAGE CURRENTS					V_{DD} = +3.3 V
Source OFF Leakage I_S (OFF)	±0.01			nA typ	V_S = 3 V/1 V, V_D = 1 V/3 V;
	±0.5	±0.1	tbd	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.01			nA typ	V_S = 3 V/1 V, V_D = 1 V/3 V;
	±0.5	±0.1	tbd	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.01			nA typ	V_S = V_D = 1 V, or 3 V;
	±0.5	±0.1	tbd	nA max	Test Circuit 3
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.4	V max	
Input Current					
I_{INL} or I_{INH}	0.005			µA typ	V_{IN} = V_{INL} or V_{INH}
			±0.1	µA max	
C_{IN}, Digital Input Capacitance	5			pF typ	
DYNAMIC CHARACTERISTICS[2]					
t_{ON}	50			ns typ	R_L = 50 Ω, C_L = 35 pF
	TBD		TBD	ns max	V_S = 1.5 V, Test Circuit 4
t_{OFF}	40			ns typ	R_L = 50 Ω, C_L = 35 pF
	TBD		TBD	ns max	V_S = 1.5 V, Test Circuit 4
Charge Injection	±20			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF, Test Circuit 5
Off Isolation	–65			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, Test Circuit 6
Bandwidth –3 dB	30			MHz typ	R_L = 50 Ω, C_L = 5 pF, Test Circuit 7
C_S (OFF)	55			pF typ	f = 1 MHz
C_D (OFF)	55			pF typ	f = 1 MHz
C_D, C_S (ON)	110			pF typ	f = 1 MHz
POWER REQUIREMENTS					V_{DD} = +3.3 V
I_{DD}	0.001			µA typ	Digital Inputs = 0 V or 3.3 V
			1.0	µA max	

NOTES

[1]Temperature ranges are as follows: Extended Temperature Range: –40°C to +125°C.

[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{DD} to GND .....–0.3 V to +7 V
Analog Inputs[2] ..... - 0.3 V to V_{DD} +0.3 V
..... or 30 mA, Whichever Occurs First
Continuous Current, S or D ..... 400 mA
Peak Current, S or D ..... 800 mA
(Pulsed at 1 ms, 10% Duty Cycle Max)
Operating Temperature Range
Extended ..... –40°C to +125°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature .....+150°C
µSOIC Package, Power Dissipation ..... 315 mW
θ_{JA} Thermal Impedance ..... 206°C/W
θ_{JC} Thermal Impedance ..... 44°C/W
SOT-23 Package, Power Dissipation ..... 282 mW
θ_{JA} Thermal Impedance .....229.6°C/W
θ_{JC} Thermal Impedance .....91.99°C/W
Lead Temperature, Soldering (10seconds) ..... 300°C
IR Reflow, Peak Temperature .....+220°C
ESD.....2kV

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

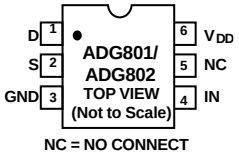
[2]Overvoltages at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

Table I. Truth Table

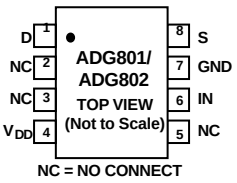
ADG801 In	ADG802 In	Switch Condition
0	1	OFF
1	0	ON

PIN CONFIGURATIONS

6-Lead Plastic Surface Mount (SOT-23)
(RT-6)



8-Lead Small Outline µSOIC
(RM-8)



ORDERING GUIDE

Model	Temperature Range	Supply Option[1]	Brand[1]	Package Descriptions	Package Options
ADG801BRT	–40°C to +125°C	3 V, 5 V	SLB	SOT-23 (Plastic Surface Mount)	RT-6
ADG801BRM	–40°C to +125°C	3 V, 5 V	SLB	µSOIC (Small Outline)	RM-8
ADG802BRT	–40°C to +125°C	3 V, 5 V	SMB	SOT-23 (Plastic Surface Mount)	RT-6
ADG802BRM	–40°C to +125°C	3 V, 5 V	SMB	µSOIC (Small Outline)	RM-8

[1]Branding on SOT-23 and µSOIC packages is limited to 3 characters due to space constraints.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG801/ADG802 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TERMINOLOGY

V_{DD}	Most positive power supply potential.
I_{DD}	Positive supply current.
GND	Ground (0 V) reference.
S	Source terminal. May be an input or output.
D	Drain terminal. May be an input or output.
IN	Logic control input.
V_D (V_S)	Analog voltage on terminals D, S
R_{ON}	Ohmic resistance between D and S.
$R_{FLAT(ON)}$	Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.
I_S (OFF)	Source leakage current with the switch "OFF."
I_D (OFF)	Drain leakage current with the switch "OFF."
I_D, I_S (ON)	Channel leakage current with the switch "ON."
V_{INL}	Maximum input voltage for logic "0".
V_{INH}	Minimum input voltage for logic "1".
$I_{INL}(I_{INH})$	Input current of the digital input.
C_S (OFF)	"OFF" switch source capacitance. Measured with reference to ground.
C_D (OFF)	"OFF" switch drain capacitance. Measured with reference to ground.
C_D,C_S(ON)	"ON" switch capacitance. Measured with reference to ground.
C_{IN}	Digital input capacitance.
t_{ON}	Delay between applying the digital control input and the output switching on. See Test Circuit 4.
t_{OFF}	Delay between applying the digital control input and the output switching off.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
Off Isolation	A measure of unwanted signal coupling through an "OFF" switch.
Crosstalk	A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.
Bandwidth	The frequency at which the output is attenuated by 3dBs.
On Response	The Frequency response of the "ON" switch.
Insertion Loss	The loss due to the ON resistance of the switch.

TYPICAL PERFORMANCE CHARACTERISTICS

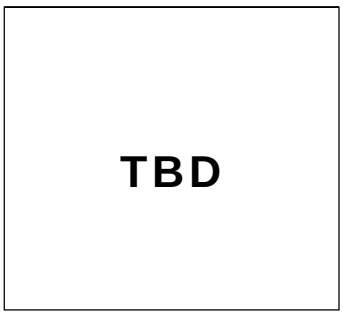


Figure 1. On Resistance as a Function of $V_D(V_S)$

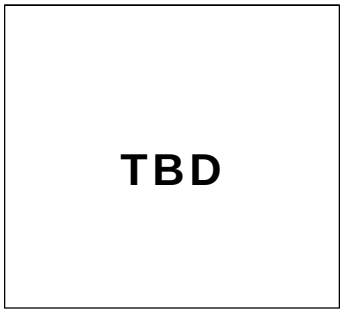


Figure 4. Leakage Currents as a function of $V_D(V_S)$

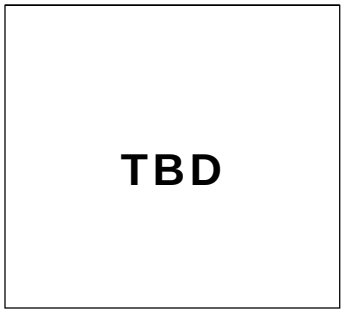


Figure 7. Leakage Currents as a Function of Temperature

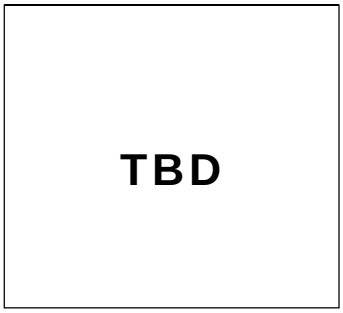


Figure 2. On Resistance as a Function of $V_D(V_S)$ for Different Temperatures

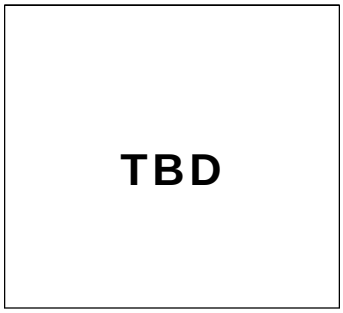


Figure 5. Leakage Currents as a function of $V_D(V_S)$

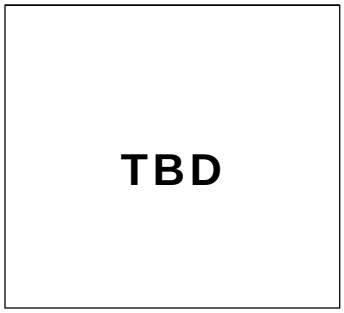


Figure 8. Supply Currents vs. Input Switching Frequency

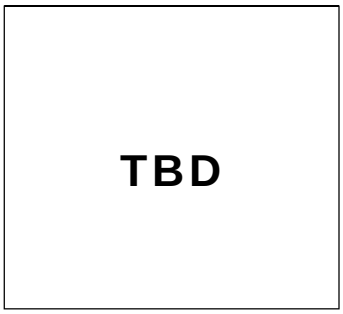


Figure 3. On Resistance as a Function of $V_D(V_S)$ for Different Temperatures

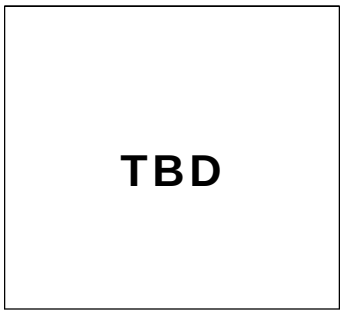


Figure 6. Leakage Currents as a function of Temperature

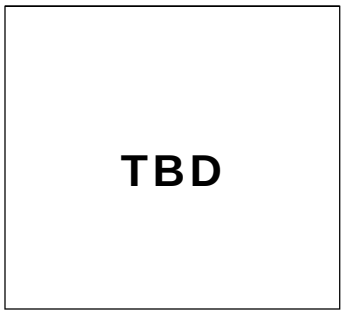


Figure 9. Charge Injection vs. Source Voltage

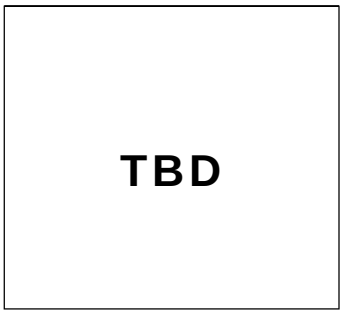


Figure 10. T_{ON}/T_{OFF} Times vs. Temperature

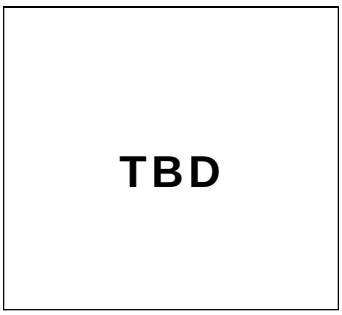


Figure 13. On Response vs. Frequency

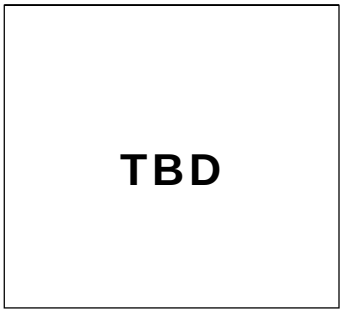


Figure 11. Off Isolation vs. Frequency

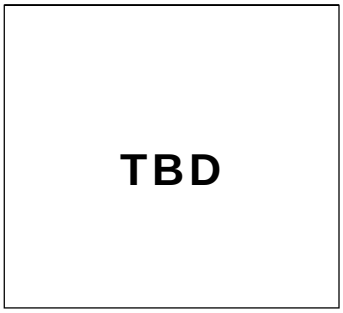
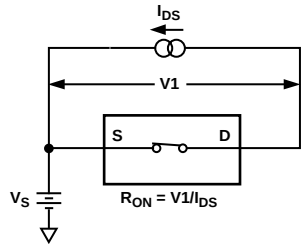


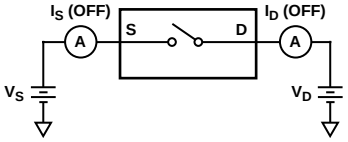
Figure 12. Crosstalk vs. Frequency

ADG801/ADG802

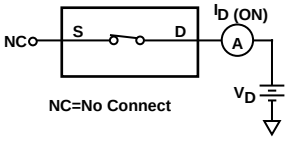
Test Circuits



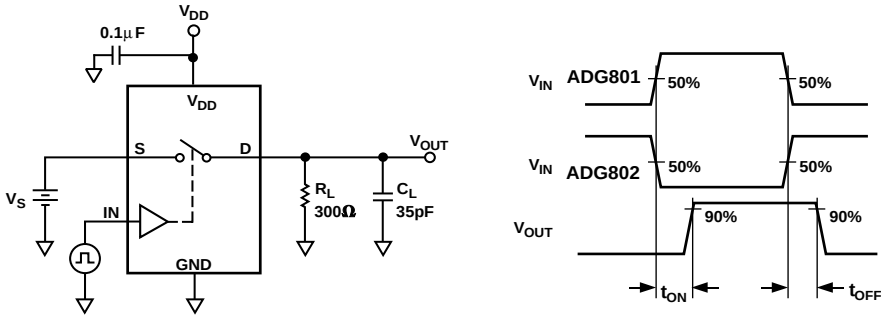
Test Circuit 1. On Resistance



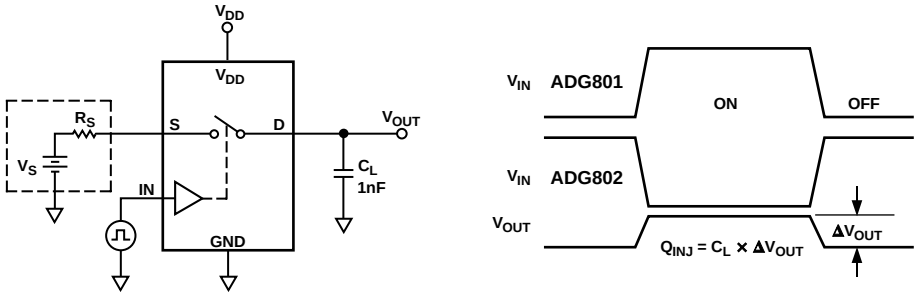
Test Circuit 2. Off Leakage



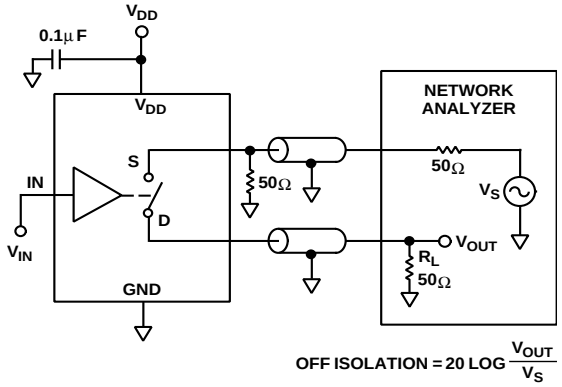
Test Circuit 3. On Leakage



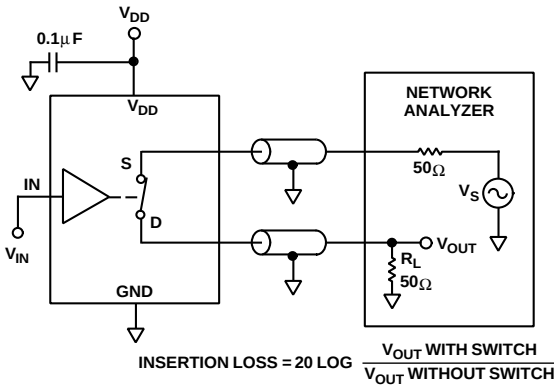
Test Circuit 4. Switching Times



Test Circuit 5. Charge Injection



Test Circuit 6. Off Isolation

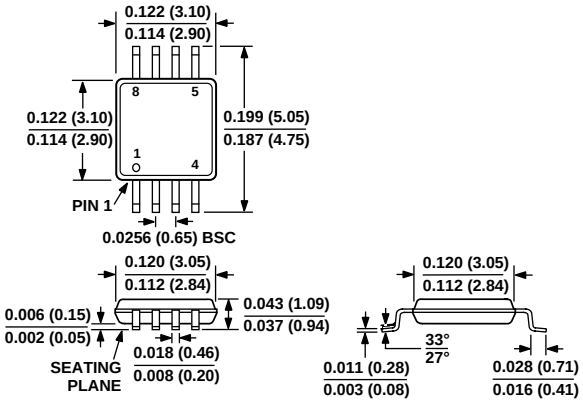


Test Circuit 7. Bandwidth

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead µSOIC (RM-8)



6-Lead SOT-23 (RT-6)