Precision Low Drift 2.048 V/2.500 V SOT-23 Voltage References with Shutdown

ADR390/ADR391

FEATURES
Initial Accuracy: ±6 mV Max
Low TCV_O: 25 ppm/°C Max
Load Regulation: 60 ppm/mA
Line Regulation: 25 ppm/V
Wide Operating Range:
2.4 V–18 V for ADR390
2.8 V–18 V for ADR391
Low Power: 120 μA Max
Shutdown to Less than 3 μA Max
High Output Current: 5 mA Min
Wide Temperature Range: −40°C to +85°C
Tiny SOT-23-5 Package

APPLICATIONS
Battery-Powered Instrumentation
Portable Medical Instruments
Data Acquisition Systems
Industrial and Process Control Systems
Hard Disk Drives
Automotive

PIN CONFIGURATION
5-Lead SOT-23
(RT Suffix)

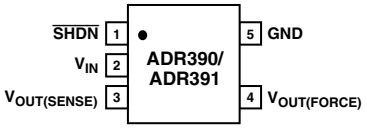

Table I.

Part Number	Nominal Output Voltage (V)
ADR390	2.048
ADR391	2.500

GENERAL DESCRIPTION

The ADR390 and ADR391 are precision 2.048 V and 2.5 V bandgap voltage references featuring high accuracy and stability and low power consumption in a tiny footprint. Patented temperature drift curvature correction techniques minimize nonlinearity of the voltage change with temperature. The wide operating range and low power consumption with additional shutdown capability make them ideal for 3 V to 5 V battery-powered applications. The V_{OUT} Sense Pin enables greater accuracy by supporting full Kelvin operation in systems using very fine or long circuit traces.

The ADR390 and ADR391 are micropower, Low Dropout Voltage (LDV) devices that provide a stable output voltage from supplies as low as 300 mV above the output voltage. They are specified over the industrial (–40°C to +85°C) temperature range. Each is available in the tiny 5-lead SOT-23 package.

The combination of V_{OUT} sense and shutdown functions also enables a number of unique applications combining precision reference/regulation with fault decision and over-current protection. Details are provided in the applications section.

REV. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703

ADR390 SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_{IN} = 5 V, T_A = 25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Initial Accuracy	V_O		2.042	2.048	2.054	V
Initial Accuracy Error	V_{OERR}		0.29		0.29	%
Temperature Coefficient	TCV_O/°C	–40°C < T_A < +85°C		5	25	ppm/°C
Minimum Supply Voltage Headroom	$V_{IN} – V_O$		300			mV
Line Regulation	$\Delta V_O/\Delta V_{IN}$	V_{IN} = 2.5 V to 15 V				
		–40°C < T_A < +85°C		10	25	ppm/V
Load Regulation	$\Delta V_O/\Delta I_{LOAD}$	V_{IN} = 3 V, I_{LOAD} = 0 mA to 5 mA				
		–40°C < T_A < +85°C			60	ppm/mA
Quiescent Current	I_{IN}	No Load		100	120	µA
		–40°C < T_A < +85°C			140	µA
Voltage Noise	e_N	0.1 Hz to 10 Hz		5		µV p-p
Turn-On Settling Time	t_R			20		µs
Long-Term Stability[1]	ΔV_O	1,000 Hours		50		ppm
Output Voltage Hysteresis[2]	V_{OHYS}			40		ppm
Ripple Rejection Ratio	RRR	f_{IN} = 60 Hz		85		dB
Short Circuit to GND	I_{SC}			30		mA
Shutdown Supply Current	I_{SHDN}				3	µA
Shutdown Logic Input Current	I_{LOGIC}				500	nA
Shutdown Logic Low	V_{INL}				0.8	V
Shutdown Logic High	V_{INH}		2.4			V

NOTES

[1]Long-term stability, typical shift in value of output voltage at 25°C on a sample of parts subjected to operation life test of 1000 hours at 125°C. $\Delta V_O = V_O(t_0) – V_O(t_{1000})$; $V_O(t_0) = V_O$ at 25°C at time 0; $V_O(t_{1000}) = V_O$ at 25°C after 1000 hours at 125°C; $\Delta V_O = (V_O(t_0) – V_O(t_{1000}))/V_O(t_0) \times 10^6$ (in ppm).

[2]Output Voltage Hysteresis, is defined as the change in 25°C output voltage before and after the device is cycled through temperature. +25°C to –40°C to +85°C to +25°C. This is a typical value from a sample of parts put through such a cycle. Refer to Figures 11 and 12. $V_{OHYS} = V_O – V_{OTC}$; $V_O = V_O$ at 25°C at time 0; $V_{OTC} = V_O$ at 25°C after temperature cycle at +25°C to –40°C to +85°C to +25°C; $V_{OHYS} = ((V_O – V_{OTC})/V_O) \times 106$ (in ppm).

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (@ V_{IN} = 15 V, T_A = 25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Initial Accuracy	V_O		2.042	2.048	2.054	V
Initial Accuracy Error	V_{OERR}		0.29		0.29	%
Temperature Coefficient	TCV_O/°C	–40°C < T_A < +85°C		5	25	ppm/°C
Minimum Supply Voltage Headroom	$V_{IN} – V_O$		300			mV
Line Regulation	$\Delta V_O/\Delta V_{IN}$	V_{IN} = 2.5 V to 15 V				
		–40°C < T_A < +85°C		10	25	ppm/V
Load Regulation	$\Delta V_O/\Delta I_{LOAD}$	V_{IN} = 3 V, I_{LOAD} = 0 mA to 5 mA				
		–40°C < T_A < +85°C			60	ppm/mA
Quiescent Current	I_{IN}	No Load		100	120	µA
		–40°C < T_A < +85°C			140	µA
Voltage Noise	e_N	0.1 Hz to 10 Hz		5		µV p-p
Turn-On Settling Time	t_R			20		µs
Long-Term Stability[1]	ΔV_O	1,000 Hours		50		ppm
Output Voltage Hysteresis[2]	V_{OHYS}			40		ppm
Ripple Rejection Ratio	RRR	f_{IN} = 60 Hz		85		dB
Short Circuit to GND	I_{SC}			30		mA
Shutdown Supply Current	I_{SHDN}				3	µA
Shutdown Logic Input Current	I_{LOGIC}				500	nA
Shutdown Logic Low	V_{INL}				0.8	V
Shutdown Logic High	V_{INH}		$V_{IN} – 1$			V

NOTES

[1]Long-term stability, typical shift in value of output voltage at 25°C on a sample of parts subjected to operation life test of 1000 hours at 125°C. $\Delta V_O = V_O(t_0) – V_O(t_{1000})$; $V_O(t_0) = V_O$ at 25°C at time 0; $V_O(t_{1000}) = V_O$ at 25°C after 1000 hours at 125°C; $\Delta V_O = (V_O(t_0) – V_O(t_{1000}))/V_O(t_0) \times 10^6$ (in ppm).

[2]Output Voltage Hysteresis, is defined as the change in 25°C output voltage before and after the device is cycled through temperature. +25°C to –40°C to +85°C to +25°C. This is a typical value from a sample of parts put through such a cycle. Refer to Figures 11 and 12. $V_{OHYS} = V_O – V_{OTC}$; $V_O = V_O$ at 25°C at time 0; $V_{OTC} = V_O$ at 25°C after temperature cycle at +25°C to –40°C to +85°C to +25°C; $V_{OHYS} = ((V_O – V_{OTC})/V_O) \times 106$ (in ppm).

Specifications subject to change without notice.

ADR391 SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_{IN} = 5 V, T_A = 25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Initial Accuracy	V_O		2.494	2.5	2.506	V
Initial Accuracy Error	V_{OERR}		0.24		0.24	%
Temperature Coefficient	TCV_O/°C	–40°C < T_A < +85°C		5	25	ppm/°C
Minimum Supply Voltage Headroom	$V_{IN} – V_O$		300			mV
Line Regulation	$\Delta V_O/\Delta V_{IN}$	V_{IN} = 2.8 V to 15 V				
		–40°C < T_A < +85°C		10	25	ppm/V
Load Regulation	$\Delta V_O/\Delta I_{LOAD}$	V_{IN} = 3.5 V, I_{LOAD} = 0 mA to 5 mA				
		–40°C < T_A < +85°C			60	ppm/mA
Quiescent Current	I_{IN}	No Load		100	120	µA
		–40°C < T_A < +85°C			140	µA
Voltage Noise	e_N	0.1 Hz to 10 Hz		5		µV p-p
Turn-On Settling Time	t_R			20		µs
Long-Term Stability[1]	ΔV_O	1,000 Hours		50		ppm
Output Voltage Hysteresis[2]	V_{OHYS}			75		ppm
Ripple Rejection Ratio	RRR	f_{IN} = 60 Hz		85		dB
Short Circuit to GND	I_{SC}			25		mA
Shutdown Supply Current	I_{SHDN}				3	µA
Shutdown Logic Input Current	I_{LOGIC}				500	nA
Shutdown Logic Low	V_{INL}				0.8	V
Shutdown Logic High	V_{INH}		2.4			V

NOTES

[1]Long-term stability, typical shift in value of output voltage at 25°C on a sample of parts subjected to operation life test of 1000 hours at 125°C. $\Delta V_O = V_O (t_0) – V_O (t_{1000})$; $V_O (t_0) = V_O$ at 25°C at time 0; $V_O (t_{1000}) = V_O$ at 25°C after 1000 hours at 125°C; $\Delta V_O = (V_O (t_0) – V_O (t_{1000}))/V_O (t_0) \times 10^6$ (in ppm).

[2]Output Voltage Hysteresis, is defined as the change in 25°C output voltage before and after the device is cycled through temperature. +25°C to –40°C to +85°C to +25°C. This is a typical value from a sample of parts put through such a cycle. Refer to Figures 11 and 12. $V_{OHYS} = V_O – V_{OTC}$; $V_O = V_O$ at 25°C at time 0; $V_{OTC} = V_O$ at 25°C after temperature cycle at +25°C to –40°C to +85°C to +25°C; $V_{OHYS} = ((V_O – V_{OTC})/V_O) \times 106$ (in ppm).

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ELECTRICAL CHARACTERISTICS (@ V_{IN} = 15 V, T_A = 25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Initial Accuracy	V_O		2.494	2.5	2.506	V
Initial Accuracy Error	V_{OERR}		0.24		0.24	%
Temperature Coefficient	TCV_O/°C	–40°C < T_A < +85°C		5	25	ppm/°C
Minimum Supply Voltage Headroom	$V_{IN} – V_O$		300			mV
Line Regulation	$\Delta V_O/\Delta V_{IN}$	V_{IN} = 2.8 V to 15 V				
		–40°C < T_A < +85°C		10	25	ppm/V
Load Regulation	$\Delta V_O/\Delta I_{LOAD}$	V_{IN} = 3.5 V, I_{LOAD} = 0 mA to 5 mA				
		–40°C < T_A < +85°C			60	ppm/mA
Quiescent Current	I_{IN}	No Load		100	120	µA
		–40°C < T_A < +85°C			140	µA
Voltage Noise	e_N	0.1 Hz to 10 Hz		5		µV p-p
Turn-On Settling Time	t_R			20		µs
Long-Term Stability[1]	ΔV_O	1,000 Hours		50		ppm
Output Voltage Hysteresis[2]	V_{OHYS}			75		ppm
Ripple Rejection Ratio	RRR	f_{IN} = 60 Hz		85		dB
Short Circuit to GND	I_{SC}			30		mA
Shutdown Supply Current	I_{SHDN}				3	µA
Shutdown Logic Input Current	I_{LOGIC}				500	nA
Shutdown Logic Low	V_{INL}				0.8	V
Shutdown Logic High	V_{INH}		V_{IN} – 1			V

NOTES

[1]Long-term stability, typical shift in value of output voltage at 25°C on a sample of parts subjected to operation life test of 1000 hours at 125°C. $\Delta V_O = V_O (t_0) – V_O (t_{1000})$; $V_O (t_0) = V_O$ at 25°C at time 0; $V_O (t_{1000}) = V_O$ at 25°C after 1000 hours at 125°C; $\Delta V_O = (V_O (t_0) – V_O (t_{1000}))/V_O (t_0) \times 10^6$ (in ppm).

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Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . 18 V
Shutdown Logic Level . . . . . 18 V
  Or Supply Voltage, Whichever is Lower . . . . . 18 V
Output Short-Circuit Duration to GND Observe Derating Curves
Storage Temperature Range
  RT Package . . . . . –65°C to +150°C
Operating Temperature Range
  ADR390/ADR391 . . . . . –40°C to +85°C
Junction Temperature Range
  RT Package . . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . 300°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Type	θ_{JA}*	θ_{JC}	Unit
5-Lead SOT-23 (RT)	230	–	°C/W

*θ_{JA} is specified for worst-case conditions, i.e., θ_{JA} is specified for device in socket for SOT packages.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Top Mark	Output Voltage	Number of Parts
ADR390ART–REEL7	–40°C to +85°C	5-Lead SOT	RT-5	R0A	2.048	3,000
ADR390ART–REEL	–40°C to +85°C	5-Lead SOT	RT-5	R0A	2.048	10,000
ADR391ART–REEL7	–40°C to +85°C	5-Lead SOT	RT-5	R1A	2.500	3,000
ADR391ART–REEL	–40°C to +85°C	5-Lead SOT	RT-5	R1A	2.500	10,000

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADR390/ADR391 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

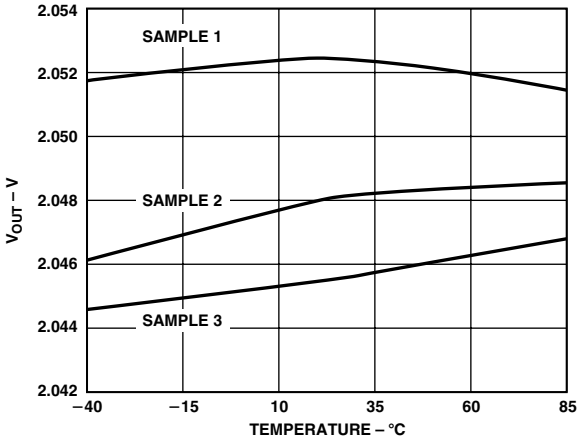


Figure 1. ADR390 Output Voltage vs. Temperature

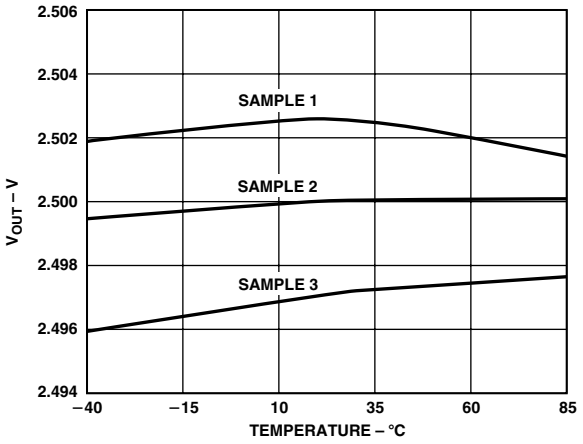


Figure 2. ADR391 Output Voltage vs. Temperature

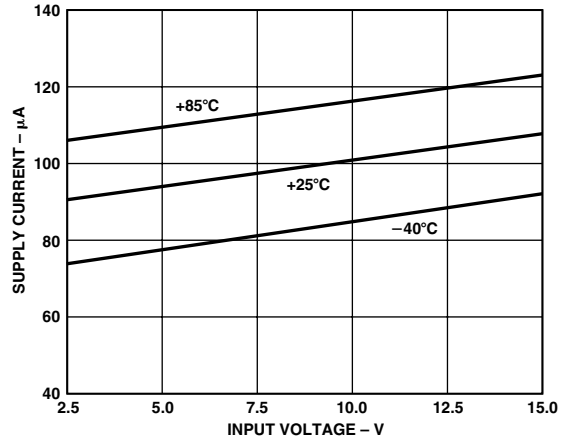


Figure 3. ADR390 Supply Current vs. Input Voltage

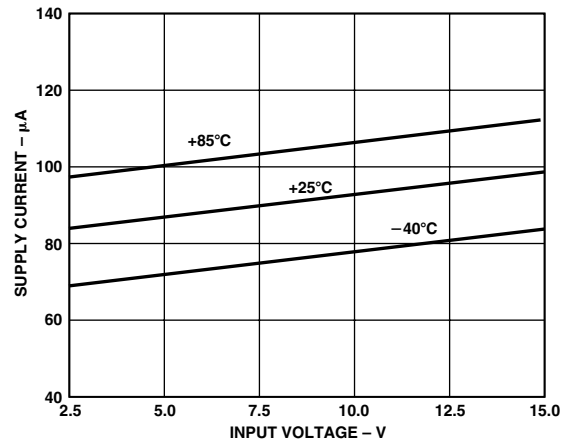


Figure 4. ADR391 Supply Current vs. Input Voltage

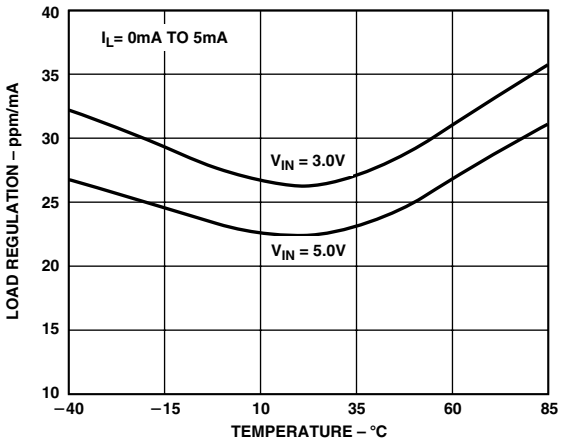


Figure 5. ADR390 Load Regulation vs. Temperature

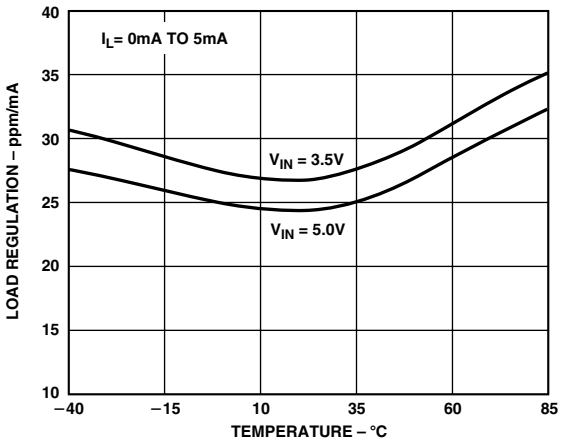


Figure 6. ADR391 Load Regulation vs. Temperature

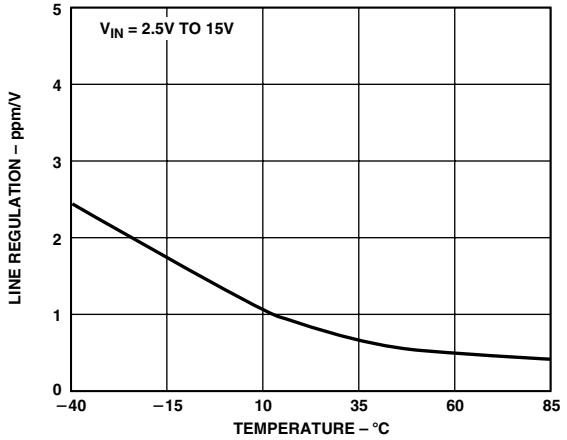


Figure 7. ADR390 Line Regulation vs. Temperature

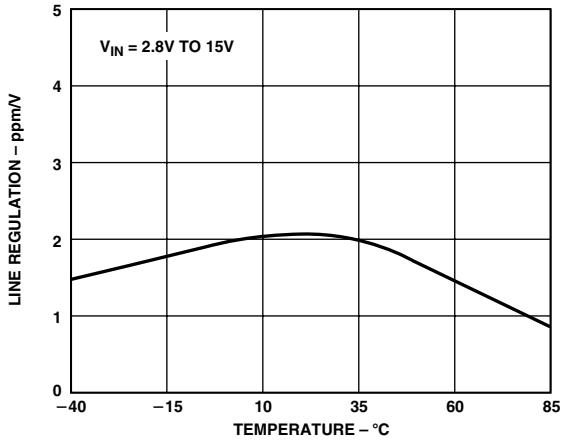


Figure 8. ADR391 Line Regulation vs. Temperature

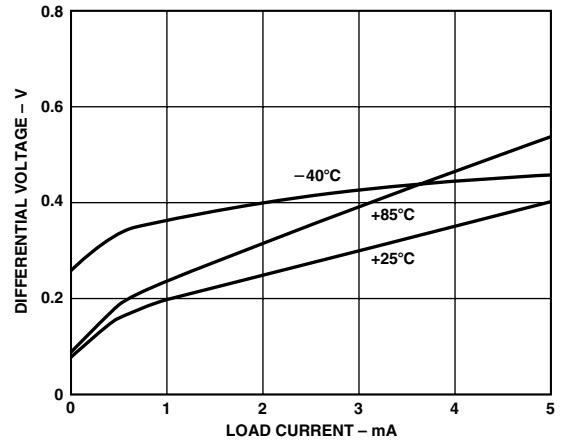


Figure 9. ADR390 Minimum Input-Output Voltage Differential vs. Load Current

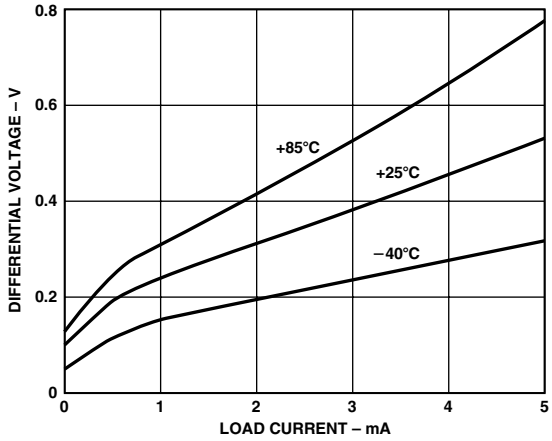


Figure 10. ADR391 Minimum Input-Output Voltage Differential vs. Load Current

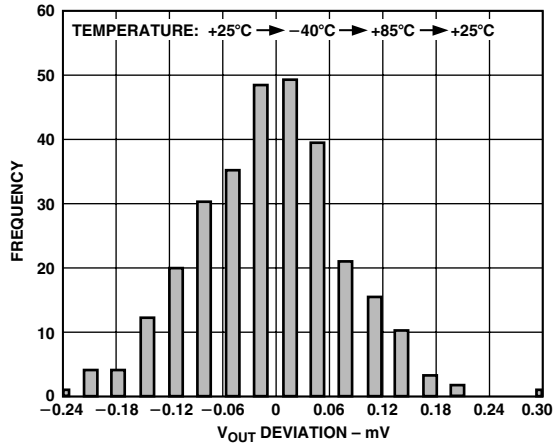


Figure 11. ADR390 V_{OUT} Hysteresis Distribution

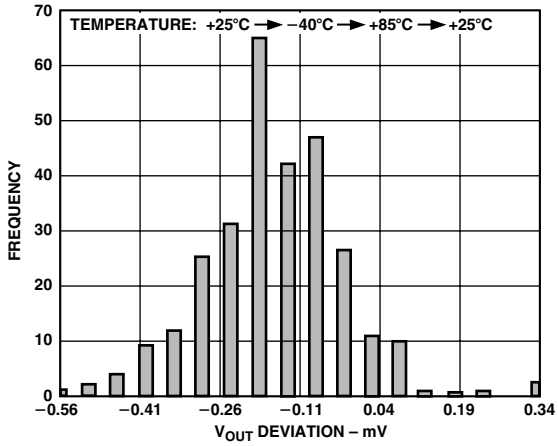


Figure 12. ADR391 V_{OUT} Hysteresis Distribution

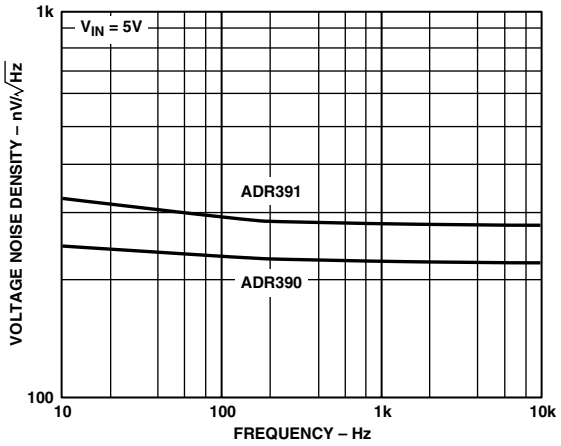


Figure 13. Voltage Noise Density vs. Frequency

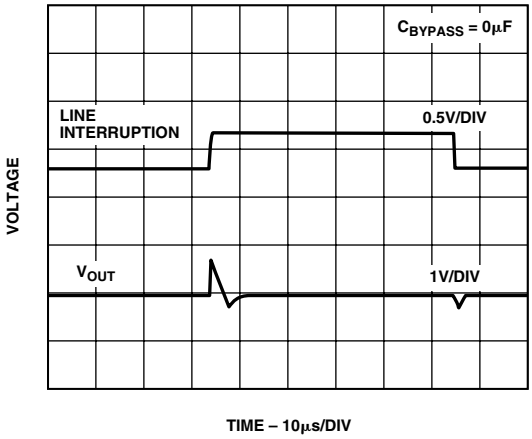


Figure 16. ADR391 Line Transient Response

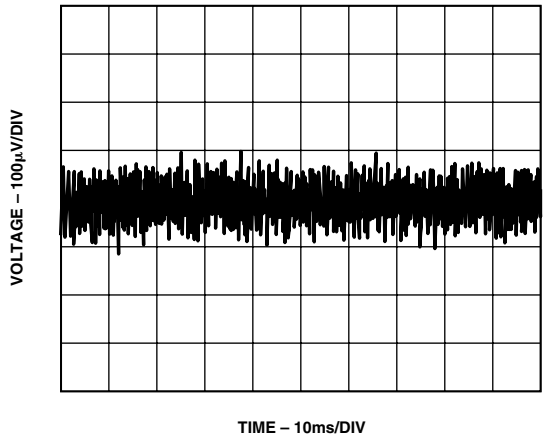


Figure 14. ADR390 Voltage Noise 10 Hz to 10 kHz

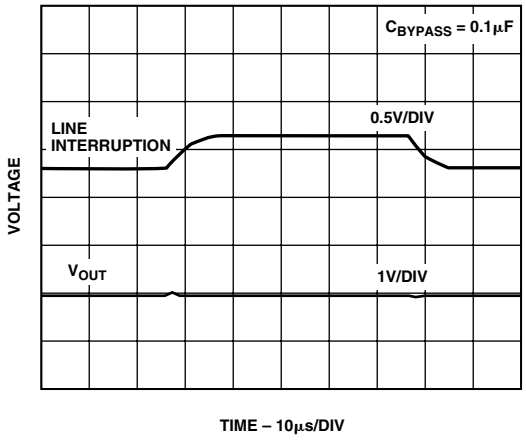


Figure 17. ADR391 Line Transient Response

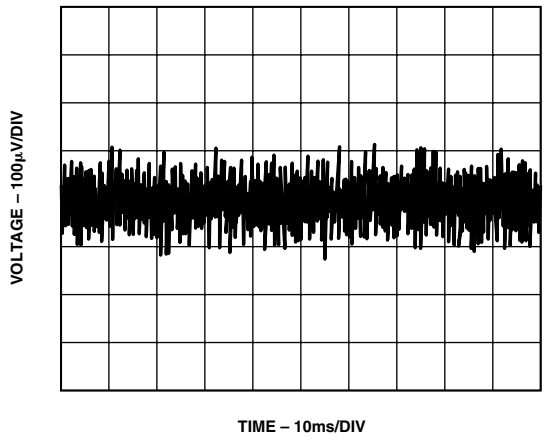


Figure 15. ADR391 Voltage Noise 10 Hz to 10 kHz

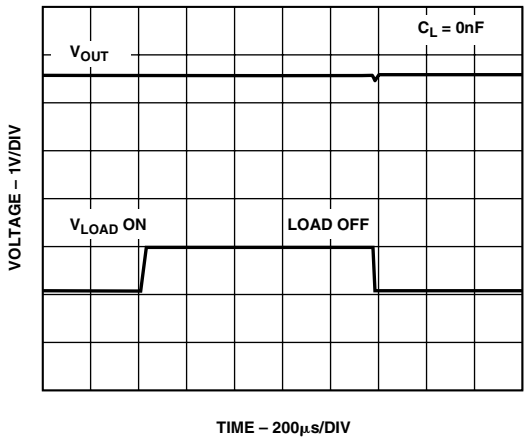


Figure 18. ADR391 Load Transient Response

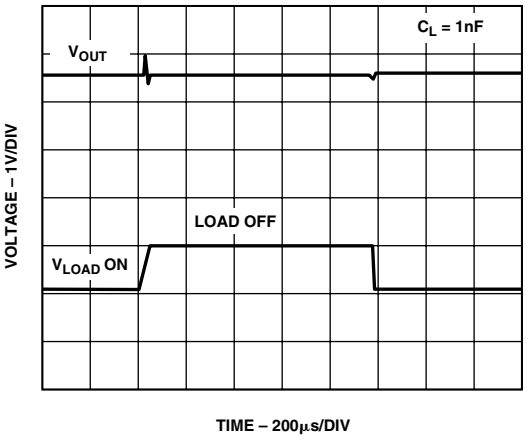


Figure 19. ADR391 Load Transient Response

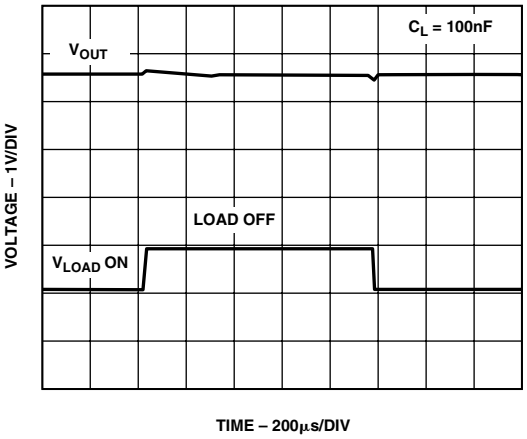


Figure 20. ADR391 Load Transient Response

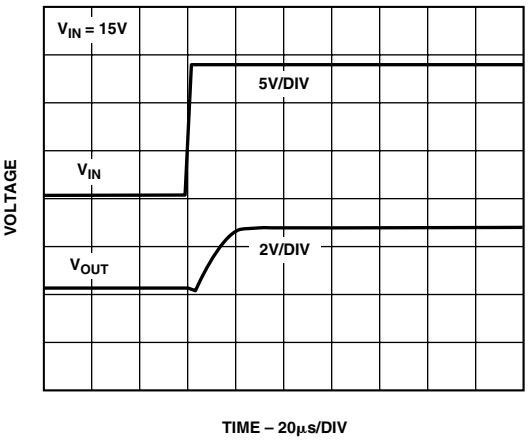


Figure 21. ADR391 Turn-On Response Time at 15 V

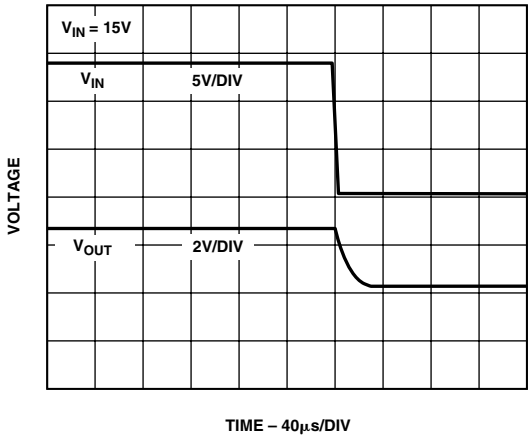


Figure 22. ADR391 Turn-Off Response at 15 V

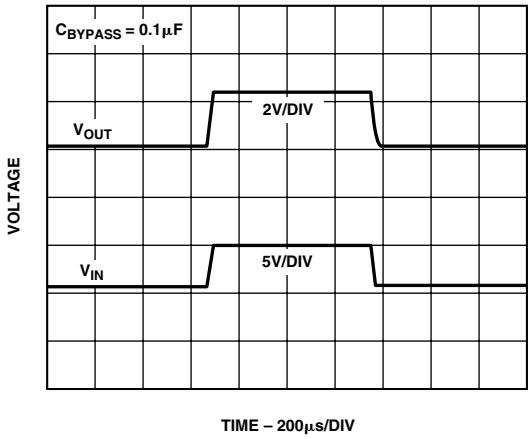


Figure 23. ADR391 Turn-On/Turn-Off Response at 5 V

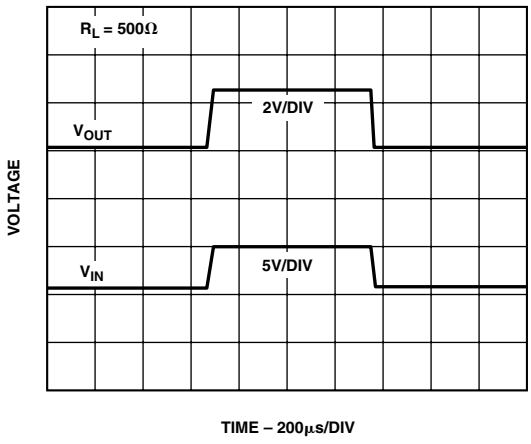


Figure 24. ADR391 Turn-On/Turn-Off Response at 5 V

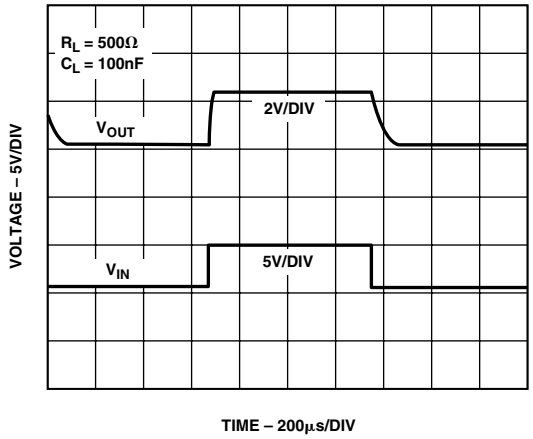


Figure 25. ADR391 Turn-On/Turn-Off Response at 5 V

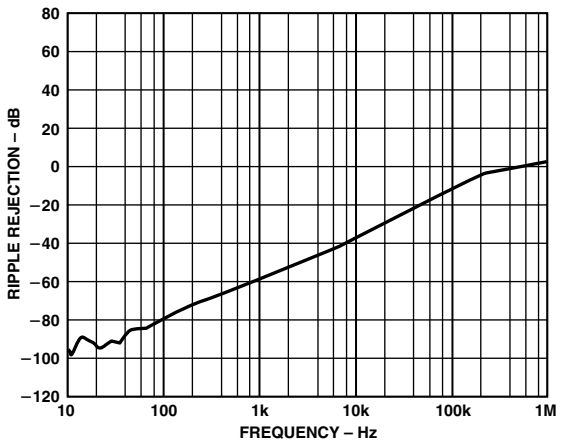


Figure 26. Ripple Rejection vs. Frequency

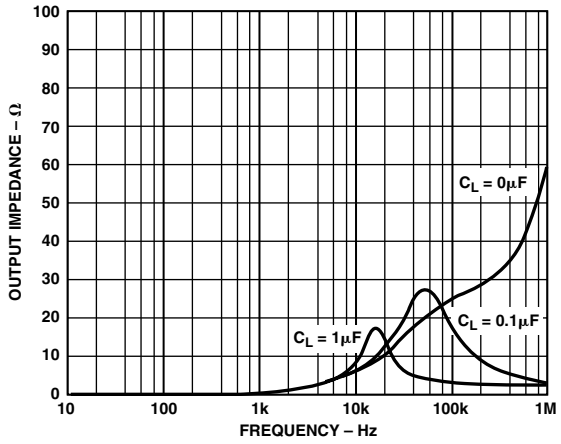


Figure 27. Output Impedance vs. Frequency

THEORY OF OPERATION

Bandgap references are the high-performance solution for low supply voltage and low power voltage reference applications, and the ADR390/ADR391 is no exception. But the uniqueness of this product lies in its architecture. By observing Figure 28, the zero TC bandgap voltage is referenced to the output, not to ground. The bandgap cell consists of the pnp pair Q51 and Q52, running at unequal current densities. The difference in V_{BE} results in a voltage with a positive TC which is amplified up by the ratio of $2\times\frac{R58}{R54}$. This PTAT voltage, combined with V_{BE}'s of Q51 and Q52 produce the stable bandgap voltage.

Reduction in the bandgap curvature is performed by the ratio of the two resistors R44 and R59. Precision laser trimming and other patented circuit techniques are used to further enhance the drift performance.

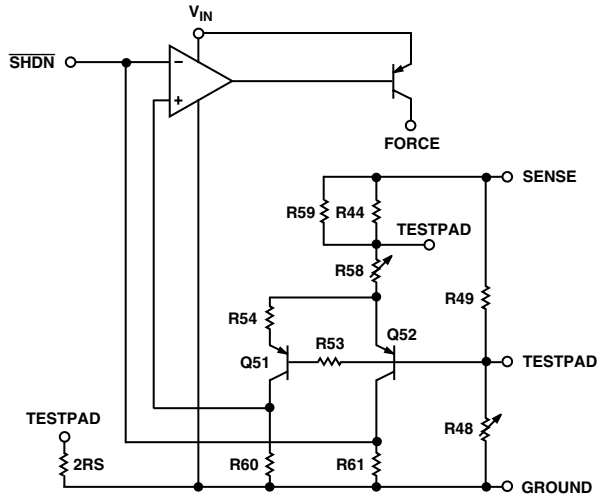


Figure 28. Simplified Schematic

Device Power Dissipation Considerations

The ADR390/ADR391 is capable of delivering load currents to 5 mA with an input voltage that ranges from 2.8 V (ADR391 only) to 15 V. When this device is used in applications with large input voltages, care should be taken to avoid exceeding the specified maximum power dissipation or junction temperature that could result in premature device failure. The following formula should be used to calculate a device's maximum junction temperature or dissipation:

$$P_D = \frac{T_J - T_A}{\theta_{JA}}$$

In this equation, T_J and T_A are, respectively, the junction and ambient temperatures, P_D is the device power dissipation, and θ_{JA} is the device package thermal resistance.

Shutdown Mode Operation

The ADR390/ADR391 includes a shutdown feature that is TTL/CMOS level compatible. A logic LOW or a zero volt condition on the $\overline{SHDN}$ pin is required to turn the device off. During shutdown, the output of the reference becomes a high impedance state where its potential would then be determined by external circuitry. If the shutdown feature is not used, the $\overline{SHDN}$ pin should be connected to V_{IN} (Pin 2).

APPLICATIONS

Membrane Switch Controlled Power Supply

The ADR390/ADR391 can operate as a low dropout power supply in hand-held instrumentation. In the following circuit, a membrane ON/OFF switch is used to control the operation of the reference. During an initial power-on condition, the $\overline{SHDN}$ pin is held to GND. Recall that this condition disables the output (read: three-state). When the membrane ON switch is pressed, the $\overline{SHDN}$ pin assumes and remains at the same potential as V_{IN}, via the 10 kΩ resistor thus enabling the output. When the membrane OFF switch is pressed, the $\overline{SHDN}$ pin is momentarily connected to GND which disables the ADR390/ADR391 output once again.

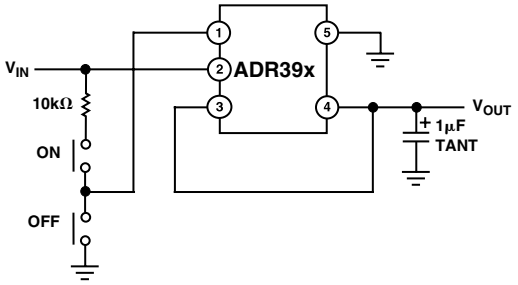


Figure 29. Membrane Switch Controlled Power Supply

Stacking Reference ICs for Arbitrary Outputs

Some applications may require two reference voltage sources which are a combined sum of standard outputs. The following circuit shows how this "stacked output" reference can be implemented:

OUTPUT TABLE

U1/U2	V_{OUT1} (V)	V_{OUT2} (V)
ADR390/ADR390	2.048	4.096
ADR391/ADR391	2.5	5.0

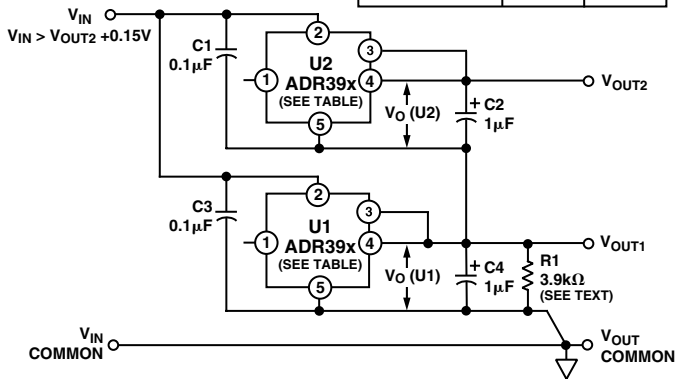


Figure 30. Stacking Voltage References with the ADR390/ ADR391

Two reference ICs are used, fed from a common unregulated input, V_{IN}. The outputs of the individual ICs are simply connected in series which provides two output voltages V_{OUT1} and V_{OUT2}. V_{OUT1} is the terminal voltage of U1, while V_{OUT2} is the sum of this voltage and the terminal voltage of U2. U1 and U2 are simply chosen for the two voltages that supply the required outputs (see Output Table). For example, if both U1 and U2 are ADR391's, V_{OUT1} is 2.5 V and V_{OUT2} is 5.0 V.

While this concept is simple, a precaution is in order. Since the lower reference circuit must sink a small bias current from U2, plus the base current from the series PNP output transistor in U2, either the external load of U1 or R1 must provide a path for this current. If the U1 minimum load is not well defined, the resistor R1 should be used, set to a value that will conservatively pass 600 µA of current with the applicable V_{OUT1} across it. Note that the two U1 and U2 reference circuits are locally treated as macrocells, each having its own bypasses at input and output for best stability. Both U1 and U2 in this circuit can source dc currents up to their full rating. The minimum input voltage, V_S, is determined by the sum of the outputs, V_{OUT2}, plus the dropout voltage of U2.

A related variation on stacking two three-terminal references is shown in the following figure where U1, an ADR391, is stacked with a two-terminal reference diode such as the AD589. Similar to the all three-terminal stacked references mentioned earlier, the two individual terminal voltage outputs of D1 and U1 are 1.235 V and 2.5 V, respectively. Thus V_{OUT2} is the sum of D1 and U1, or 3.735 V. When using two-terminal reference diodes such as D1, the rated minimum and maximum device currents must be observed, and the maximum load current from V_{OUT1} can be no greater than the current set up by R1 and $V_{O(U1)}$.

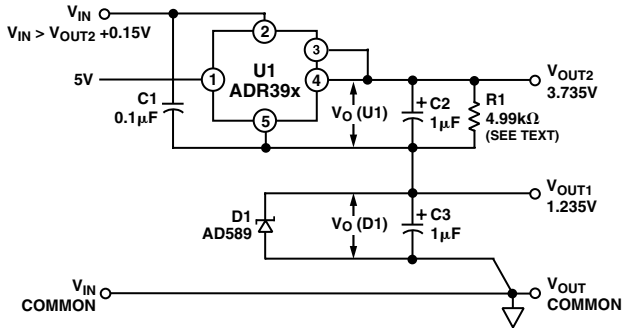


Figure 31. Stacking Voltage References with the ADR390/ ADR391

A Negative Precision Reference without Precision Resistors

In many current-output CMOS DAC applications where the output signal voltage must be of the same polarity as the reference voltage, it is often required to reconfigure a current-switching DAC into a voltage-switching DAC through the use of a 1.25 V reference, an op amp, and a pair of resistors. Using a current-switching DAC directly requires the need for an additional operational amplifier at the output to reinvert the signal. A negative voltage reference is then desirable from the point that an additional operational amplifier is not required for either reinversion (current-switching mode) or amplification (voltage switching mode) of the DAC output voltage. In general, any positive voltage reference can be converted into a negative voltage reference through the use of an operational amplifier and a pair of matched resistors in an inverting configuration. The disadvantage to this approach is that the largest single source of error in the circuit is the relative matching of the resistors used.

The following circuit avoids the need for tightly matched resistors with the use of an active integrator circuit. In this circuit, the output of the voltage reference provides the input drive for the integrator. The integrator, to maintain circuit equilibrium, adjusts its output to establish the proper relationship between the reference's V_{OUT} and GND. Thus, any negative output voltage desired can be chosen by simply substituting for the appropriate reference IC. The shutdown feature is maintained in the circuit with the simple addition of a PNP transistor and

a 10 kΩ resistor. A precaution should be noted with this approach: although rail-to-rail output amplifiers work best in the application, these operational amplifiers require a finite amount (mV) of headroom when required to provide any load current. The choice for the circuit's negative supply should take this issue into account.

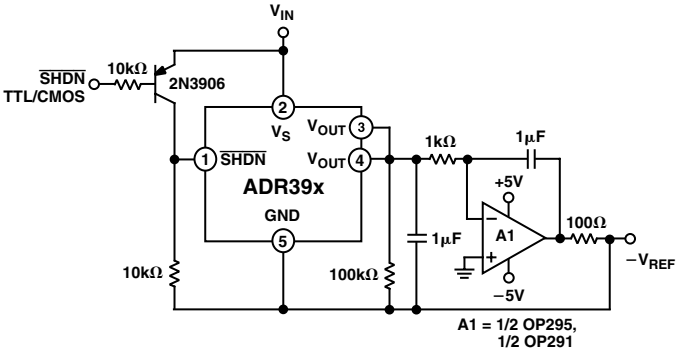


Figure 32. A Negative Precision Voltage Reference Uses No Precision Resistors

Precision Current Source

Many times in low-power applications, the need arises for a precision current source that can operate on low supply voltages. As shown in the following figure, the ADR390/ADR391 can be configured as a precision current source. The circuit configuration illustrated is a floating current source with a grounded load. The reference's output voltage is bootstrapped across R_{SET}, which sets the output current into the load. With this configuration, circuit precision is maintained for load currents in the range from the reference's supply current, typically 90 µA to approximately 5 mA.

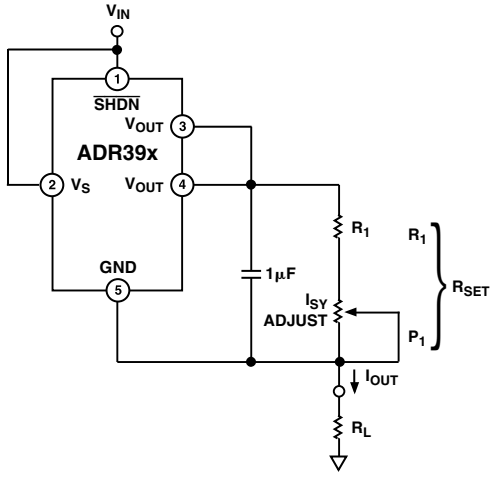


Figure 33. A Precision Current Source

High-Power Performance with Current Limit

In some cases, the user may want higher output current delivered to a load and still achieve better than 0.5% accuracy out of the ADR390/ADR391. The accuracy for a reference is normally specified on the data sheet with no load. However, the output voltage changes with load current.

The circuit below provides high current without compromising the accuracy of the ADR390/ADR391. The series pass transistor Q1 provides up to 1 A load current. The ADR390/ADR391 delivers only the base drive to Q1 through the force pin. The sense pin of the ADR390/ADR391 is a regulated output and is connected to the load.

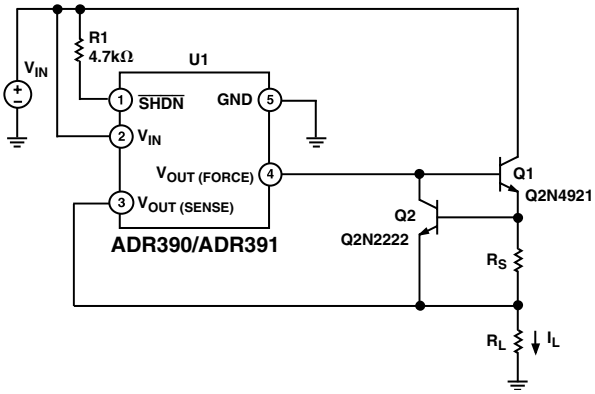


Figure 34. ADR390/ADR391 for High-Power Performance with Current Limit

A similar circuit function can also be achieved with the Darlington transistor configuration, see Figure 35.

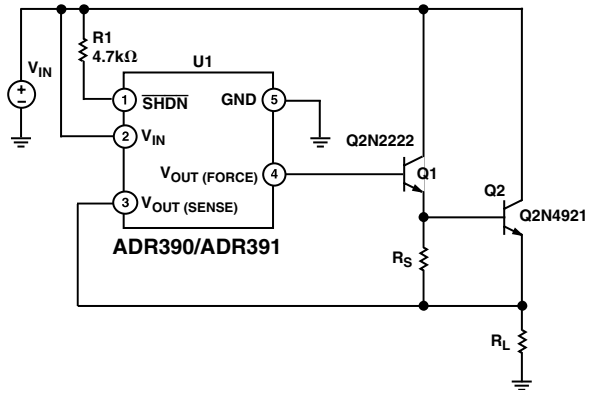


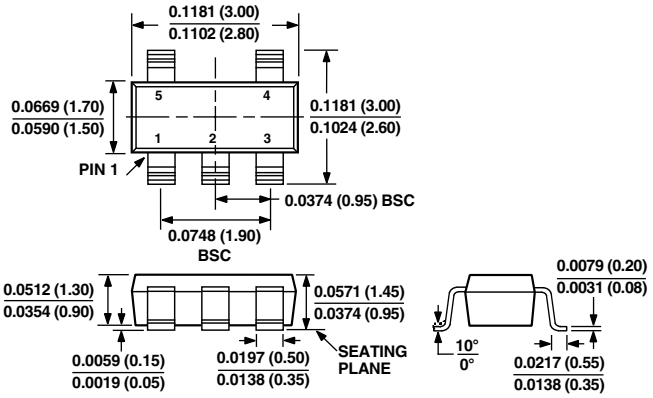
Figure 35. ADR390/ADR391 High Output Current with Darlington Drive Configuration

The transistor Q2 protects Q1 during short circuit limit faults by robbing its base drive. The maximum current is $I_{LMAX} \approx 0.6\ V/R_S$.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

5-Lead SOT-23
(RT Suffix)



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