a

Dual Channel, Gain Ranging ADC with RSSI

12/97 Preliminary — AD6600

Features
20 MSPS Sample Rate
>100 dB dynamic range -
90 dB from ADC + RSSI
15 dB from Oversampling @ 6.5 MSPS & 200 kHz BW
IF Sampling to 250 MHz Ain
0.30 pS aperture jitter
Dual Inputs -
Diversity or two independent IF signals
Separate Gain Paths
Automatic gain ranging (AGC)
Digital RSSI Output
Single +5V Power Supply or
+3.3V for Digital Supplies
725mW Power Dissipation

Applications
Communications receivers
PCS/Cellular Base Stations
GSM, CDMA, TDMA

Product Description
The AD6600 is a mixed signal receive chip designed to directly sample signals at frequencies up to 250 MHz Ain. The device includes an 11 bit 20MSPS ADC, input amplifiers, automatic gain ranging circuitry, a 450 MHz T/H, digital RSSI outputs, references, and control circuitry. Digital signals are CMOS/TTL compatible and are designed to interface directly with the AD6620 Dual Decimating Receiver.

The AD6600 can be configured for several different applications. The primary use is for the dual analog inputs to be used to sample diversity antennas. However, two independent IF signals can be sampled. The AD6600 can be used to sample one input at the full clock rate of the chip to get maximum processing gain benefit.

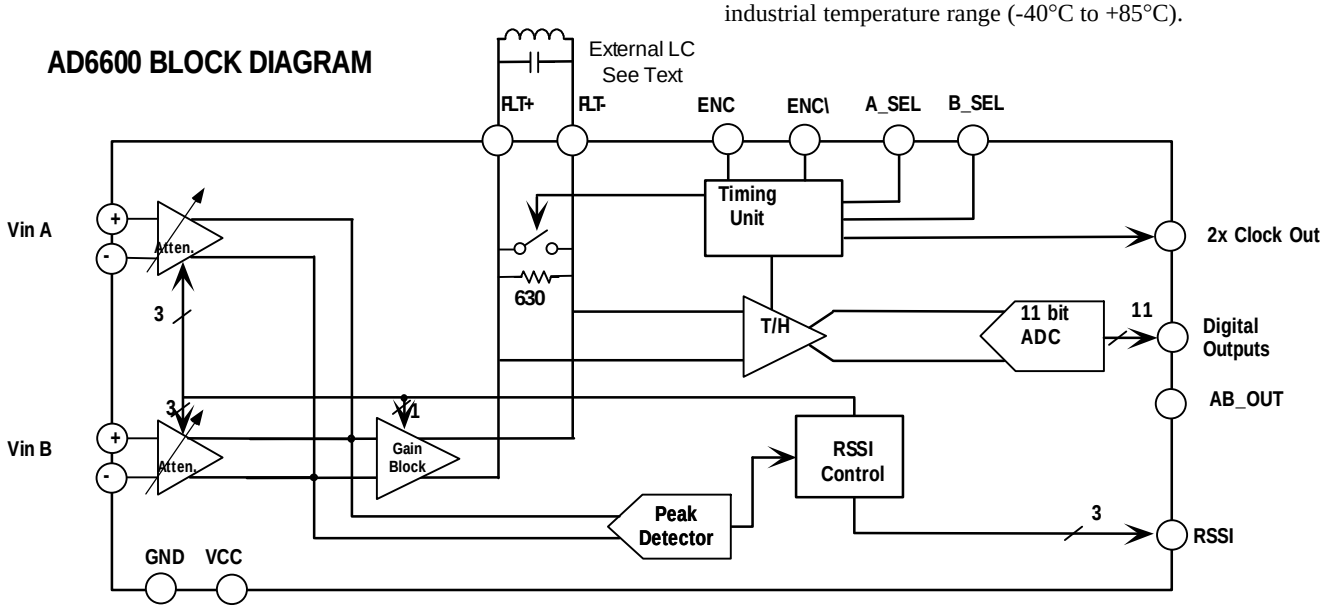
Although the AD6600 is designed to interface with other ADI core products, it interfaces effectively with both digital and analog ASICs and other industry standard devices. However, the AD6600 does provides the digitization portion of a three chip digital receiver architecture consisting of the AD6600, AD6620 and any of the ADI DSP family of processors. All chips are designed to gluelessly interface to one another, taking full advantage of Analog Devices' wide range of technologies. Together this chip set reduces board space and eases SAW filter requirements by implementing much of the channel filtering digitally within the AD6620.

Designed specifically for cellular/PCS receivers, the AD6600 is especially useful in applications where single RF channels must be processed, including GSM, CDMA, IS-136, wireless LAN and other proprietary air interfaces. The analog input to the AD6600 consists of two parallel attenuator stages; the attenuation levels are set by the on-chip automatic RSSI circuitry. Simple off chip filtering reduces the wideband noise presented to the ADC to minimize receiver noise figure.

The AD6600 uses many of the same core technologies introduced in the AD9042, 12 bit 41MSPS ADC resulting in extremely high dynamic range at high analog input frequencies. While intended primarily for "high IF" sampling, the AD6600 can be used in baseband applications. The minimum sample rate is tbd, due to T/H droop.

The AD6600 is built using Analog Devices' proprietary high speed complementary process. Units will be available in plastic surface mount packages (44 PQFP) and specified to operate over the industrial temperature range (-40°C to +85°C).

AD6600 BLOCK DIAGRAM



This information applies to a product which is currently in development. Characteristics and specifications are subject to change without notice. Consult factory for most current preliminary data sheet.

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AD6600-SPECIFICATIONS

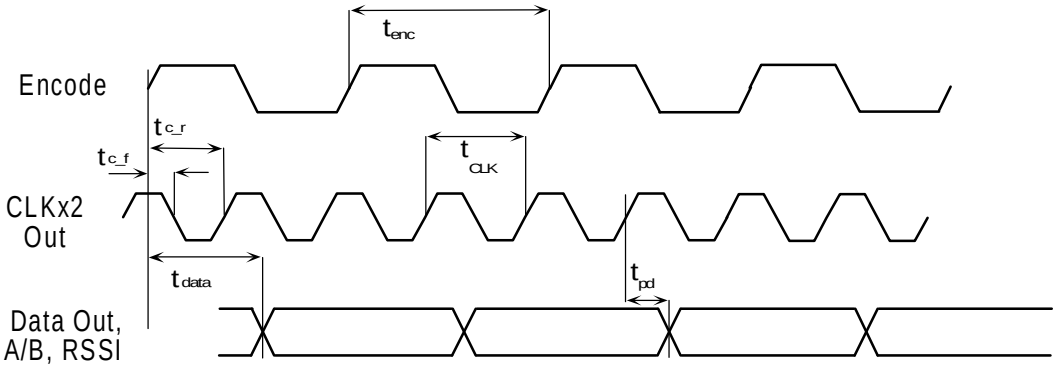
SPECIFICATIONS[1]

Parameter (Conditions)	Temp	Test Level	AD6600 Min	Typ	Max	Units
ANALOG INPUT						
Input Impedance[2]				200		ohms
Input Capacitance[2]				2		pF
Analog Input Bandwidth[3]				450		MHz
Analog Input Range[4]						V
70 MHz				2.1 ± 0.625		
250 MHz				2.7 ± 0.625		
Full-scale Input Power[4]						dBm
70 MHz				4.4		
250 MHz				6.6		
Gain Tolerance			-1		+1	dB
Range-Range Gain Tolerance						
70 MHz				.5		dB
250 MHz				.5		dB
RSSI Gain Step				6		dB
RSSI Hysterisis				6		dB
Gain Matching (Input A:B)				.5		dB
Range-Range Phase Tolerance						
70 MHz				.2@100 MHz		degree
250 MHz				.5@250 MHz		degree
Offset Error						
Attenuator 3OIP				+38		dBm
Noise[5]						
Minimum attenuation level				26		mVrms
Maximum attenuation level				735		mVrms
RESONANT PORT						
Port Resistance[6]				630		Ω
Port Capacitance[6]				2		pF/side
CONVERTER						
Resolution				11		Bits
Maximum Conversion Rate[7]			20			MSPS
Minimum Conversion Rate[8]					4	MSPS
Encode Duty Cycle						%
Aperture Uncertainty (jitter)				.3		pS
TIMING[9]						
tenc			50			nS
tc_f			4	5.5	7	nS
tc_r			(.25*tenc)+3.5		(.25*tenc)+10	nS
tclk				tenc/2		nS
tdata			(.25*tenc)+21		(.25*tenc)+31	nS
tpd			17.4		20.5	nS

1.
2. See input impedance graph in figure x.
3. See input band width graph in figure x.
4. See input full scale in figure x and resonant port performance chart y.
5. Thermal and quantization noise. Noise due to aperture uncertainty not included.
6. See Smith Chart of resonant port in figure x.
7. Minimum Conversion rate
8. Maximum Conversion rate
9. Timing is based on an internal synthesizer, therefore, propagation delay is a function of the period of the encode clock (tenc).

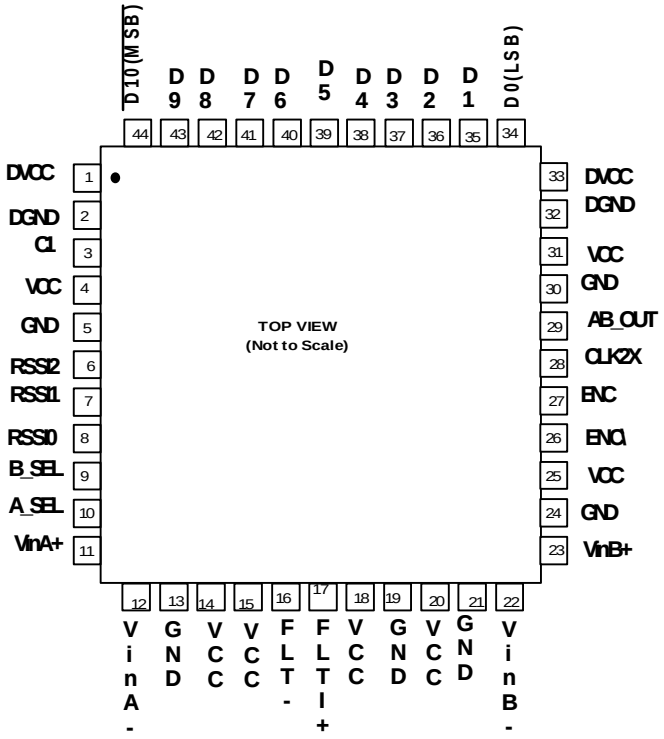
SYSTEM PERFORMANCE[1]					
SNR					
70 MHz			60		dB
150 MHz			59		dB
200 MHz			58		dB
250 MHz			57		dB
SINAD					
70 MHz			59		dB
150 MHz			58		dB
200 MHz			57		dB
250 MHz			56		dB
Worst Spur					
70 MHz			-70		dBc
150 MHz			-65		dBc
200 MHz			-60		dBc
250 MHz			-53		dBc
2nd Harmonic[2]					
70 MHz			-70		dBc
150 MHz			-65		dBc
200 MHz			-60		dBc
250 MHz			-53		dBc
3rd Harmonic					
70 MHz			-75		dBc
150 MHz			-70		dBc
200 MHz			-58		dBc
250 MHz			-50		dBc
Channel Isolation					
70 MHz			60		dB
150 MHz			57		dB
200 MHz			54		dB
250 MHz			50		dB
INTERFACE					
Logic Inputs[3]					
Logic Compatibility			TTL/CMOS		
Logic "1" Voltage		2.0			V
Logic "0" Voltage				0.8	V
Logic "1" Current		450	625	800	µA
Logic "0" Current		-400	-300	-200	µA
Input Capacitance			2.5		pF
Logic Outputs			CMOS/TTL		
5V Logic Compatibility					
Logic "1" V (I_{OH} = 10µA)		4.5	4.7		V
Logic "0" V (I_{OL} = 10µA)			0.35	0.50	V
3.3V Logic Compatibility					V
Logic "1" V (I_{OH} = 10µA)		2.8	3.0		
Logic "0" V (I_{OL} = 10µA)			0.2	0.50	
Output Coding			Twos Complement		
Total Icc Supply Current					
Analog Supply			150		mA
Digital Supply (3.3 volts)			15		mA
Power Dissipation			799		mW

1. Analog VCC +5V, Digital VCC +3.3V, Resonated to 200 MHz and Sample Rate is 20 MSPS unless otherwise stated.
2. Second harmonic depends on signal and amplitude matching
3.
4. Supply is 5 volt compliant.

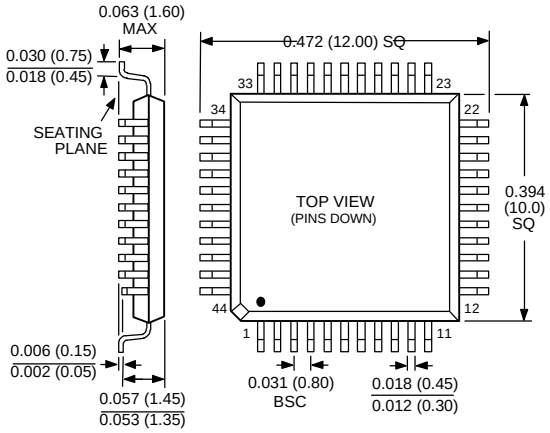


Input Signal Level (single ended)	RSSI	Equivalent 16 Bit Output Word															
Vin>=.5Vpp	101	B10\	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	0	0	0	0	0
.25Vpp<=Vin<.5Vpp	100	B10\	B10\	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	0	0	0	0
.125Vpp<=Vin<.25	011	B10\	B10\	B10\	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	0	0	0
.0625Vpp<=Vin</125	010	B10\	B10\	B10\	B10\	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	0	0
.03125Vpp<=Vin<.0625	001	B10\	B10\	B10\	B10\	B10\	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	0
Vin<.03125Vpp	000	B10\	B10\	B10\	B10\	B10\	B10\	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0

Output Data Format Table. See text below under RSSI Usage.



AD6600AST Pin Designations



AD6600 PACKAGE OUTLINE

AD6600 PIN DESCRIPTIONS

Pin No.	Name	Function
1, 33	DVCC	Digital VCC for Digital outputs. Can be +3.3V.
2, 32	DGND	Digital Ground for Digital outputs.
3	C1	Internal bias point. Bypass by .01 uF to GND.
4, 14, 15, 18, 20	VCC	+5 V power supply.
5, 13, 19, 21	GND	Ground.
6	RSSI2	Most significant bit of RSSI digital output bit.
7	RSSI1	RSSI digital output bit.
8	RSSI0	Least significant bit of RSSI digital output bit.
9, 10	B_SEL, A_SEL	Mode Select pins for analog input sampling. See text below.
11	VinA+	True Analog input A.
12	VinA-	Complimentary Analog Input A.
16, 17	FLT-, FLT+	External noise filter pins. See text.
22	VinB-	Complimentary Analog Input B.
23	VinB+	True Analog input B.
24	GND	Ground.
25	VCC	+5 V power supply.
26	ENC\	Complimentary Encode input.
27	ENC	True Encode input.
28	CLK2X	2 x clock output used for clocking digital filter chips.
29	AB_OUT	Digital output flag indicating whether output is input A (high) or B (low).
30	GND	Ground.
31	VCC	+5 V power supply.
34	D0	Digital data output bit (Least significant bit).
35 - 43	D1-D9	Digital data output bits.
44	D10	Digital data output bit (Most significant bit).

Analog and Digital Grounds should be connected together for optimal performance.

DEFINITIONS OF SPECIFICATIONS

Analog Bandwidth
The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis is reduced by 3 dB after the filter node has been resonated.

Gain Tolerance
Unit to unit variation in full scale power.

Range-Range Gain Tolerance
The gain error in the RSSI attenuator ladder from one range to the next. Ideally each gain step should be exactly 6 dB to correspond to the 1 bit data shift.

RSSI Gain Step
The input amplitude span between taps of the RSSI attenuator ladder. Ideally each stage should span 6 dB of input power.

RSSI Hysterisis
The amount of movement in the RSSI switch points depending on the direction of approach. Hysterisis prevents un-necessary RSSI toggling when input signal power is near a threshold.

Range-Range Phase Tolerance
The phase error in the RSSI attenuator ladder from one range to the next.

Gain Matching (Input A:B)
Variation in full scale power between the A and B inputs.

Port Resistance
The resistance shunted across the resonant port. Used to determine the filter bandwidth. Nominally 600 ohms.

Port Capacitance
The capacitance between each of the resonant pins to ground. Used to determine filter bandwidth and resonant frequency.

Maximum Conversion Rate
Then encode rate at which parametric testing is performed.

Minimum Conversion Rate
The encode rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

Encode Pulse Width/Duty Cycle
Pulse width high is the minimum amount of time that the ENCODE pulse should be left in logic “1” state to achieve rated performance; pulse width low is the minimum time ENCODE pulse should be left in low state. At a give clock rate, these specs define an acceptable Encode duty cycle.

Aperture Delay
The delay between the 50% point of the rising edge of the ENCODE command and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)
The sample-to-sample variation in aperture delay.

Differential Nonlinearity
The deviation of any code from an ideal 1 LSB step.

Integral Nonlinearity
The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a "best straight line" determined by a least square curve fit.

Output Propagation Delay
The delay between the 50% point of the rising edge of ENCODE command and the time when all output data bits are within valid logic levels.

Power Supply Rejection Ratio
The ratio of a change in input offset voltage to a change in power supply voltage.

Signal-to-Noise Ratio (without Harmonics)
The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, excluding the first five harmonics and dc.

Signal-to-Noise-and-Distortion (SINAD)
The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, including harmonics but excluding dc.

Worst Spur
The ratio of the rms signal amplitude to the rms value of the worst spurious component, reported in dBc.

2^{nd} Harmonic Distortion
The ratio of the rms signal amplitude to the rms value of the second harmonic component, reported in dBc.

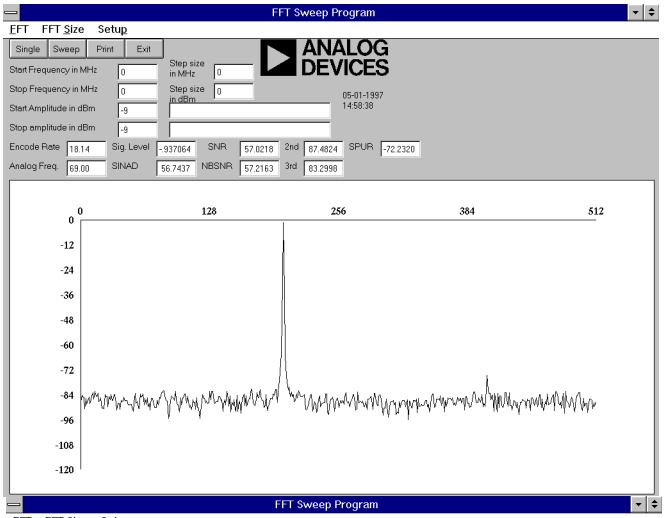
3^{rd} Harmonic Distortion
The ratio of the rms signal amplitude to the rms value of the third harmonic component, reported in dBc.

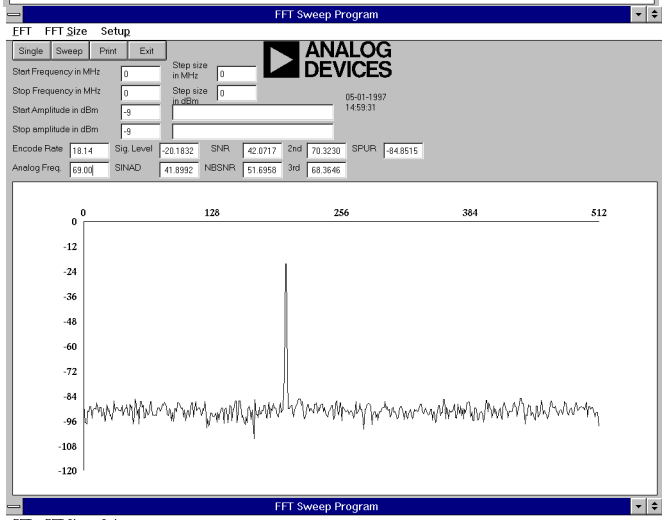
Channel Isolation
The ratio of the rms signal amplitude of the drive side to the rms signal amplitude of the non-driven side, reported in dB.

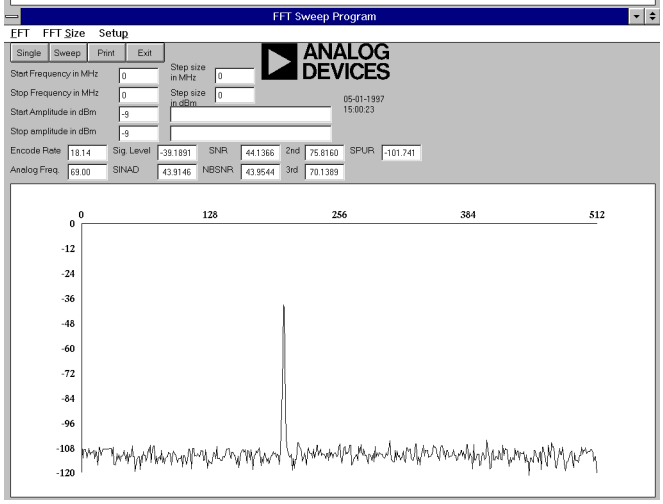
Spurious-Free Dynamic Range
The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic. May be reported in dBc (i.e., degrades as signal level is lowered), or in dBFS (always related back to converter full scale).

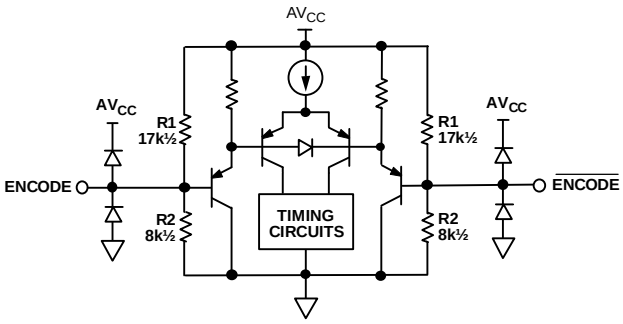
Two-Tone Intermodulation Distortion Rejection
The ratio of the rms value of either input tone to the rms value of the worst third order intermodulation product; reported in dBc.

Two-Tone SFDR
The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product. May be reported in dBc (i.e., degrades as signal level is lowered), or in dBFS (always related back to converter full scale).

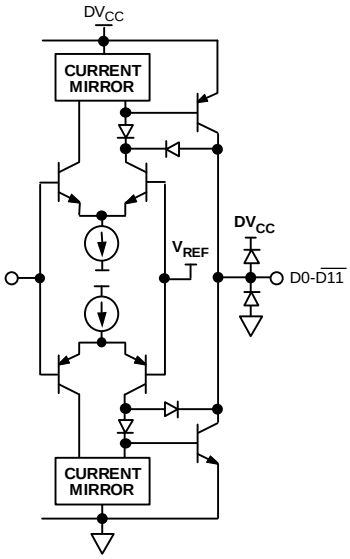








Encode Input Circuitry



Digital Output Driver

Freq	CH A Mag	CH A Phase	CH B Mag	CH B Phase
70	-24.3	-14.8	-25.9	-19.7
150	-22.8	-23.4	-23.9	-37.0
200	-21.8	-25.8	-23.3	-44.0
250	-21.0	-25.5	-22.6	-48.4
300	-20.6	-22.0	-22.2	-50.8

Typical Input Return Loss

THEORY OF OPERATION

The AD6600 Dual Channel, Gain Ranging ADC with RSSI (Receiver Signal Strength Indicator) is designed to bridge the gap between baseband digitization and high IF stages, eliminating a complete down conversion stage. The AD6600 consists of three stages. The first consists of a pair of 1 GHz phase compensated step attenuators followed by an output selection multiplexor. The second stage is a wide input bandwidth 11 bit ADC based on the AD9042. The third stage is a high speed synchronous peak detector and RSSI control interface. Together these on-chip systems form a high dynamic range IF sampling ADC. Before the operations of the chip are discussed, a detailed description of each sub-circuit are presented.

INPUT ATTENUATION

The input attenuator consists of two identical inputs. These dual inputs may be diversity channels, two independent IF signals or only one input may be used. The attenuation factor, controlled on chip switches between 0 and -30 dB is 6 dB steps. The matching between the gain settings is better than 0.5dB and maintains a bandwidth of almost 1 GHz so the phase delay is

small. Likewise the phase mismatches between different attenuator settings is very small, less than 0.2 degrees up to 200 MHz analog input. Additionally, the input impedance does not change with attenuator settings so there is no AM to PM distortion.

INPUT MODE

Since one ADC serves both attenuator inputs, two control pins are provided to select which attenuator is connected to the ADC. A_SEL and B_SEL arbitrate the selection of how these input channels are connected to the output. The table below shows the truth table for selection of the input.

Mode	A_SEL	B_SEL	Enc. n	Enc. n+1	Enc. n+2	Enc. n+3
alt A/B	1	1	ch. A	ch. B	ch. A	ch. B
A	1	0	ch. A	ch. A	ch. A	ch. A
B	0	1	ch. B	ch. B	ch. B	ch. B
invalid	0	0				

If both inputs are high, each encode clock alternates which attenuator is connected to the output and ultimately digitized by the wideband ADC.

In mode 10, only the A input is connected to the output. Likewise, mode 01 only connects the B input to the output. Mode 00 is invalid.

The digital output AB_OUT indicates which input is currently available on the digital output. When the AB_OUT is 0, the digital output is the digitized version of the B input. Likewise, when AB_OUT is 1, the A input is available on the digital output.

RSSI FUNCTIONALITY

The Input attenuator is controlled by the on chip RSSI (receive strength signal indicator). The RSSI peak detector function consists of a high speed comparator bank. The peak detector has five reference points, with each reference point being 6 dB lower than the previous one. A regenerative positive feedback comparator is tied to each point and referenced to full-scale of the A/D converter. Once one of the comparators is tripped it stays in the state until it is reset by the falling edge of the encode. The 5 comparator outputs are decoded into a 3 bit word that is used to select the proper attenuation. Six dB of digital hysterisis is used to eliminate level uncertainty at the threshold points due to noise and amplitude variations. The peak detector monitors both positive and negative excursions of the input signal to accurately track complex modulated signals.

RSSI USAGE

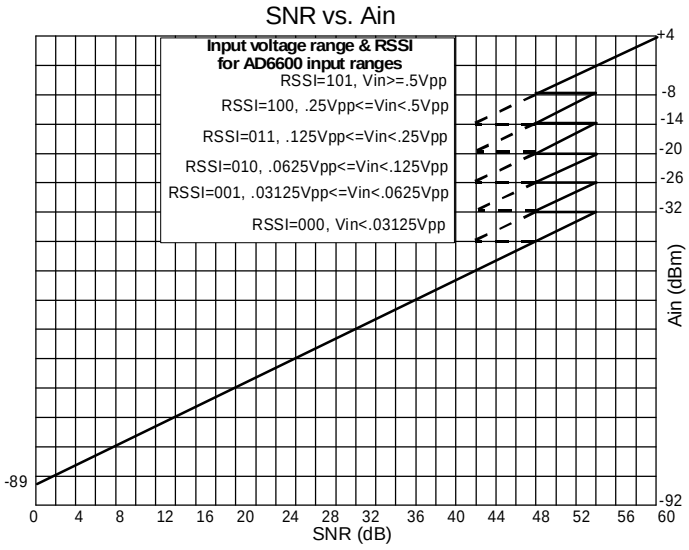
The RSSI follows the IF envelop one clock cycle before the conversion is made. During this time period, the RSSI watches for the signal peaks and prior to digitization, the RSSI word is set to the appropriate attenuation factor to prevent the ADC from over-ranging on the following conversion cycle. The RSSI always allows an extra 6 dB of ADC headroom to prevent clipping if the signal power has increased unexpectedly. This is true until the last attenuator is selected. Then the ADC will clip in a normal manner. The RSSI word is made available to read via the RSSI pins. Hysterisis prevents un-necessary gain fluctuations during signal acquisition.

The 11 bit ADC output forms the mantissa of a binary floating point word, while the RSSI the exponent. See Output Data Format table above. This table shows how the RSSI data can be interpreted using a programmable logic device (PLD). The logic diagram of an example PLD is available upon request by contacting the factory. Basically, the PLD performs a right shift of the data depending on the RSSI word. This can also be performed in software using the following code fragment.

```
r0=dm(rssi);
r2=5;
r0=r2-r0;
r1=dm(adc);(11 bits, MSB justified into DSP word)
rshift r1, r0;(arithmatic shift to extend the sign bit)
```

The results of the shifted data is a 16 bit fixed point word that can be used as any normal 16 bit word. As the gain range changes, less that .2 degree of phase error results. In terms of amplitude error, matching is maintained to 11 bits, the resolution of the ADC itself.

The AD6620, the matching digital decimating digital receiver, performs the necessary data conversion from floating point to fixed point. In applications which use the AD6620, this allows for simple hardware interfacing. However, if this device is not used, the floating point data can be interpreted using a DSP, PLD or ASIC.



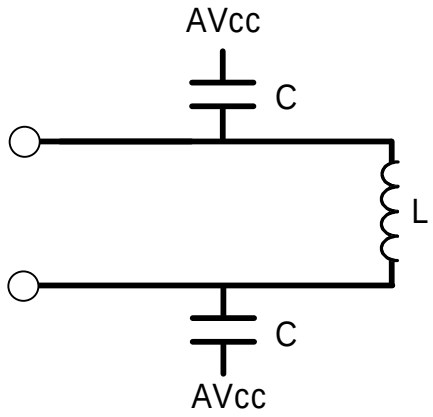
The graph above shows the SNR performance expected from the AD6600 based on analog input level. As seen, the gain ranging keeps the SNR performance in the 48 dB range for a wide range of inputs.

EXTERNAL ANALOG FILTER

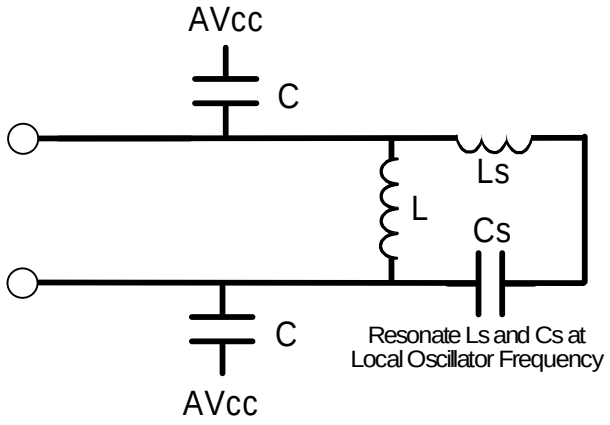
Since the analog front end has a bandwidth of nearly one gigahertz and the ADC a bandwidth of 500 MHz, a filter is

required to bandwidth limit the wideband noise out of the attenuator and MUX stage. This simple external LC filter is tuned to the chosen IF frequency and is designed to settle quickly between clock cycles. If a band pass filter is required, the following should be used. R is the internal load resistor and equals 600 ohms nominally. To expedite settling between samples, an internal clamp circuit is utilized to discharge the filter. This minimizes feed through between inputs because of the natural time constant of the resonant network.

Center Frequencies > 50 MHz



If local oscillator feed through is a problem, an additional series LC tuned to the LO frequency will aid in the suppression of LO feed through as shown below.



The filter is placed between the FLT+ and FLT- pins of the AD6600.

DESIGNING THE ANALOG FILTER

The first step is to determine what the parasitics are on the filter pins of the AD6600. This includes the internal parasitics plus the layout dependent values. This can be done by building the board up without the resonant components installed (L and C). Sweeping the frequency from DC (or some low frequency) and determining the 3 dB frequency. Without the resonant circuit, the parasitics form a RC low pass filter, from which the 3 dB frequency can be used to determine the parasitic capacitance.

The filter node is configured differentially, thus using a half circuit model of the filter node, the internal R is found to be 300 ohms typically. The parasitic capacitance to ground is therefore calculated by the following:

$$C = \frac{1}{2*pi*R*BW}$$

Where R is 300 ohms and BW is the 3 dB bandwidth of the basic board layout. In a typical layout, such as found on the evaluation board, parasitic capacitance is about 5 pF, giving an un-resonated bandwidth of about 106 MHz.

Bandwidth selection is a trade-off between minimized aliased noise and envelope settling. If the envelope is not allowed to settle to a reasonable point, signal compression will result. However, after a few time constants, little is lost in terms of dB compression. The trade off between bandwidth and envelop settling is given by:

$$BW = \frac{\ln 2^{n}}{2*pi*(2/fs)}$$

Where BW is the desired bandwidth, n is the number of bits that the envelop settles to (in terms of relative accuracy) and FS is the sample rate. In general, n need only be 3 to 4 bits of accuracy. This is not overall converter accuracy or quantization, but relative accuracy of the envelop at the filter node. Thus, with a sample rate of 13 MSPS (a period of 76 nS), 38 nS is the allowed settling time (one half the period). If 4 bits of amplitude accuracy is required, the bandwidth must be 11.6 MHz. If the bandwidth is made too narrow, the RSSI will respond to the correct amplitude but because of the time constant of the noise limiting filter, the ADC will have reduced amplitude.

With an IF frequency of 170 MHz, this is a Q of 14.6. If more accuracy is desired, a wider bandwidth can be used at the expense of noise, or if less noise is required, then a narrower bandwidth can be used at the expense of amplitude compression. In general, the widest bandwidth should be used that provides the required noise performance.

Now that bandwidth is chosen, the external C can be calculated. If a slightly larger bandwidth is chosen, perhaps 15 MHz, then C is found to be 35 pF. Since parasitic capacitance is already 5 pF, 30 pF per filter pin is required. This capacitance should be between each filter pin and analog Vcc. This causes any supply noise to common mode the differential inputs and minimize performance degradation.

Finally, once the total capacitance is determined, the inductor can be determined, again by the half circuit model:

$$f_o = \frac{1}{2pi\sqrt{LC}}$$

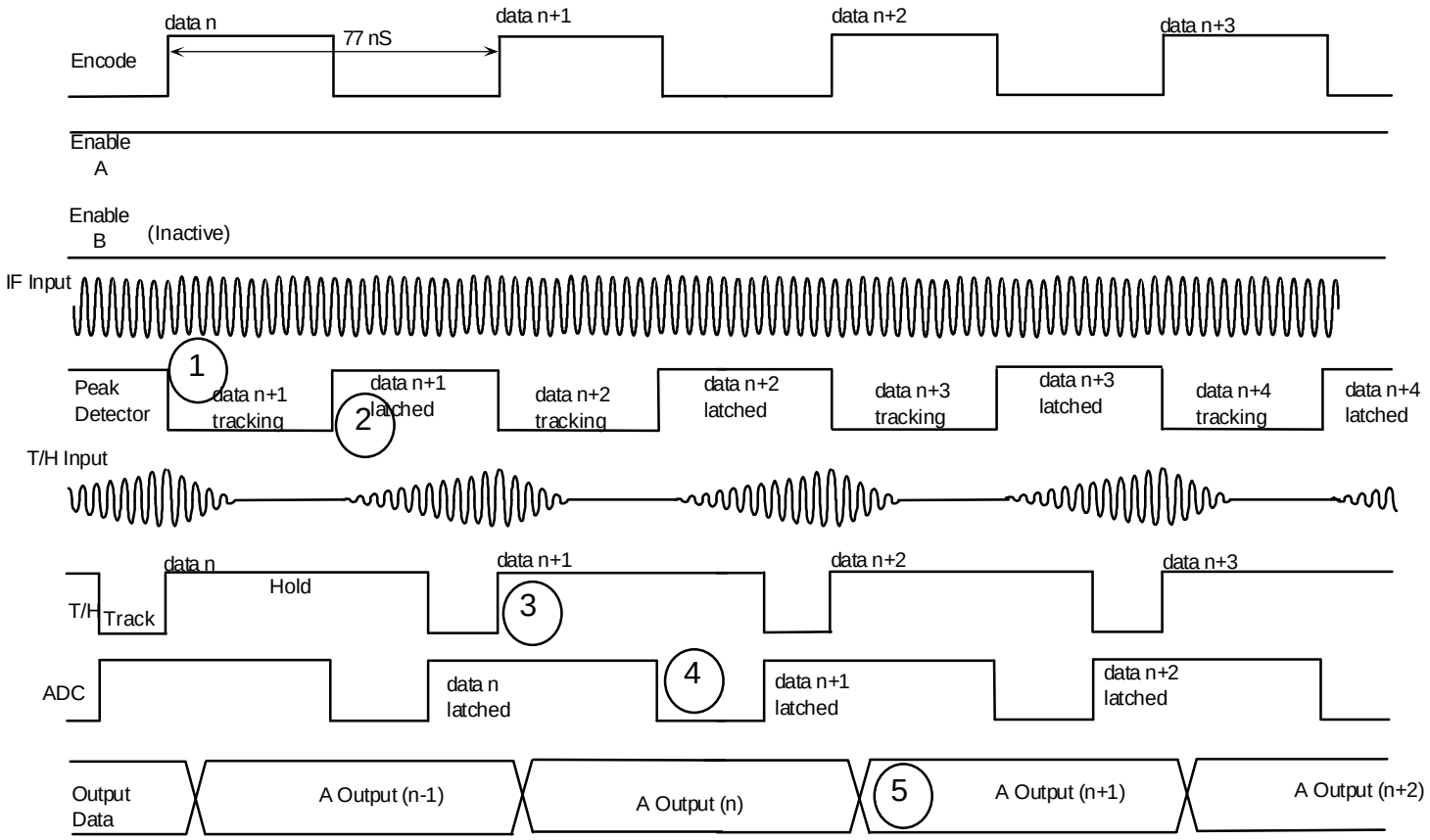
Therefore to resonate our circuit to 170 MHz, our capacitance is 35 pF, therefore, the half circuit inductance is 25 nH. Since the inductance is placed between the filter pins, the whole circuit

value must be used, or 50 nH. High quality chip inductors should be used such as Coilcraft part number 1008CS.

ADC OPERATION

The ADC is based on the high dynamic range AD9042. The ADC input is designed to take advantage of the excellent small signal linearity's of the track and hold. Therefore the full scale input to the ADC section is 50 mV peak to peak. Other than this, the ADC section behave much as any other ADC. The integrated on-board track and hold is followed by an integrated gain block with a gain of 4 to increase the signal level to a level suitable for digitization with the 11 bit ADC. The track and hold has an input bandwidth of 450 MHz allowing accurate digitization of common IF frequencies up to 250 MHz. Once the signal is sampled with the track and hold, the frequency of the signal is reduced by the aliasing properties of the sampling process.

AD6600 Timing Diagram



AD6600 Digital Output Timing (13 MSPS example)

AD6600 OPERATIONS

The timing diagram above shows the internal sequencing of the AD6600. For ease of understanding, this discussion assumes that the mode select pins are set so that only the A input is selected (10). Details of operations follow.

During the time that the encode signal is high, the peak detector tracks the IF input, see reference point 1 above. Since the AD6600 is designed as a super-Nyquist converter, at least one cycle of the input sinusoid should occur while the encode is low. This allows the peak detector to see both the positive and negative excursions of the input signal. If one complete cycle occurs during the input low time, this means that the minimum analog input for proper conversion is approximately twice the sample rate. Therefore for a 20 MSPS encode, the minimum analog IF frequency would be 40 MHz.

When the encode signal returns low, the peak detector value is latched and the appropriate input range is determined. This information is then used to set the channel A input attenuator. At the same time the gain block that follows the attenuators is enabled. This allows the desired signal to begin feeding the external LC filter network and Track and Hold input. The settling time of this signal is defined previously in the text. The Track and Hold is also placed into track and allowed to track the signal as it stabilizes. Then on the next rising edge of the encode, the Track and Hold is placed into hold and samples its input at point 3.

On the next falling edge of the encode input, the ADC samples the Track and Hold output and the digital word is formed. This data is transferred to the digital output at point 5. The RSSI data for the ADC output is also latched at this time to the output, thus producing an 11 bit mantissa and a 3 bit exponent.

In applications where A and B alternate (mode 11), the input is alternated between the two inputs. The data rate per channel is reduced to one half of the clock rate.

Aperture Jitter

One of the key concerns when performing IF sampling is that of aperture jitter or aperture uncertainty. Aperture Uncertainty is the sample to sample variation in the encode process. Aperture uncertainty has three residual effects, the first is an increase in system noise, the second is an uncertainty in the actual phase of the sampled signal itself and third is inter-symbol interference. Since aperture uncertainty is less than 1 pS, the latter two have very little effect.

In terms of phase accuracy and inter-symbol interference the effects of jitter are small. Even in a worst case scenario of 1 pS rms. and an IF of 250 MHz, effects are quite minimal. In this case, the phase uncertainty or error is 0.09 degrees rms. This is much less than even a demanding specification such as GSM. Therefore, jitter effects on time domain specs are minimal and focus will be on overall noise contribution due to jitter.

Jitters Contribution to Overall System Performance

In oversampling converters such as the AD6600, clock purity is of extreme importance. As with the mixing process, the input signal is multiplied by local oscillator or sampling clock in the example. Since multiplication in time is convolution in the frequency domain, the spectrum of the sample clock is convolved with the spectrum of the input signal. Of course since an ADC is a sampling system, the spectrum is periodic about FS.

Therefore, since jitter often shows up as wideband noise on the sample clock, this wideband noise gets convolved with the analog input raising the noise floor performance of the ADC. The theoretical SNR for an ADC as limited by aperture jitter is determined by the following equation.

$$SNR = -20\log\left[\left(2\pi F_{ana\log} t_{j_{rms}}\right)^2\right]^{1/2}$$

When evaluated at 201 MHz and .7 pS jitter, the theoretical SNR is limited to 61 dB. Therefore, in systems that require very high dynamic range and very high analog input frequencies also require a very low jitter encode source. When using standard clock oscillators modules, 0.7 pS rms. has been verified for both the ADC and oscillator. Better numbers can be achieved with low noise modules.

When considering overall system performance, a more generalized equation may be used. This equation builds on the previous equation but includes the effects of thermal noise (NF) and differential non-linearity.

$$SNR = -20\log\left[\left(2\pi F_{ana\log} t_{j_{rms}}\right)^2 + \left(\frac{1+\varepsilon}{2^{11}}\right)^2 + \left(\frac{v_{noise_{rms}}}{2^{11}}\right)^2\right]^{1/2}$$

$F_{ana\log}$ = Analog IF Frequency

$t_{j_{rms}}$ = Effective Aperture uncertainty

ε = average dnl of converter (~.4 lsb)

$v_{noise_{rms}}$ = thermal noise in lsbs.

Although this is a simple equation, it provide much insight into the noise performance that can be expected from a data converter.

AD6600 Noise Considerations in Digital Receivers

Noise considerations in a digital receiver must take special considerations, since noise in even a band limited system will often cover more than one Nyquist range (Sample Rate/2). As a consequence, wideband noise is aliased back into band.

The AD6600 is a complete IF sampling system, not just a sampler. Therefore, in addition to the sampled noise, there is a front-end noise figure. When an analog system is integrated with a digital system, there is often a lot of confusion about how to consider the effects of noise such a system. The following section will specifically address this issue and in particular, applying the AD6600 in such a manner.

The analog front end of the AD6600 consists of a gain ranging amplifier which provides a worst case noise of 12.2 $nV/\sqrt{Hz}$ and 800 MHz of signal bandwidth. However, if 800 MHz of noise were allowed to pass into the ADC, the total integrated noise at the ADC would be about 345 uV which would severely limit chip SNR. Therefore, the LC filter network between the gain ranging stage and the ADC serve to limit the wideband noise delivered to the ADC.

Because the ADC is shared between the two channels, main and diversity, the filter must have a time constant that will allow sufficient settling between channels. This prevents un-wanted signal leakage between samples. To facilitate this, the AD6600 incorporates a clamp that discharges the LC filter between samples. Since the LC filter acquires the signal from the same voltage each sample, cross channels effects are eliminated within the filter.

The band pass filter therefore removes about 750 MHz of noise by allowing only about 50 MHz of noise to pass. From the three dB signal bandwidth of 50 MHz, the noise bandwidth can be calculated. Since the filter rolls off at 12 dB/octave, text book evaluations usually allow for a relative bandwidth increase pi/2 to account for the integrated noise in the filter skirts. Therefore, when accounting for total integrated noise in the bandwidth specified,

$$12.2\,{nV}/{\sqrt{Hz}} \times \left(\frac{p}{2} 50\times 10^{6}\right)^{\frac{1}{2}} = 108mV$$

In addition to gain ranging thermal noise, the ADC also exhibits input referred thermal noise. The quantizer in the AD6600 has about 79 uV of thermal noise. Combining the gain range noise and the ADC thermal noise gives:

$$\sqrt{(108mV)^2 + (79mV)^2} = 134mV\ .$$

On the smallest analog input range, an LSB is 86 uV rms. Thus, the input referred thermal noise is $134 \div 86$ or 1.56 lsbs.

The final contribution to noise is quantization noise. This basic noise is introduced by all ADC and is defined by the equation:

$$\frac{2\sqrt{2}}{\sqrt{12}} = .816 lsb$$

Therefore, total noise from all sources in the AD6600 (thermal and quantization) are found to be:

$$\sqrt{(1.56)^2 + (.816)^2} = 1.76 lsb$$

The ADC in the AD6600 is an 11 bit converter and will all noise sources in lsbs, the SNR can then be calculated.

$$20\log\left(\frac{2^{11}}{1.76}\right) = 61.3 dB$$

Since the AD6600 employs a unique gain ranging circuit which improves the SNR by 30 dB, the effective SNR is actually -91.2 dB (-61.2-30). This effectively creates an ADC which has nearly the noise performance of a 16 bit converter.

Process Gain

When considering the effects of digital processing, an additional SNR improvement is provided. Process gain is effective because digitally, out of band noise and spurious are removed. Only the inband channel noise remains. Thus, the SNR is effectively improved beyond that of the analog performance.

In a typical GSM application, the AD6600 may be used in diversity mode with a 13 MSPS clock. This effectively samples each IF input at 6.5 MSPS. When considering this GSM channel, the amount of process gain is calculated by:

$$\Pr ocess_gain = 10\log(3.25/.1) = 15.1 dB$$

Therefore, total SNR in this GSM application is 61.3+15.1 or 76.4 dB plus 30 dB of additional dynamic range from the gain ranging.

In a simple CDMA application with a sample rate of 19.6608 MSPS, process gain is found to be 12 dB providing an overall ADC SNR to 73.3 dB, again with an additional 30 dB of dynamic range from the gain ranging.

In a simple AMPS configuration, the sample rate is like to be 20.48 MSPS. With a channel bandwidth of 25.6 kHz, process gain will be 29 dB. ADC SNR for this example will be 90.3 dB, with 30 dB of additional dynamic range.

Noise Figure

Since we have already calculated the SNR for various applications, these can be used to calculate noise figure. The first step is to convert these SNR numbers into a noise voltage. Then this can be used in comparison with the input noise into the 200 ohm input resistance.

From above, the SNR was 76.4, 73.3 and 90.3 for GSM, CDMA and AMPS respectively. Based on the rearranged SNR equation below, the input referred noise voltages are, 107 uV, 153 uV and 21.6 uV respectively.

$$V_{noise} = \frac{V_{rms}}{10^{SNR/20}}$$

V_{noise} = effective front end noise

V_{rms} = full-scale range of AD6600 in rms. volts (.707)

With the noise voltages calculated, the noise figure may then be computed using the following equation:

$$NF(db) = 10\log\left(1 + \frac{V_{noise}^{\ 2}}{KTBR}\right)$$

V_{noise} = AD6600 input referred noise

K = Boltzmann Constant (1.380659E-23J/K)

T = Absolute temperature (300K)

B = Bandwidth

R = Input resistance of AD6600 (200 ohms)

Therefore, evaluation of this expression again with respect to our various noise voltages gives effective noise figures of 48.4, 43.6 and 43.4 dB respectively.

HARMONIC PLACEMENT

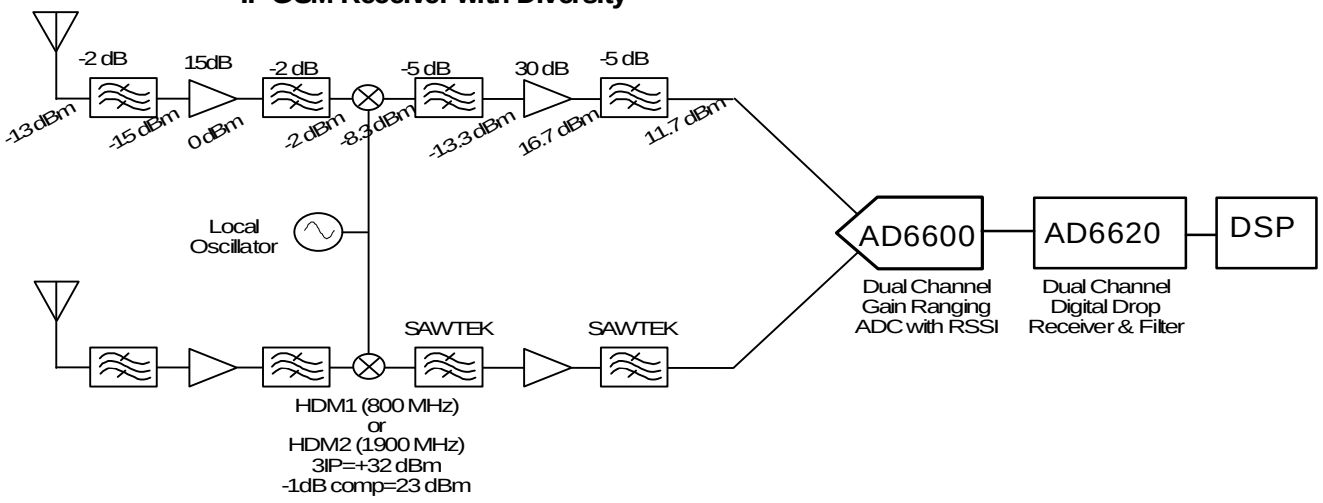
Since the AD6600 is designed to sample IF frequencies using up to a 20 MSPS clock, some of the advantages of undersampling can be exploited. For example, if the analog input signal range is placed in a higher Nyquist zone, the drive amplifier is no longer required to meet the harmonic performance required by the system specifications since all harmonics would fall outside the passband filter. For additional information, see the SAW filter examples in later text. This effectively passes much of the burden from the amplifier to the filter design. In many applications, this is a worthwhile tradeoff since many complex filters can easily be realized using SAW, LCR and digital techniques at these relatively high IF frequencies. Although harmonic performance of the drive amplifier is relaxed by this technique, intermodulation performance cannot be sacrificed since intermods must be assumed to fall in-band for both amplifiers and converters.

Another property that can be exploited is through the use of aliasing the ADC harmonics out of band. Once the IF signal is sampled by the track and hold, the frequency of the input signal will be converted to a signal in the first Nyquist zone. Any harmonics of the ADC and track and hold will become relative to the frequency of the signal as it appears in the first Nyquist zone. Therefore by carefully selecting where the IF signal falls within the first Nyquist zone, the second and third harmonics can be aliased out of band if needed where they can be easily filtered with a digital filter such as the AD6620. For example, by carefully selecting the encode rate and signal frequency, the second and third harmonics can be placed out-of-band. For the case of an encode rate equal to 13.0 MSPS and a signal bandwidth of 400 kHz, placing the fundamental at 4.5 MHz places the second and third harmonics out of band as shown in the table below.

Encode Rate:	13.0 MSPS
Fundamental:	4.5 -4.9 MHz
Second Harmonic:	4.0 - 3.2 MHz
Third Harmonic:	.5 - 1.7 MHz

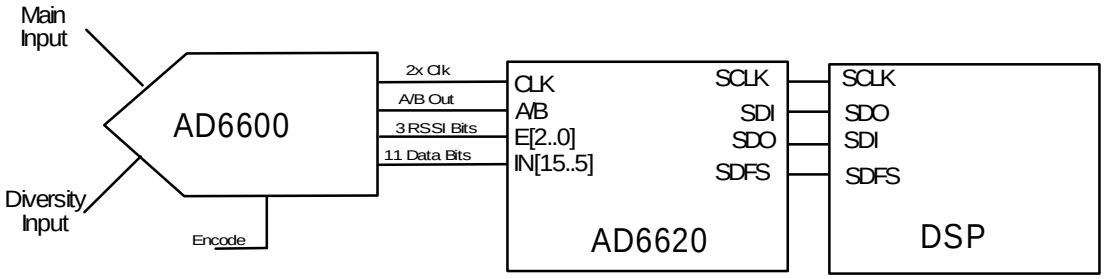
By careful selection of the encode rate and analog input frequency, the harmonics of the ADC can be placed out of band. This allows decimation and FIR filtering to remove only the signals of interest while filtering the remaining spurious performance of the ADC.

IF GSM Receiver with Diversity

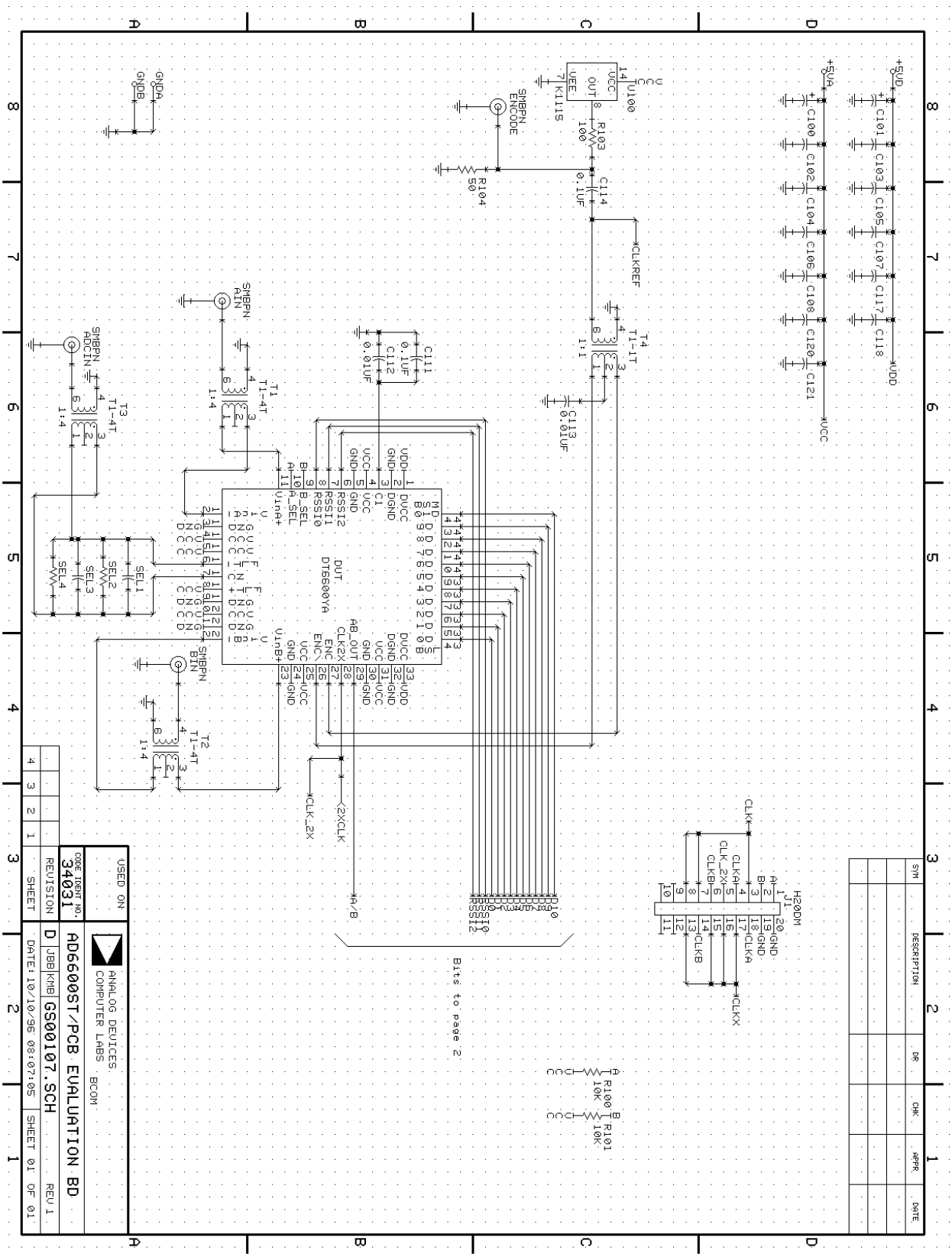


GSM RF Front End Review with the AD6600

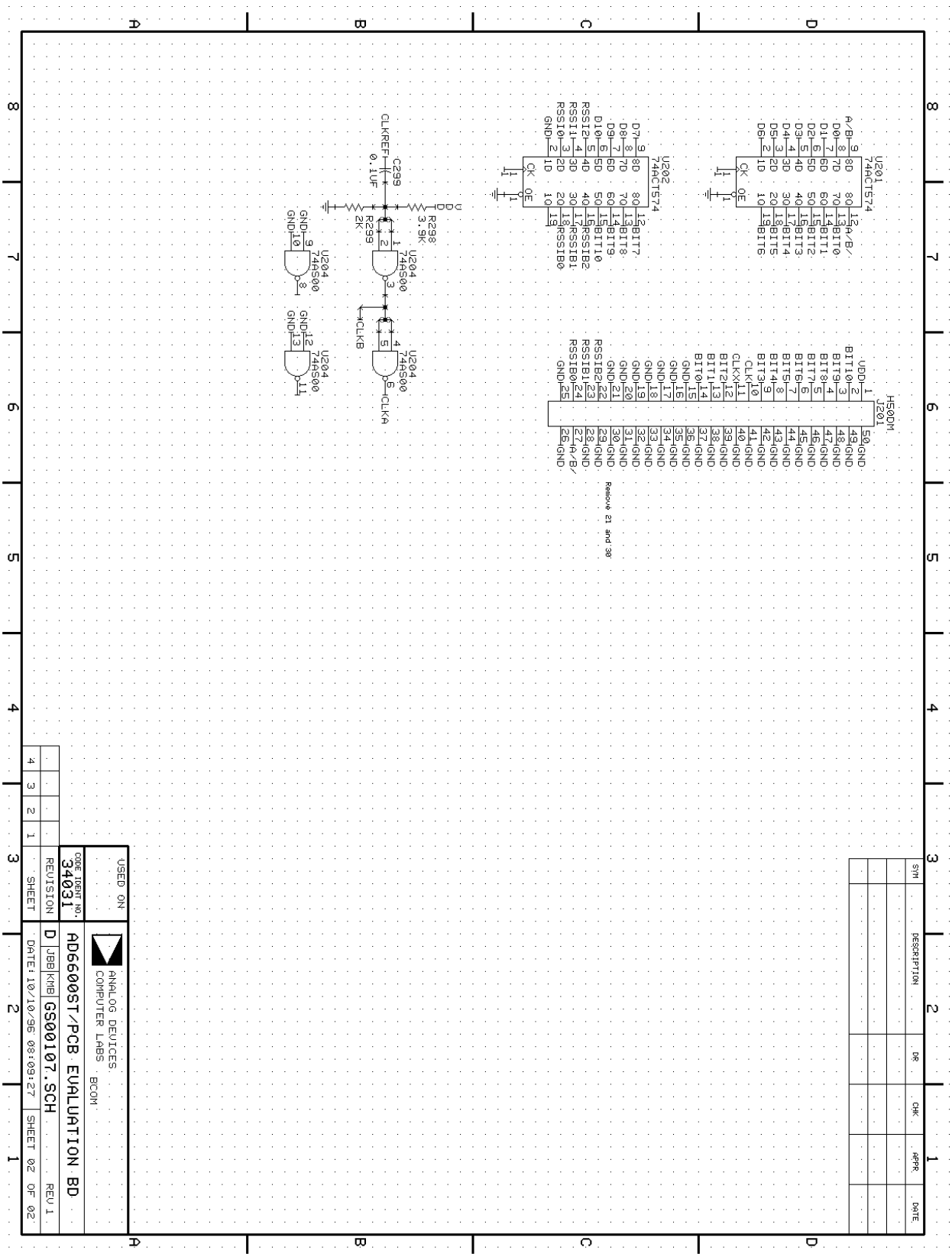
Reference Design Information Available for GSM, CDMA and PHS



Typical AD6600 Application with AD6620 and DSP



AD6600 Evaluation Board Schematic



AD6600 Evaluation Board Schematic