4-Channel, 1.5 MSPS, 12-& 10-Bit Parallel ADCs with a Sequencer

Preliminary Technical Data

AD7934/AD7933

FEATURES

Fast Throughput Rate: 1.5 MSPS
Specified for V_{DD} of 2.7 V to 5.25 V
Low Power:
8 mW max at 1.5 MSPS with 3V Supplies
16 mW max at 1.5 MSPS with 5V Supplies
4 Analog Input Channels with a Sequencer
Software Configurable Analog Inputs:
4-Channel Single Ended Inputs
2-Channel Fully Differential Inputs
2-Channel Pseudo Differential Inputs
Accurate On-chip 2.5 V Reference
Wide Input Bandwidth:
70dB SNR at 50kHz Input Frequency
No Pipeline Delays
High Speed Parallel Interface - Word/Byte Modes
Full Shutdown Mode: 1µA max
28 Lead TSSOP Package

GENERAL DESCRIPTION

The AD7934/AD7933 are 12- & 10-bit, high speed, low power, successive approximation (SAR) ADCs. The parts operate from a single 2.7 V to 5.25 V power supply and feature throughput rates up to 1.5 MSPS. The parts contain a low noise, wide bandwidth, differential track/hold amplifier that can handle input frequencies up to 3.5MHz.

The AD7934/AD7933 feature 4 analog input channels with a channel sequencer to allow a consecutive sequence of channels to be converted on. These parts can accept either Single-ended, Fully Differential or Pseudo Differential analog inputs.

The conversion process and data acquisition are controlled using standard control inputs allowing easy interfacing to Microprocessors and DSPs. The input signal is sampled on the falling edge of $\overline{\text{CONVST}}$ and the conversion is also initiated at this point.

The AD7934/AD7933 has an accurate on-chip 2.5 V reference that can be used as the reference source for the analog to digital conversion. Alternatively, this pin can be overdriven to provide an external reference.

These parts use advanced design techniques to achieve very low power dissipation at high throughput rates. They also feature flexible power management options. An on-chip Control register allows the user to set up different operating conditions including analog input range and configuration, output coding, power management and channel sequencing.

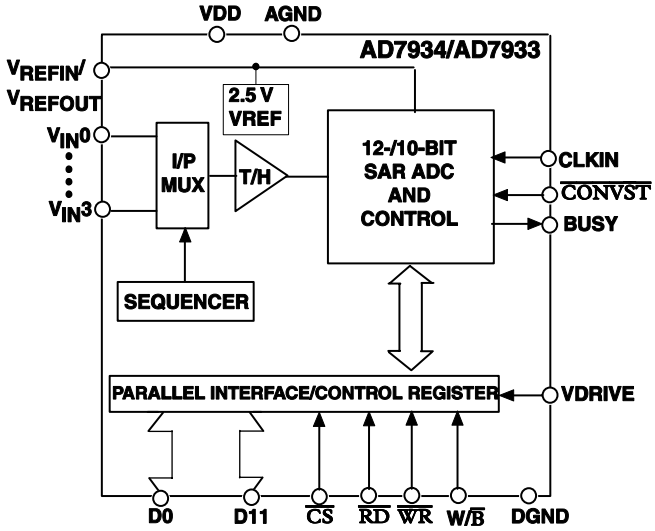

Figure 1. Functional Block Diagram

PRODUCT HIGHLIGHTS

1. High Throughput with Low Power Consumption.
2. Four Analog Inputs with a Channel Sequencer.
3. Accurate on-chip 2.5 V reference.
4. Software Configurable Analog Inputs. Single-Ended, Pseudo Differential or Fully Differential analog inputs that are software selectable.
5. Single-supply Operation with V_{DRIVE} Function. The V_{DRIVE} function allows the parallel interface to connect directly to 1.8 V, 3V or 5 V processor systems independent of V_{DD}.
6. No Pipeline Delay.
7. Accurate control of the sampling instance via a $\overline{\text{CONVST}}$ input and once off conversion control.

Rev. PrF

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REVISION HISTORY

Revision PrF: Initial Version

SPECIFICATIONS

AD7934–SPECIFICATIONS

V_{DD} = V_{DRIVE}=2.7 V to 5.25V, Internal/External V_{REF} = 2.5V unless otherwise noted, F_{CLKIN} = 24MHz, F_{SAMPLE} = 1.5 MSPS; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	B Version[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE			F_{IN}=50kHz Sine Wave
Signal to Noise + Distortion[2] (SINAD)	70	dB min	
Signal to Noise Ratio (SNR)[2]	70	dB min	
Total Harmonic Distortion (THD)[2]	–75	dB max	–80dB typ
Peak Harmonic or Spurious Noise (SFDR)[2]	–75	dB max	–82dB typ
Intermodulation Distortion (IMD)[2]			fa = 40.1kHz, fb = 51.5kHz
Second Order Terms	–85	dB typ	
Third Order Terms	–85	dB typ	
Aperture Delay[2]	5	ns typ	
Aperture Jitter[2]	50	ps typ	
Full Power Bandwidth[2, 3]	20	MHz typ	@ 3 dB
	2.5	MHz typ	@ 0.1 dB
DC ACCURACY			
Resolution	12	Bits	
Integral Nonlinearity[2]	± 1	LSB max	
Differential Nonlinearity[2]	± 0.95	LSB max	Guaranteed No Missed Codes to 12 Bits.
Total Unadjusted Error	TBD	LSB max	
Single Ended & Pseudo Differential Input			Straight Binary Output Coding
Offset Error[2]	± 4.5	LSB max	
Offset Error Match[2]	± 0.5	LSB max	
Gain Error[2]	± 2	LSB max	
Gain Error Match[2]	± 0.6	LSB max	
Fully Differential Input			Twos Complement Output Coding
Positive Gain Error[2]	± 2	LSB max	
Positive Gain Error Match[2]	± 0.6	LSB max	
Zero Code Error[2]	± 3	LSB max	
Zero Code Error Match[2]	± 1	LSB max	
Negative Gain Error[2]	± 1	LSB max	
Negative Gain Error Match[2]	± 0.5	LSB max	
ANALOG INPUT			
Single Ended Input Range	0 to V_{REF} or 0 to 2 x V_{REF}	V	Depending on RANGE bit in the control register
Pseudo Differential Input Range: V_{IN+}	0 to V_{REF} or 2 x V_{REF}	V	Depending on RANGE bit in the control register
V_{IN-}	-0.1 to 0.4	V	
Fully Differential Input Range: V_{IN+} and V_{IN-}	V_{CM} ± V_{REF}/2	V	V_{CM} = Common Mode Voltage = V_{REF}/2
V_{IN+} and V_{IN-}	V_{CM} ± V_{REF}	V	Only when V_{DD} = 4.75 V to 5.25 V. V_{CM} = V_{REF}
DC Leakage Current[4]	± 1	µA max	
Input Capacitance	45/10	pF typ	When in Track/Hold
REFERENCE INPUT/OUTPUT			
V_{REF} Input Voltage	2.5[5]	V	±1% Specified Performance

[1] Temperature ranges as follows: B Versions: –40°C to +85°C.
[2] See Terminology Section.
[3] Analog inputs with slew rates exceeding 27V/µs (full-scale input sine wave > 3.5MHz) within the acquisition time may cause an incorrect result to be returned by the converter
[4] Guaranteed by characterization
[5] This device is operational with an external reference in the range 0.1 V to 3.5 V in differential mode and 0.1V to V_{DD} in pseudo differential and single ended modes. See the Reference Section for more information.

Parameter	B Version[1]	Units	Test Conditions/Comments
DC Leakage Current	± 1	µA max	
V_{REF} Input Impedance	10	kΩ typ	
V_{REFOUT} Output Voltage	2.5	V	± 0.1% @ 25°C
V_{REFOUT} Tempco	15	ppm/°C typ	
V_{REF} Noise	10	µV typ	0.1Hz to 10Hz Bandwidth
	130	µV typ	0.1Hz to 1MHz Bandwidth
V_{REF} Output Impedance	10	Ω typ	
V_{REF} Input Capacitance	15/25	pF typ	When in Track/hold
LOGIC INPUTS			
Input High Voltage, V_{INH}	2.4	V min	V_{DRIVE} = 2.7 V to 5.25 V
	0.8 x V_{DRIVE}	V min	V_{DRIVE} < 2.7V
Input Low Voltage, V_{INL}	0.8	V max	V_{DRIVE} = 2.7 V to 5.25 V
	0.2 x V_{DRIVE}	V max	V_{DRIVE} < 2.7V
Input Current, I_{IN}	± 1	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DRIVE}
Input Capacitance, C_{IN} [4]	10	pF max	
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	2.4	V min	I_{SOURCE}= 200 µA; V_{DRIVE}= 2.7 V to 5.25 V
	V_{DRIVE} – 0.2	V min	I_{SOURCE}= 200 µA; V_{DRIVE} < 2.7 V
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK}=200µA
Floating-State Leakage Current	±10	µA max	
Floating-State Output Capacitance[4]	10	pF max	
Output Coding	Straight (Natural) Binary		CODING bit in the control register set to 0.
	2s Complement		CODING bit in the control register set to 1.
CONVERSION RATE			
Conversion Time	$t_2 + 13\ t_{clk} + t_{20}$	ns	
Track/Hold Acquisition Time	135	ns max	Full Scale Step input.
Throughput Rate	1.5	MSPS max	
POWER REQUIREMENTS			
V_{DD}	2.7/5.25	V min/max	
V_{DRIVE}	3.6 /5.25	V min/max	V_{DD} = 3.6 V to 5.25 V
	1.6/3.6	V min/max	V_{DD} = 2.7 V to 3.6 V
I_{DD} [6]			Digital I/Ps = 0V or V_{DRIVE}.
Normal Mode(Static)	0.5	mA typ	V_{DD}= 2.7V to 5.25V. SCLK on or off.
Normal Mode (Operational)	3.2	mA max	V_{DD}= 4.75V to 5.25V.
	2.6	mA max	V_{DD}= 2.7V to 3.6V.
Auto StandBy Mode	1.55	mA typ	F_{sample} = 250kSPS
	90	µA max	(Static)
Auto Shutdown Mode	1	mA typ	F_{sample} = 250kSPS
	1	µA max	(Static)
Full Shut-Down Mode	1	µA max	SCLK On or Off.
Power Dissipation			
Normal Mode (Operational)	16	mW max	V_{DD}= 5V.
	8	mW max	V_{DD}= 3V.
Auto Standby-Mode (Static)	450	µW max	V_{DD}= 5V.
	270	µW max	V_{DD}= 3V.
Auto Shutdown-Mode (Static)	5	µW max	V_{DD}= 5V.
	3	µW max	V_{DD}= 3V.
Full Shutdown-Mode	5	µW max	V_{DD}= 5V.
	3	µW max	V_{DD}= 3V.

[6] Measured with a midscale dc input.

AD7933–SPECIFICATIONS

V_{DD} = V_{DRIVE}=2.7 V to 5.25V, Internal/External V_{REF} = 2.5V unless otherwise noted, F_{CLKIN} = 24MHz, F_{SAMPLE} = 1.5MSPS; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	B Version[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE			F_{IN}=50kHz Sine Wave
Signal to Noise + Distortion (SINAD)[2]	60	dB min	
Signal to Noise Ratio (SNR)[2]	60	dB min	
Total Harmonic Distortion (THD) [2]	–73	dB max	
Peak Harmonic or Spurious Noise [2] (SFDR)	–73	dB max	
Intermodulation Distortion (IMD) [2]			fa = 40.1kHz, fb = 51.5kHz
Second Order Terms	–75	dB typ	
Third Order Terms	–75	dB typ	
Aperture Delay[2]	5	ns typ	
Aperture Jitter[2]	50	ps typ	
Full Power Bandwidth[2,3]	20	MHz typ	@ 3 dB
	2.5	MHz typ	@ 0.1 dB
DC ACCURACY			
Resolution	10	Bits	
Integral Nonlinearity[2]	± 0.5	LSB max	
Differential Nonlinearity[2]	± 0.5	LSB max	Guaranteed No Missed Codes to 10 Bits.
Total Unadjusted Error	TBD	LSB max	
Single Ended and Pseudo Differential Input			Straight Binary Output Coding
Offset Error[2]	± 4.5	LSB max	
Offset Error Match[2]	± 0.5	LSB max	
Gain Error[2]	± 2	LSB max	
Gain Error Match[2]	± 0.6	LSB max	
Fully Differential Input			Twos Complement Output Coding Offset
Positive Gain Error[2]	± 2	LSB max	
Positive Gain Error Match[2]	± 0.6	LSB max	
Zero Code Error[2]	± 3	LSB max	
Zero Code Error Match[2]	±1	LSB max	
Negative Gain Error[2]	± 1	LSB max	
Negative Gain Error Match[2]	± 0.5	LSB max	
ANALOG INPUT			
Single Ended Input Range	0 to V_{REF} or 0 to 2 x V_{REF}	V	Depending on RANGE bit in the control register
Pseudo Differential Input Range: V_{IN+}	0 to V_{REF} or 2 x V_{REF}	V	Depending on RANGE bit in the control register
V_{IN-}	-0.1 to 0.4	V	
Fully Differential InputRange: V_{IN+} and V_{IN-}	V_{CM} ± V_{REF}/2	V	V_{CM} = Common Mode Voltage = V_{REF}/2
V_{IN+} and V_{IN-}	V_{CM} ± V_{REF}	V	Only when V_{DD} = 4.75 V to 5.25 V. V_{CM} = V_{REF}
DC Leakage Current[4]	± 1	µA max	
Input Capacitance	45/10	pF typ	When in Track/Hold
REFERENCE INPUT/OUTPUT			
V_{REF} Input Voltage	2.5[5]	V	±1% Specified Performance
DC Leakage Current[4]	± 1	µA max	
V_{REF} Input Impedance	10	kΩ	
V_{REFOUT} Output Voltage	2.5	V	± 0.1% @ 25°C

[1] Temperature ranges as follows: B Versions: –40°C to +85°C
[2] See terminology section
[3] Analog inputs with slew rates exceeding 27V/µs (full-scale input sine wave >3.5MHz) within the acquisition time may cause an incorrect conversion result to be returned by the converter
[4] Guaranteed by characterization
[5] This device is operational with an external reference in the range 0.1 V to 3.5 V in differential mode and 0.1V to V_{DD} in pseudo differential and single ended modes. See the Reference Section for more details.

Parameter	B Version[1]	Units	Test Conditions/Comments
V_{REFOUT}Tempco	15	ppm/°C typ	
V_{REF} Noise	10	µV typ	0.1Hz to 10Hz Bandwidth
	130	µV typ	0.1Hz to 1MHz Bandwidth
V_{REF} Output Impedance	10	Ω typ	
V_{REF} Input Capacitance	15/25	pF typ	When in Track/hold
LOGIC INPUTS			
Input High Voltage, V_{INH}	2.4	V min	V_{DRIVE} = 2.7 V to 5.25 V
	0.8 x V_{DRIVE}	V min	V_{DRIVE} < 2.7V
Input Low Voltage, V_{INL}	0.8	V max	V_{DRIVE} = 2.7 V to 5.25 V
	0.2 x V_{DRIVE}	V max	V_{DRIVE} < 2.7V
Input Current, I_{IN}	± 1	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DRIVE}
Input Capacitance, C_{IN} [4]	10	pF max	
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	2.4	V min	I_{SOURCE}= 200 µA; V_{DRIVE}= 2.7 V to 5.25 V
	V_{DRIVE} – 0.2	V min	I_{SOURCE}= 200 µA; V_{DRIVE} < 2.7 V
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK}=200µA
Floating-State Leakage Current	±10	µA max	
Floating-State Output Capacitance [4]	10	pF max	
Output Coding	Straight (Natural) Binary		CODING bit in the control register set to 0.
	2s Complement		CODING bit in the control register set to 1.
CONVERSION RATE			
Conversion Time	$t_2 + 13\ t_{clk} + t_{20}$	ns	
Track/Hold Acquisition Time	135	ns max	Full Scale Step input
Throughput Rate	1.5	MSPS max	
POWER REQUIREMENTS			
V_{DD}	2.7/5.25	V min/max	
V_{DRIVE}	3.6 /5.25	V min/max	V_{DD} = 3.6 V to 5.25 V
	1.6/3.6	V min/max	V_{DD} = 2.7 V to 3.6 V
I_{DD}[6]			Digital I/Ps = 0V or V_{DRIVE}.
Normal Mode(Static)	0.5	mA typ	V_{DD}= 2.7V to 5.25V. SCLK on or off.
Normal Mode (Operational)	3.2	mA max	V_{DD}= 4.75V to 5.25V.
	2.6	mA max	V_{DD}= 2.7V to 3.6V.
Auto StandBy Mode	1.55	mA typ	F_{sample} = 250kSPS
	90	µA max	(Static)
Auto Shutdown Mode	1	mA typ	F_{sample} = 250kSPS
	1	µA max	(Static)
Full Shut-Down Mode	1	µA max	SCLK On or Off.
Power Dissipation			
Normal Mode (Operational)	16	mW max	V_{DD}= 5V.
	8	mW max	V_{DD}= 3V.
Auto Standby-Mode (Static)	450	µW max	V_{DD}= 5V.
	270	µW max	V_{DD}= 3V.
Auto Shutdown-Mode (Static)	5	µW max	V_{DD}= 5V.
	3	µW max	V_{DD}= 3V.
Full Shutdown-Mode	5	µW max	V_{DD}= 5V.
	3	µW max	V_{DD}= 3V.

[6] Measured with a midscale dc input.

TIMING SPECIFICATIONS[1]

(V_{DD} = V_{DRIVE}=2.7 V to 5.25V, Internal/External V_{REF} = 2.5V unless otherwise noted, F_{CLKIN} = 24MHz, F_{SAMPLE} = 1.5MSPS; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Table 3.

	Limit at T_{MIN}, T_{MAX}			
Parameter	**AD7934**	**AD7933**	**Units**	**Description**
f_{CLKIN}[2]	10	10	kHz min	
	24	24	MHz max	
t_{quiet}	10	10	ns min	Minimum time between conversions (i.e. time from when the data bus goes into three-state until the next falling edge of $\overline{CONVST}$)
t_1	10	10	ns min	$\overline{CONVST}$ pulsewidth
t_2	20	20	ns min	$\overline{CONVST}$ falling edge to CLKIN falling edge setup time
t_3	Tbd	Tbd	ns min	CLKIN falling edge to BUSY rising edge
t_4	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ setup time
t_5	0	0	ns max	$\overline{CS}$ to $\overline{WR}$ hold time
t_6	25	25	ns min	$\overline{WR}$ Pulse Width
t_7	10	10	ns min	Data Setup time before $\overline{WR}$
t_8	5	5	ns min	Data Hold after $\overline{WR}$
t_9	1/2 t_{CLKIN}	1/2 t_{CLKIN}	ns min	New data valid before falling edge of BUSY
t_{10}	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ setup time
t_{11}	0	0	ns max	$\overline{CS}$ to $\overline{RD}$ hold time
t_{12}	55	55	ns min	$\overline{RD}$ Pulse Width
t_{13} [3]	50	50	ns max	Data access time after $\overline{RD}$
t_{14} [4]	5	5	ns min	Bus relinquish time after $\overline{RD}$
	40	40	ns max	Bus relinquish time after $\overline{RD}$
t_{15}	15	15	ns min	HBEN to $\overline{RD}$ setup time
t_{16}	5	5	ns min	HBEN to $\overline{RD}$ hold time
t_{17}	10	10	ns min	Minimum time between Reads/Writes
t_{18}	0	0	ns min	HBEN to $\overline{WR}$ setup time
t_{19}	5	5	ns max	HBEN to $\overline{WR}$ hold time
t_{20}	Tbd	Tbd	ns min	CLKIN falling edge to BUSY rising edge

[1] Guaranteed by characterization. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 Volts. All timing specifications given above are with a 25pF load capacitance. See Figure 2, Figure 3, Figure 4 and Figure 5.
[2] Mark/Space ratio for CLKIN is 40/60 to 60/40.
[3] The time required for the output to cross TBD.
[4] t_{14} is derived from the measured time taken by the data outputs to change 0.5 V. The measured number is then extrapolated back to remove the effects of charging or discharging the 25 pF capacitor. This means that the time, t_{14} quoted in the timing characteristics is the true bus relinquish time of the part and is independent of the bus loading.

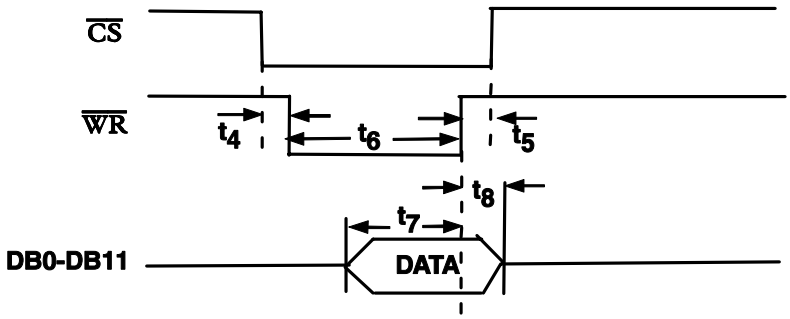

Figure 2. AD7934/AD7933 Parallel Interface – Write Cycle timing for Word Mode Operation (W/$\overline{B}$ = 1)

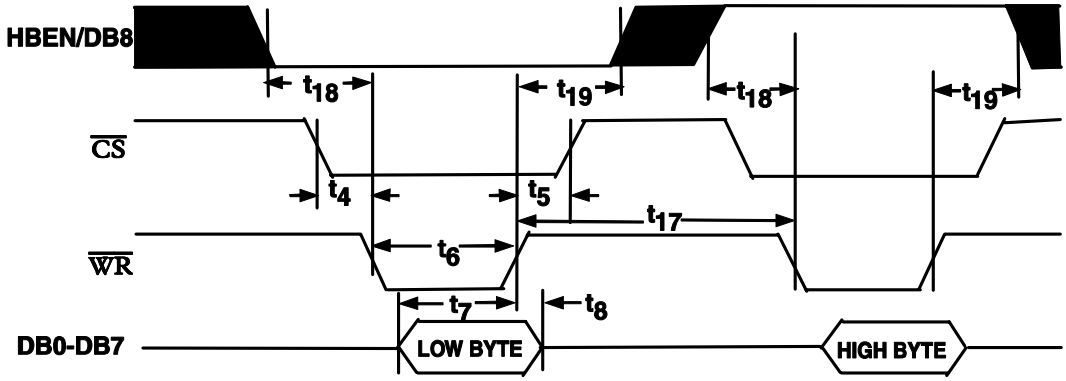

Figure 3. AD7934/AD7933 Parallel Interface - Write Cycle Timing for Byte Mode Operation (W/$\overline{B}$ = 0)

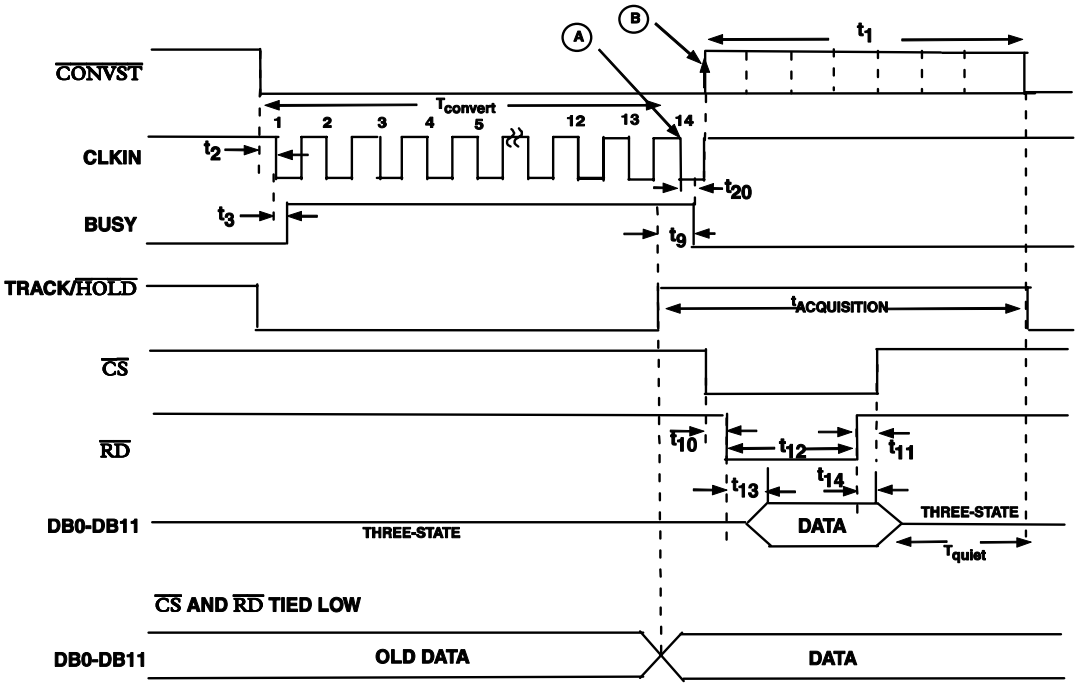

Figure 4. AD7934/AD7933 Parallel Interface - Conversion and Read Cycle in Word Mode (W/$\overline{B}$ = 1)

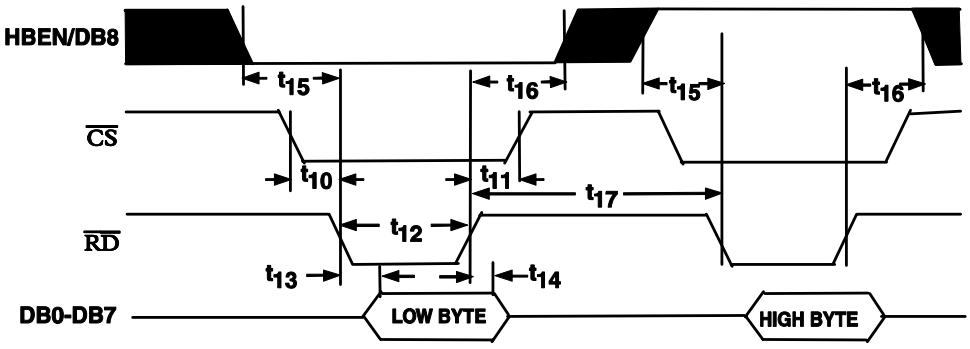

Figure 5. AD7934/AD7933 Parallel Interface - Read Cycle Timing for Byte Mode Operation (W/$\overline{B}$ = 0)

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

Table 4.

Parameter	Rating
V_{DD} to AGND/DGND	–0.3 V to 7 V
V_{DRIVE} to AGND/DGND	–0.3 V to 7 V
Analog Input Voltage to AGND	–0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to DGND	–0.3 V to 7 V
V_{DRIVE} to V_{DD}	–0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to AGND	–0.3 V to V_{DD} + 0.3 V
V_{REFIN} to AGND	–0.3 V to V_{DD} + 0.3 V
Input Current to Any Pin Except Supplies[1]	±10 mA
Operating Temperature Range	
Commercial (B Version)	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	+150°C
θ_{JA} Thermal Impedance	97.9°C/W (TSSOP)
θ_{JC} Thermal Impedance	14°C/W (TSSOP)
Lead Temperature, Soldering	
Vapor Phase (60 secs)	+215°C
Infared (15 secs)	+220°C
ESD	2kV

[1] Transient currents of up to 100 mA will not cause SCR latch up.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Caution

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTION

PIN CONFIGURATION

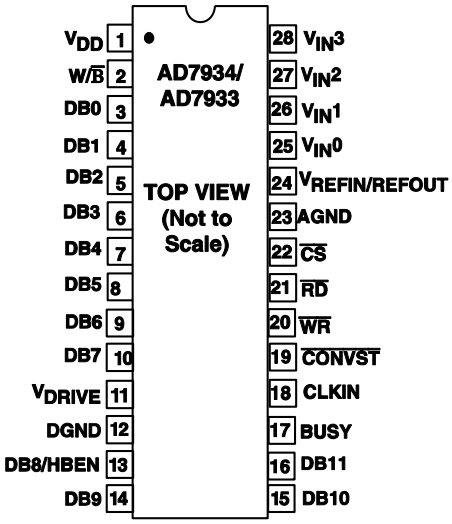

Figure 6. Pin Configuration

Table 5. Pin Configuration

Pin no.	Pin Mnemonic	Function
1	V_{DD}	Power Supply Input. The V_{DD} range for the AD7934/AD7933 is from +2.7V to +5.25V. The supply should be decoupled to AGND with a 0.1µF capacitor and a 10µF tantalum capacitor.
2	W / $\overline{B}$	Word/Byte Input. When this input is logic high, data is transferred to and from the AD7934/AD7933 in 12/10-bit words on pins DB0/2 to DB11. When this pin is logic low, byte transfer mode is enabled. Data and the channel ID is transferred on pins DB0 to DB7 and pin DB8/HBEN assumes its HBEN functionality.
3-10	DB0 to DB7	Data Bits 0 to 7. Three state parallel digital I/O pins that provide the conversion result and also allows the Control register to be programmed. These pins are controlled by $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$. The logic high/low voltage levels for these pins are determined by the V_{DRIVE} input. When reading from the AD7933, the two LSBs (DB0 and DB1) are always zero and the LSB of the conversion result is available on DB2.
11	V_{DRIVE}	Logic Power Supply Input. The voltage supplied at this pin determines at what voltage the parallel interface of the AD7934/AD7933 will operate.
12	DGND	Digital Ground. This is the ground reference point for all digital circuitry on the AD7934/AD7933. The DGND and AGND voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
13	DB8/HBEN	Data Bit 8/High Byte Enable. When W/$\overline{B}$ is high, this pin acts as Data Bit 8, a three state I/O pin that is controlled by $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$. When W/$\overline{B}$ is low, this pin acts as the high byte enable pin. When HBEN is low, the low byte of data being written to or read from the AD7934/AD7933 is on DB0 to DB7. When reading from the AD7933 the two LSBs in the low byte are zeros, followed by 6 bits of conversion data. When HBEN is high, the top 4 bits of the data being written to or read from the AD7934/AD7933 are on DB0 to DB3. When reading from the device, DB4 of the high byte will always be zero and DB5 and DB6 will contain the ID of the channel for which the conversion result corresponds (See Channel Address Bits in Table 8). When writing to the device, DB4 to DB7 of the high byte must be all zeros.
14-16	DB9 to DB11	Data Bits 9 to 11. Three state parallel digital I/O pins that provide the conversion result and also allows the Control register to be programmed in Word Mode. These pins are controlled by $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$. The logic high/low voltage levels for these pins are determined by the V_{DRIVE} input.
17	BUSY	Busy Output. Logic output indicating the status of the conversion. The BUSY output goes high following the falling edge of $\overline{CONVST}$ and stays high for the duration of the conversion. Once the conversion is complete and the result is available in the output register, the BUSY output will go low. The track/hold returns to track mode just prior to the falling edge of BUSY and the acquisition time for the part begins when BUSY goes low.
18	CLKIN	Master Clock Input. The clock source for the conversion process is applied to this pin. Conversion time for the AD7934/AD7933 takes 13.5 clock cycles. The frequency of the master clock input therefore determines the conversion time and achievable throughput rate.

Pin no.	Pin Mnemonic	Function
19	$\overline{\text{CONVST}}$	Conversion Start Input. A falling edge on $\overline{\text{CONVST}}$ is used to initiate a conversion. The track/hold goes from track to hold mode on the falling edge of $\overline{\text{CONVST}}$ and the conversion process is initiated at this point. Following powerdown, when operating in the Auto-shutdown or Auto Standby mode, a rising edge on $\overline{\text{CONVST}}$ is used to power up the device.
20	$\overline{\text{WR}}$	Write Input. Active low logic input used in conjunction with $\overline{\text{CS}}$ to write data to the Control register.
21	$\overline{\text{RD}}$	Read Input. Active low logic input used in conjunction with $\overline{\text{CS}}$ to access the conversion result. The conversion result is placed on the data bus following the falling edge of $\overline{\text{RD}}$ read while $\overline{\text{CS}}$ is low.
22	$\overline{\text{CS}}$	Chip Select. Active low logic input used in conjunction with $\overline{\text{RD}}$ and $\overline{\text{WR}}$ to Read conversion data or to Write data to the Control register.
23	AGND	Analog Ground. This is the ground reference point for all analog circuitry on the AD7934/AD7933. All analog input signals and any external reference signal should be referred to this AGND voltage. The AGND and DGND voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
24	V_{REFIN}/V_{REFOUT}	Reference Input/Output. This pin is connected to the internal reference and is the reference source for the ADC. The nominal internal reference voltage is 2.5 V and this appears at this pin. This pin can be overdriven by an external reference. The input voltage range for the external reference is 0.1 V to 3.5 V for differential mode and is 0.1 V to V_{DD} in single ended and pseudo differential mode, depending on V_{DD}.
25-28	$V_{IN}0 – V_{IN}3$	Analog Input 0 to Analog Input 3. Four analog input channels that are multiplexed into the on-chip track/hold. The analog inputs can be programmed to be four single ended inputs, two fully differential pairs or two pseudo differential pairs by setting the MODE bits in the Control register appropriately (see Table 8). The analog input channel to be converted can either be selected by writing to the Address bits (ADD1 and ADD0) in the control register prior to the conversion, or the on-chip sequencer can be used. The input range for all input channels can either be 0 V to V_{REF} or 0 V to 2 x V_{REF} and the coding can be binary or two's complement, depending on the states of the RANGE and CODING bits in the Control register. Any unsed input channels should be connected to AGND to avoid noise pickup.

TERMINOLOGY

Integral Nonlinearity

This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point 1 LSB below the first code transition, and full scale, a point 1 LSB above the last code transition.

Differential Nonlinearity

This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error

This is the deviation of the first code transition (00 . . .000) to (00 . . . 001) from the ideal, i.e. AGND + 1 LSB

Offset Error Match

This is the difference in offset error between any two channels.

Gain Error

This is the deviation of the last code transition (111 . . .110) to (111 . . . 111) from the ideal (i.e., V_{REF} – 1 LSB) after the offset error has been adjusted out.

Gain Error Match

This is the difference in Gain error between any two channels.

Zero Code Error

This applies when using the 2's complement output coding option, in particular to the 2 x V_{REF} input range with -V_{REF} to +V_{REF} biased about the V_{REFIN} point. It is the deviation of the mid scale transition (all 0s to all 1s) from the ideal V_{IN} voltage, i.e. V_{REF} – 1 LSB.

Zero Code Error Match

This is the difference in Zero Code Error between any two channels.

Positive Gain Error

This applies when using the 2's complement output coding option, in particular to the 2 x V_{REF} input range with -V_{REF} to +V_{REF} biased about the V_{REFIN} point. It is the deviation of the last code transition (011. . .110) to (011 .. . 111) from the ideal (i.e., +V_{REF} – 1 LSB) after the Zero Code Error has been adjusted out.

Positive Gain Error Match

This is the difference in Positive Gain Error between any two channels.

Negative Gain Error

This applies when using the 2's complement output coding option, in particular to the 2 x V_{REF} input range with – V_{REF} to +V_{REF} biased about the V_{REF} point. It is the deviation of the first code transition (100 . . . 000) to (100 . . . 001) from the ideal (i.e., – V_{REFIN} + 1 LSB) after the Zero Code Error has been adjusted out.

Negative Gain Error Match

This is the difference in Negative Gain Error between any two channels.

Channel-to-Channel Isolation

Channel-to-Channel Isolation is a measure of the level of crosstalk between channels. It is measured by applying a fullscale sine wave signal to all 3 nonselected input channels and applying a 50kHz signal to the selected channel. The channel to channel isolation is defined as the ratio of the power of the 50kHz signal on the selected channel, to the power of the noise signal that appears in the FFT of this channel.

PSRR (Power Supply Rejection Ratio)

The power supply rejection ratio is defined as the ratio of the power in the ADC output at full-scale frequency, f, to the power of a 100mV p-p sine wave applied to the ADC V_{DD} supply of frequency fs. The frequency of the input varies from 1kHz to 1MHz.

$$PSRR\ (dB) = 10log(Pf/Pfs)$$

Pf is the power at frequency f in the ADC output; *Pfs* is the power at frequency fs in the ADC output.

Track/Hold Acquisition Time

The track/hold amplifier returns into track mode and the end of conversion. Track/Hold acquisition time is the time required for the output of the track/hold amplifier to reach its final value, within ±1/2 LSB, after the end of conversion.

Signal to (Noise + Distortion) Ratio (SINAD)

This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the sum of all non-fundamental signals up to half the sampling frequency (fs/2), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

Signal to (Noise + Distortion) = (6.02 N + 1.76) dB

Thus for a 12-bit converter, this is 74 dB and for a 10-bit converter, this is 62 dB.

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7934/AD7933, it is defined as:

$$THD(dB) = -20\log\frac{\sqrt{V_2^{\,2} + V_3^{\,2} + V_4^{\,2} + V_5^{\,2} + V_6^{\,2}}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise

Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to fs/2 and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it will be a noise peak

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

The AD7934/AD7933 is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dBs.

TYPICAL PERFORMANCE CHARACTERISTICS AD7934/AD7933

PERFORMANCE CURVES

Ta = 25°C, unless otherwise noted

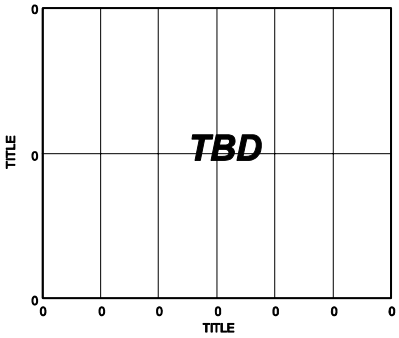

Figure 7. PSRR versus Supply ripple Frequency without supply decoupling

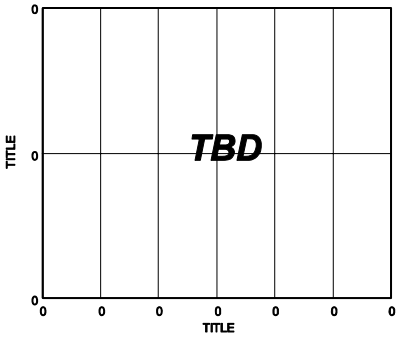

Figure 8. Channel to Channel Isolation

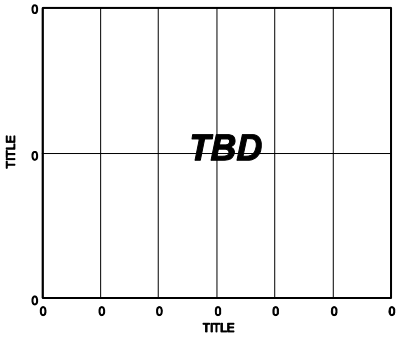

Figure 9. AD7934 SINAD vs Analog Input Frequency for various Supply Voltages

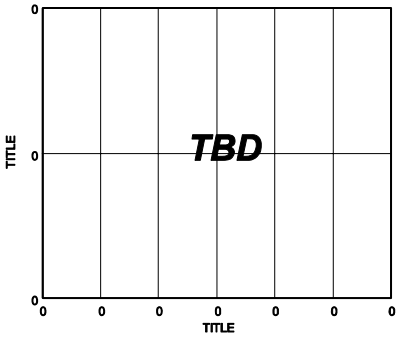

Figure 10. AD7934 FFT @ V_{DD}=5V

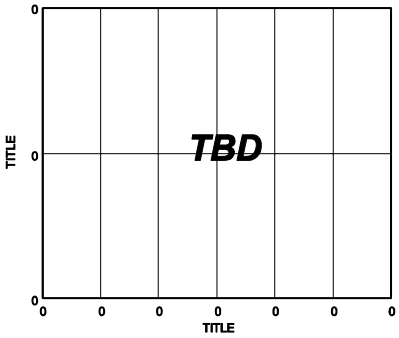

Figure 11. AD7934 Typical DNL @ V_{DD}=5V

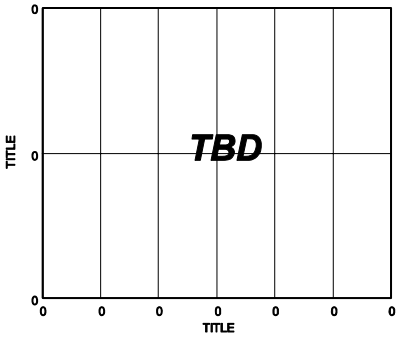

Figure 12. AD7934 Typical INL @ V_{DD}=5V

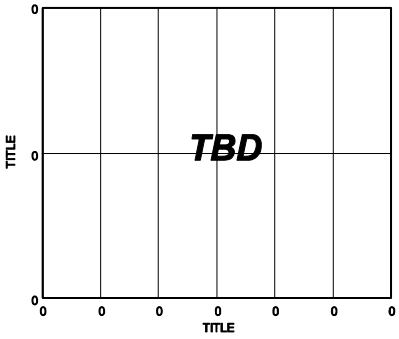

Figure 13. AD7934 Change in INL vs V_{REF} for V_{DD}=5V

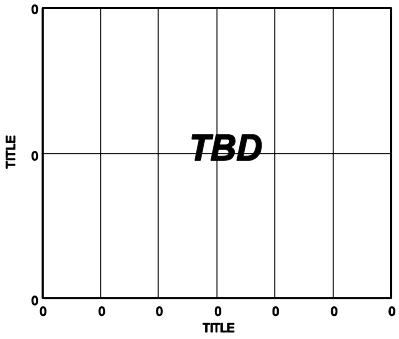

Figure 14.AD7934 Change in DNL vs V_{REF} for V_{DD}=5V

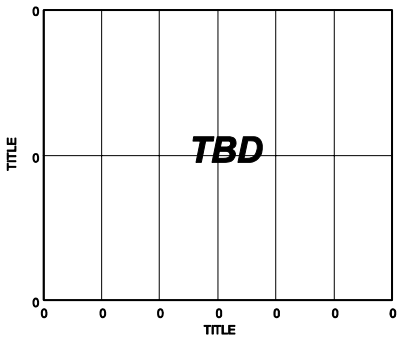

Figure 15. AD7934 Change in ENOB vs V_{REF} for V_{DD}=5V

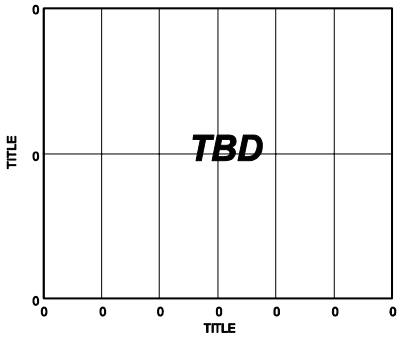

Figure 16. AD7934 Offset vs V_{REF}

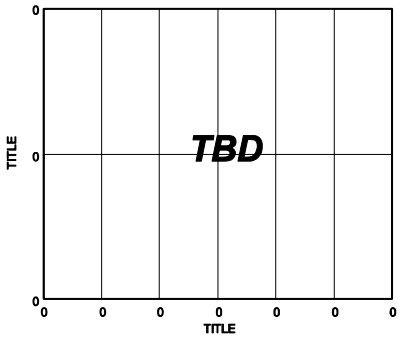

Figure 17. AD7934 Histogram of codes @ V_{DD}=5V with the Internal Reference

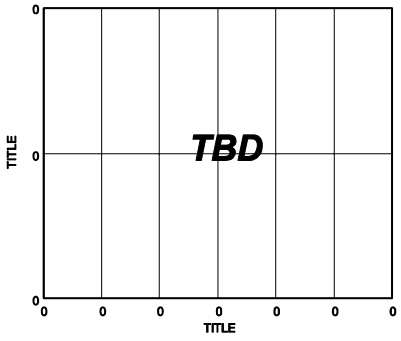

Figure 18. AD7934 Histogram of codes @ V_{DD}=5V with an External Reference

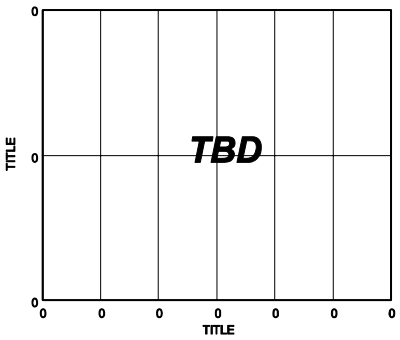

Figure 19. AD7933 FFT @ V_{DD}=5V

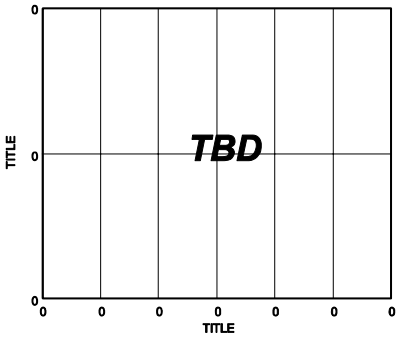

Figure 20. AD7933 Typical DNL @ V_{DD}=5V

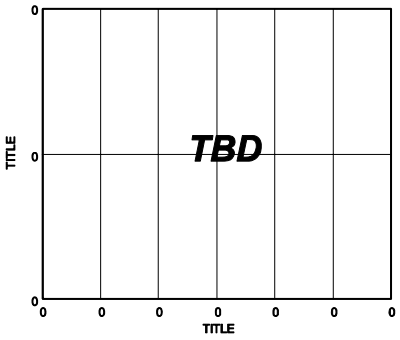

Figure 21. AD7933 Typical INL @ V_{DD}=5V

CONTROL REGISTER

The Control Register on the AD7934/AD7933 is a 12-bit, write-only register. Data is written to this register using the $\overline{CS}$ and $\overline{WR}$ pins. The Control Register is shown below and the functions of the bits are described in Table 6. At power up, the default bit settings in the Control Register are all 0s.

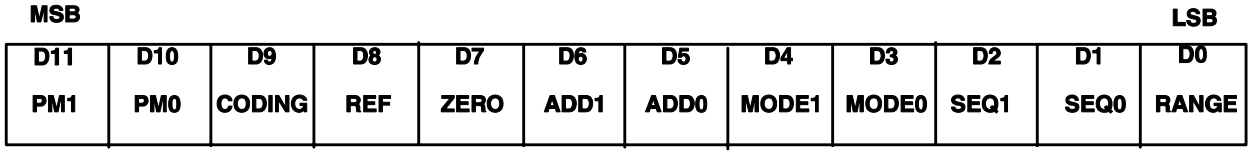

Figure 22. Control Register Bits.

Table 6. Control Register Bit Function Description

Bit	Mnemonic	Comment
11, 10	PM1, PM0	Power Management Bits. These two bits are used to select the power mode of operation. The user can choose between either normal mode or various power down modes of operation as shown in Table 7.
9	C O D I N G	This bit selects the output coding of the conversion result. If this bit is set to 0, the output coding will be straight (natural) binary. If this bit is set to 1, the output coding will be twos complement.
8	R E F	This bit selects whether the internal or an external reference is used to perform the conversion. If this bit is logic 0, an external reference should be applied to the V_{REF} pin and if it is 1, the internal reference is selected (see the Reference Section).
7	ZERO	This bit is not used so should always be set to logic 0.
6, 5	ADD1, ADD0	These two address bits are used to either select which analog input channel is to be converted on in the next conversion if the sequencer is not being used, or to select the final channel in a consecutive sequence when the sequencer is being used as described in Table 9. The selected input channel is decoded as shown in Table 8.
4,3	MODE1, MODE0	The two Mode pins select the type of analog input on the four V_{IN} pins. The AD7934/AD7933 can have either 4 Single Ended inputs, 2 Fully Differential inputs or 2 Pseudo Differential inputs. See Table 8.
2	SEQ1	The SEQ1 bit in the control register is used in conjunction with the SEQ0 bit to control the sequencer function. See Table 9.
1	SEQ0	The SEQ0 bit in the control register is used in conjunction with the SEQ1 bit to control the sequencer function. See Table 9.
0	RANGE	This bit selects the analog input range of the AD7934/AD7933. If it is set to 0 then the analog input range will extend from 0V to V_{REF}. If it is set to 1 then the analog input range will extend from 0V to $2xV_{REF}$. When this range is selected, AV_{DD} must be 4.75 V to 5.25 V.

Table 7. Power Mode Selection using the Power Management Bits in the Control Register

PM1	PM0	Mode	Description
0	0	Normal Mode	When operating in Normal Mode, all circuitry is fully powerered up at all times.
0	1	Auto Shutdown	When operating in Auto Shutdown mode, the AD7934/AD7933 will enter Full Shutdown mode at the end of each conversion. In this mode, all circuitry is powered down.
1	0	Auto Standby	When the AD7934/AD7933 enter this mode, all circuitry is partially powered down. This mode is similar to Auto Shutdown but allows the part to power up in 1µsec.
1	1	Full Shutdown	When the AD7934/AD7933 enters this mode, all circuitry is powered down. The information in the Control Register is retained.

Table 8. Analog Input Type Selection

Channel Address		MODE0=0, MODE1=0		MODE0=0, MODE1=1		MODE0=1, MODE1=0		MODE0=1, MODE1=1
		4 Single-Ended I/P Channels		2 Fully Differential I/P Channels		2 Pseudo Differential I/P Channels		NOT USED
ADD1	ADD0	V_{IN+}	V_{IN-}	V_{IN+}	V_{IN-}	V_{IN+}	V_{IN-}	
0	0	VIN0	AGND	VIN0	VIN1	VIN0	VIN1	
0	1	VIN1	AGND	VIN1	VIN0	VIN1	VIN0	
1	0	VIN2	AGND	VIN2	VIN3	VIN2	VIN3	
1	1	VIN3	AGND	VIN3	VIN2	VIN3	VIN2	

SEQUENCER OPERATION

The configuration of the SEQ0 and SEQ1 bits in the control register allow the user use the sequencer function. Table 9 outlines the two modes of operation of the Sequencer.

Table 9. Sequence Selection

SEQ0	SEQ1	Sequence Type
0	0	This configuration is selected when the sequence function is not used. The analog input channel selected on each individual conversion is determined by the contents of the channel address bits ADD1 and ADD0 in each prior write operation. This mode of operation reflects the normal operation of a multi-channel ADC, without the Sequencer function being used, where each write to the AD7934/AD7933 selects the next channel for conversion.
0	1	NOT USED
1	0	NOT USED
1	1	This configuration is used in conjunction with the Channel Address bits (ADD1 and ADD0) to program continuous conversions on a consecutive sequence of channels from Channel 0 through to a selected final channel as determined by the Channel Address bits in the Control Register. When in differential or pseudo differential mode, inverse channels (e.g. VIN1, VIN0) are not converted in this mode.

CIRCUIT INFORMATION

The AD7934/AD7933 are fast, 4 channel, 12-&10-bit, single supply, successive approximation Analog to Digital converters. The parts can be operated from a either a 2.7 V to 3.6 V or a 4.75 V to 5.25 V power supply and feature throughput rates up to 1.5MSPS.

The AD7934/AD7933 provide the user with an on-chip track/hold, an internal accurate reference, an analog to digital converter, and a parallel interface housed in a 28–Lead TSSOP package.

The AD7934/AD7933 have four analog input channels which can be configured to be 4 single ended inputs, 2 fully differential pairs or 2 pseudo differential pairs. There is an on-chip channel sequencer which allows the user to select a consecutive sequence of channels through which the ADC can cycle with each falling edge of $\overline{\text{CONVST}}$.

The analog input range for the AD7934/AD7933 is 0 to V_{REF} or 0 to 2 x V_{REF} depending on the status of the RANGE bit in the Control register. The output coding of the ADC can be either Binary or Twos complement, depending on the status of the CODING bit in the Control register.

The AD7934/AD7933 provides flexible power management options to allow the user to achieve the best power performance for a given throughput rate. These options are selected by programming the power management bits, PM1 and PM0, in the Control Register.

CONVERTER OPERATION

The AD7934/AD7933 is a successive approximation ADC based around two capacitive DACs. Figure 23 and Figure 24 show simplified schematics of the ADC in Acquisition and Conversion phase respectively. The ADC comprises of Control Logic, a SAR and two capacitive DACs. Both figures show the operation of the ADC in Differential/Pseudo Differential Mode. Single Ended mode operation is similar but V_{IN}- is internally tied to AGND. In acquisition phase, SW3 is closed and SW1 and SW2 are in position A, the comparator is held in a balanced condition and the sampling capacitor arrays acquire the differential signal on the input.

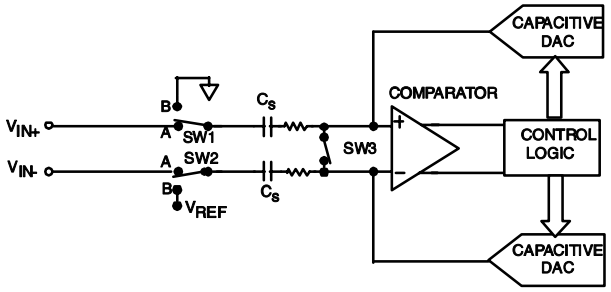

Figure 23. ADC Acquisition Phase

When the ADC starts a conversion (Figure 24), SW3 will open and SW1 and SW2 will move to position B, causing the comparator to become unbalanced. Both inputs are disconnected once the conversion begins. The Control Logic and the charge redistribution DACs are used to add and subtract fixed amounts of charge from the sampling capacitor arrays to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The Control Logic generates the ADC's output code. The output impedances of the sources driving the V_{IN}+ and the V_{IN-} pins must be matched otherwise the two inputs will have different settling times, resulting in errors.

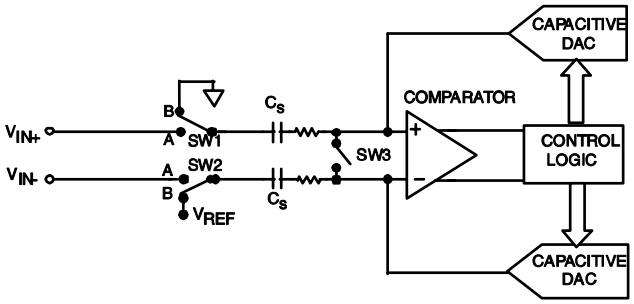

Figure 24. ADC Conversion Phase

ADC TRANSFER FUNCTION

The output coding for the AD7934/AD7933 is either straight binary or two's complement, depending on the status of the CODING bit in the control register. The designed code transitions occur at successive LSB values (i.e. 1LSB, 2LSBs, etc.) and the LSB size is V_{REF}/4096 for the AD7934 and V_{REF}/1024 for the AD7933. The ideal transfer characteristics of the AD7934/AD7933 for both straight binary and twos complement output coding are shown in Figure 25 and Figure 26 respectively.

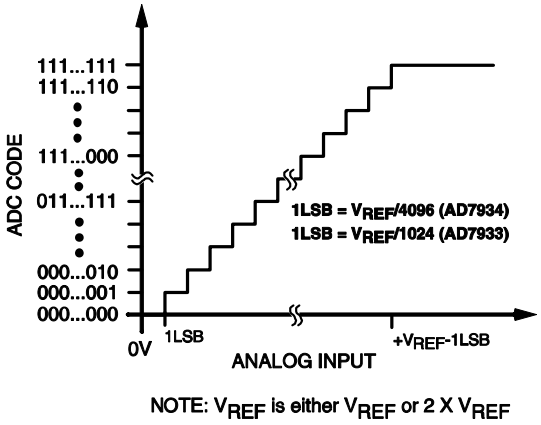

Figure 25. AD7934/AD7933 Ideal Transfer Characteristic with Straight Binary Output Coding

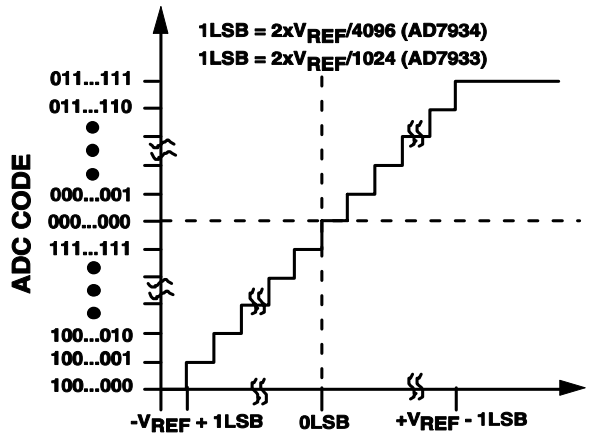

Figure 26. AD7934/AD7933 Ideal Transfer Characteristic with Twos Complement Output Coding

TYPICAL CONNECTION DIAGRAM

Figure 27 shows a typical connection diagram for the AD7934/AD7933. The AGND and DGND pins are connected together at the device for good noise suppression. The V_{REFIN}/V_{REFOUT} pin is decoupled to AGND with a 0.47µF capacitor to avoid noise pickup if the internal reference is used. Alternatively, V_{REFIN}/V_{REFOUT} can be connected to a external reference source and in this case the reference pin should be decoupled with a 0.1µF capacitor. In both cases the analog input range can either be 0V to V_{REF} (Range bit = 0) or 0V to 2 x V_{REF} (Range bit = 1). The analog input configuration can be either 4 Single Ended inputs, 2 Differential Pairs or 2 Pseudo Differential Pairs (see Table 8). The V_{DD} pin is connected to either a 3V or 5V supply. The voltage applied to the V_{DRIVE} input controls the voltage of the digital interface and here, it is connected to the same 3V supply of the microprocessor to allow a 3V logic interface (See the digital inputs section).

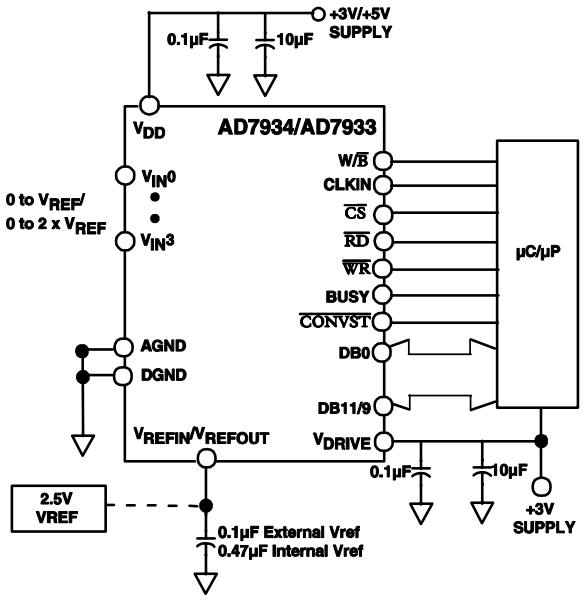

Figure 27. Typical Connection Diagram

ANALOG INPUT STRUCTURE

Figure 28 shows the equivalent circuit of the analog input structure of the AD7934/AD7933 in Differential/Pseudo Differential Mode. In Single Ended mode, V_{IN-} is internally tied to AGND. The four diodes provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signals never exceed the supply rails by more than 300mV. This will cause these diodes to become forward biased and start conducting into the substrate. These diodes can conduct up to 10mA without causing irreversible damage to the part.

The capacitors C1, in Figure 28 are typically 4pF and can primarily be attributed to pin capacitance. The resistors are lumped components made up of the on-resistance of the switches. The value of these resistors is typically about 100Ω. The capacitors, C2, are the ADC's sampling capacitors and have a capacitance of 16pF typically.

For ac applications, removing high frequency components from the analog input signal is recommended by the use of an RC low-pass filter on the relevant analog input pins. In applications where harmonic distortion and signal to noise ratio are critical, the analog input should be driven from a low impedance source. Large source impedances will significantly affect the ac performance of the ADC. This may necessitate the use of an input buffer amplifier. The choice of the opamp will be a function of the particular application.

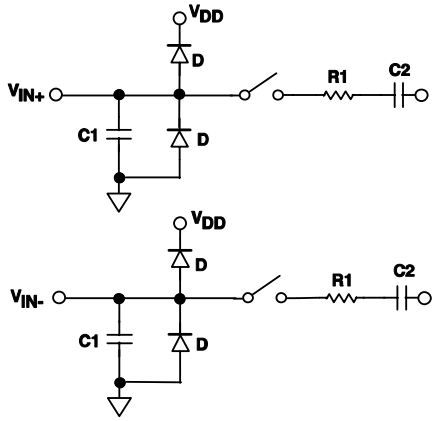

Figure 28. Equivalent Analog Input Circuit. Conversion Phase –Switches Open Track Phase – Switches Closed

When no amplifier is used to drive the analog input, the source impedance should be limited to low values. The maximum source impedance will depend on the amount of Total Harmonic Distortion (THD) that can be tolerated. The THD will increase as the source impedance increases and performance will degrade. Figure 29 shows a graph of the THD versus analog input signal frequency for different source impedances for both V_{DD} = 5 V and 3 V.

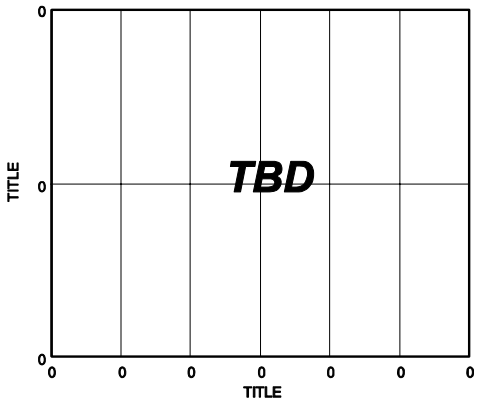

Figure 29. THD vs Analog Input Frequency for Various Source Impedances

Figure 30 shows a graph of THD versus analog input frequency for various supplies, while sampling at 1.5MHz with an SCLK of 20 MHz. In this case the source impedance is 10Ω.

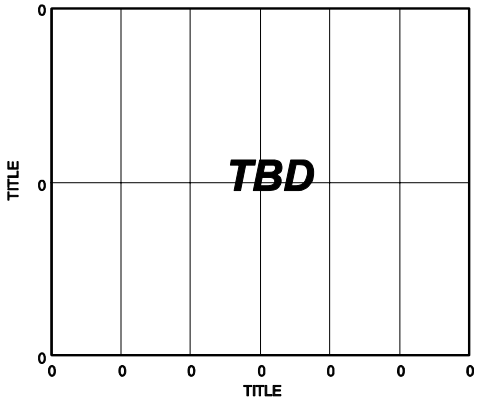

Figure 30. THD vs Analog Input Frequency for various Supply Voltages

THE ANALOG INPUTS

The AD7934/AD7933 has software selectable analog input configurations. The user can choose either 4 Single Ended Inputs, 2 Fully Differential Pairs or 2 Pseudo Differential Pairs. The analog input configuration is chosen with the MODE0/MODE1 bits in the internal Control register (See Table 8).

Single Ended Mode

The AD7934/AD7933 can have 4 single ended analog input channels by setting the MODE0 and MODE1 bits in the control register both to 0. In applications where the signal source has a high impedance, it is recommended to buffer the analog input before applying it to the ADC. The analog input range can be either 0 to V_{REF} or 0 to 2 x V_{REF}.

If the analog input signal to be sampled is bipolar, the internal reference of the ADC can be used to externally bias up this signal to make it of the correct format for the ADC.

Figure 31 shows a typical connection diagram when operating the ADC in single ended mode.

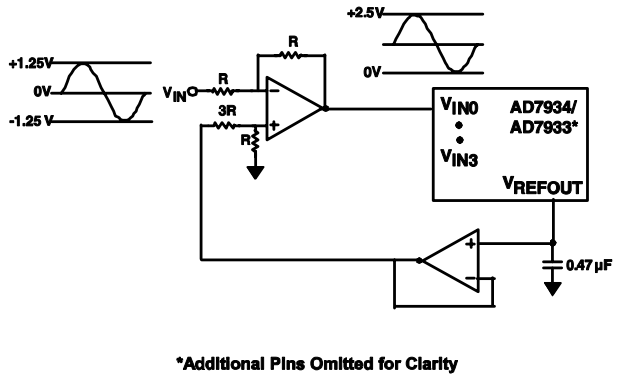

Figure 31. Single Ended Mode Connection Diagram

Differential Mode

The AD7934/AD7933 can have 2 Differential Analog Input Pairs by setting the MODE0 and MODE1 bits in the control register to 0 and 1 respectively.

Differential signals have some benefits over single ended signals including noise immunity based on the device's common mode rejection and improvements in distortion performance. Figure 32 defines the fully differential analog input of the AD7934/AD7933.

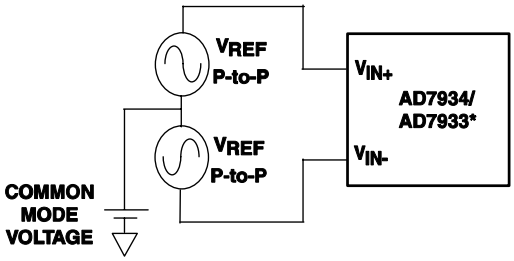

Figure 32. Differential Input Definition

The amplitude of the differential signal is the difference between the signals applied to the V_{IN+} and V_{IN-} pins in each differential pair (i.e. $V_{IN+} - V_{IN-}$). V_{IN+} and V_{IN-} should be simultaneously driven by two signals each of amplitude V_{REF} that are 180° out of phase. The amplitude of the differential signal is therefore $-V_{REF}$ to $+V_{REF}$ peak-to-peak (i.e. 2 x V_{REF}). This is regardless of the common mode (CM). The common mode is the average of the two signals, i.e. $(V_{IN+} + V_{IN-})/2$ and is therefore the voltage that the two inputs are centered on. This results in the span of each input being CM ± $V_{REF}/2$. This voltage has to be set up externally and its range varies with V_{REF}. As the value of V_{REF} increases, the common mode range decreases. When driving the inputs with an amplifier, the actual common mode range will be determined by the amplifier's output voltage swing.

Figure 33 and Figure 34 show how the common mode range typically varies with V_{REF} for both a 5 V and a 3 V power supply. The common mode must be in this range to guarantee the functionality of the AD7934/AD7933.

When a conversion takes place, the common mode is rejected resulting in a virtually noise free signal of amplitude $-V_{REF}$ to $+V_{REF}$ corresponding to he digital codes of 0 to 4096 for the AD7934 and 0 to 1024 for the AD7933.

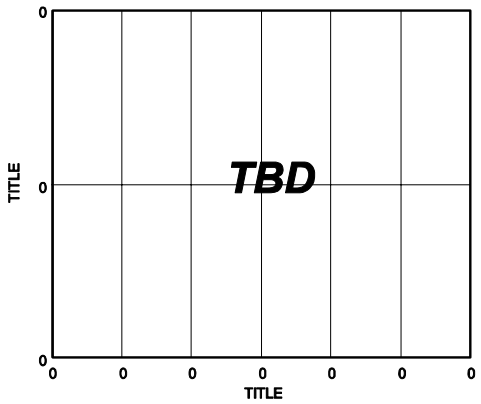

Figure 33. Input Common Mode Range versus V_{REF} (V_{DD}=5V and V_{REF} (max) = 3.5V)

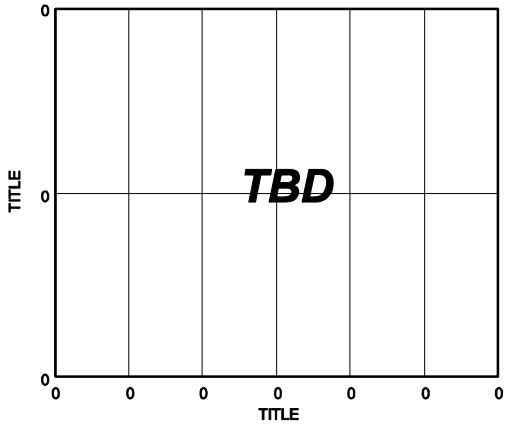

Figure 34. Input Common Mode Range versus V_{REF} (V_{DD}=3V and V_{REF} (max)=2.2V)

Driving Differential Inputs

Differential operation requires that V_{IN+} and V_{IN-} be simultaneously driven with two equal signals that are 180° out of phase. The common mode must be set up externally and has a range which is determined by V_{REF}, the power supply and the particular amplifier used to drive the analog inputs. Differential modes of operation with either an ac or dc input, provide the best THD performance over a wide frequency range. Since not all applications have a signal preconditioned for differential operation, there is often a need to perform single ended to differential conversion.

Using an Opamp Pair

An op amp pair can be used to directly couple a differential signal to one of the analog input pairs of the AD7934/AD7933. The circuit configurations shown in Figure 35 and Figure 36 show how a dual op amp can be used to convert a single-ended signal into a differential signal for both a bipolar and unipolar input signal, respectively.

The voltage applied to Point A sets up the common-mode voltage. In both diagrams, it is connected in some way to the reference, but any value in the common-mode range can be input here to set up the common mode. A suitable dual op amp that could be used in this configuration to provide differential drive to the AD7934/AD7933 is the AD8022.

Take care when choosing the op amp; the selection depends on the required power supply and system performance objectives. The driver circuits in Figure 35 and Figure 36 are optimized for dc coupling applications requiring best distortion performance.

The circuit configuration shown in Figure 35 converts a unipolar, single-ended signal into a differential signal.

The circuit configuration in Figure 36 is configured to convert and level shift a single-ended, ground-referenced (bipolar) signal to a differential signal centered at the V_{REF} level of the ADC.

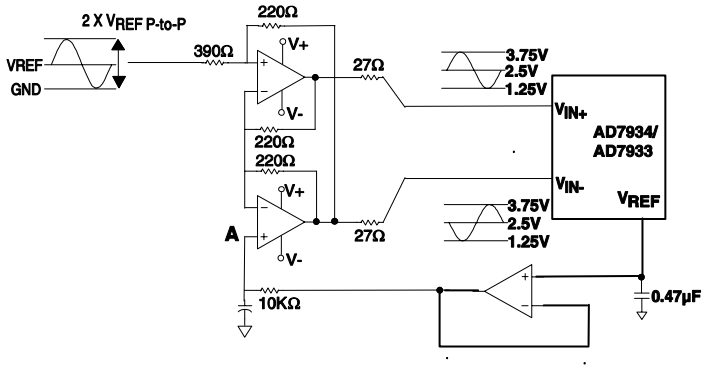

Figure 35. Dual Op Amp Circuit to Convert a Single-Ended Unipolar Signal into a Differential Signal

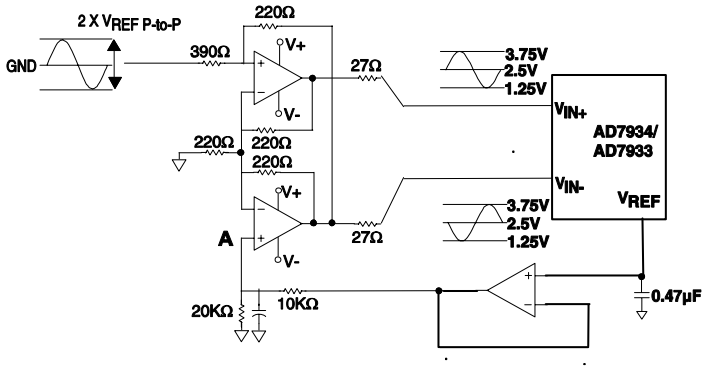

Figure 36. Dual Op Amp Circuit to Convert a Single-Ended Bipolar Signal into a Differential Signal

Pseudo Differential Mode

The AD7934/AD7933 can have 2 Pseudo Differential pairs by setting the MODE0 and MODE1 bits in the control register to 1, 0 respectively. V_{IN}+ is connected to the signal source which must have an amplitude of V_{REF} to make use of the full dynamic range of the part. A DC input is applied to the V_{IN}– pin. The voltage applied to this input provides an offset from ground or a pseudo ground for the V_{IN}+ input. The benefit of pseudo differential inputs is that they separate the analog input signal ground from the ADC's ground allowing DC common mode voltages to be cancelled. Figure 37 shows a connection diagram for Pseudo Differential Mode.

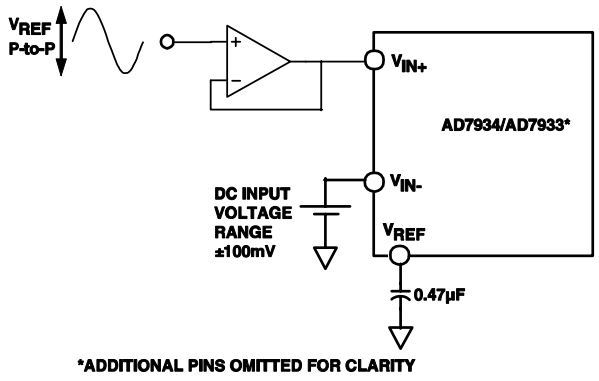

Figure 37. Pseudo Differential Mode Connection Diagram

ANALOG INPUT SELECTION

As shown in Table 8, the user can set up their analog input configuration by setting the values in the MODE0 and MODE1 bits in the Control Register. Assuming the configuration has been chosen, there are two different ways of selecting the analog input to be converted on depending on the state of the SEQ0 and SEQ1 bits in the Control register.

Normal Multichannel Operation (SEQ0=SEQ1= 0)

Any one of four analog input channels or 2 pairs of channels may be selected for conversion in any order by setting the SEQ0 & SEQ1 bits in the Control register both to 0. The channel to be converted on is selected by writing to the address bits ADD1 and ADD0 in the Control register to program the multiplexer prior to the conversion. This mode of operation is of a normal multichannel ADC where each data write selects the next channel for conversion. Figure 38 shows a flow chart of this mode of operation. The channel configurations are shown in Table 8.

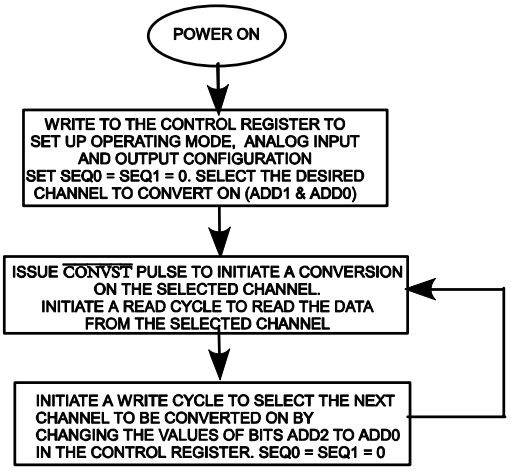

Figure 38. Normal Multichannel Operation Flow Chart

Using the Sequencer

Consecutive Sequence (SEQ0 =1, SEQ1 = 1)

A sequence of consecutive channels can be converted on beginning with channel 0 and ending with a final channel selected by writing to the ADD1 and ADD0 bits in the Control register. This is done by setting the SEQ0 and SEQ1 bits in the control register both to 1. Once the control register has been written to to set this mode up, the next conversion will be on Channel 0, then Channel 1 and so on until the channel selected by the address bits (ADD1 and ADD0) is reached. The ADC will then return to channel 0 and start the sequence again. The $\overline{WR}$ input must be kept high to ensure that the Control register is no accidentally overwritten and the sequence interrupted. This pattern will continue until such time as the AD7938/AD7933 is written to. Figure 39 shows the flow chart of the Consecutive Sequence mode.

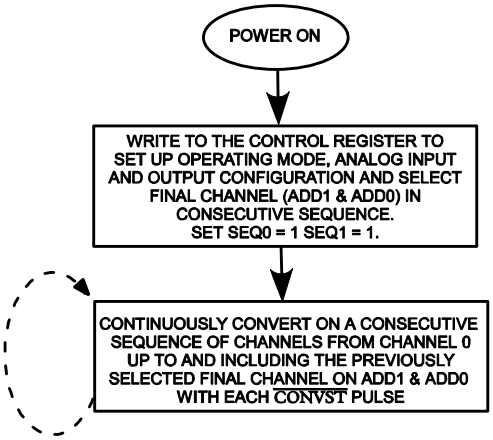

Figure 39. Consecutive Sequence Mode Flow Chart

REFERENCE SECTION

The AD7934/AD7933 can operate with either the on chip reference or an external reference. The internal reference is selected by setting the REF bit in the internal Control register to 1. A block diagram of the internal reference circuitry is shown in Figure 40. The internal reference circuitry includes an on-chip 2.5 V band gap reference, and a reference buffer. When using the internal reference the V_{REFIN}/V_{REFOUT} pin should be decoupled to AGND with a 0.47µF capacitor. This internal reference not only provides the reference for the analog to digital conversion but can also be used externally in the system. It is recommended that the reference output is buffered using an external precision opamp before applying it anywhere in the system.

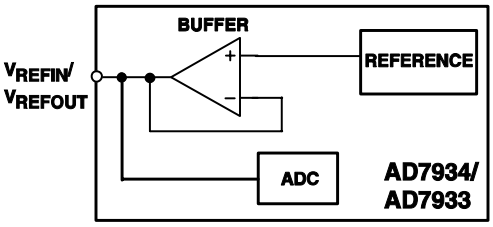

Figure 40. Internal Reference Circuit Block Diagram

Alternatively, an external reference can be applied to the V_{REFIN}/V_{REFOUT} pin of the AD7934/AD7933. An external reference input is selected by setting the REF bit in the internal Control register to 0. When using an external reference, the V_{REFIN}/V_{REFOUT} pin should be decoupled to AGND with a 0.1µF capacitor. When operating in Differential mode, the external reference input range is 0.1 V to 3.5V and in Single ended and pseudo differential mode, the external reference input range is 0.1V to V_{DD}. In all cases, the specified reference is 2.5 V.

It is important to ensure that, when chosing the reference value, the maximum analog input range (V_{IN}max) is never greater than V_{DD} + 0.3V to comply with the maximum ratings of the device. In Pseudo Differential Mode, the user must ensure that $V_{REFIN} - V_{IN-} \leq V_{DD}$.

The following two examples calculate the maximum V_{REF} input that can be used when operating the AD7934/AD7933 in Differential mode with a V_{DD} of 5 V and 3 V respectively.

Example 1:

$V_{IN}max = V_{DD} + 0.3$

$V_{IN}max = V_{REF} + V_{REF}/2$

If $V_{DD} = 5$ *V*

then $V_{IN}max = 5.3$ *V*

Therefore $3xV_{REF}/2 = 5.3$ *V*

$\boldsymbol{V_{REF}\ max = 3.5\ V}$

Therefore, when operating at V_{DD} = 5 V, the value of V_{REF} can range from 100mV to a maximum value of 3.5V. When V_{DD} = 4.75 V, V_{REF} max = 3.17 V.

Example 2:

$V_{IN}max = V_{DD} + 0.3$

$V_{IN}max = V_{REF} + V_{REF}/2$

If $V_{DD} = 3.6V$

then $V_{IN}max = 3.9$ *V*

Therefore $3xV_{REF}/2 = 3.6$ *V*

$\boldsymbol{V_{REF}\ max = 2.6\ V}$

Therefore, when operating with at V_{DD} = 3 V, the value of V_{REF} can range from 100mV to a maximum value of 2.4V. When V_{DD} = 2.7 V, V_{REF} max = 2 V.

These examples show that the maximum reference applied to the AD7934/AD7933 is directly dependant on the value applied to V_{DD}.

The performance of the part at different reference values is shown in Figures TBD to TBD. The value of the reference sets the analog input span and the common mode voltage range. Errors in the reference source will result in gain errors in the AD7934/AD7933 transfer function and will add to specified full scale errors on the part. Table 10 lists examples of suitable voltage references that could be used that are available from Analog Devices and Figure 41shows a typical connection diagram for an external reference.

Table 10. Examples of Suitable Voltage References

Reference	Output Voltage	Initial Accuracy (% max)	Operating Current (µA)
AD780	2.5/3	0.04	1000
ADR421	2.5	0.04	500
ADR420	2.048	0.05	500

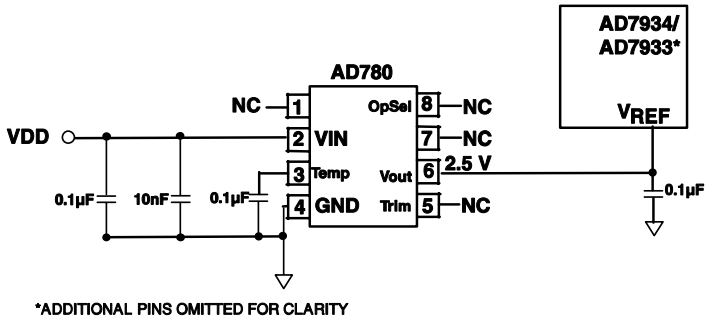

Figure 41. Typical V_{REF} Connection Program

Digital Inputs

The digital inputs applied to the AD7934/AD7933 are not limited by the maximum ratings which limit the analog inputs. Instead, the digital inputs applied can go to 7V and are not restricted by the AV_{DD} +0.3V limit as on the analog inputs.

Another advantage of the digital inputs not being restricted by the AV_{DD} + 0.3 V limit is the fact that power supply sequencing issues are avoided. If any of these inputs are applied before AV_{DD} then there is no risk of latch-up as there would be on the analog inputs if a signal greater than 0.3 V was applied prior to $AV_{DD.}$

V_{DRIVE} Input

The AD7934/AD7933 has a V_{DRIVE} feature. V_{DRIVE} controls the voltage at which the Parallel Interface operates. V_{DRIVE} allows the ADC to easily interface to 1.8V, 3 V and 5 V processors. V_{DRIVE} of 1.8 V can only be used if V_{DD} = 2.7 V to 3.6 V.

An example is, if the AD7934/AD7933 were operated with an AV_{DD} of 5V, and the V_{DRIVE} pin could be powered from a 3V supply, the AD7934/AD7933 has better dynamic performance with an AV_{DD} of 5V while still being able to interface to 3V processors. Care should be taken to ensure V_{DRIVE} does not exceed AV_{DD} by more than 0.3 V. (See Absolute Maximum Ratings Section).

PARALLEL INTERFACE

The AD7934/AD7933 has a flexible, high speed, parallel interface. This interface is 12-bits (AD7934) or 10-bits (AD7933) wide and is capable of operating in either Word (W/$\overline{B}$ tied high) or Byte (W/$\overline{B}$ tied low) mode. The $\overline{CONVST}$ signal is used to initiate conversions and when operating in Auto Shutdown or Auto Standby mode, it is used to power up the ADC.

A falling edge on the $\overline{CONVST}$ signal is used to initiate conversions and it also puts the ADC track and hold into track. Once the $\overline{CONVST}$ signal goes low, the BUSY signal goes high for the duration of the Conversion. In between conversions, $\overline{CONVST}$ must be brought high for a minimum time of t_1. This must happen after the 14th rising edge of CLKIN otherwise the conversion will be aborted and the track and hold will go back into track. At the end of the Conversion, BUSY goes low and can be used to activate an Interrupt Service Routine. The $\overline{CS}$ and $\overline{RD}$ lines are then activated in parallel to read the 12- or 10-bits of conversion data. When power supplies are first applied to the device, a rising edge on $\overline{CONVST}$ puts the track and hold into track. The acquisition time of 135ns min must be allowed before $\overline{CONVST}$ is brought low to initiate a conversion. The ADC will then go into hold on the falling edge of $\overline{CONVST}$ and back into track on the 13th rising edge of CLKIN after this. See Figure 4. When operating the device in Auto Shutdown or Auto Standby mode, where the ADC powers down at the end of each conversion, a rising edge on the $\overline{CONVST}$ signal is used to power up the device.

Reading Data from the AD7934/AD7933

With the W/$\overline{B}$ pin tied logic high, the AD7934/AD7933 interface operates in Word mode. In this case, a single read operation from the device accesses the Conversion data word on pins DB0/2 to DB11. The DB8/HBEN pin assumes its DB8 function. With the W/$\overline{B}$ pin tied to logic low, the AD7934/AD7933 interface operates in Byte mode. In this case, the DB8/HBEN pin assumes its HBEN function. Conversion data from the AD7934/ AD7933 must be accessed in two read operations with 8 bits of data provided on DB0 to DB7 for each of the read operations. The HBEN pin determines whether the read operation accesses the high byte or the low byte of the12- or 10-bit word. For a low byte read, DB0 to DB7 provide the 8 LSBs of the 12-bit word. For 10-bit operation, the two LSBs of the low byte are zeros and are followed by 6-bits of conversion data. For a high byte read, DB0 to DB3 provide the 4MSBs of the 12-/10-bit word. DB4 of the high byte is always zero and DB5 and DB6 of the high byte provide the Channel ID. Figure 4 shows the read cycle timing diagram for a 12-/10-bit transfer. When operated in Word mode, the HBEN input does not exist and only the first read operation is required to access data from the device. When operated in Byte mode, the two read cycles shown in Figure 5 are required to access the full data word from the device.

The $\overline{CS}$ and $\overline{RD}$ signals are gated internally and level triggered active low. In either Word mode or Byte mode, $\overline{CS}$ and $\overline{RD}$ may be tied together as the timing specification t_{10} and t_{11} is 0ns min. The data is placed onto the data bus a time t_{13} after both $\overline{CS}$ and $\overline{RD}$ go low. The $\overline{RD}$ rising edge can be used to latch data out of the device. After a time, t_{14}, the data lines will become three-stated.

Alternatively, $\overline{CS}$ and $\overline{RD}$ can be tied permanently low and the conversion data will be valid and placed onto the data bus a time t_9 before the falling edge of BUSY.

Writing Data to the AD7934/AD7933

With W/$\overline{B}$ tied logic high, a single Write operation transfers the full data word on DB0 to DB11to the Control Register on the AD7934/AD7933. The DB8/HBEN pin assumes its DB8 function. Data to be written to the AD7934/AD7933 should be provided on the DB0 to DB11 inputs with DB0 being the LSB of the data word. With W/$\overline{B}$ tied logic low, the AD7934/AD7933 requires two write operations to transfer a full 12 Bit word. DB8/HBEN assumes its HBEN function. Data to be written to the AD7934/AD7933 should be provided on the DB0 to DB7 inputs. HBEN determines whether the byte which is to be written is high byte or low byte data. The low byte of the data word has DB0 being the LSB of the full data word. For the high byte write, HBEN should be high and the data on the DB0 input should be data bit 8 of the 12 bit word.

Figure 2 shows the write cycle timing diagram of the AD7934/AD7933. When operated in Word mode, the HBEN input does not exist and only the one write operation is required to write the word of data to the device. Data should be provided on DB0 to DB11. When operated in Byte mode, the two write cycles shown in Figure 3 are required to write the full data word to the AD7934/AD7933. In Figure 3 the first write transfers the lower 8 bits of the data word from DB0 to DB7 and the second write transfers the upper 4 bits of the data word.

When writing to the AD7934/AD7933, the top 4 bits in the high byte must be 0s.

The $\overline{CS}$ and $\overline{WR}$ signals are gated internally. $\overline{CS}$ and $\overline{WR}$ may be tied together as the timing specification for t_4 and t_5 is 0ns min. The data is latched into the device on the rising edge of $\overline{WR}$. The data needs to be setup a time t_7 before the $\overline{WR}$ rising edge and held for a time t_8 after the $\overline{WR}$ rising edge.

POWER MODES OF OPERATION

The AD7934/AD7933 have four different power modes of operation. These modes are designed to provide flexible power management options. Different options can be chosen to optimize the power dissipation/throughput rate ratio for differing applications. The mode of operation is selected by the power management bits, PM1 and PM0, in the Control register, as detailed in Table 7. At power on reset, the default power up condition is Normal Mode.

Normal Mode (PM1 = PM0 = 0)

This mode is intended for the fastest throughput rate performance as the user does not have to worry about any power up times as the AD7934/AD7933 remains fully powered up at all times. At power on reset, this mode is the default setting in the control register.

AutoShutdown (PM1 = 0; PM0 = 1)

In this mode of operation, the AD7934/AD7933 automatically enters full shutdown at the end of each conversion which is shown at point A in Figure 4. In shutdown mode, all internal circuitry on the device is powered. The part retains information in the Control register during shutdown. It remains in shutdown mode until the next rising edge of $\overline{CONVST}$ (see point B in Figure 4). On this rising edge, the part will begin to power up and the power up time will depend on whether the user is operating with the internal or external reference. With the internal reference, the power up time is typically TBD and with an external reference, the power up time is typically TBD. The user should ensure that the power up time has elapsed before initiating a conversion.

Auto Standby (PM1 = 1; PM0 = 0)

In this mode of operation, the AD7934/AD7933 automatically enters Standby mode at the end of each conversion. When this mode is entered, all circuitry on the AD7934/AD7933 is partially powered down. A rising edge on $\overline{CONVST}$ will power up the device which will take at least TBD.

Full Shutdown Mode (PM1 =1; PM0 = 1)

When this mode is entered, all circuitry on the AD7934/AD7933 is powered down. The part retains the information in the Control Register during the Full Shutdown. The AD7934/AD7933 remains in Full Shutdown mode until the power management bits (PM1 and PM0) in the Control Register are changed. If a write to the Control register occurs while the part is in Full Shutdown mode, and the Power Management bits are changed to PM0 = PM1 = 0, i.e. Normal Mode, the part will begin to power up on the $\overline{CONVST}$ rising edge. To ensure the part is fully powered up before a conversion is initiated, the power up time, TBD, should be allowed before the $\overline{CONVST}$ falling edge, otherwise, invalid data will be read.

POWER VS. THROUGHPUT RATE

A big advantage of powering the ADC down after a conversion is that the power consumption of the part is significantly reduced at lower throughput rates. When using the different power modes, the AD7934/AD7933 is only powered up for the duration of the conversion. Therefore, the average power consumption per cycle is significantly reduced. Figure 42 and Figure 43 show plots of power vs. throughput when operating in Auto shutdown and Auto Standby modes.

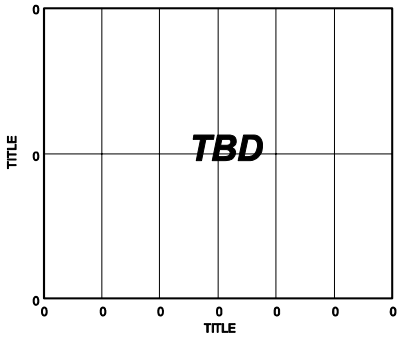

Figure 42. Power vs. Throughput in Auto Shutdown Mode

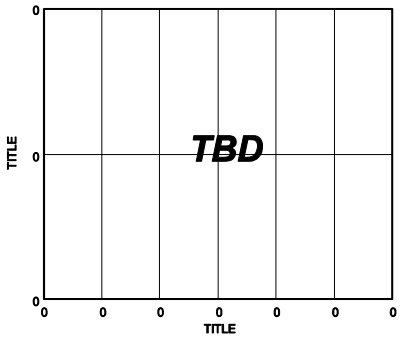

Figure 43. Power vs. Throughput in Auto Standby Mode.

MICROPROCESSOR INTERFACING

AD7934/AD7933 To ADSP-21xx Interface

Figure 44 shows the AD7934/AD7933 interfaced to the ADSP-21xx series of DSPs as a memory mapped device. A single wait state may be necessary to interface the AD7934/AD7933 to the ADSP-21xx depending on the clock speed of the DSP. The wait state can be programmed via the Data Memory Wasitstate Control Register of the ADSP-21xx (please see the ADSP-21xx family Users Manual for details). The following instruction reads from the AD7934/AD7933:

MR = DM(ADC)

Where **ADC** is the address of the AD7934/AD7933.

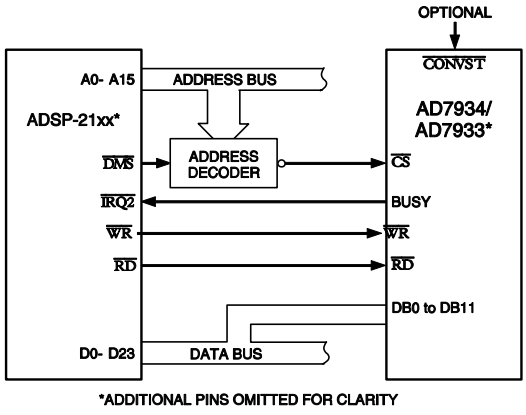

Figure 44. Interfacing to the ADSP-21xx

AD7934/AD7933 To ADSP-21065 Interface

Figure 45 shows a typical interface between the AD7934/AD7933 and the ADSP-21065L SHARC processor. This interface is an example of one of three DMA handshake modes. The $\overline{MS_x}$ control line is actually three memory select lines. Internal $ADDR_{25-24}$ are decoded into $\overline{MS_{3-0}}$, these lines are then asserted as chip selects. The $\overline{DMAR_1}$ (DMA request 1) is used in this setup as the interrupt to signal end of conversion. The rest of the interface is standard handshaking operation.

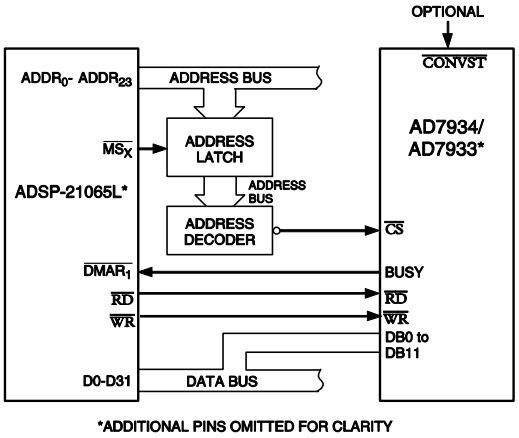

Figure 45. Interfacing to the ADSP-21065L

AD7934/AD7933 To TMS32020, TMS320C25 and TMS320C5x Interface

Parallel interfaces between the AD7934/AD7933 and the TMS32020, TMS320C25 and TMS320C5x family of DSPs are shown in

Figure 46. The memory mapped address chosen for the AD7934/AD7933 should be chosen to fall in the I/O memory space of the DSPs. The parallel interface on the AD7934/AD7933 is fast enough to interface to the TMS32020 with no extra wait states. If high speed glue logic such as 74AS devices are used to drive the $\overline{RD}$ and the $\overline{WR}$ lines when interfacing to the TMS320C25, then again, no wait states are necessary. However, if slower logic is used, data accesses may be slowed sufficiently when reading from and writing to the part to require the insertion of one wait state. Extra wait states will be necessary when using the TMS320C5x at their fastest clock speeds. (please see the TMS320C5x User Guide for details).

Data is read from the ADC using the following instruction:

IN D, ADC

Where **D** is Data Memory address and the **ADC** is the AD7934/AD7933 address.

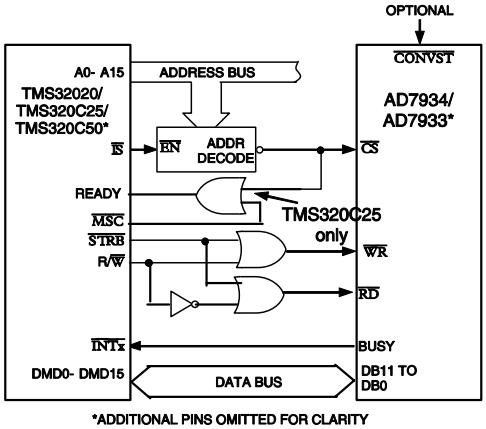

Figure 46. Interfacing to the TMS32020/C25/C5x

AD7934/AD7933 to 80C186 Interface

Figure 47 shows the AD7934/AD7933 interfaced to the 80C186 microprocessor. The 80C186 DMA controller provides two independent high speed DMA channels where data transfer can occur between memory and I/O spaces. Each data transfer consumes two bus cycles, one cycle to fetch data and the other to store data. After the AD7934/AD7933 has finished a conversion, the BUSY line generates a DMA request to Channel 1 (DRQ1). As a result of the interrupt, the processor performs a DMA READ operation which also resets the interrupt latch. Sufficient priority must be assigned to the DMA channel to ensure that the DMA request will be serviced before the completion of the next conversion.

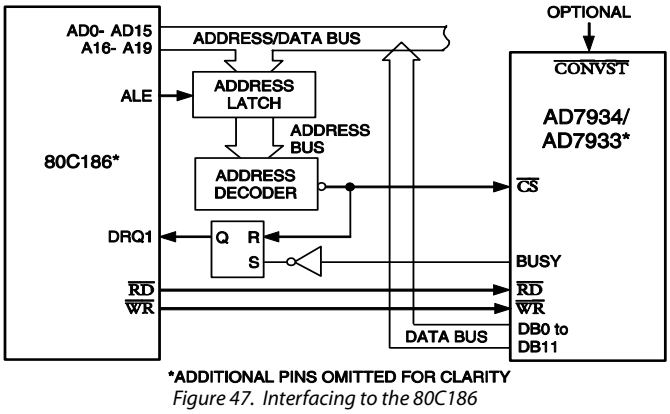

Figure 47. Interfacing to the 80C186

APPLICATION HINTS

GROUNDING AND LAYOUT

The printed circuit board that houses the AD7934/AD7933 should be designed so that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be easily separated. A minimum etch technique is generally best for ground planes as it gives the best shielding. Digital and analog ground planes should be joined in only one place and the connection should be a star ground point established as close to the Ground pins on the AD7934/AD7933 as possible. Avoid running digital lines under the device as this will couple noise onto the die. The analog ground plane should be allowed to run under the AD7934/AD7933 to avoid noise coupling. The power supply lines to the AD7934/AD7933 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line.

Fast switching signals like clocks should be shielded with digital ground to avoid radiating noise to other sections of the board, and clock signals should never run near the analog inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This will reduce the effects of feedthrough through the board. A microstrip technique is by far the best but is not always possible with a doublesided board.

In this technique the component side of the board is dedicated to ground planes while signals are placed on the solder side.

Good decoupling is also important. All analog supplies should be decoupled with 10μF tantalum capacitors in parallel with 0.1μF capacitors to GND. To achieve the best from these decoupling components, they must be placed as close as possible to the device.

OUTLINE DIMENSIONS

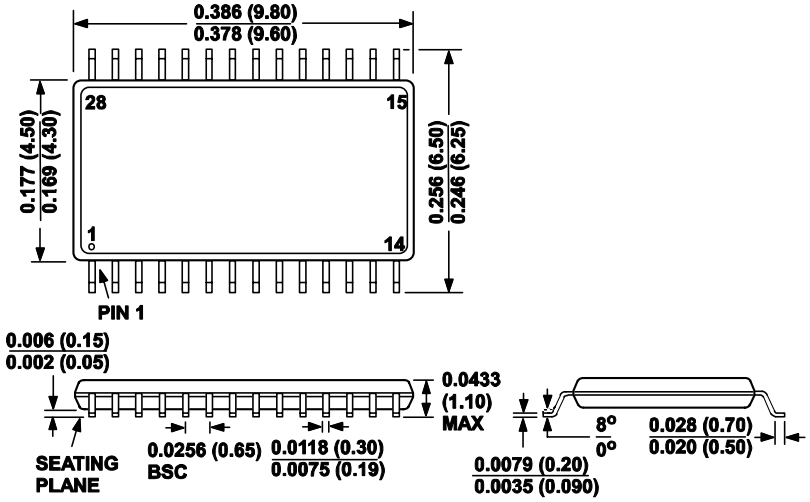

Figure 48. 28 Lead TSSOP Package Dimensions

Dimensions shown in inches and mm

ORDERING GUIDE

Model	Range	Linearity Error (LSB)[1]	Package Option	Package Descriptions
AD7934BRU	–40°C to +85°C	±1	RU-32	TSSOP
AD7933BRU	–40°C to +85°C	±1	RU-32	TSSOP
EVAL-ADxxxxCB[2]	Evaluation Board			
EVAL-CONTROL BRD2[3]	Controller Board			

[1] Linearity error here refers to integral linearity error.
[2] This can be used as a stand-alone evaluation board or in conjunction with the Evaluation Board Controller for evaluation/demonstration purposes.
[3] Evaluation Board Controller. This board is a complete unit allowing a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators. The following needs to be ordered to obtain a complete evaluation kit: the ADC Evaluation Board (EVALADxxxxCB), the EVAL-CONTROL BRD2 and a 12 V ac transformer. See the ADxxxx evaluation board technical note for more details.

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