14/12/10-Bit, 1200 MSPS D/A Converters

Preliminary Technical Data

AD9736/AD9735/AD9734

FEATURES

- 1.8/3.3 V Dual Supply Operation
- AD9736 SFDR > 53 dBc to f_{OUT} = 600 MHz
- AD9736 IMD > 65 dBc to f_{OUT} = 600 MHz
- AD9736 DNL = ± 1.0 LSB
- AD9736 INL = ± 2.0 LSB
- Low power: 380 mW (I_{OUTFS} = 20 mA; f_{OUT} = 330 MHz)
- LVDS data interface with on-chip 100 Ω terminations
- Analog Output: Adjustable 10-30mA (RL=25 Ω to 50 Ω)
- On-Chip 1.2 V Reference
- 160 pin BGA Package

APPLICATIONS

- Instrumentation
- Automatic Test Equipment
- RADAR
- Avionics
- Wideband Communications Systems:
  - Point-to-Point Wireless
  - LMDS
  - PA Linearization

PRODUCT DESCRIPTION

The AD9736, AD9735, and AD9734 are high performance, high frequency DACs that provide sample rates of up to 1200 MSPS, permitting multi-carrier generation up to their Nyquist frequency. The AD9736 is the 14 bit member of the family, while the AD9735 and the AD9734 are the 12 and 10 bit members, respectively. They include a serial peripheral interface (SPI) port that provides for programming many internal parameters and also enables read-back of status registers. They use a reduced specification LVDS interface to minimize data interface noise that may degrade performance. The output current can be programmed over a range of 10mA to 30mA. The AD9736 family is manufactured on a 0.18µm CMOS process and operates from 1.8V and 3.3V supplies for a total power consumption of 380mW in bypass mode. It is supplied in a 160 pin BGA package for reduced package parasitics.

FUNCTIONAL BLOCK DIAGRAM

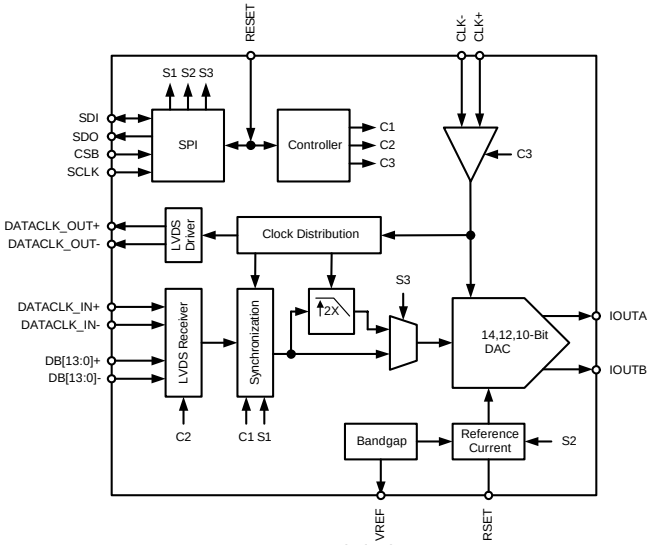

Figure 1. Functional Block Diagram

PRODUCT HIGHLIGHTS

Ultra-low Noise and Intermodulation Distortion (IMD) enable high quality synthesis of wideband signals at intermediate frequencies up to 600 MHz.

Double Data Rate (DDR) LVDS data receivers support the maximum conversion rate of 1200 MSPS.

Direct pin programmability of basic functions or SPI port access for complete control of all AD9736 family functions.

Manufactured on a CMOS process, the AD9736 family uses a proprietary switching technique that enhances dynamic performance.

The current output(s) of the AD9736 family can be easily configured for various single-ended or differential circuit topologies.

Rev. PrJ 9/7/2004

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REVISION HISTORY

Revision PrA: Initial Version

Revision PrB: Updated data based on initial evaluation results

Revision PrC: Updated data for web display and ongoing evaluation results

Revision PrD: Added SPI port information

Revision PrE: Cleaned up SPI port tables, added AD9736 rev A evaluation board schematics

Revision PrF: Added BGA Package Outline Drawing

Revision PrG: Added Package Pinout

Revision PrH: Added SPI Port Description

Revision PrI: Edits for readability and clarity, Added Idd typical values and plots, Updated SPI register tables, Added LVDS and SYNC controller sections, Added pin function table, Added BIST description, Added Analog control section, Added Vref section, Updated eval board schematic and PCB layout

Revision PrJ: Update BIST information, Update SPI definition to include SCLK edge change for read operation, Add SPI timing, Annotate schematic to show component values for output circuit, Update ACLR plots, Add PCB fabrication details.

AD9736/AD9735/AD9734—SPECIFICATIONS[1]

DC SPECIFICATIONS

(VDDA33 = VDDD33 = 3.3 V, VDDA18 = VDDD18 = VDDCLK = 1.8 V, MAXIMUM SAMPLE RATE, FS = 20MA, 1X MODE, 25 OHM 1% BALANCED LOAD, UNLESS OTHERWISE NOTED)

Parameter		Temp	Test Level	AD9736			AD9735			AD9734			Unit
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
RESOLUTION					14			12			10		Bits
ACCURACY	Integral Nonlinearity (INL)				± 2.0			TBD			TBD		LSB
	Differential Nonlinearity (DNL)				± 1.0			TBD			TBD		LSB
ANALOG OUTPUTS	Offset Error				TBD			TBD			TBD		% FSR
	Gain Error (With Internal Reference)				± 0.5			± 0.5			± 0.5		% FSR
	Gain Error (Without Internal Reference)				± 0.5			± 0.5			± 0.5		% FSR
	Full Scale Output Current			10	20	30	10	20	30	10	20	30	mA
	Output Compliance Range			1.0			1.0			1.0			V
	Output Resistance				TBD			TBD			TBD		kΩ
	Output Capacitance				TBD			TBD			TBD		pF
TEMPERATURE DRIFT	Offset				TBD			TBD			TBD		ppm/°C
	Gain				TBD			TBD			TBD		ppm/°C
	Reference Voltage				TBD			TBD			TBD		ppm/°C
REFERENCE	Internal Reference Voltage				1.2			1.2			1.2		V
	Output Current				100			100			100		nA
ANALOG SUPPLY VOLTAGES	VDDA33			3.13	3.3	3.47	3.13	3.3	3.47	3.13	3.3	3.47	V
	VDDA18			1.70	1.8	1.90	1.70	1.8	1.90	1.70	1.8	1.90	V
DIGITAL SUPPLY VOLTAGES	VDDD33			3.13	3.3	3.47	3.13	3.3	3.47	3.13	3.3	3.47	V
	VDDD18			1.70	1.8	1.90	1.70	1.8	1.90	1.70	1.8	1.90	V
POWER CONSUMPTION	Bypass Mode				380			380			380		mW
	FIR Interpolation Filter Enabled				550			550			550		mW
	Standby Power				TBD			TBD			TBD		mW
SUPPLY CURRENTS 1X Mode	IDDA33				25			TBD			TBD		mA
	IDDA18				47			TBD			TBD		mA
	IDDD33				10			TBD			TBD		mA
	IDDD18				122			TBD			TBD		mA
SUPPLY CURRENTS 2x Mode, Interpoation Enabled	IDDA33				25			TBD			TBD		mA
	IDDA18				47			TBD			TBD		mA
	IDDD33				10			TBD			TBD		mA
	IDDD18				234			TBD			TBD		mA

Table 1: DC Specifications

[1] Specifications subject to change without notice

DIGITAL SPECIFICATIONS[1]

(VDDA33 = VDDD33 = 3.3 V, VDDA18 = VDDD18 = VDDCLK = 1.8 V, MAXIMUM SAMPLE RATE, FS = 20MA, 1X MODE, 25 OHM 1% BALANCED LOAD, UNLESS OTHERWISE NOTED)

Parameter		Temp	Test Level	AD9736,35,34			Unit
				Min	Typ	Max	
LVDS DATA INPUTS (DB[13:0]+, DB[13:0]-) DB+ = Via, DB- = Vib	Input voltage range, Via or Vib			825		1575	mV
	Input differential threshold			-100		100	mV
	Input differential hysteresis				20		mV
	Receiver differential input impedance			80		120	Ω
	LVDS input rate			1200			MSPS
	LVDS data Bit Error Rate				TBD		Err/Bit
LVDS CLOCK INPUT (DATACLK_IN+, DATACLK_IN-) DATACLK+ = Via, DATACLK- = Vib	Input voltage range, Via or Vib			825		1575	mV
	Input differential threshold			-100		100	mV
	Input differential hysteresis				20		mV
	Receiver differential input impedance			80		120	Ω
	Maximum Clock Rate			600			MHz
LVDS CLOCK OUTPUT (DATACLK_OUT+, DATACLK_ OUT-) DATACLK_OUT+ = Voa, DATACLK_OUT- = Vob 100 ohm termination	Output voltage high, Voa or Vob					1375	mV
	Output voltage low, Voa or Vob			1025			mV
	Output differential voltage			150	200	250	mV
	Output offset voltage			1150		1250	mV
	Output impedance, single ended			80	100	120	Ω
	Ro mismatch between A & B					10	%
	Change in |Vod| between '0' and '1'					25	mV
	Change in Vos between '0' and '1'					25	mV
	Output current – Driver shorted to ground					20	mA
	Output current – Drivers shorted together					4	mA
	Power-off output leakage					TBD	mA
	Maximum Clock Rate			600			MHz
DAC CLOCK INPUT (CLK+, CLK-)	Differential peak-to-peak Voltage				800		mV
	Common Mode Voltage				400		mV
	Maximum Clock Rate			1200			MHz
SERIAL PERIPHERAL INTERFACE	Maximum Clock Rate (SCLK, $1/t_{SCLK}$)					20	MHz
	Minimum pulse width high, t_{PWH}			20			ns
	Minimum pulse width low, t_{PWL}			20			ns
	Minimum SDIO and CSB to SCLK setup, t_{DS}				10		ns
	Minimum SCLK to SDIO hold, t_{DH}				5		ns
	Maximum SCLK to valid SDIO and SDO, t_{DV}				20		ns
	Minimum SCLK to invalid SDIO and SDO, t_{DNV}				5		ns

Table 2: Digital Specifications

[1] LVDS Drivers and Receivers are compliant to the IEEE-1596 Reduced Range Link, unless otherwise noted

AC SPECIFICATIONS

(VDDA33 = VDDD33 = 3.3 V, VDDA18 = VDDD18 = VDDCLK = 1.8 V, MAXIMUM SAMPLE RATE, FS = 20MA, 1X MODE, 25 OHM 1% BALANCED LOAD, UNLESS OTHERWISE NOTED)

Parameter		Temp	Test Level	AD9736			AD9735			AD9734			Unit
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
DYNAMIC PERFORMANCE	Maximum Update Rate				1200			1200			1200		MSPS
	Output Settling Time (tst) (to 0.025%)				TBD			TBD			TBD		ns
	Output Rise Time (10% to 90%)				TBD			TBD			TBD		ns
	Output Fall Time (90% to 10%)				TBD			TBD			TBD		ns
	Output Noise (IoutFS=20mA)				TBD			TBD			TBD		pA/rtHz
SPURIOUS FREE DYNAMIC RANGE (SFDR)	f_{DAC} = 1200 MSPS, f_{OUT} = 50 MHz				80								dBc
	f_{DAC} = 1200 MSPS, f_{OUT} = 100 MHz				77								dBc
	f_{DAC} = 1200 MSPS, f_{OUT} = 316 MHz				63								dBc
	f_{DAC} = 1200 MSPS, f_{OUT} = 550 MHz				55								dBc
Two Tone Intermodulation Distortion (IMD)	f_{DAC} = 1200 MSPS, f_{OUT} = 50 MHz				85								dBc
	f_{DAC} = 1200 MSPS, f_{OUT} = 100 MHz				84								dBc
	f_{DAC} = 1200 MSPS, f_{OUT} = 316 MHz				74								dBc
	f_{DAC} = 1200 MSPS, f_{OUT} = 550 MHz				65								dBc
Noise Spectral Density (NSD)	f_{DAC} = 1200 MSPS, f_{OUT} = 50 MHz				-165								dBm/Hz
	f_{DAC} = 1200 MSPS, f_{OUT} = 100 MHz				-164								dBm/Hz
	f_{DAC} = 1200 MSPS, f_{OUT} = 316 MHz				-158								dBm/Hz
	f_{DAC} = 1200 MSPS, f_{OUT} = 550 MHz				-155								dBm/Hz

Table 3: AC Specifications

EXPLANATION OF TEST LEVELS

TEST LEVEL

I 100% production tested.

II 100% production tested at +25°C and guaranteed by design and characterization at specified temperatures.

III Sample Tested Only

IV Parameter is guaranteed by design and characterization testing.

V Parameter is a typical value only.

VI 100% production tested at +25°C and guaranteed by design and characterization for industrial temperature range.

PIN FUNCTION DESCRIPTIONS

Pin No.	Name	Description
A1, A2, A3, B1, B2, B3, C1, C2, C3, D2, D3	VDDC	1.8V, Clock supply
A4, A5, A6, A9, A10, A11, B4, B5, B6, B9, B10, B11, C4, C5, C6, C9, C10, C11, D4, D5, D6, D9, D10, D11	VSSA	Analog supply ground
A7, B7, C7, D7	IOUTB	DAC negative output, 10mA to 30mA full scale output current
A8, B8, C8, D8	IOUTA	DAC positive output, 10mA to 30mA full scale output current
A12, A13, B12, B13, C12, C13, D12, D13	VDDA	3.3V Analog supply
A14, K1	DNC	Do Not Connect
B14	I120	Nominal 1.2V reference tied to analog ground via 10kohm resistor to generate a 120uA reference current
C14	VREF	Bandgap voltage reference I/O, tie to analog ground via 1nF capacitor, output impedance approximately 5kohms
D1, E2, E3, E4, F2, F3, F4, G1, G2, G3, G4	VSSC	Clock supply ground
D14	IPTAT	Factory test, output current proportional to absolute temperature, approximately 10uA at 25C with approximately 20nA/C slope
E1, F1	CLK-, CLK+	Negative, Positive DAC clock input (DACCLK)
E11, E12, F11, F12, G11, G12	VSSA	Analog supply ground shield
E13	IRQ / UNSIGNED	If PIN_MODE = 0, IRQ: Active low open-drain interrupt request output, pull up to VDD3.3 with 10kohm resistor If PIN_MODE = 1, UNSIGNED: Digital input pin where 0 = two's complement input data format, 1 = unsigned
E14	RESET / PD	If PIN_MODE = 0, RESET: 1 resets the AD9736 If PIN_MODE = 1, PD: 1 puts the AD9736 in the power down state
F13	CSB / 2x	See SPI and PIN Mode sections for pin description
F14	SDIO / FIFO	See SPI and PIN Mode sections for pin description
G13	SCLK / FSC0	See SPI and PIN Mode sections for pin description
G14	SDO / FSC1	See SPI and PIN Mode sections for pin description
H1, H2, H3, H4, H11, H12, H13, H14, J1, J2, J3, J4, J11, J12, J13, J14	VDD	1.8V Digital supply
K2, K3, K4, K11, K12, L2, L3, L4, L5, L6, L9, L10, L11, L12, M3, M4, M5, M6, M9, M10, M11, M12	VSS	Digital supply ground
K13, K14	DB<13> -, +	Negative, Positive data input bit 13 (MSB), reduced swing LVDS
L1	PIN_MODE	0, SPI Mode, SPI enabled 1, PIN Mode, SPI disabled, direct pin control
L7, L8, M7, M8, N7, N8, P7, P8	VDD33	3.3V Digital supply
L13, L14	DB<12> -, +	Negative, Positive data input bit 12, reduced swing LVDS
M2, M1	DB<0> -, +	Negative, Positive data input bit 0 (LSB), reduced swing LVDS
M13, M14	DB<11> -, +	Negative, Positive data input bit 11, reduced swing LVDS
N1, P1	DB<1> -, +	Negative, Positive data input bit 1, reduced swing LVDS
N2, P2	DB<2> -, +	Negative, Positive data input bit 2, reduced swing LVDS
N3, P3	DB<3> -, +	Negative, Positive data input bit 3, reduced swing LVDS
N4, P4	DB<4> -, +	Negative, Positive data input bit 4, reduced swing LVDS
N5, P5	DB<5> -, +	Negative, Positive data input bit 5, reduced swing LVDS
N6, P6	DATACLK_OUT -, +	Negative, Positive output clock, reduced swing LVDS
N9, P9	DATACLK_IN -, +	Negative, Positive data input clock, reduced swing LVDS
N10, P10	DB<6> -, +	Negative, Positive data input bit 6, reduced swing LVDS
N11, P11	DB<7> -, +	Negative, Positive data input bit 7, reduced swing LVDS
N12, P12	DB<8> -, +	Negative, Positive data input bit 8, reduced swing LVDS
N13, P13	DB<9> -, +	Negative, Positive data input bit 9, reduced swing LVDS
N14, P14	DB<10> -, +	Negative, Positive data input bit 10, reduced swing LVDS

PIN CONFIGURATION

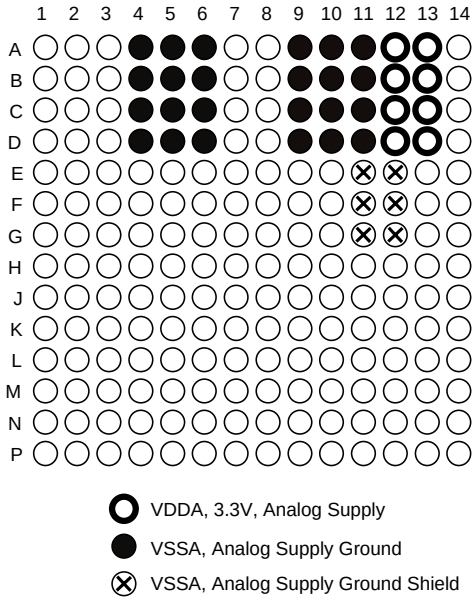


Figure 2. AD9736 Analog Supply Pins (TOP view)

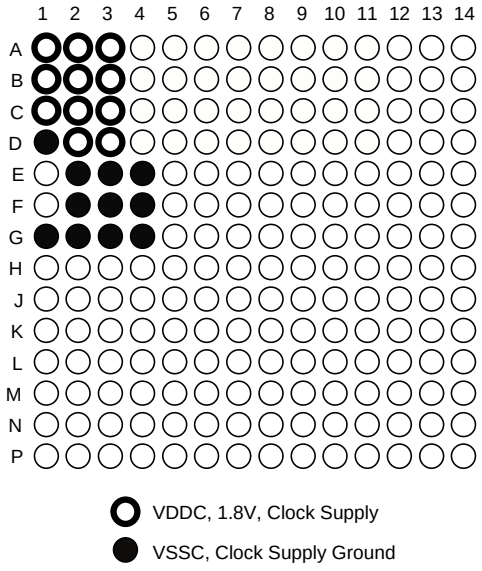


Figure 3. AD9736 Clock Supply Pins (TOP view)

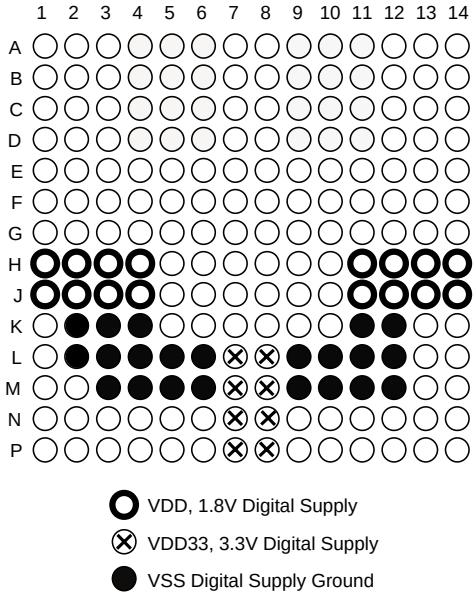


Figure 4. AD9736 Digital Supply Pins (TOP view)

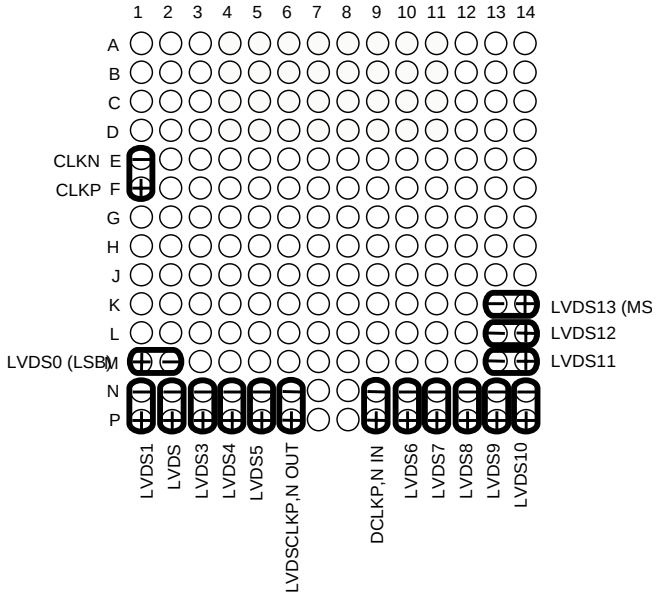


Figure 5. AD9736 Digital LVDS Inputs, Clock I/O (TOP view)

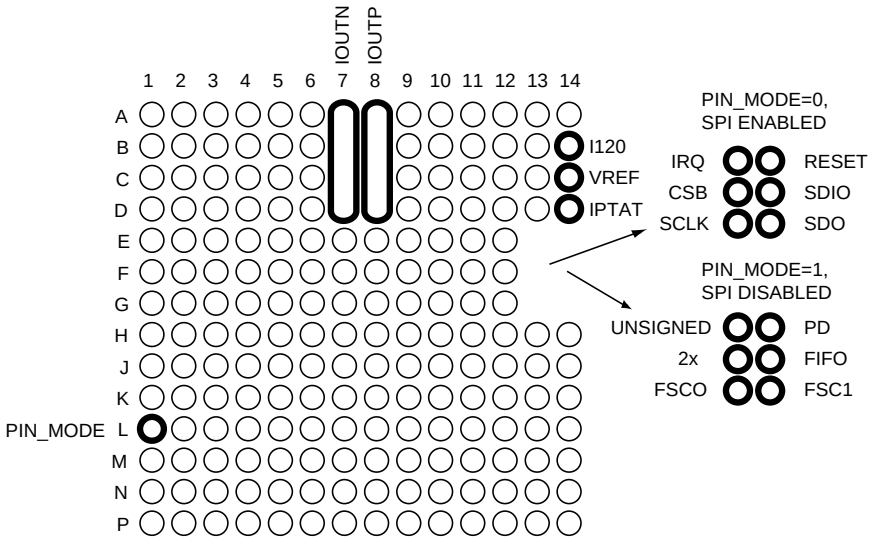
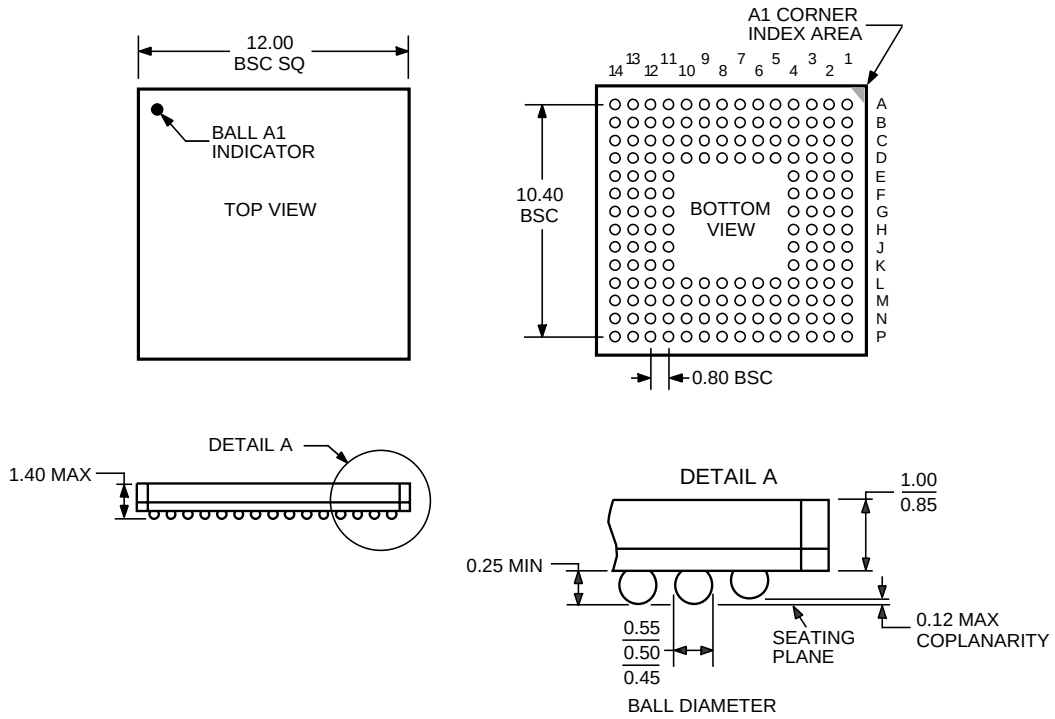


Figure 6. AD9736 Analog I/O and SPI Control Pins (TOP view)

PACKAGE OUTLINE

ANALOG DEVICES

160-Lead Chip Scale Ball Grid Array [CSPBGA]
(BC-160)
Dimensions shown in millimeters



COMPLIANT WITH JEDEC STANDARDS MO-205-AE.

Figure 7. AD9736 BGA Package Outline Drawing

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Ordering Guide

Model	Temperature Range	Description
AD9736BBC	-40°C to +85°C (Ambient)	160-Lead Chip Scale BGA
AD9736-EB	25°C (Ambient)	Evaluation Board

Table 4: Ordering Guide

TYPICAL PERFORMANCE CHARACTERISTICS

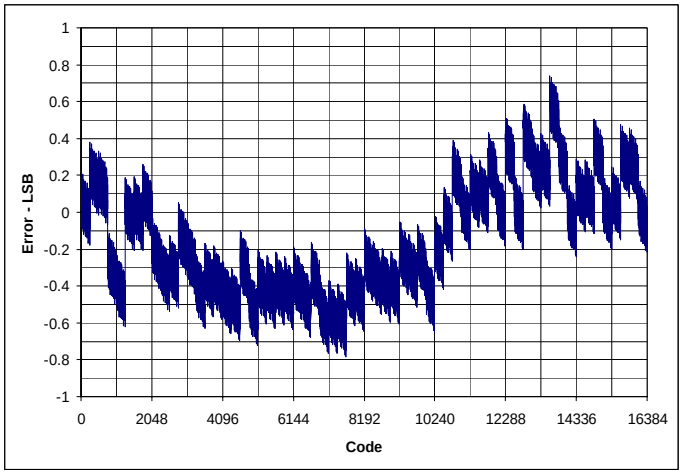


Figure 8. AD9736, Typical INL

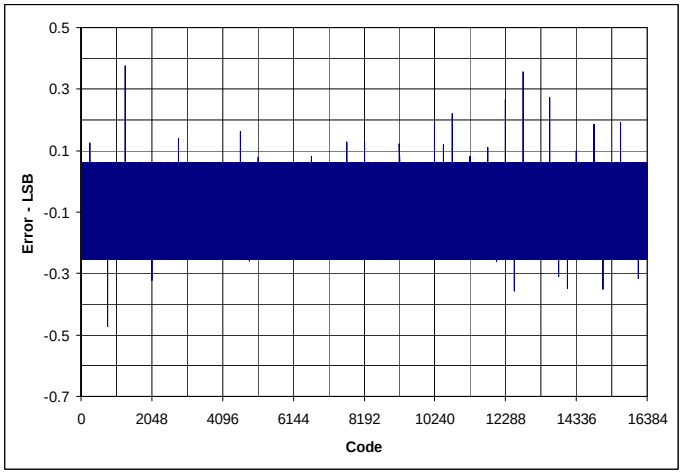


Figure 9. AD9736, Typical DNL

Figure 10. AD9736, 3rd Order IMD vs. Fout and Sample Rate

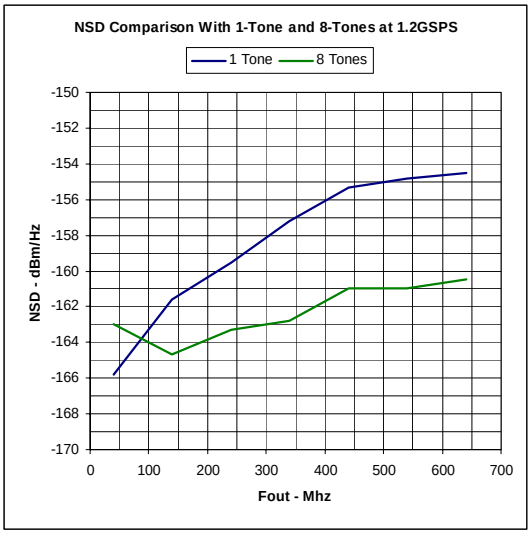


Figure 11. AD9736, Noise Spectral Density (NSD) vs. Fout at 1.2GSPS

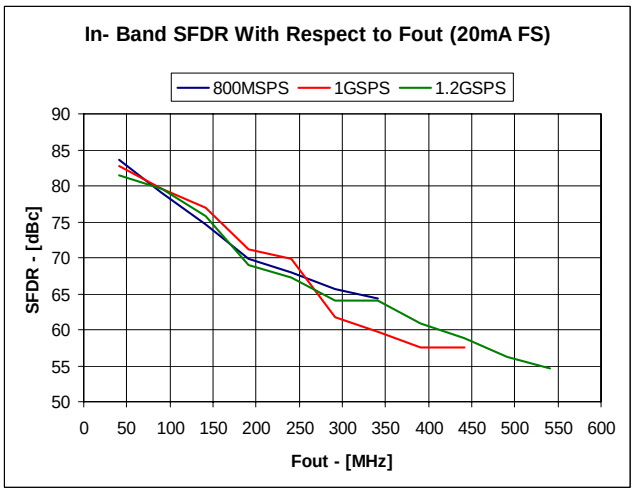


Figure 12. AD9736, In Band SFDR vs. Fout and Sample Rate

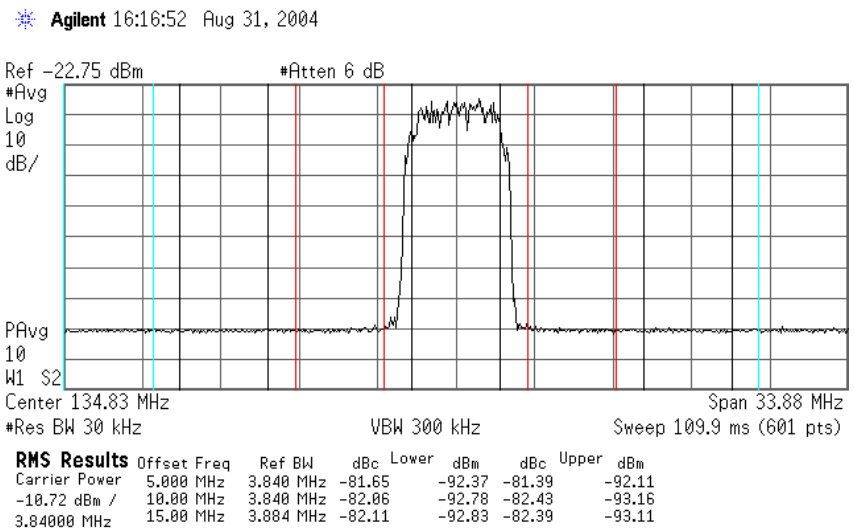


Figure 13. AD9736, WCDMA carrier at 134.83MHz, fdata=491.52MSPS

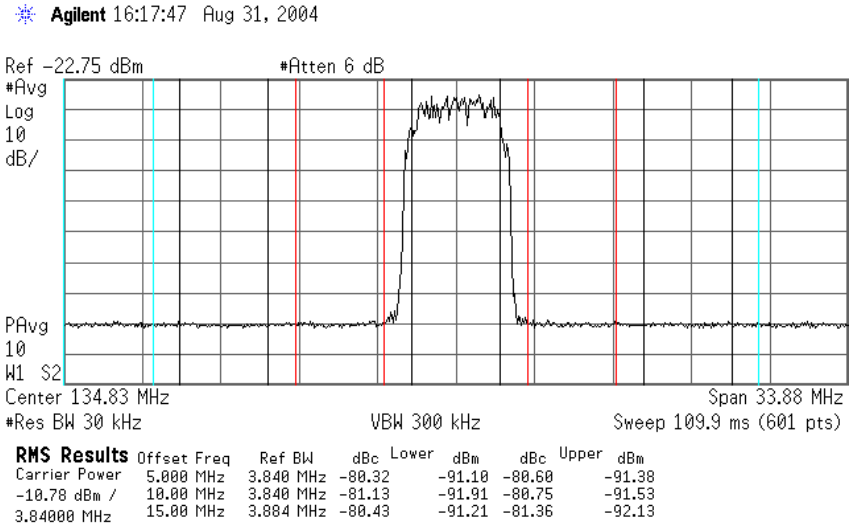


Figure 14. AD9735, WCDMA carrier at 134.83MHz, fdata=491.52MSPS

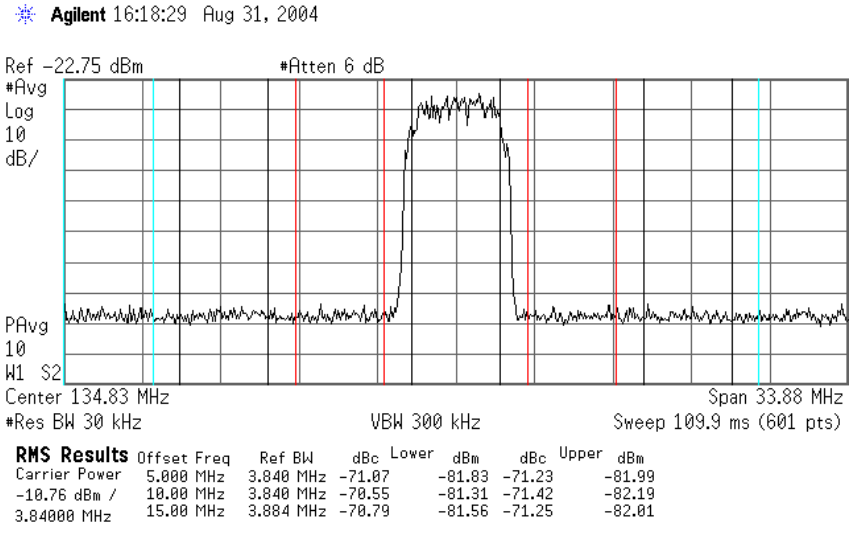


Figure 15. AD9734, WCDMA carrier at 134.83MHz, fdata=491.52MSPS

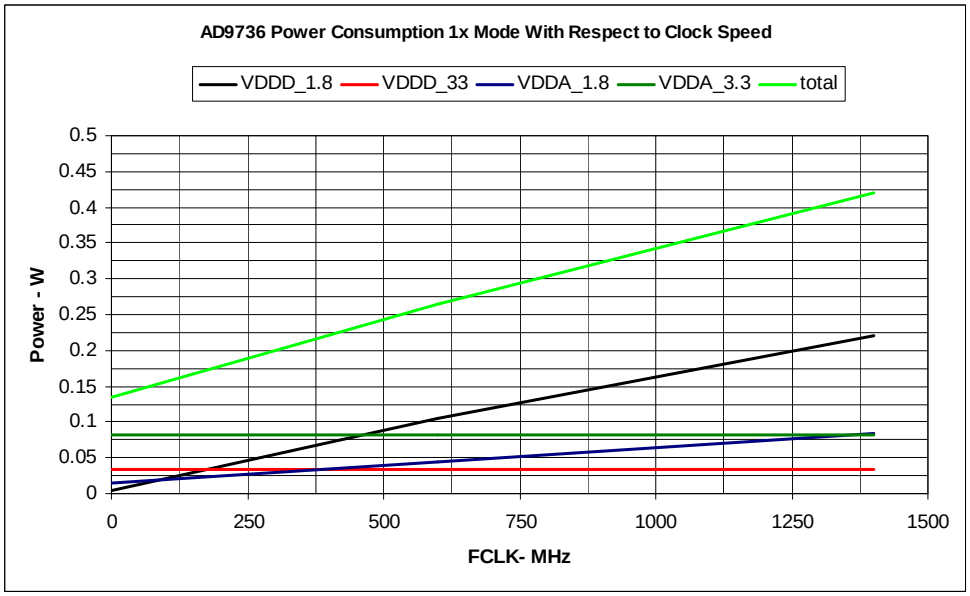


Figure 16. AD9736 Power vs. Clock Frequency

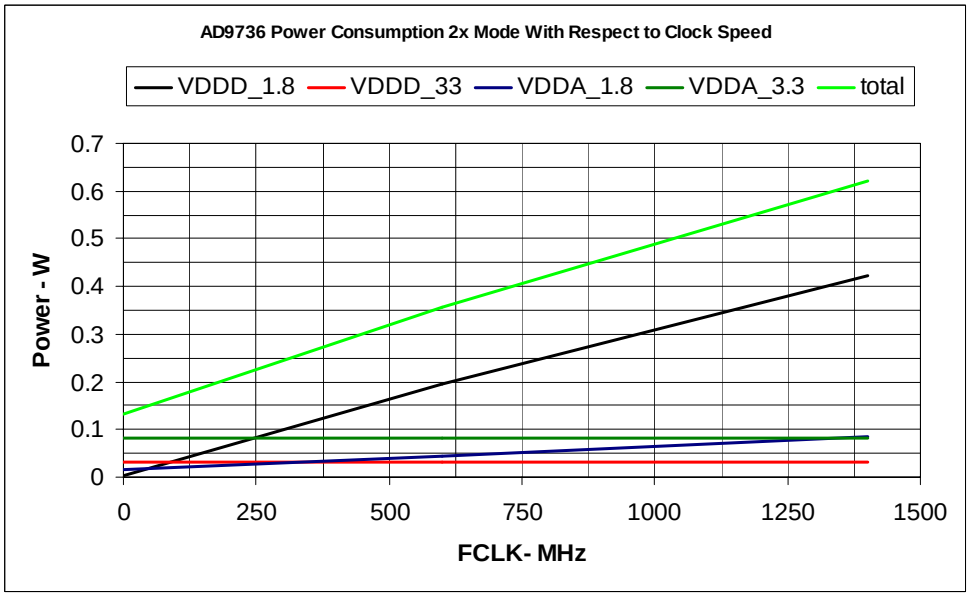


Figure 17. AD9736 Power vs. Clock Frequency in 2x Mode

SPI REGISTER MAP

ADR DEC	ADR HEX	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default (HEX)	PIN MODE (HEX)
0	00	**MODE**	SDIO_DIR	LSBFIRST	RESET	LONG_INS	2X MODE	FIFO MODE	DATAFRMT	PD	00	00
1	01	**IRQ**	LVDS	SYNC	CROSS	RESV'D	IE_LVDS	IE_SYNC	IE_CROSS	RESV'D	00	00
2	02	**FSC_1**	SLEEP						FSC<9>	FSC<8>	02	02
3	03	**FSC_2**	FSC<7>	FSC<6>	FSC<5>	FSC<4>	FSC<3>	FSC<2>	FSC<1>	FSC<0>	00	00
4	04	**LVDS_CNT1**	MSD<3>	MSD<2>	MSD<1>	MSD<0>	MHD<3>	MHD<2>	MHD<1>	MHD<0>	00	00
5	05	**LVDS_CNT2**	SD<3>	SD<2>	SD<1>	SD<0>	LCHANGE	ERR_HI	ERR_LO	CHECK	00	00
6	06	**LVDS_CNT3**	LSURV	LAUTO	LFLT<3>	LFLT<2>	LFLT<1>	LFLT<0>	LTRH<1>	LTRH<0>	00	00
7	07	**SYNC_CNT1**	FIFOSTAT3	FIFOSTAT2	FIFOSTAT1	FIFOSTAT0	VALID	SCHANGE	PHOF<1>	PHOF<0>	00	00
8	08	**SYNC_CNT2**	SSURV	SAUTO	SFLT<3>	SFLT<2>	SFLT<1>	SFLT<0>	RESV'D	STRH<0>	00	00
9	09	**RESERVED**										
10	0A	**RESERVED**										
11	0B	**RESERVED**										
12	0C	**RESERVED**										
13	0D	**RESERVED**										
14	0E	**ANA_CNT1**	MSEL<1>	MSEL<0>				TRMBG<2>	TRMBG<1>	TRMBG<0>	C0	C0
15	0F	**ANA_CNT2**	HDRM<7>	HDRM<6>	HDRM<5>	HDRM<4>	HDRM<3>	HDRM<2>	HDRM<1>	HDRM<0>	CA	CA
16	10	**RESERVED**										
17	11	**BIST_CNT**	SEL<1>	SEL<0>	SIG_READ			LVDS_EN	SYNC_EN	CLEAR	00	00
18	12	**BIST<7:0>**										
19	13	**BIST<15:8>**										
20	14	**BIST<23:16>**										
21	15	**BIST<31:24>**										
22	16	**CCLK_DIV**	RESV'D	RESV'D	RESV'D	RESV'D	CCD<3>	CCD<2>	CCD<1>	CCD<0>	00	00
31	1F	**VERSION**	VER<5>	VER<4>	VER<3>	VER<2>	VER<1>	VER<0>	RES10	RES12		

Note: Write '0' to unspecified or reserved bit locations. Reading these bits will return unknown values.

Table 5. SPI Register Map

SPI REGISTER DESCRIPTIONS

REG 00 -> MODE
Reading REG 00 returns previously written values for all defined register bits unless otherwise noted. Reset value in **bold** text.

ADR	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	MODE	SDIO_DIR	LSB/MSB	RESET	LONG_INS	2X MODE	FIFO MODE	DATAFRMT	PD

SDIO_DIR	: WRITE ->	**0**, Input only per SPI standard 1, Bidirectional per SPI standard
LSBFIRST	: WRITE ->	**0**, MSB first per SPI standard 1, LSB first per SPI standard NOTE: Only change LSB/MSB order in single byte instructions to avoid erratic behavior due to bit order errors
RESET	: WRITE->	**0**, Execute software reset of SPI and controllers, reload default register values EXCEPT registers 0x00 and 0x04 1, Set software reset prior to writing '0' to execute the software reset
LONG_INS	: WRITE ->	**0**, Short (single-byte) instruction word 1, Long (two-byte) instruction word, not necessary since the maximum internal address is REG31 (0x1F)
2X_MODE	: WRITE ->	**0**, Disable 2x Interpolation Filter 1, Enable 2x Interpolation Filter
FIFO_MODE	: WRITE ->	**0**, Disable FIFO synchronization 1, Enable FIFO synchronization
DATAFRMT	: WRITE ->	**0**, Signed input DATA with midscale = 0x0000 1, Unsigned input DATA with midscale = 0x2000
PD	: WRITE ->	**0**, Enable LVDS Receiver, DAC and Clock Circuitry 1, Power down LVDS Receiver, DAC and Clock Circuitry

REG 01 -> Interrupt Request (IRQ)
Reading REG 01 returns previously written values for all defined register bits unless otherwise noted. Reset value in **bold** text.

ADR	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x01	IRQ	LVDS	SYNC	CROSS	RESV'D	IE_LVDS	IE_SYNC	IE_CROSS	RESV'D

LVDS	: WRITE ->	Don't Care
	: READ ->	0, No active LVDS receiver interrupt 1, Interrupt in LVDS receiver occurred
SYNC	: WRITE ->	Don't Care
	: READ ->	0, No active SYNC logic interrupt 1, Interrupt in SYNC logic occurred
CROSS	: WRITE ->	Don't Care
	: READ ->	0, No active CROSS logic interrupt 1, Interrupt in CROSS logic occurred
IE_LVDS	: WRITE ->	**0**, Reset LVDS receiver interrupt and disable future LVDS receiver interrupts 1, Enable LVDS receiver interrupt to activate IRQ pin
IE_SYNC	: WRITE ->	**0**, Reset SYNC logic interrupt and disable future SYNC logic interrupts 1, Enable SYNC logic interrupt to activate IRQ pin
IE_CROSS	: WRITE ->	**0**, Reset CROSS logic interrupt and disable future CROSS logic interrupts 1, Enable CROSS logic interrupt to activate IRQ pin

REG 02, 03 -> Full Scale Current (FSC)
Reading REG 02 & 03 return previously written values for all defined register bits unless otherwise noted. Reset value in **bold** text.

ADR	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x02	FSC_1	SLEEP						FSC<9>	FSC<8>
0x03	FSC_2	FSC<7>	FSC<6>	FSC<5>	FSC<4>	FSC<3>	FSC<2>	FSC<1>	FSC<0>

SLEEP	: WRITE ->	**0**, Enable DAC output 1, Set DAC output current to 0mA
FSC<9:0>	: WRITE ->	0x000, 10mA full scale output current **0x200**, 20mA full scale output current 0x3FF, 30mA full scale output current NOTE: Iout = (72 + 192 * (FSC<9:0> / 1024)) * I120 where I120 = Vref / R120u, for example 1.2V / 10k = 120uA

REG 04, 05, 06 -> LVDS Controller (LVDS_CNT)
Reading REG 04, 05 & 06 return previously written values for all defined register bits unless otherwise noted. Reset value in **bold** text.

ADR	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x04	LVDS_CNT1	MSD<3>	MSD<2>	MSD<1>	MSD<0>	MHD<3>	MHD<2>	MHD<1>	MHD<0>
0x05	LVDS_CNT2	SD<3>	SD<2>	SD<1>	SD<0>	LCHANGE	ERR_HI	ERR_LO	CHECK
0x06	LVDS_CNT3	LSURV	LAUTO	LFLT<3>	LFLT<2>	LFLT<1>	LFLT<0>	LTRH<1>	LTRH<0>

MSD<3:0>	: WRITE ->	**0x0**, Set setup delay for the measurement system
	: READ ->	If (LAUTO == 1) the latest measured value for the setup delay If (LAUTO == 0) read back of the last SPI write to this bit
MHD<3:0>	: WRITE ->	**0x0**, Set hold delay for the measurement system
	: READ ->	If (LAUTO == 1) the latest measured value for the hold delay If (LAUTO == 0) read back of the last SPI write to this bit
SD<3:0>	: WRITE->	**0x0**, Set sample delay
	: READ ->	If (LAUTO == 1) the result of a measurement cycle is stored in this register If (LAUTO == 0) read back of the last SPI write to this bit
LCHANGE	: READ ->	0, No change from previous measurement 1, Change in value from the previous measurement NOTE: The average filter and the threshold detection are not applied to this bit
ERR_HI	: READ ->	One of the 15 LVDS inputs is above the input voltage limits of the IEEE reduce link spec.
ERR_LO	: READ ->	One of the 15 LVDS inputs is below the input voltage limits of the IEEE reduced link spec.
CHECK	: READ ->	0, Phase measurement – sampling in the previous or following DATA cycle 1, Phase measurement – sampling in the correct DATA cycle
LSURV	: WRITE ->	**0**, The controller stops after completion of the current measurement cycle 1, Continuous measurements are taken and an interrupt is issued if the clock alignment drifts beyond the threshold value
LAUTO	: WRITE ->	**0**, Sample delay is not automatically updated 1, Continuously starts measurement cycles and updates the sample delay according to the measurement NOTE: LSURV (REG06 Bit 7) must be set to 1 and the LVDS IRQ (REG01 Bit 3) must be set to 0 for AUTO mode
LFLT<3:0>	: WRITE ->	**0x0**, Average filter length, Delay = Delay + Delta Delay / 2^ LFLT<3:0>, values greater than 12 (0x0C) are clipped to 12

LTRH<2:0> :	: WRITE ->	**000**, Set auto update threshold values

REG 07, 08 -> SYNC Controller (SYNC_CNT)
Reading REG 07 & 08 return previously written values for all defined register bits unless otherwise noted. Reset value in **bold** text.

ADR	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x07	SYNC_CNT1	FIFOSTAT3	FIFOSTAT2	FIFOSTAT1	FIFOSTAT0	VALID	SCHANGE	PHOF<1>	PHOF<0>
0x08	SYNC_CNT2	SSURV	SAUTO	SFLT<3>	SFLT<2>	SFLT<1>	SFLT<0>	RESV'D	STRH<0>

FIFOSTAT<2:0>	: READ ->	Position of FIFO read counter, range from 0 to 7
FIFOSTAT<3>	: READ ->	0, SYNC logic OK 1, Error in SYNC logic
VALID	: READ ->	0, FIFOSTAT<3:0> is not valid yet 1, FIFOSTAT<3:0> is valid after a reset
SCHANGE	: READ ->	0, No change in FIFOSTAT<3:0> 1, FIFOSTAT<3:0> has changed since the previous measurement cycle when SSURV = 1 (surveillance mode active)
PHOF<1:0>	: WRITE ->	**00**, Change the readout counter
	: READ ->	Current setting of the readout counter (PHOF<1:0>) in surveillance mode (SSURV = 1) after an interrupt Current calculated optimal readout counter value in AUTO mode (SAUTO = 1)
SSURV	: WRITE ->	**0**, The controller stops after completion of the current measurement cycle 1, Continuous measurements are taken and an interrupt is issued if the readout counter drifts beyond the threshold value
SAUTO	: WRITE ->	**0**, Readout counter (PHOF<3:0>) is not automatically updated 1, Continuously starts measurement cycles and updates the readout counter according to the measurement NOTE: SSURV (REG08 Bit 7) must be set to 1 and the SYNC IRQ (REG01 Bit 2) must be set to 0 for AUTO mode
SFLT<3:0>	: WRITE ->	**0x0**, Average filter length, FIFOSTAT = FIFOSTAT + Delta FIFOSTAT / 2 ^ SFLT<3:0>, values greater than 12 (0x0C) are clipped to 12
STRH<0>	: WRITE ->	**0**, If FIFOSTAT<2:0> = 0 | 7, generate a SYNC interrupt 1, If FIFOSTAT<2:0> = 0 | 1 | 6 | 7, generate a SYNC interrupt

REG 14, 15 -> Analog Control (ANA_CNT)
Reading REG 14 & 15 return previously written values for all defined register bits unless otherwise noted. Reset value in **bold** text.

ADR	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0E	ANA_CNT1	MSEL<1>	MSEL<0>				TRMBG<2>	TRMBG<1>	TRMBG<0>
0x0F	ANA_CNT2	HDRM<7>	HDRM<6>	HDRM<5>	HDRM<4>	HDRM<3>	HDRM<2>	HDRM<1>	HDRM<0>

MSEL<1:0>	: WRITE ->	00, Mirror roll off frequency control = bypass 01, Mirror roll off frequency control = narrowest bandwidth 10, Mirror roll off frequency control = medium bandwidth **11**, Mirror roll off frequency control = widest bandwidth NOTE: See plot in the applications section
TRMBG<2:0>	: WRITE ->	**000**, Bandgap temperature characteristic trim NOTE: See plot in the applications section
HDRM<7:0>	: WRITE ->	**0xCA**, Output stack headroom control HDRM<7:4> set reference offset from Vdd3v (vcas centering) HDRM<3:0> set overdrive (current density) trim (temperature tracking) Note: Set to 0xCA for optimum performance

REG 17, 18, 19, 20, 21 -> Built-in Self Test Control (BIST_CNT)
Reading REG17, 18, 19, 20 & 21 return previously written values for all defined register bits unless otherwise noted. Reset value in **bold** text.

ADR	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x11	BIST_CNT	SEL<1>	SEL<0>	SIG_READ			LVDS_EN	SYNC_EN	CLEAR
0x12	BIST<7:0>	BIST<7>	BIST<6>	BIST<5>	BIST<4>	BIST<3>	BIST<2>	BIST<1>	BIST<0>
0x13	BIST<15:8>	BIST<15>	BIST<14>	BIST<13>	BIST<12>	BIST<11>	BIST<10>	BIST<9>	BIST<8>
0x14	BIST<23:16>	BIST<23>	BIST<22>	BIST<21>	BIST<20>	BIST<19>	BIST<18>	BIST<17>	BIST<16>
0x15	BIST<31:24>	BIST<31>	BIST<30>	BIST<29>	BIST<28>	BIST<27>	BIST<26>	BIST<25>	BIST<24>

SEL<1:0>	: WRITE ->	00, Write result of the LVDS Phase 1 BIST to BIST<31:0> 01, Write result of the LVDS Phase 2 BIST to BIST<31:0> 10, Write result of the SYNC Phase 1 BIST to BIST<31:0> 11, Write result of the SYNC Phase 2 BIST to BIST<31:0>
SIG_READ	: WRITE ->	0, No action 1, Enable BIST signature readback
LVDS_EN	: WRITE->	0, No action 1, Enable LVDS BIST
SYNC_EN	: WRITE ->	0, No Action 1, Enable SYNC BIST
CLEAR	: WRITE ->	0, No Action 1, Clear all BIST registers
BIST<31:0>	: READ ->	Results of the Built-in Self Test

REG 22 -> Controller Clock Pre-divider (CCLK_DIV)
Reading REG 22 returns previously written values for all defined register bits unless otherwise noted. Reset value in **bold** text.

ADR	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x16	CCLK_DIV	RESV'D	RESV'D	RESV'D	RESV'D	CCD<3>	CCD<2>	CCD<1>	CCD<0>

CCD<3:0>	: WRITE ->	**0x0**, Controller Clock = DACCLK / 16 0x1, Controller Clock = DACCLK / 32 0x2, Controller Clock = DACCLK / 64 … 0xF, Controller Clock = DACCLK / 524288 NOTE: The 100MHz to 1.2GHz DACCLK must be divided to less than 10MHz for correct operation. CCD<3:0> must be programmed to divide the DACCLK so that this relationship is not violated. Controller Clock = DACCLK / (2 ^ (CCD<3:0> + 4))

REG 31 -> VERSION
Reading REG 31 returns previously written values for all defined register bits unless otherwise noted. Reset value in **bold** text.

ADR	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x1F	VERSION	VER<5>	VER<4>	VER<3>	VER<2>	VER<1>	VER<0>	RES10	RES12

VER<5:0>	: READ ->	Version number (part ID), 00001, Revision 1, initial release
RES10 (msb) RES12 (lsb)	: READ ->	00, 14-bit DAC 01, 12-bit DAC 10, 10-bit DAC

GENERAL DESCRIPTION

The AD9736/35/34 are 14/12/10-bit DACs which run at an update rate up to 1.2GSPS. Input data can be accepted up to the full 1.2GSPS rate or a 2x interpolation filter may be enabled (2x mode) allowing full-speed operation with a 600MSPS input data rate. DATA and DATACLK_IN inputs are parallel LVDS meeting the IEEE reduced swing LVDS specifications with the exception of input hysteresis. The DATACLK_IN input runs at one half the input DATA rate in a double data rate (DDR) format. Each edge of DATACLK_IN is used to transfer DATA into the AD9736 as shown in Figure 25.

The DACCLK (pins E1, F1) directly drives the DAC core to minimize clock jitter. It is also divided by two (1x and 2x mode) then output as the DATACLK_OUT. The DATACLK_OUT signal is used to clock the data source. The DAC expects DDR LVDS data (DB<13:0>) aligned with the DDR input clock (DATACLK_IN) from a circuit similar to the one shown in Figure 35. Clock relationships are shown in Table 6.

MODE	DACCLK	DATACLK OUT	DATACLK IN	DATA
1x	1.2GHz	600MHz	600MHz	1.2GSPS
2x	1.2GHz	600MHz	300MHz	600MSPS

Table 6. AD9736 Clock Relationships

Maintaining correct alignment of data and clock is a common challenge with high-speed DACs, complicated by changes in temperature and other operating conditions. The AD9736 simplifies this high-speed data capture problem with two adaptive closed-loop timing controllers.

One timing controller manages the LVDS data and data clock alignment (LVDS controller) and the other manages the LVDS data and DACCLK alignment (SYNC controller). The LVDS controller locates the data transitions and delays the DATACLK_IN so that its transition is in the center of the valid data window. The SYNC controller manages the FIFO that moves data from the LVDS DATACLK_IN domain to the DACCLK domain. Both controllers can be operated in manual mode under external processor control, surveillance mode where error conditions generate external interrupts or automatic mode where errors are automatically corrected.

The LVDS and SYNC controllers include moving average filtering for noise immunity and variable thresholds to control their activity. Normally the controllers can be set to run in automatic mode and they will make any necessary adjustments without dropping or duplicating samples sent to the DAC. Both controllers require initial calibration prior to entering automatic update mode.

Control of the AD9736 functions is via the serially programmed registers listed in Table 5.

Serial Peripheral Interface

The AD9736 serial port is a flexible, synchronous serial communications port allowing easy interface to many industry-standard microcontrollers and microprocessors. The serial I/O is compatible with most synchronous transfer formats, including both the Motorola SPI® and Intel® SSR protocols. The interface allows read/write access to all registers that configure the AD9736. Single or multiple byte transfers are supported, as well as MSB first or LSB first transfer formats. The AD9736's serial interface port can be configured as a single pin I/O (SDIO) or two unidirectional pins for in/out (SDIO/SDO).

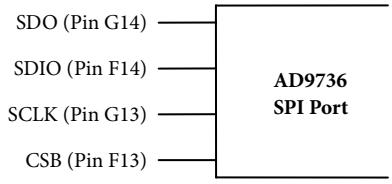


Figure 18. AD9736 SPI Port

The AD9736 may optionally be configured via external pins rather than the serial interface. When the PIN_MODE input (pin L1) is high the serial interface is disabled and its pins are reassigned for direct control of the DAC. Specific functionality is described in the PIN Mode section.

GENERAL OPERATION OF THE SERIAL INTERFACE

There are two phases to a communication cycle with the AD9736. Phase 1 is the instruction cycle, which is the writing of an instruction byte into the AD9736, coincident with the first eight SCLK rising edges. The instruction byte provides the AD9736 serial port controller with information regarding the data transfer cycle, which is Phase 2 of the communication cycle. The Phase 1 instruction byte defines whether the upcoming data transfer is read or write, the number of bytes in the data transfer, and the starting register address for the first byte of the data transfer. The first eight SCLK rising edges of each communication cycle are used to write the instruction byte into the AD9736.

The remaining SCLK edges are for Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the AD9736 and the system controller. Phase 2 of the communication cycle is a transfer of 1, 2, 3, or 4 data bytes as determined by the instruction byte. Using one multibyte transfer is the preferred method. Single byte data transfers are useful to reduce CPU overhead when register access requires one byte only. Registers change immediately upon writing to the last bit of each transfer byte.

CSB can be raised after each sequence of 8 bits (except the last byte) to stall the bus. The serial transfer will resume when CSB is lowered. Stalling on non-byte boundaries will reset the SPI.

SHORT INSTRUCTION MODE (8-BIT INSTRUCTION)

The short instruction byte is shown in Table 7.

MSB							LSB
I7	I6	I5	I4	I3	I2	I1	I0
R/W	N1	N0	A4	A3	A2	A1	A0

Table 7. SPI Instruction Byte

R/W, Bit 7 of the instruction byte, determines whether a read or a write data transfer will occur after the instruction byte write. Logic high indicates read operation. Logic 0 indicates a write operation.
N1, N0, Bits 6 and 5 of the instruction byte, determine the number of bytes to be transferred during the data transfer cycle. The bit decodes are shown in Table 8.

A4, A3, A2, A1, A0, Bits 4, 3, 2, 1, 0 of the instruction byte, determine which register is accessed during the data transfer portion of the communications cycle. For multibyte transfers, this address is the starting byte address. The remaining register addresses are generated by the AD9736 based on the LSBFIRST bit (REG00, bit 6).

N1	N2	Description
0	0	Transfer 1 Byte
0	1	Transfer 2 Bytes
1	0	Transfer 3 Bytes
1	1	Transfer 4 Bytes

Table 8. Byte Transfer Count

LONG INSTRUCTION MODE (16-BIT INSTRUCTION)

The long instruction bytes are shown in Table 7.

MSB							LSB
I15	I14	I13	I12	I11	I10	I9	I8
R/W	N1	N0	A12	A11	A10	A9	A8
I7	I6	I5	I4	I3	I2	I1	I0
A7	A6	A5	A4	A3	A2	A1	A0

Table 9. SPI Instruction Byte

If LONG_INS = 1 (REG00, bit 4) the instruction byte is extended to two bytes where the second byte provides an additional 8 bits of address information. Addresses 0x00 – 0x1F are equivalent in short and long instruction modes. The AD9736 does not use any addresses greater than 31 (0x1F) so always set LONG_INS = 0.

SERIAL INTERFACE PORT PIN DESCRIPTIONS

SCLK—Serial Clock. The serial clock pin is used to synchronize data to and from the AD9736 and to run the internal state machines. SCLK's maximum frequency is 20 MHz. All data input to the AD9736 is registered on the rising edge of SCLK. All data is driven out of the AD9736 on the rising edge of SCLK.

CSB—Chip Select. Active low input starts and gates a communication cycle. It allows more than one device to be used on the same serial communications lines. The SDO and SDIO pins will go to a high impedance state when this input is high. Chip select should stay low during the entire communication cycle.

SDIO—Serial Data I/O. Data is always written into the AD9736 on this pin. However, this pin can be used as a bidirectional data line. The configuration of this pin is controlled by SDIO_DIR at REG00, bit 7. The default is Logic 0, which configures the SDIO pin as unidirectional.

SDO—Serial Data Out. Data is read from this pin for protocols that use separate lines for transmitting and receiving data. In the case where the AD9736 operates in a single bidirectional I/O mode, this pin does not output data and is set to a high impedance state.

MSB/LSB TRANSFERS

The AD9736 serial port can support both most significant bit (MSB) first or least significant bit (LSB) first data formats. This functionality is controlled by LSBFIRST at REG00, bit 6. The default is MSB first (LSBFIRST = 0).

When LSBFIRST = 0 (MSB first) the instruction and data bytes must be written from most significant bit to least significant bit. Multibyte data transfers in MSB first format start with an instruction byte that includes the register address of the most significant data byte. Subsequent data bytes should follow in order from high address to low address. In MSB first mode, the serial port internal byte address generator decrements for each data byte of the multibyte communication cycle.

When LSBFIRST = 1 (LSB first) the instruction and data bytes must be written from least significant bit to most significant bit. Multibyte data transfers in LSB first format start with an instruction byte that includes the register address of the least significant data byte followed by multiple data bytes. The serial port internal byte address generator increments for each byte of the multibyte communication cycle.

The AD9736 serial port controller data address will decrement from the data address written toward 0x00 for multibyte I/O operations if the MSB first mode is active. The serial port controller address will increment from the data address written toward 0x1F for multibyte I/O operations if the LSB first mode is active.

NOTES ON SERIAL PORT OPERATION

The AD9736 serial port configuration is controlled by REG00, bits 4, 5, 6 and 7. It is important to note that the configuration changes immediately upon writing to the last bit of the register. For multibyte transfers, writing to this register may occur during the middle of communication cycle. Care must be taken to compensate for this new configuration for the remaining bytes of the current communication cycle. The same considerations apply to setting the software reset, RESET (REG00, bit 5). All registers are set to their default values EXCEPT REG00 and REG04 which remain unchanged.

Use of only single byte transfers when changing serial port

configurations or initiating a software reset is highly recommended. In the event of unexpected programming sequences the AD9736 SPI may become inaccessible. For example, if user code inadvertently changes the LONG_INS bit or LSBFIRST bit the following bits may have unexpected results. The SPI can be returned to a known state by writing an incomplete byte (1-7 bits) of all zeroes followed by three bytes of 0x00. This will return to MSB first short instructions (REG00 = 0x00) so the device may be reinitialized.

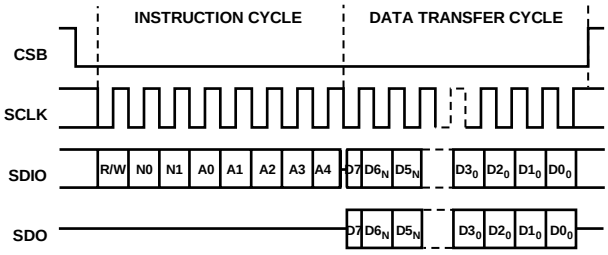


Figure 19. Serial Register Interface Timing MSB First

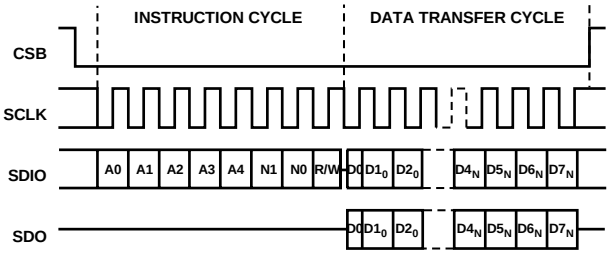


Figure 20. Serial Register Interface Timing LSB First

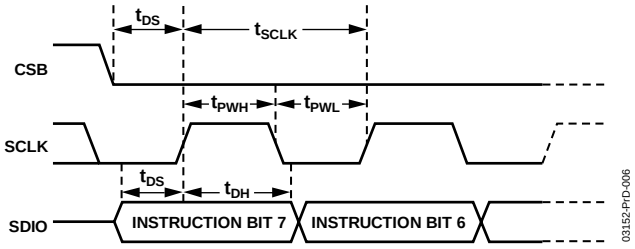


Figure 21. Timing Diagram for SPI Register Write

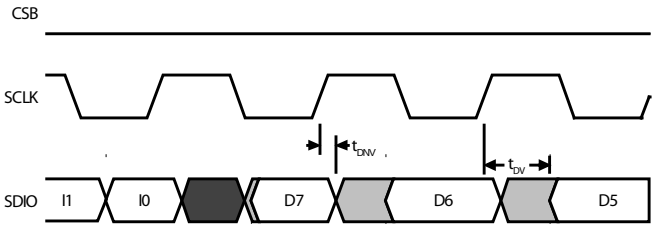


Figure 22. Timing Diagram for SPI Register Read

After the last instruction bit is written to the SDIO pin the driving signal must be set to a high impedance in time for the bus to turn around. The serial output data from the AD9736 will be enabled by the falling edge of SCLK. This causes the first output data bit to be shorter than the remaining data bits as shown in Figure 22.

PIN MODE OPERATION

When the PIN_MODE input (pin L1) is set high, the SPI port is disabled. The SPI port pins are remapped as shown in Table 10. The function of these pins is described in Table 11. The remaining PIN_MODE register settings are shown in Table 5, the SPI register map.

Pin Number	PIN_MODE = 0	PIN_MODE = 1
E13	IRQ	UNSIGNED
F13	CSB	2X
G13	SCLK	FSC0
E14	RESET	PD
F14	SDIO	FIFO
G14	SDO	FSC1

Table 10. SPI_MODE vs. PIN_MODE Inputs

Pin	Function
UNSIGNED	0, Two's complement input data format 1, Unsigned input data format
2X	0, Interpolation disabled 1, Interpolation = 2x enabled
FSC1, FSC0	00, Sleep mode 01, 10mA full scale output current 10, 20mA full scale output current 11, 30mA full scale output current
PD	0, Chip enabled 1, Chip in power down state
FIFO	0, Input FIFO disabled 1, Input FIFO enabled

Table 11. PIN_MODE Input Functions

Care must be taken when using PIN_MODE since only the control bits shown in Table 11 can be changed. If the remaining register default values are not suitable for the desired operation PIN_MODE cannot be used.

AD9736 DATA INTERFACE CONTROLLERS

There are 2 internal controllers that can be utilized in the operation of the AD9736. The first controller helps maintain optimum LVDS data sampling and the second controller helps maintain optimum synchronization between the DACCLK and the incoming data. The LVDS controller is responsible for optimizing the sampling of the data from the LVDS bus (DB13:0) while the SYNC controller resolves timing problems between the DAC_CLK (CLK+, CLK-) and the DATACLK. A block diagram of these controllers is shown in Figure 23.

The controllers are clocked with a divided down version of the DAC_CLK. The divide ratio is set utilizing the controller clock predivider bits (CCD<3:0>) located at REG22 bits 3:0 to generate the controller clock as follows:

Controller Clock = DAC_CLK / (2 ^ (CCD<3 :0> + 4))

NOTE: The controller clock may not exceed 10MHz for correct operation. Until CCD<3:0> has been properly programmed to meet this requirement the DAC output may not be stable.

The LVDS and SYNC controllers can be independently operated in 3 different modes via SPI port REG06 and REG08.

1. Manual Mode
2. Surveillance Mode
3. Auto Mode

In manual mode all of the timing measurements and updates are externally controlled via the SPI.

In surveillance mode each controller takes measurements and calculates a new "optimal" value continuously. The result of the measurement can be passed through an averaging filter before evaluating the results for increased noise immunity. The filtered result is compared to a threshold value set via REG06 and REG08 of the SPI port. If the error is greater then the threshold, an interrupt is triggered and the controller stops. REG01 of the SPI port controls the interrupts with bits 3 and 2 enabling the respective interrupts and bits 7 and 6 indicating the respective controller's interrupt. If an interrupt is enabled it will also activate the AD9736's IRQ pin. In order to clear an interrupt the interrupt enable bit of the respective controller must be set to a zero for at least one controller clock cycle (controller clock < 10MHz).

Auto mode is almost identical to surveillance mode. Instead of triggering an interrupt and stopping the controller, the controller automatically updates its settings to the newly calculated "optimal" value and continues to run.

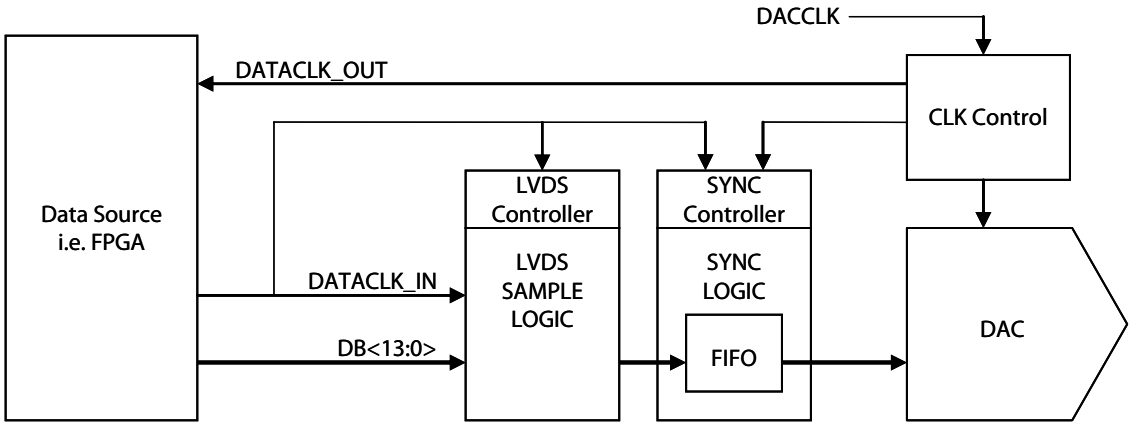


Figure 23.AD9736 Internal Synchronization Engine

AD9736 LVDS Sample Logic

A simplified diagram of the AD9736 LVDS data sampling engine is shown in Figure 24, with the timing relationships shown in Figure 25.

The incoming LVDS data is latched by the DATA SAMPLING SIGNAL (DSS) which is derived from DATACLK_IN. The LVDS controller delays DATACLK_IN to create the DATA SAMPLING SIGNAL (DSS) which is adjusted to sample the LVDS data in the center of the valid data window. The skew between the DATACLK_IN and the LVDS data bits (DB<13:0>) must be minimal (t1 and t2 in Figure 25) for proper operation. Therefore, it is recommended that the DATACLK_IN be generated in the same manner as the LVDS data bits (DB<13:0>) with the same driver and data lines (i.e. it should just be another LVDS data bit running a constant 01010101… sequence, as shown in Figure 35).

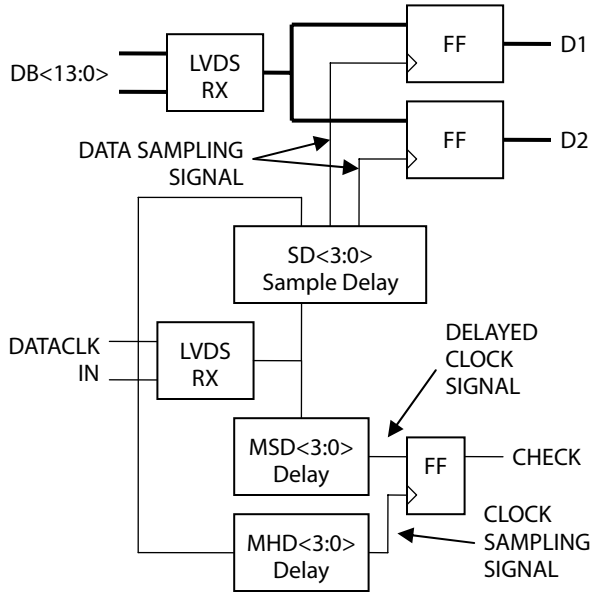


Figure 24. AD9736 Internal LVDS Data Sampling Logic

LVDS SAMPLE LOGIC CALIBRATION

The internal DATA SAMPLING SIGNAL delay must be calibrated to optimize the data sample timing. Once calibrated, the AD9736 can generate an IRQ or automatically correct its timing if temperature or voltage variations change the timing too much. This calibration is done by using the delayed CLOCK SAMPLING SIGNAL (CSS) to sample the DELAYED CLOCK SIGNAL (DCS). The LVDS sampling logic can find the edges of the DATACLK_IN signal and from this measurement the center of the valid data window can be located.

The internal delay line which derives the delayed DATA SAMPLING SIGNAL (DSS) from DATACLK_IN is controlled by SD3:0 (REG05, bits 7:4) while the DELAYED CLOCK SIGNAL (DCS) is controlled by MSD3:0 (REG04, bits 7:4) and the CLOCK SAMPLING SIGNAL (CSS) is controlled by MHD3:0 (REG04, bits 3:0).

DATACLK_IN transitions must be time aligned with the LVDS data (DB<13:0>) transitions. This allows the CLOCK SAMPLING SIGNAL (CSS, derived from the DATACLK_IN), to find the valid data window of DB<13:0> by locating the DATACLK_IN edges. The latching (rising) edge of CSS is initially placed using bits SD<3:0> and can then be shifted to the left using MSD<3:0> and to the right using MHD<3:0>. When CSS samples the DELAYED CLOCK SIGNAL (DCS) and the result is a 1, (which can be read back via the CHECK bit at REG05, bit 0) then the sampling is occurring in the correct data cycle. In order to find the leading edge of the data cycle, increment MSD (Measured Set-up Delay) until CHECK goes low. In order to find the trailing edge, increment MHD (Measured Hold Delay) until CHECK goes low. Always set MHD = 0 when incrementing MSD and vice-versa.

Note: The incremental units of SD, MSD, and MHD are in units of real time, not fractions of a clock cycle. At this time, the delay from each increment of these bits has not been fully characterized. Over process, voltage, and temperature, each increment may introduce between 25 and 100ps of delay with a nominal target of 80ps.

OPERATING THE LVDS CONTROLLER IN MANUAL MODE VIA THE SPI PORT

The manual operation of the LVDS controller allows the user to step through both the set-up and hold delays to calculate the optimal sampling delay (i.e. center of the data eye).

With SD<3:0> and MHD<3:0> set to zero, increment the set-up time delay (MSD<3:0>, REG04, bits 7:4) until the check bit (REG05, bit 0) goes low and record this value. This locates the leading DATACLK_IN (and DATA) transition as shown in Figure 26.

With SD<3:0> and MSD<3:0> set to zero, increment the hold time delay (MHD<3:0>, REG04, bits 3:0) until the check bit (REG05 bit 0) goes low and record this value. This locates the trailing DATACLK_IN (and DATA) transition as shown in Figure 27.

Once both DATACLK_IN edges are located the Sample Delay (SD<3:0>, REG05, bits 7:4) must be updated according to the following equation:

Sample Delay = (MHD – MSD) / 2

After updating SD<3:0>, verify that the sampling signal is in the middle of the valid data window by adjusting both MHD then MSD with the new sample delay until the CHECK bit goes low. The new MHD and MSD values should be equal or within one unit delay if SD<3:0> was set correctly.

NOTE: The Sample Delay calibration just described should be performed prior to enabling Surveillance mode or Auto mode.

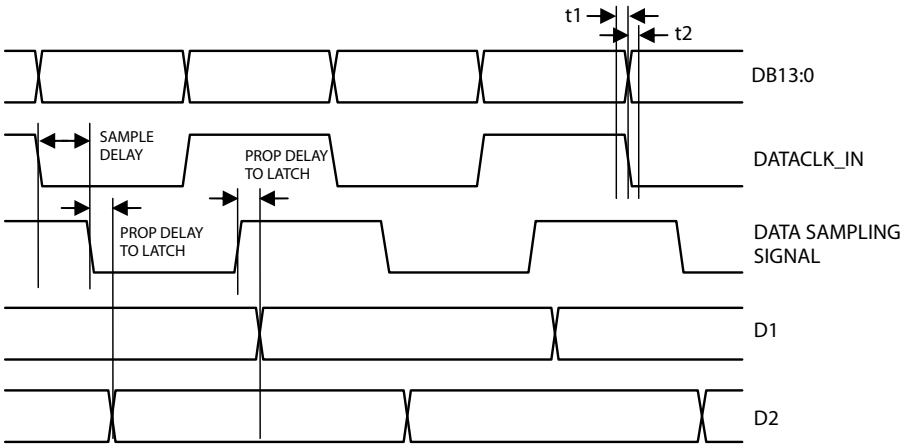


Figure 25. AD9736 Internal LVDS Data Sampling Logic Timing

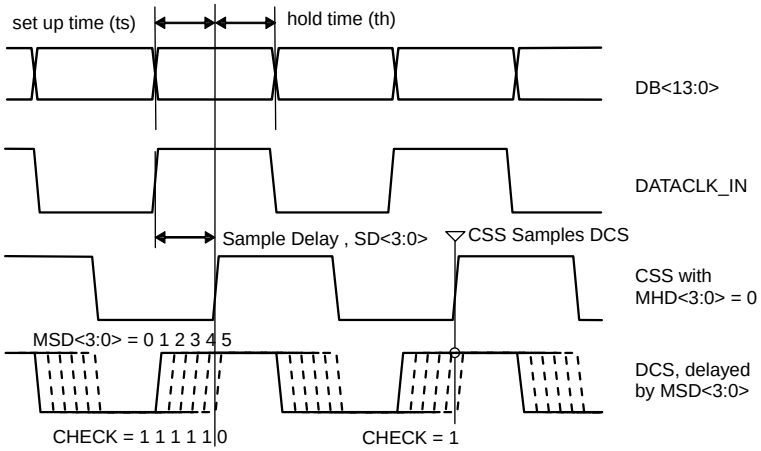


Figure 26. Set-Up Delay Measurement

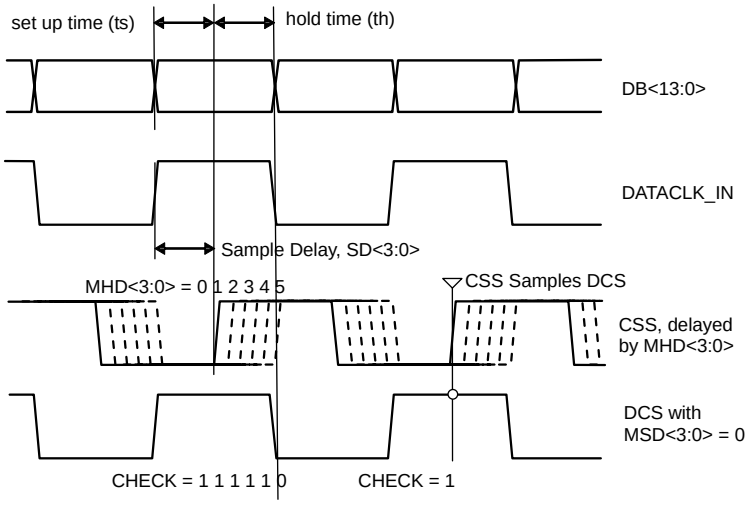


Figure 27. Hold Delay Measurement

OPERATING THE LVDS CONTROLLER IN SURVEILLANCE AND AUTO MODE

In surveillance mode, the controller searches for the edges of the data eye in the same manner as above in the manual mode of operation and triggers an interrupt if the CLOCK SAMPLING SIGNAL (CSS) has moved more than the threshold value set by LTHR<1:0> (REG06, bits 1:0).

There is an internal filter which averages the set-up and hold time measurements to filter out noise and glitches on the clock lines.

Average Value = (MHD – MSD) / 2

New Average = Average Value + (Delta Average / 2 ^ LFLT<3:0>)

If an accumulating error in the Average Value causes it to exceed the Threshold value (LTHR<1:0>) an interrupt will be issued.

The maximum allowable value for LFLT<3:0> is 12.

In surveillance mode, the ideal sampling point should first be found using manual mode and applied to the sample delay registers. The user should then set the threshold and filter values depending on how far the CSS signal is allowed to drift before an interrupt occurs. Then set the surveillance bit high (REG06, bit 7) and monitor the interrupt signal either via the SPI port read back (REG01, bit 3) or the IRQ pin.

In auto mode, the same steps should be taken to set up the sample delay, threshold and filter length. In order to run the controller in auto mode both the LAUTO (REG06, bit 6) and LSURV (REG06, bit 7) bits need to be set to 1. In AUTO mode the LVDS interrupt should be set low (REG01, bit 7) to allow the Sample Delay to be automatically updated if the threshold value is exceeded.

AD9736 SYNC Logic and Controller

A FIFO structure is utilized to synchronize the data transfer between the DACCLK and the DATACLK_IN clock domains. The SYNC Controller writes data from DB<13:0> into an eight word memory based on a cyclic write counter clocked by the CLOCK SAMPLING SIGNAL (CSS) which is a delayed version of DACCLK_IN. The data is read out of the memory based on a second cyclic read counter clocked by DACCLK. The eight word deep FIFO shown in Figure 28 provides sufficient margin to maintain proper timing under most conditions. The SYNC logic is designed to prevent the read and write pointers from crossing. If the timing drifts far enough to require an update of the phase offset (PHOF<1:0>) two samples will be duplicated or dropped. Figure 29 shows the timing diagram for the SYNC logic.

SYNC LOGIC AND CONTROLLER OPERATION

The relationship between the readout pointer and the write pointer will initially be unknown since the startup relationship between DACCLK and DATACLK_IN is unknown. The SYNC logic measures the relative phase between the two counters with the zero detect block and the Flip Flop in Figure 5 above. The relative phase is returned in FIFOSTAT<2:0> (REG07, bits 6:4) and SYNC logic errors are indicated by FIFOSTAT<3> (REG07, bit 7). If FIFOSTAT<2:0> returns a value of zero or seven it signifies that the memory is sampling in a critical state (read and write pointers are close to crossing). If the FIFOSTAT<2:0> returns a value of 3 or 4 it signifies the memory is sampling at the optimal state (read and write pointers are farthest apart). If FIFOSTAT<2:0> returns a critical value the pointer can be adjusted with the phase offset PHOF<1:0> (REG07, bits 1:0). Due to the architecture of the FIFO the phase offset can only adjust the read pointer in steps of two.

OPERATING IN MANUAL MODE

Allow DACCLK and DATACLK_IN to stabilize then enable FIFO mode (REG00, bit 2). Read FIFOSTAT<2:0> (REG07, bits 6:4) to determine if adjustment is needed. For example if FIFOSTAT<2:0> = 6 the timing is not yet critical but it is not optimal. To return to an optimal state (FIFOSTAT<2:0> = 4) the PHOF<1:0> (REG07, bits 1:0) needs to be set to 1. Setting PHOF<1:0> = 1 effectively increments the read pointer by 2. This causes the write pointer value to be captured two clocks later decreasing FIFOSTAT<2:0> from 6 to 4.

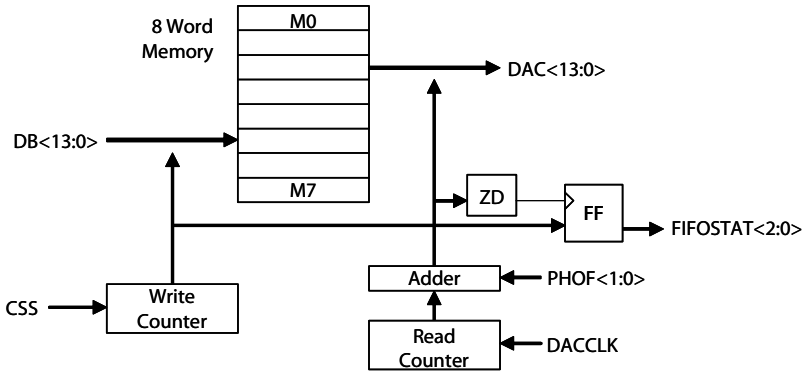


Figure 28. SYNC Logic Block Diagram

OPERATION IN SURVEILLANCE AND AUTO MODES

Once FIFOSTAT<2:0> has been manually placed in an optimal state the AD9736 SYNC logic can be run in Surveillance or Auto mode. To start, turn on Surveillance mode by setting SSURV = 1 (REG08, bit 7) then enable the sync interrupt (REG01, bit 2). If STRH<0> = 0 (REG08, bit 0) an interrupt will occur if FIFOSTAT<2:0> = 0 or 7. If STRH<0> = 1 (REG08, bit 0) an interrupt will occur if FIFOSTAT<2:0> = 0, 1, 6 or 7. The interrupt can be read at REG01, bit 6 at the AD9736 IRQ pin.

To enter Auto mode, complete the preceding steps then set SAUTO = 1 (REG09, bit 6). Next set the SYNC interrupt = 0 (REG01, bit 2), to allow the phase offset (PHOF<1:0>) to be automatically updated if FIFOSTAT<2:0> violates the threshold value.

The FIFOSTAT signal is filtered to improve noise immunity and reduce unnecessary phase offset updates. The filter operates with the following algorithm:

FIFOSTAT = FIFOSTAT + Delta FIFOSTAT / 2 ^ SFLT<3:0>

Where 0 <= SFLT<3:0> <= 12. Values greater than 12 are set to 12.

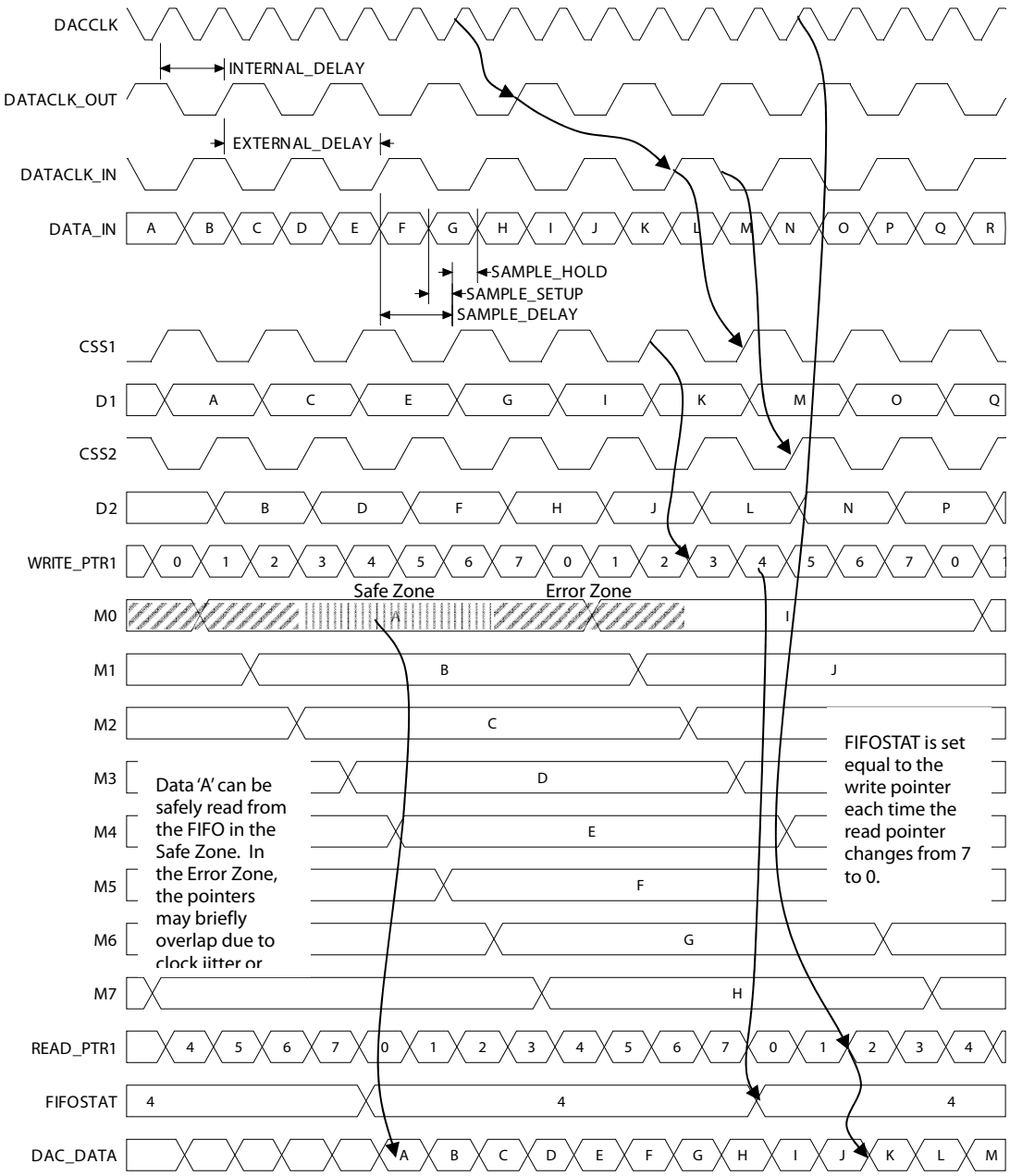


Figure 29. SYNC Logic Timing Diagram

AD9736 DIGITAL BUILT-IN SELF TEST

BIST may be used to validate data transfer to the AD9736 in addition to final ATE device verification. There are 4 BIST signatures that can be read back using Registers 18-21 based on the setting of the BIST selection bits (REG17, bits 7:6) as shown in Table 12.

	SEL<1>	SEL<0>
1 - LVDS Phase 1	0	0
2 - LVDS Phase 2	0	1
3 - SYNC Phase 1	1	0
4 - SYNC Phase 2	1	1

Table 12. BIST Selection Bits

The BIST signature returned from the AD9736 will depend on the input DATA during the test. Since the filters in the DAC have memory, it is important to put the correct idle value on the DATA inputs to flush the memory prior to reading the BIST signature. Placing the idle value on the data inputs also allows the BIST to be setup while the DAC clock is running. The idle value should be all zeroes in unsigned mode (0x0000) and all zeroes except for the MSB in two's complement mode (0x2000).

The BIST consists of two stages; the first stage is after the LVDS receiver and the second stage is after the FIFO stage. The first BIST stage verifies correct sampling of the data from the LVDS bus while the second BIST stage verifies correct synchronization between the DAC_CLK domain and the DATA_CLK domain. The BIST vector is generated using 32 bit LFSR signature logic. Since the internal architecture is a two bus parallel system there are two 32-bit LFSR signature logic blocks on the both the LVDS and SYNC blocks. Figure 30 shows where the LVDS and SYNC phases are located.

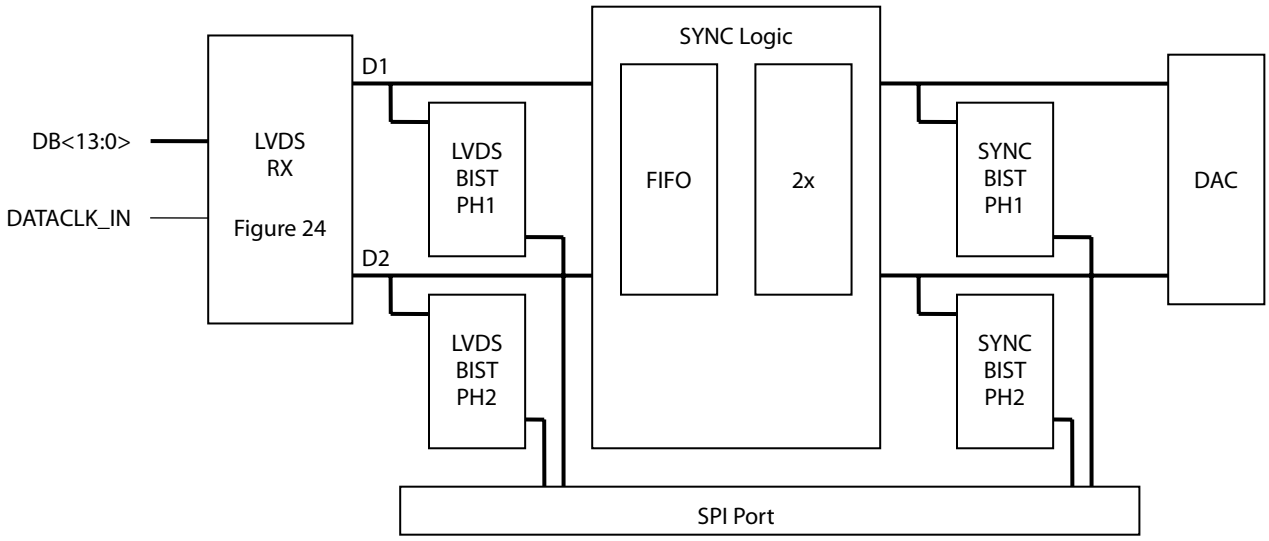


Figure 30. Block Diagram Showing LVDS and SYNC Phase 1 and Phase 2

BIST OPERATION

The internal signature generator processes the input data to create the BIST signatures. An external program which implements the same algorithm may be used to generate the expected signature for comparison. A Matlab routine can be provided upon request to perform this function.

Clock the test vector in as described below and compare the signature register values to the expected value to verify correct operation and input data capture.

With all clocks running:

1. Apply the idle vector to the data inputs (0x0000 if unsigned, 0x2000 if two's complement) for 1024 clocks,
2. Set LVDS_EN (REG17, bit 2) and SYNC_EN (REG17, bit 1) high,
3. Set CLEAR (REG17, bit 0) high,
4. Set CLEAR low to clear the BIST signature register,
5. Clock the BIST vector into the LVDS data inputs,
6. After the BIST vector is complete, return the inputs to the idle vector value,
7. Set LVDS_EN (REG17, bit 2) and SYNC_EN (REG17, bit 1) low,
8. Set the desired SEL<1:0> bits and read back the four BIST signature registers (REG18, 19, 20 and 21).

When the DAC is in 1x mode, the signature at SYNC BIST, Phase 1 should equal the signature at LVDS BIST, Phase 1. The same is true for Phase 2. BIST does not support 2x mode.

AD9736 ANALOG CONTROL REGISTER

The AD9736 includes some registers for optimizing its analog performance. These registers include temperature trim for the bandgap, noise reduction in the output current mirror and output current mirror headroom adjustments.

BANDGAP TEMPERATURE CHARACTERISTIC TRIM BITS

Using TRMBG<2:0> (REG14, bits 2:0) the temperature characteristic of the internal bandgap can be trimmed to minimize the drift over temperature as shown in Figure 31.

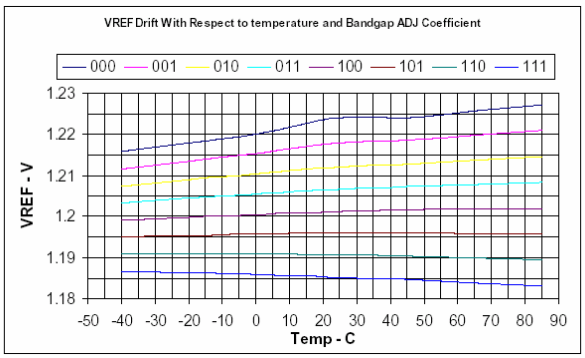


Figure 31. BANDGAP Temperature Characteristic for Various TRMBG Values

It is important to note that the temperature changes are sensitive to process variations and the above plot may not be representative of all fabrication lots. Optimum adjustment requires measurement of the device operation at two temperatures and development of a trim algorithm to program the correct TRMBG<2:0> values in external non-volatile memory.

MIRROR ROLL OFF FREQUENCY CONTROL

With MSEL<1:0> (REG14, bits 7:6) the user can adjust the noise contribution of the internal current mirror to optimize the 1/F noise. Figure 32 shows MSEL vs. the 1/F noise with 20mA Full-Scale current into a 50ohm resistor.

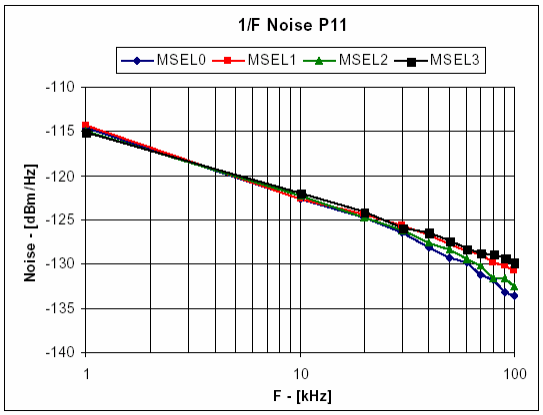


Figure 32. 1/F Noise With Respect to MSEL Bits

HEADROOM BITS

HDRM<7:0> (REG15, bits 7:0) is for internal evaluation and it is not recommended to change them from their default reset values.

VOLTAGE REFERENCE

The AD9736 output current is set by a combination of digital control bits and the I120 reference current as shown in Figure 33.

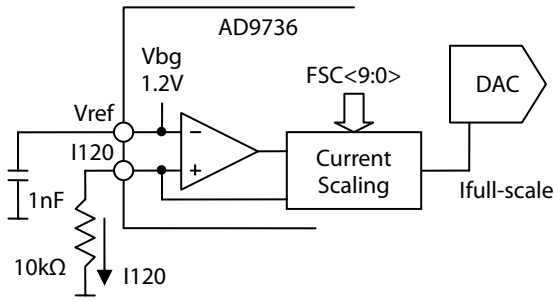


Figure 33. Voltage Reference Circuit

The reference current is obtained by forcing the bandgap voltage across an external 10kohm resistor from I120 (pin B14) to ground. The 1.2V nominal bandgap voltage (Vref) will generate a 120uA reference current in the 10k resistor. This current is adjusted digitally by FSC<9:0> (REG02, REG03) to set the output full scale current I_{FS}:

$$I_{FS} = \frac{\text{Vref}}{\text{R}} \times \left(72 + \left(\frac{192}{1024} \times FSC < 9:0 > \right) \right)$$

The full scale output current range is 10mA to 30mA for register values from 0x000 to 0x3FF. The default value of 0x200 generates 20mA full scale. The typical range is shown in *Figure 34*.

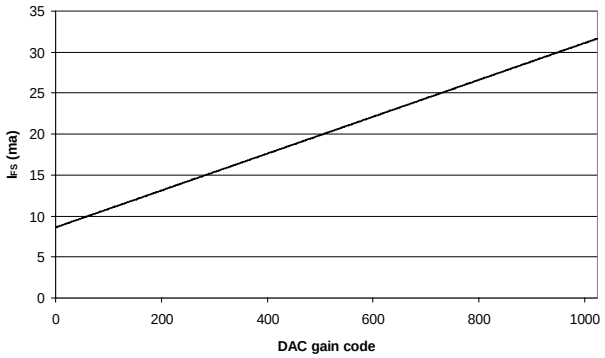


Figure 34. I_{FS} vs. DAC Gain Code

VREF (pin C14) must be bypassed to ground with a 1nF capacitor. The bandgap voltage is present on this pin and may be buffered for use in external circuitry. The typical output impedance is near 5kohms. If desired, an external reference may be used to overdrive the internal reference by connecting it to the VREF pin.

IPTAT (pin D14) is used for factory testing. It may be left floating (preferred) or tied to analog ground. It will output a current which is proportional to absolute temperature. The nominal output is approximately 10uA at 25C. The slope is approximately 20nA per degree C.

APPLICATIONS INFORMATION

FPGA/ASIC DAC DRIVER REQUIREMENTS

To achieve data synchronization using the high speed capability of the AD9736, ADI recommends the configuration in Figure 35 for the FPGA/ASIC driving the digital inputs. Using the Double Data Rate DATACLK_OUT, this configuration will generate the LVDS DATACLK_IN to drive the AD9736 at the DDR rate. The circuit also synchronizes the DATACLK_IN and the digital input data (DB<13:0>) as required by the AD9736. The synchronization engine in the AD9736 then uses DATACLK_IN to generate the internal CLOCK SAMPLING SIGNAL to capture the incoming data via the Manual, Surveillance or Auto mode.

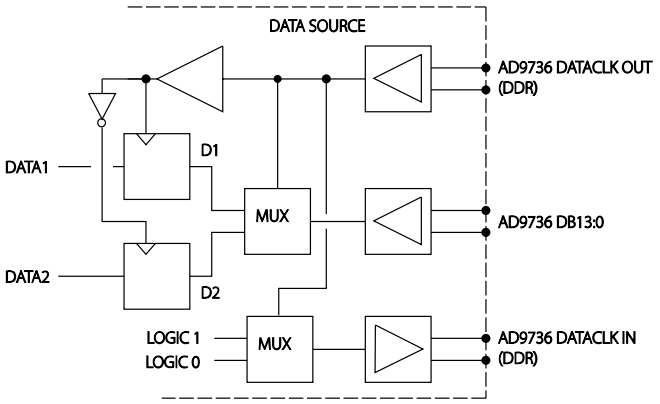


Figure 35. Recommended FPGA/ASIC Configuration for Driving AD9736 Digital Inputs, 1x Mode

To operate in 2x mode, the circuit in Figure 35 must be modified to include a divide-by-two block in the DATACLK_OUT path. Without this additional divider the DATA and DATACLK_IN will be running 2x too fast. DATACLK_OUT is always DACCLK/2.

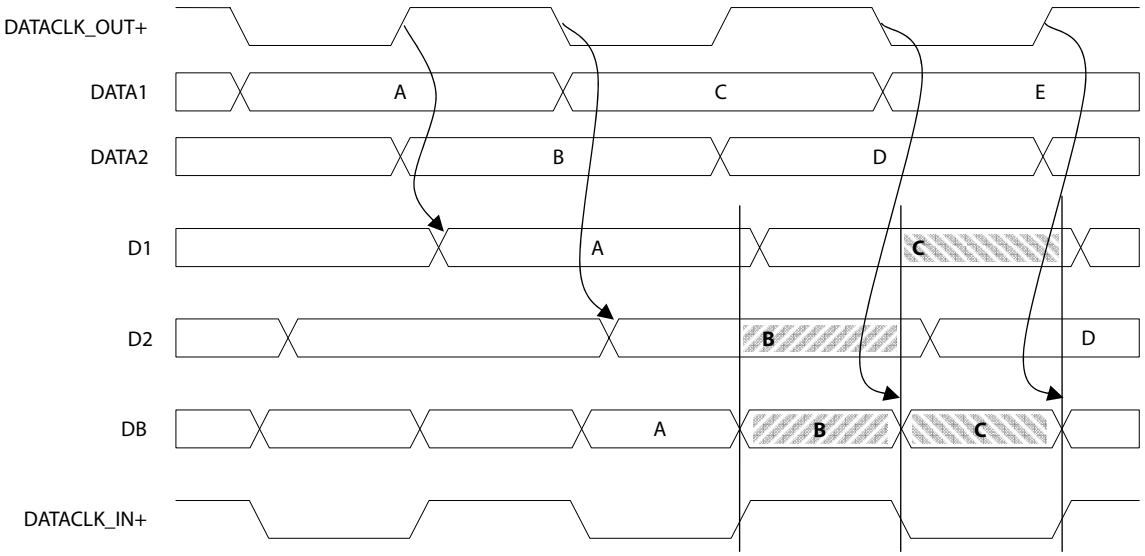


Figure 36. FPGA/ASIC Timing for Driving AD9736 Digital Inputs, 1x Mode

TIMING ERROR BUDGET

The following components make up the timing error budget for the AD9736:

1. AD9736 DATACLK_OUT jitter
2. AD9736 DATACLK_IN jitter
3. DB13:0 jitter
4. DB13:0 skew from data source
5. DB13:0 receiver skew margin (board + AD9736 internal delays)
6. DB13:0 to DATACLK_IN skew from data source

AD9736 EVALUATION BOARD SCHEMATICS

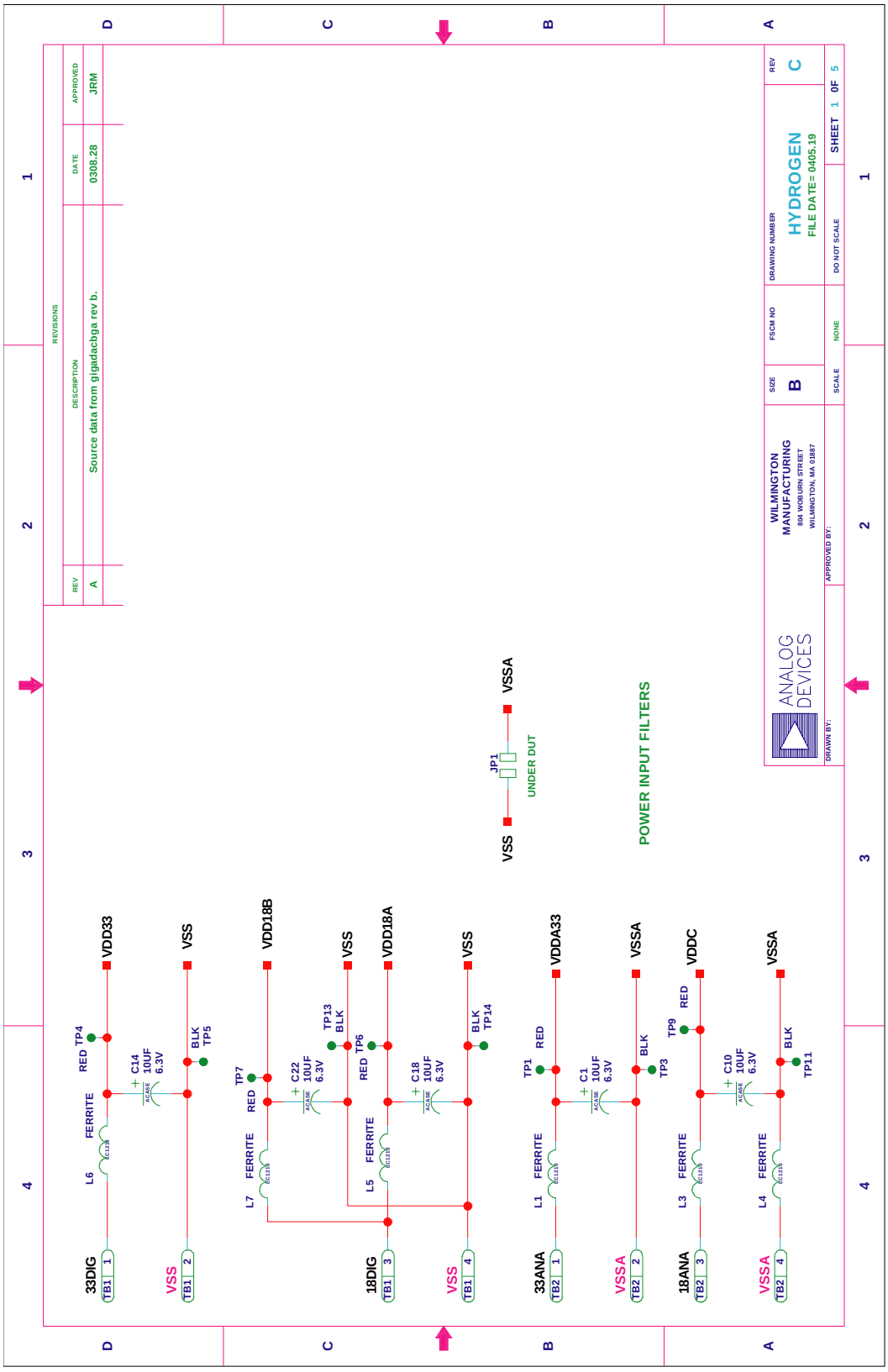


Figure 37. Power Supply Inputs for AD9736 Evaluation Board, Rev C

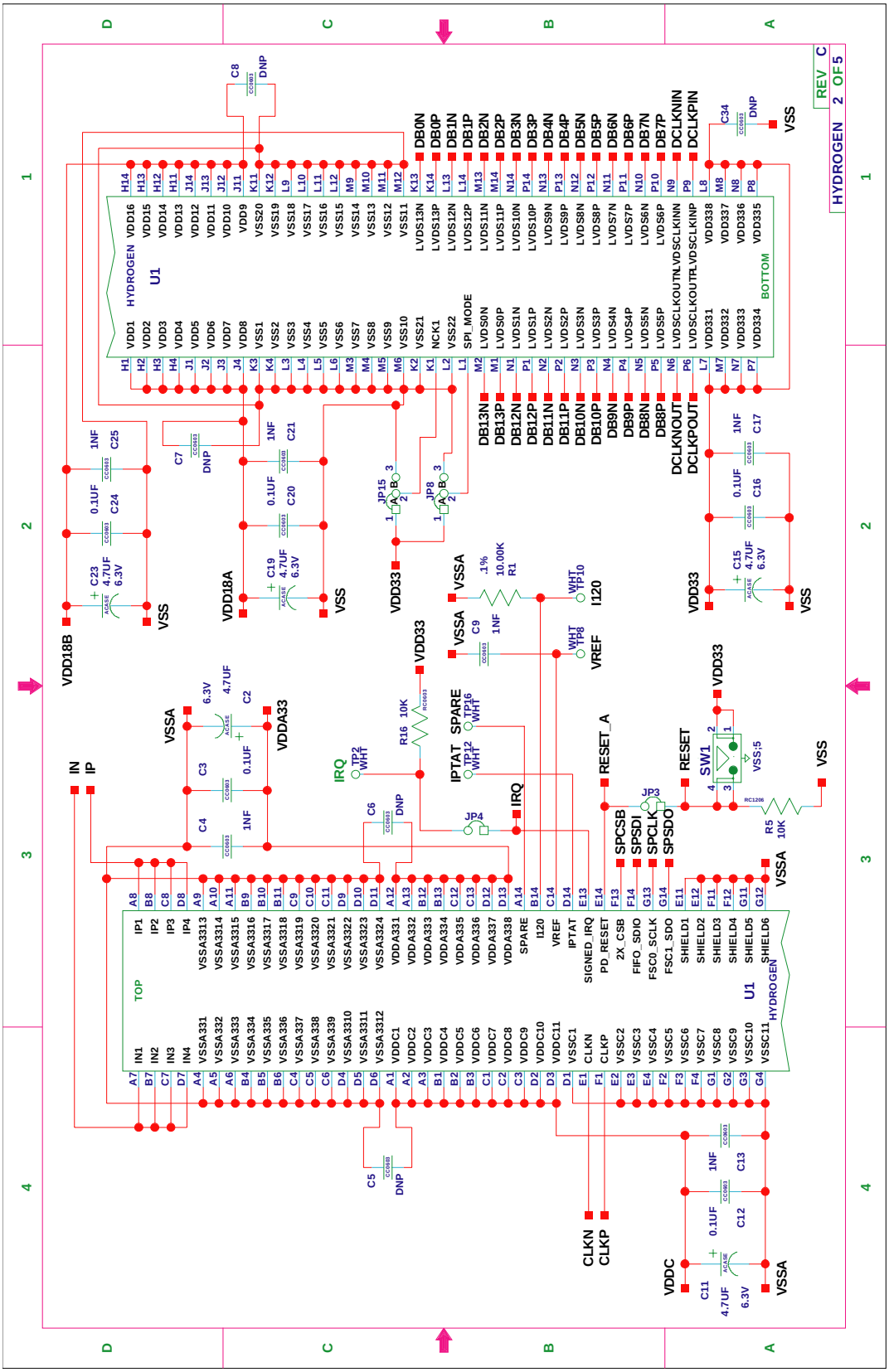


Figure 38. Circuitry Local to AD9736, Evaluation Board, Rev C

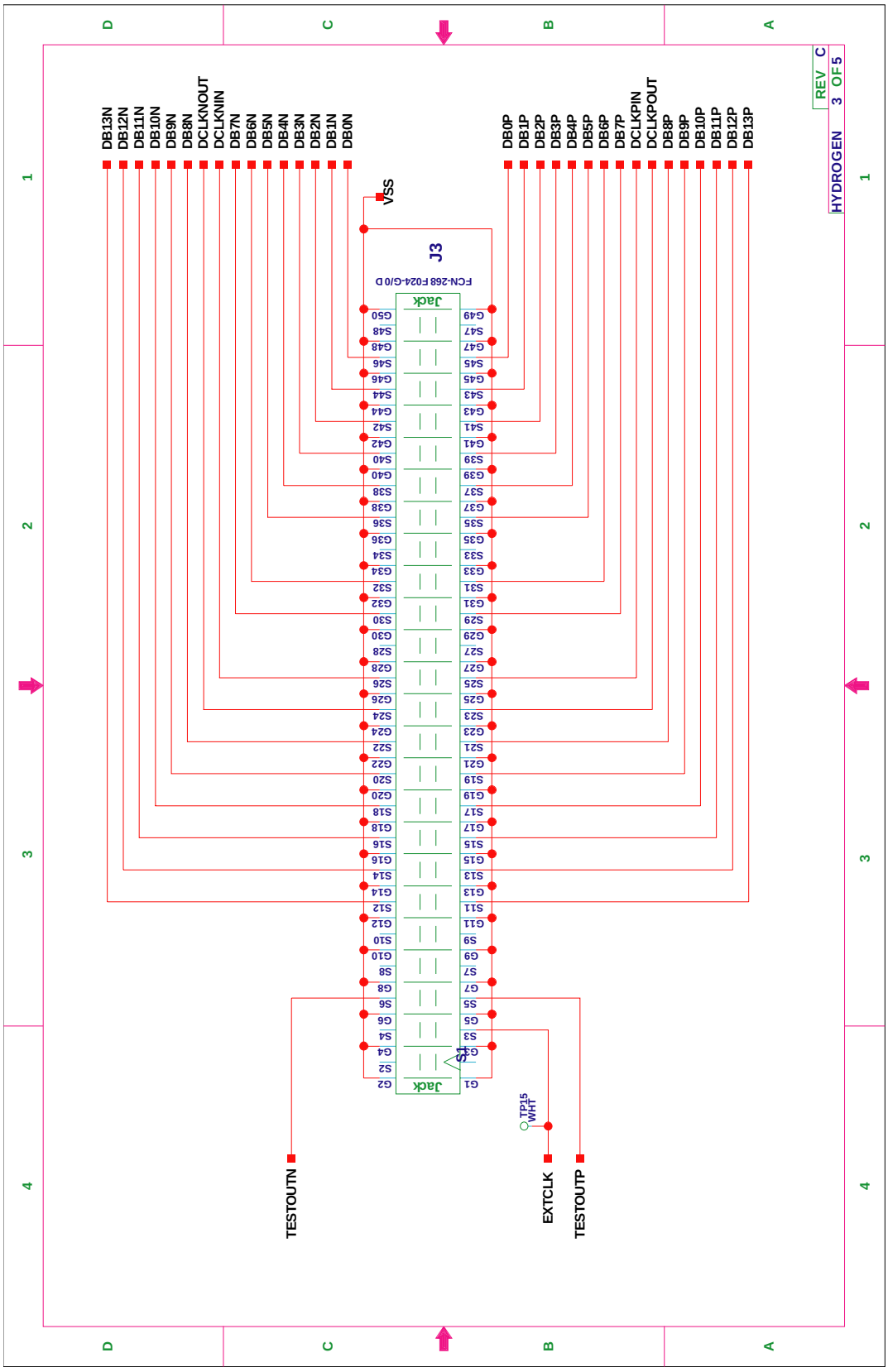


Figure 39. High Speed Digital I/O Connector, AD9736 Evaluation Board, Rev C

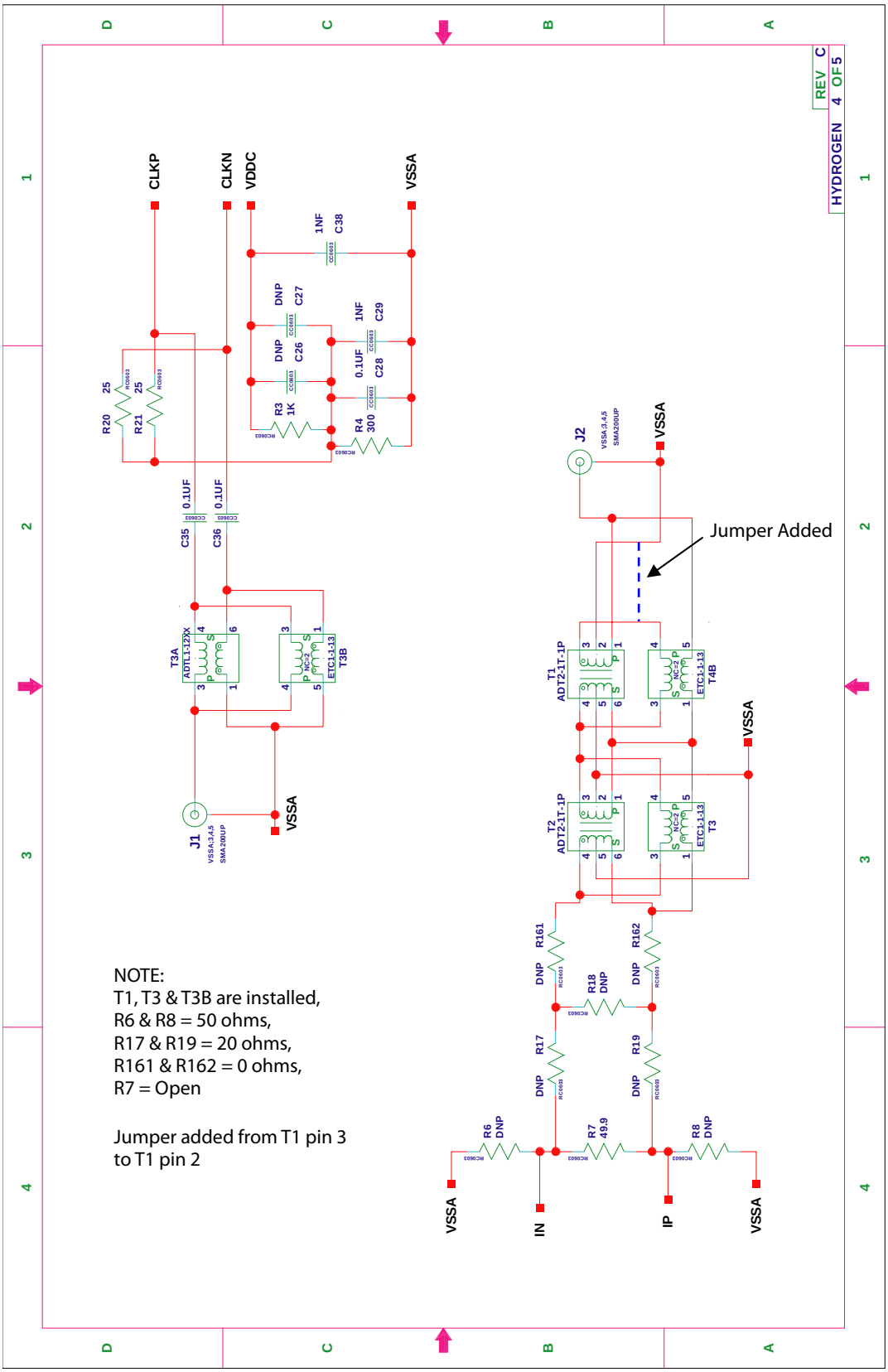


Figure 40. Clock Input and Analog Output, AD9736 Evaluation Board, Rev C

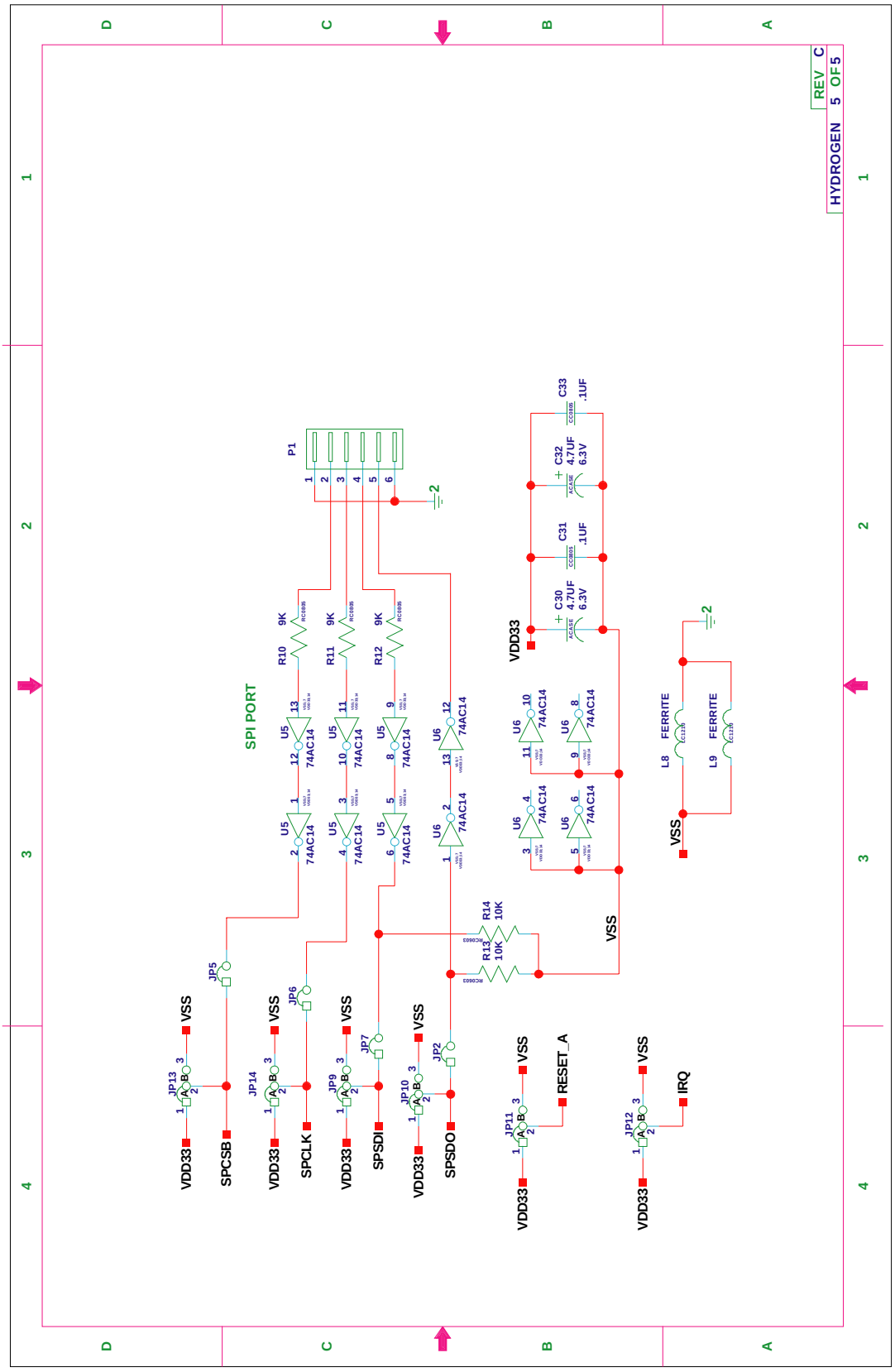


Figure 41. SPI Port Interface, AD9736 Evaluation Board, Rev C

AD9736 EVALUATION BOARD PCB LAYOUT

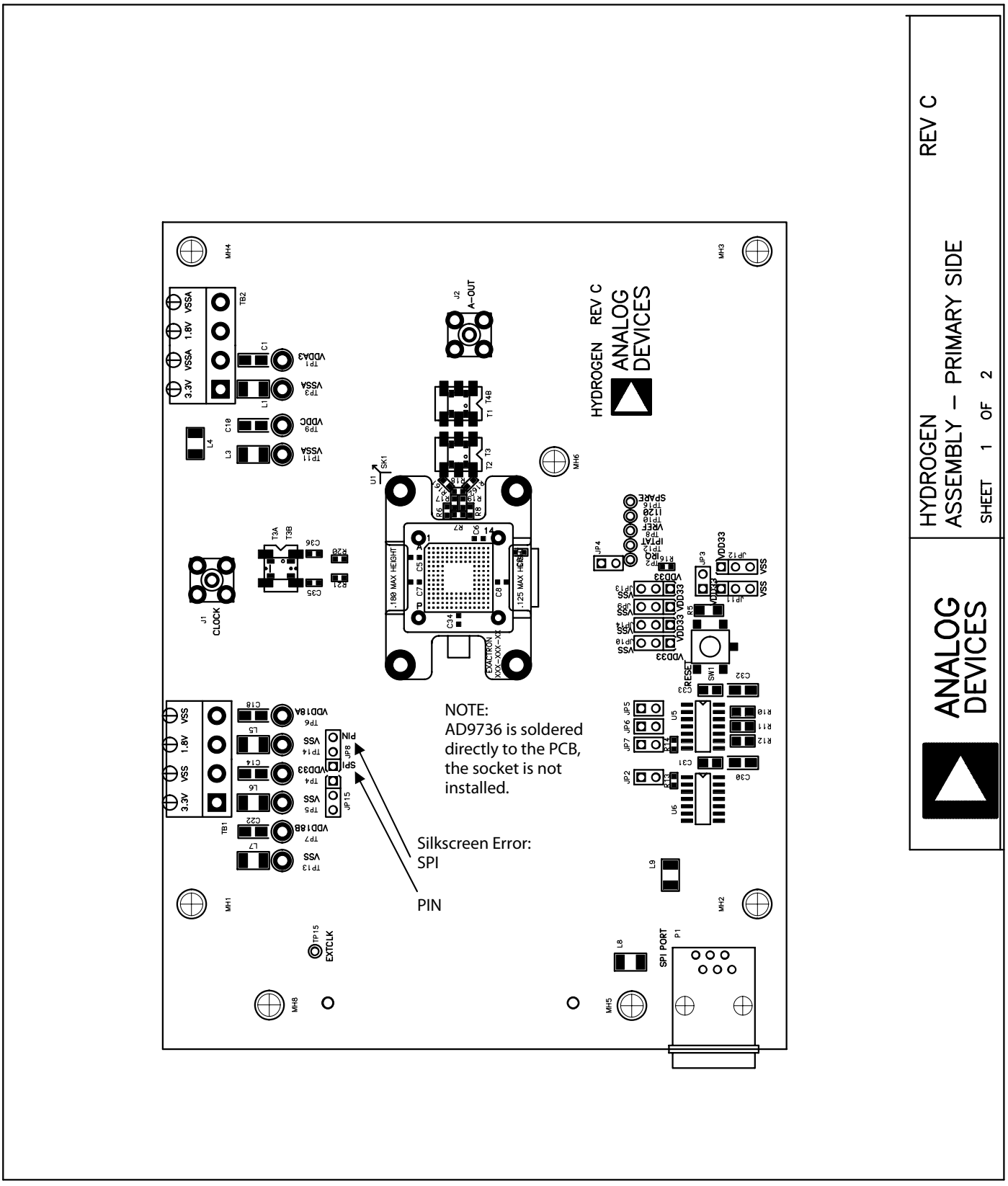


Figure 42. PCB Layout Top Placement, AD9736 Evaluation Board, Rev C

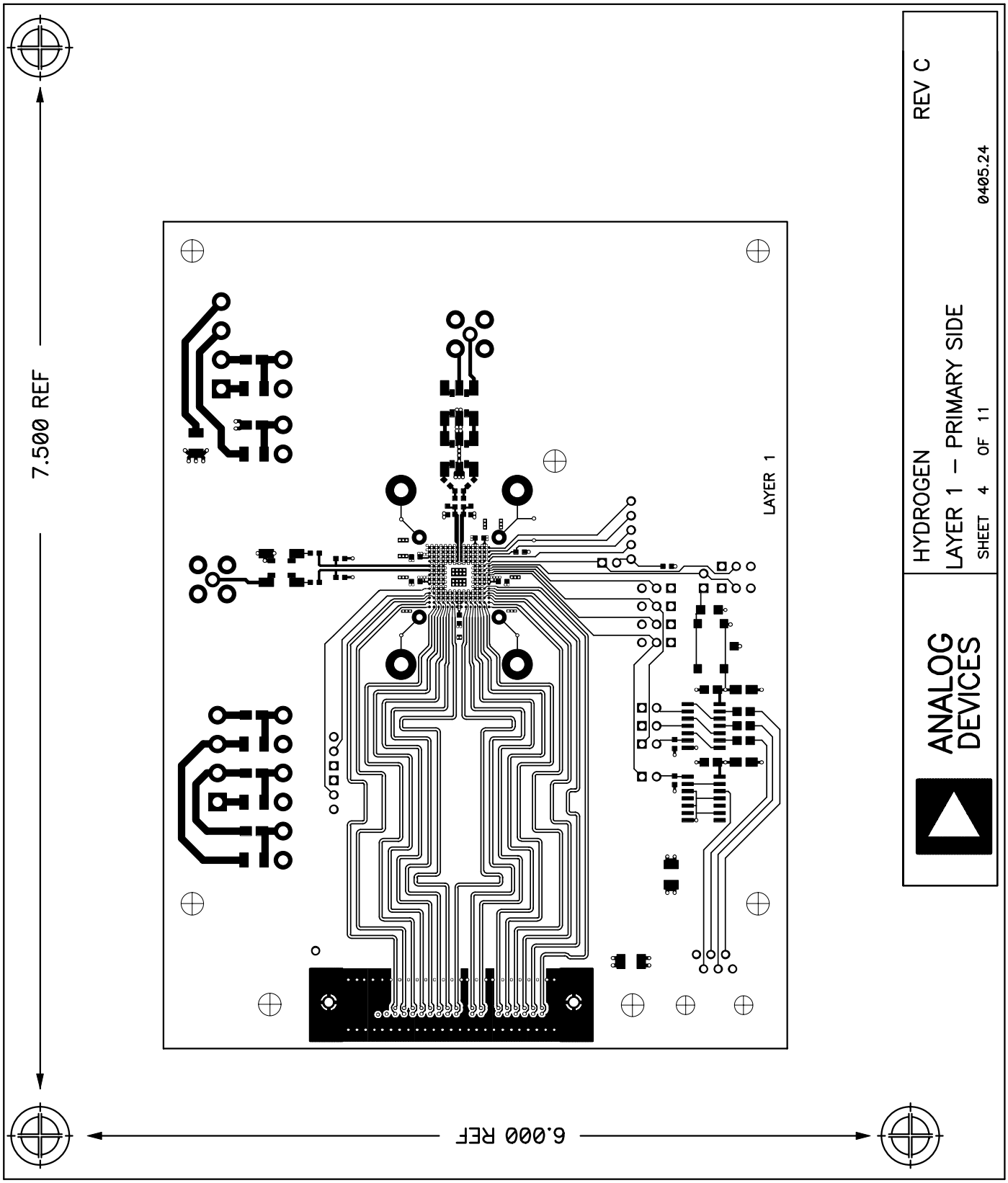


Figure 43. PCB Layout Layer 1, AD9736 Evaluation Board, Rev C

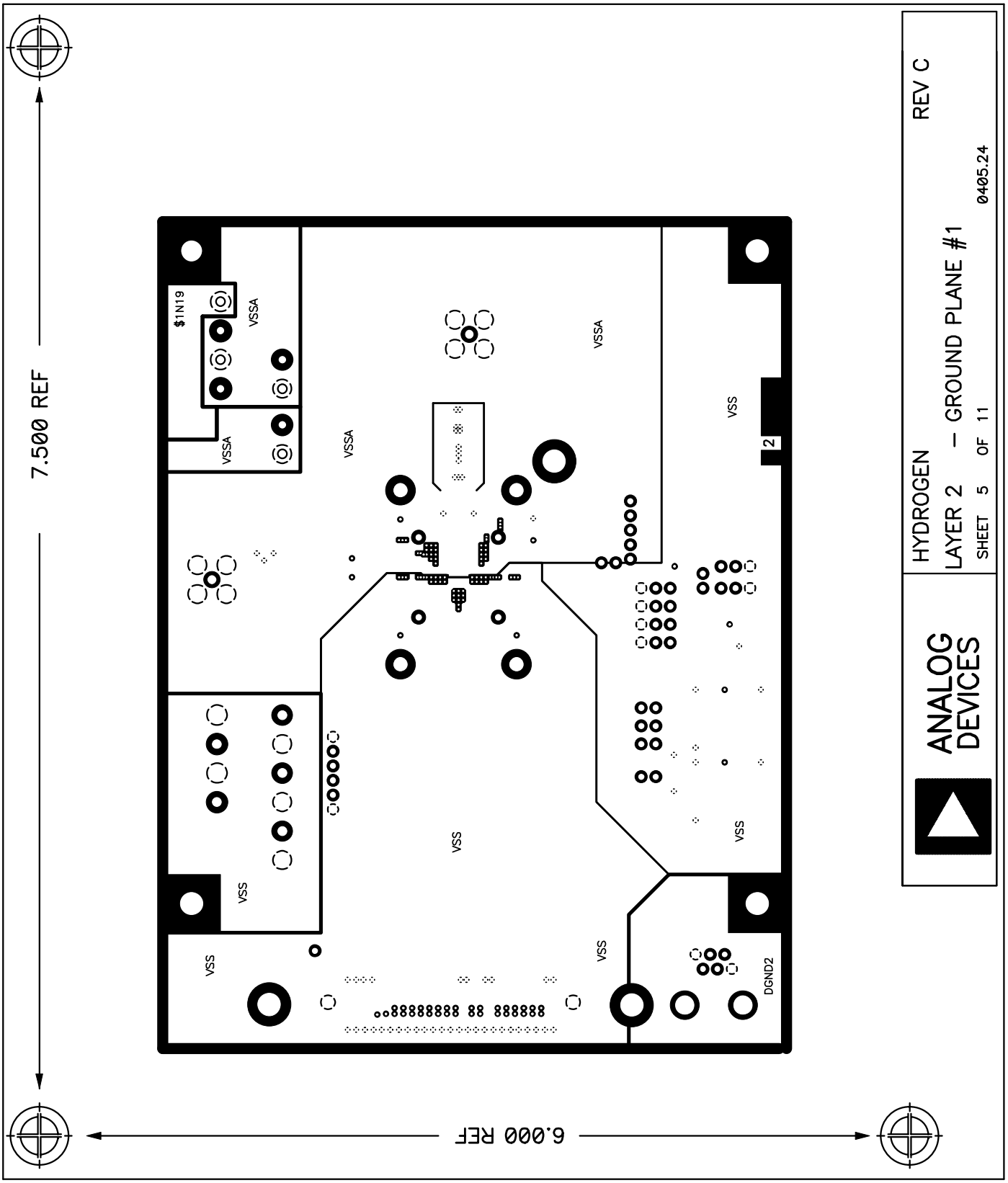


Figure 44. PCB Layout Layer 2, AD9736 Evaluation Board, Rev C

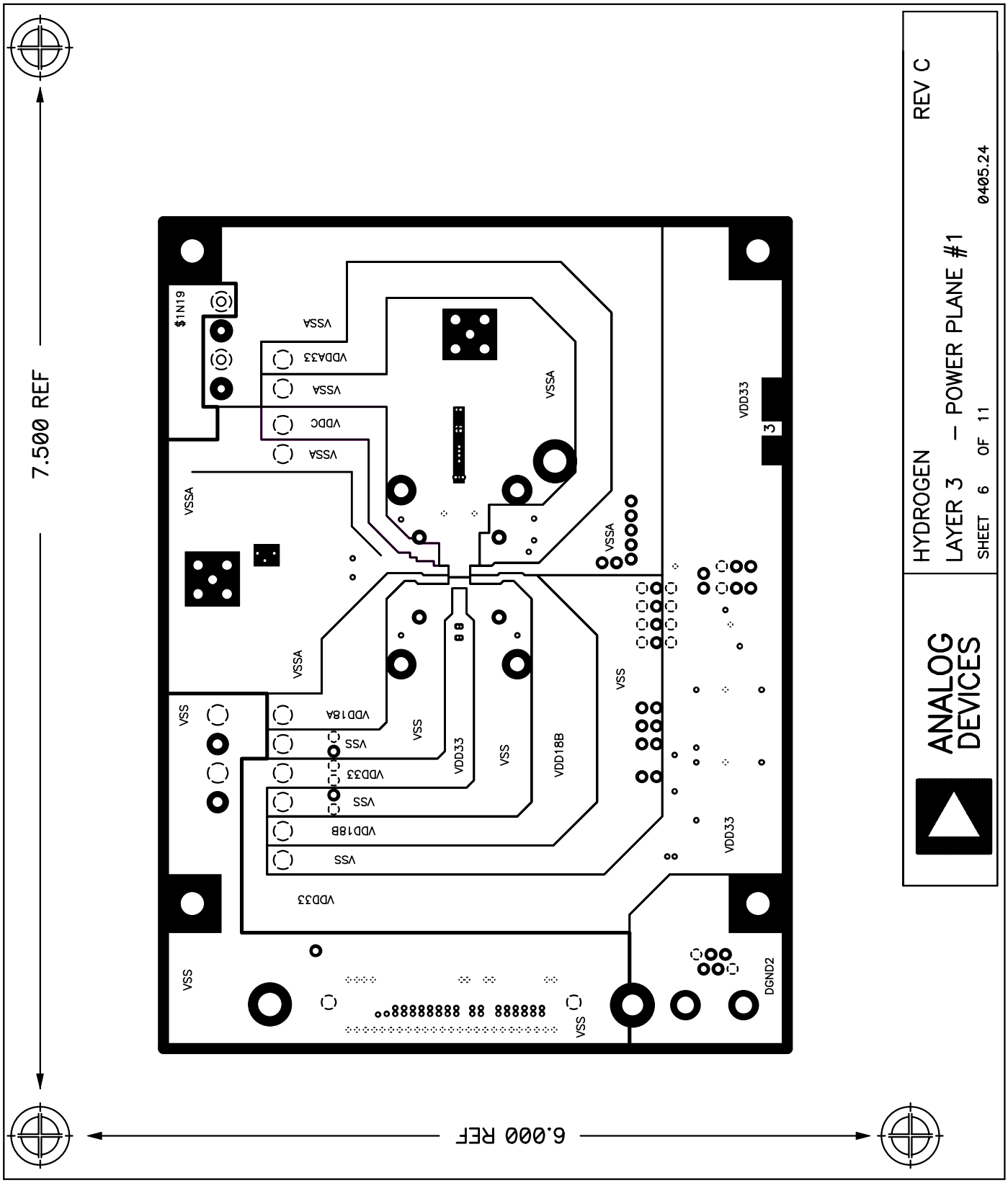


Figure 45. PCB Layout Layer 3, AD9736 Evaluation Board, Rev C

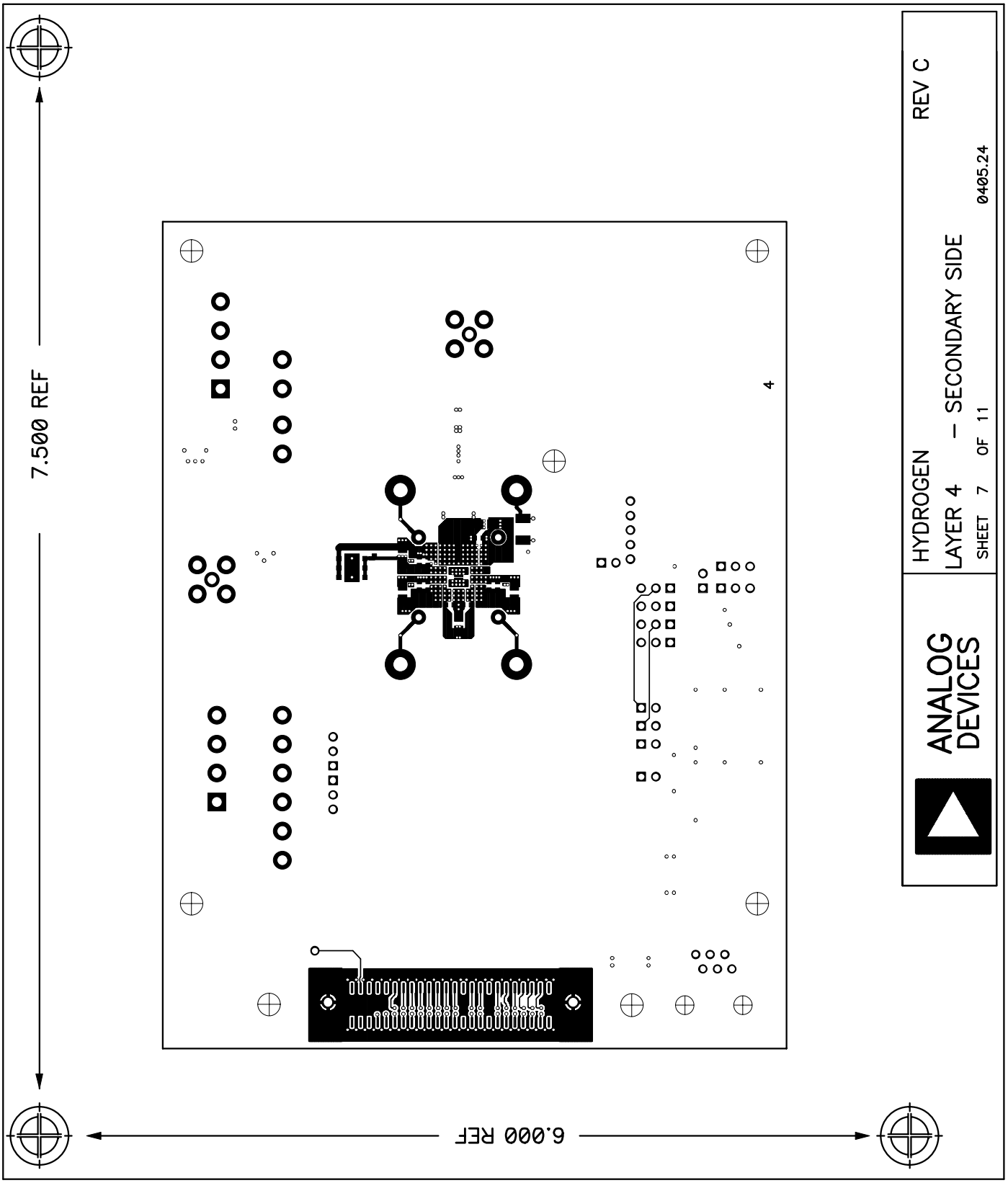


Figure 46. PCB Layout Layer 4, AD9736 Evaluation Board, Rev C

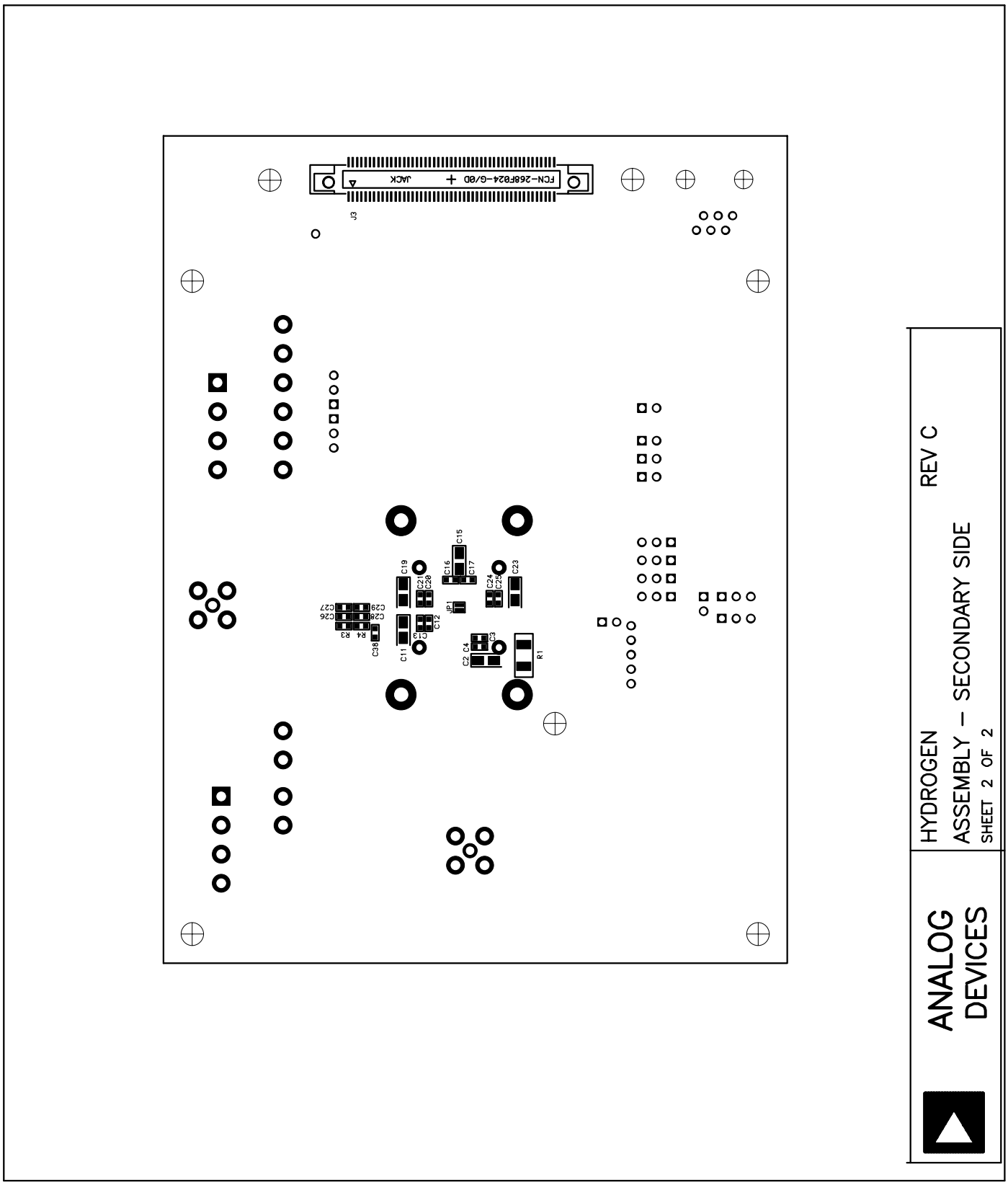


Figure 47. PCB Layout Bottom Placement, AD9736 Evaluation Board, Rev C

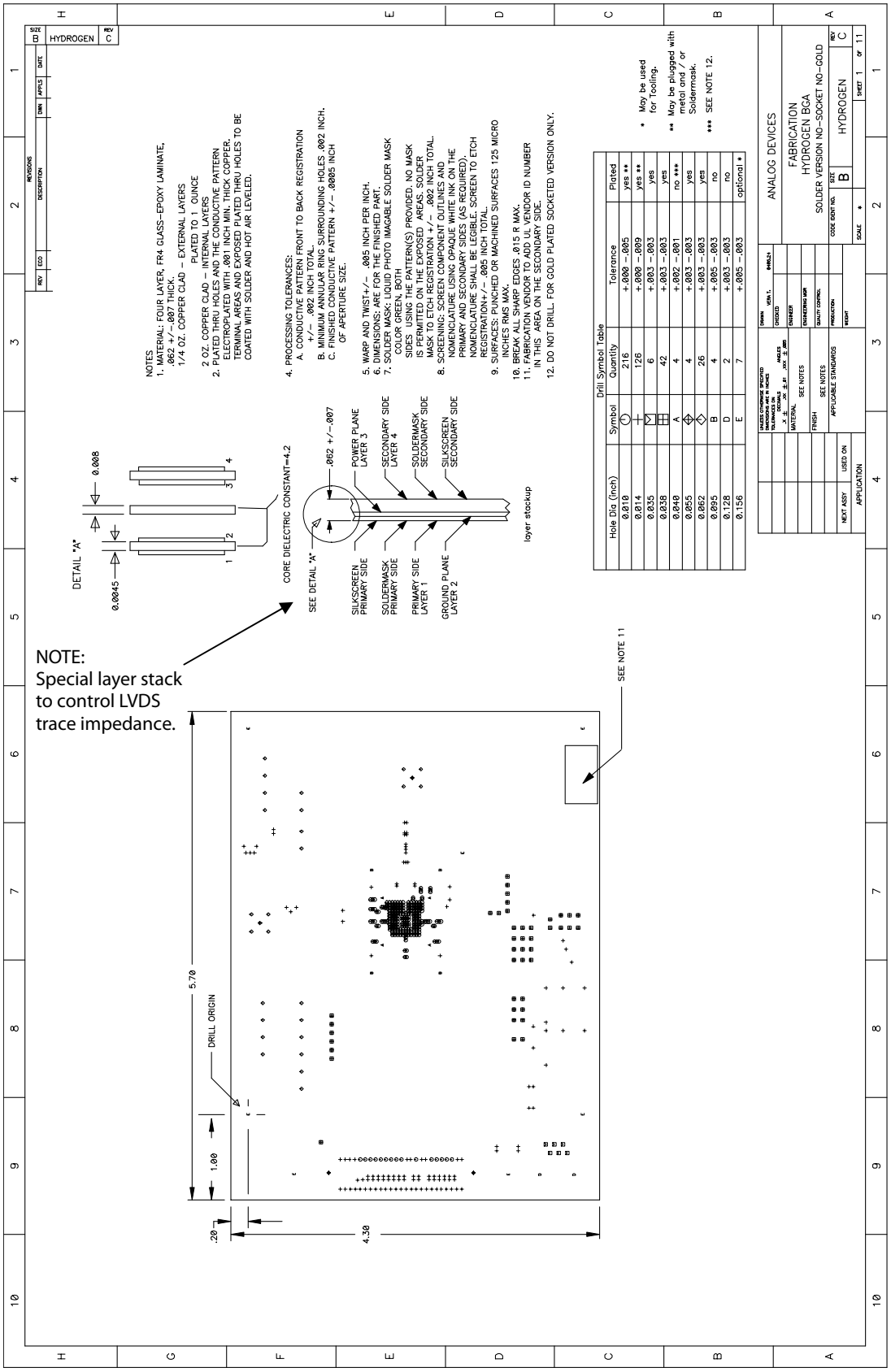


Figure 48. PCB Fabrication Detail, AD9736 Evaluation Board, Rev C

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