

# High Speed, Fast Settling IC Op Amp AD509

PIN CONFIGURATION TO-99



PRODUCT DESCRIPTION

ers

**FEATURES** 

Drives 500pF Low Price

Videband A

Pulse Amplif

Multiplex

APPEICATIONS D/A and AXD Conversion

**Fast Settling Time** 

~0.1% in 500ns max 0.01% in 2.5μs max

Low Ios: 25nA max

High CMRR: 80dB min

mplif

High Slew Rate: 100V/µs min .

Guaranteed Vos Drift: 30µV/°C max

iars.

The AD509J, AD509K and AU509S are monolithic operational amplifiers specifically designed for applications requiring fast settling times to high accuracy other comparable dynamic parameters include a small signal banowidth of 20MHz, slew rate of 100V/µs min and a full power response of 150kHz min. The devices are internally compensated for all closed loop gains greater than 3, and are compensated with a single capacitor for lower gains.

The input characteristics of the AD509 are consistent with 0.01% accuracy over limited temperature ranges; offset current is 25nA max, offset voltage is 8mV max, nullable to zero, and offset voltage drift is limited to  $30\mu V/^{\circ}C$  max. PSRR and CMRR are typically 90dB.

The AD509 is designed for use with high speed D/A or A/D converters where the minimum conversion time is limited by the amplifier settling time. If 0.01% accuracy of conversion is required, a conversion cannot be made in a shorter period than the time required for the amplifier to settle to within 0.01% of its final value.

All devices are supplied in the TO-99 package. The AD509J and AD509K are specified for 0 to  $+70^{\circ}$ C temperature range; the AD509S for operation from  $-55^{\circ}$ C to  $+125^{\circ}$ C. 1. The AD509 is internally compensated for all closed loop gains above 3, and compensated with a single capacitor for lower gains thus eliminating the claborate stabilizing techniques required by other high speed 1C op amps

PRODUCT HIGHLIGHTS

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- The AD509 will drive capacitive loads of 500pF without deterioration in settling time. Larger capacitive loads can be driven by tailoring the compensation to minimize settling time.
- 3. Common Mode Rejection, Gain and Noise are compatible with a 0.01% accuracy device.
- 4. The AD509K and AD509S are 100% tested for minimum slew rate and guaranteed to settle to 0.01% of its final value in less than  $2.5\mu$ s.

## AD509 — SPECIFICATIONS (@ $\pm 25^{\circ}$ C and V<sub>s</sub> = $\pm 15V$ dc unless otherwise specified)

Mode)	Min	AD509J	Max	Min	AD509K Typ	Mex	Min	AD509S Typ	Max	Units
OPEN LOOPGAIN		- 11			-77		-			
$V_{\Omega} = \pm 10V, R_{T} \ge 2k\Omega$	7.500	15.000		10,000	15,000		10,000	15,000		V/V
$T_{min}$ to $T_{max}$ , $R_L = 2k\Omega$	5,000	,		7,500			7,500			V/V
OUTPUT CHARACTERISTICS										
Voltage (a) $R_L = 2k\Omega$ , $T_{min}$ to $T_{max}$	±10	± 12		±10	± 12		± 10	±12		v
FREQUENCY RESPONSE										
Unity Gain Small Signal		20			20			20		MHz
Full Power Response	1.2	1.6		1.5	2.0		1.5	2.0		MHz
Slew Rate, Unity Gain	80 .	120		80	120		100	120		V/µs
Settling Time										
10 0.1%		200			200			200	500	m5
to 0.01%		1.0			1.0			1.0	2.5	μs
INPUT OFFSET VOL TAGE										
Initial Officet		5	10		4	8		4	8	mV
Input Offset Voltage T to T		-	14			11			11	mV
Input Offset Voltage vs. Supply,										
T <sub>max</sub> to T <sub>max</sub>			200			100			100	μV/V
DEPUT BIASCURRENT										
Initial		125	250		100	200		100	200	nA
	$\mathcal{V}$	$\bigcirc$	500			400			400	nA
DIRIT OFFICE OUR PANT	$ \leftarrow \  \  $	< 1	$ \bot  $							
INPUT OFFSET CORRENT		20	50	$ \wedge $	10	25		10	25	nA
		40	100	$  \rangle \rangle$	10	50		10	50	nA
$I_A = \min to \max$	1	$ \rightarrow $							,0	101
INPUT IMPEDANCE		$\smile$	/ ( (				1	7.5		
Differential	40	100	$ \land \land \land$	29/	100		20	Trob		MII
INPUT VOLTAGE RANGE						/		1	$\sim$	
Differential		±15		<b>—</b>	± 15	_ / /	$\square$	±15	1	
Common Mode	1	±10			±10	$\neg I L$		±10	1	
Common Mode Rejection	74	90		80	90		80	90		dB
INPUT NOISE VOLTAGE	Ι						$\sim$			
f = 10Hz		100			100			100		aV/√Hz
f = 100Hz		30			30			30	L	nV/VHz
f = 100kHz	1	19			19			19		nV/VHz
POWER SUPPLY	1									
Rated Performance		±15			±15			±15		v
Operating	±5		± 20	±5		± 20	±5		±20	v
Quiescent Current		4	6		4	6		4	6	mA
TEMPERATURERANGE	1			1			1			
Operating, Rated Performance	0		+ 70	0		+ 70	- 55		+ 125	°C
Storage	-65		+ 150	-65		+ 150	- 65		+ 150	°C
	1									

NOTES

Specifications subject to change without notice.

All min and max specifications are guaranteed.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

#### **ORDERING GUIDE**

Model	Temperature Range	Package Option*			
AD509JH	0°C to +70°C	H-08A			
AD509KH	0°C to +70°C	H-08A			
AD509SH	-55°C to +125°C	H-08A			

\*H-08A = TO-99 Style Metal Can. For outline information see Package Information section.

## Applying the AD509

### **APPLYING THE AD509**

MEASURING SETTLING TIME. Settling time is defined as that period required for an amplifier output to swing from 0 volts to full scale, usually 10 volts, and to settle to within a specified percentage of the final output voltage. For high accuracy systems, the accuracy requirement is normally specified as either 0.1% (10-bit accuracy) or 0.01% (12-bit accuracy) of the 10 volt output level. The settling time period is comprised of an initial propagation delay, an additional time for the amplifier to slew to the vicinity of 10 volts, and a final time period to recover from internal saturation and other effects, and settle within the specified error band. Because settling time depends on both linear and nonlinear factors, there is no simple approach to predicting its final value to different levels of accuracy. In particular, extremely high slew rates do not assure a rapid settling time, since this is only one of many factors affecting In most high speed amplifiers, after the ettling time. amplifier has slewed to the visinity of the final output oltage, it must recover from internal saturation and then low any overshoot and ringing to damp out. These definitions are illustrated in Figure



Figure 1. Settling Time

The AD509K and AD509S are guaranteed to settle to 0.1% in 500ns and 0.01% in 2.5 $\mu$ s when tested as shown in Figure 2. There is no appreciable degradation in settling time when the capacitive load is increased to 500pF, as discussed below. The settling time is computed by summing the output and the input into a differential amplifier, which then drives a scope





display. The resultant waveform of  $(E_O - E_{IN})$  of a typical AD509 is shown in Figure 3. Note that the waveform crosses the 1mV point representing 0.01% accuracy in approximately 1.5 $\mu$ s. The top trace represents the output signal; the bottom trace represents the error signal.



Figure 3. Settling Time of AD509

SETTLING TIME VS.  $R_f$  AND  $R_i$ . Settling time of an amplifier is a function of the feedback and input resistors, since they interact with the input capacitance of the amplifier. When operating in the non-inverting mode, the source impedance should be kept relatively low; e.g.,  $5k\Omega$ ; in order to infure optimum performance. The small feedback capacitor (5pF) is used in the settling time test circuit in parallel with the feedback resistor to reduce ringing. This capacitor partially cancels the pole formed in the loop gain response as a result of the feedback and input resistors, and the input capacitance

SETTLING TIME VS. CAPACITIVE LOAD. The AD509 will drive capacitive loads of 500pF without appreciable deterioration in settling time. Larger capacitive loads can be driven by tailoring the compensation to minimize settling time. Figure 4 shows the settling time of a typical AD509 compensated for unity gain with a 15pF capacitor, with a 500pF capacitive load on the output. Note that settling time to 0.01% is still under  $2.0\mu s$ .



Figure 4. AD509 with 500pF Capacitive Load

SUGGESTIONS FOR MINIMIZING SETTLING TIME. The AD509 has been designed to settle to 0.01% accuracy in 1 to 2.5 $\mu$ s. However, this amplifier is only a building block in a circuit that also has a feedback network, input and output connections, power supply connections, and a number of external components. What has been painstakingly gained in amplifier design can be lost without careful circuit design. Some of the elements of a good high speed design are......

CONNECTIONS. It is essential that care be taken in the signal and power ground circuits to avoid inducing or generating extraneous voltages in the ground signal paths.

### AD509

The 0.1µF ceramic power supply bypass capacitors are considerably more important for the AD509 than for low frequency general purpose amplifiers. Their main purpose is to convert the distributed high frequency ground to a lumped single point (the V+ point). The V+ to V-  $0.1\mu$ F capacitor equalizes the supply grounds while the  $0.1 \mu F$ capacitor from V+ to signal ground should be returned to signal common. The signal common, which is bypassed to pin 7, is defined as that point at which the input signal source, the feedback network, and the return side of the load are joined to the power common.

Note that the diagram shows each individual capacitor directly connected to the appropriate terminal (pin 7 [V+]).



Figure 6. Open Loop Frequency and Phase Response

THE AD509 AS AN OUTPUT AMPLIFIER FOR FAST **CURRENT-OUTPUT D-TO-A CONVERTERS** 

Most fast integrated circuit digital to analog converters have current outputs. That is, the digital input code is translated to an output current proportional to the digital code. In many applications, that output current is converted to a voltage by connecting an operational amplifier in the current-tovoltage conversion mode.

The settling time of the combination depends on the settling time of the DAC and the output amplifier. A good approximation is:

$$t_s TOTAL = \sqrt{(t_s DAC)^2 + (t_s AMP)^2}$$

Some IC DACs settle to final output value in 100-500 nanoseconds. Since most IC op amps require a longer time to settle to  $\pm 0.1\%$  or  $\pm 0.01\%$  of final value, amplifier settling time can dominate total settling time. And for a 12-bit DAC, one least significant bit is only 0.024% of full-scale, so low drift and high linearity and precision are also required of the output amplifier.

In addition, it is suggested that all connections be short and direct, and as physically close to the case as possible, so that the length of any conducting path shared by external components will be minimized.

COMPONENTS. Resistors are preferably metal film types, because they have less capacitance and stray inductance than wirewound types, and are available with excellent accuracies and temperature coefficients.

Diodes are hot carrier types for the very fastest-settling applications, but 1N914 types are suitable for more routine uses.

Capacitors in critical locations are polystyrene, teflon, or polycarbonate to minimize dielectric absorption.



verter. The 10 picofarad capacitor, C1, compensates for the 25pF AD565 output capacitance. The voltage output of the AD565K/AD509K combination settles to ±0.01% in one microsecond. The low input voltage drift and high open loop gain of the AD509K assures 12-bit accuracy over the operating temperature range.





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