

FEATURES

AD7788: 16-bit resolution

AD7789: 24-bit resolution

Power

Supply: 2.5 V to 5.25 V operation

Normal: 75 μ A maximum

Power-down: 1 μ A maximum

RMS noise: 1.5 μ V

AD7788: 16-bit p-p resolution

AD7789: 19-bit p-p resolution (21.5 bits effective)

Integral nonlinearity: 3.5 ppm typical

Simultaneous 50 Hz and 60 Hz rejection

Internal clock oscillator

V_{DD} monitor channel

10-lead MSOP

INTERFACE

3-wire serial

SPI[®], QSPI[™], MICROWIRE[™], and DSP compatible

Schmitt trigger on SCLK

APPLICATIONS

Smart transmitters

Battery applications

Portable instrumentation

Sensor measurement

Temperature measurement

Pressure measurement

Weigh scales

4 to 20 mA loops

FUNCTIONAL BLOCK DIAGRAM

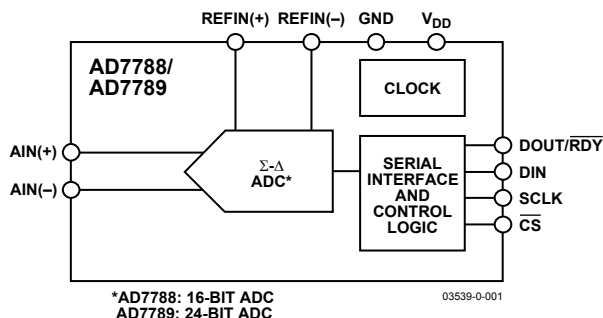


Figure 1.

GENERAL DESCRIPTION

The AD7788/AD7789 are low power, low noise, analog front ends for low frequency measurement applications. The AD7789 contains a low noise 24-bit Σ - Δ ADC with one differential input. The AD7788 is a 16-bit version of the AD7789.

The device operates from an internal clock. Therefore, the user does not have to supply a clock source to the device. The output data rate is 16.6 Hz, which gives simultaneous 50 Hz/60 Hz rejection.

The part operates with a single power supply from 2.5 V to 5.25 V. When operating from a 3 V supply, the power dissipation for the part is 225 μ W maximum. The AD7788/AD7789 is housed in a 10-lead MSOP.

Rev. 0

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REVISION HISTORY

Revision 0: Initial Version

AD7789—SPECIFICATIONS¹

Table 1. ($V_{DD} = 2.5\text{ V to }5.25\text{ V}$; $REFIN(+) = 2.5\text{ V}$; $REFIN(-) = GND$; $GND = 0\text{ V}$; all specifications T_{MIN} to T_{MAX} , unless otherwise noted.)

| Parameter | AD7789B | Unit | Test Conditions/Comments |
|---|-------------------------|-----------------------------------|--|
| ADC CHANNEL SPECIFICATION | | | |
| Output Update Rate | 16.6 | Hz nom | |
| ADC CHANNEL | | | |
| No Missing Codes ² | 24 | Bits min | |
| Resolution | 19 | Bits p-p | |
| Output Noise | 1.5 | $\mu\text{V rms typ}$ | |
| Integral Nonlinearity | ± 15 | ppm of FSR max | |
| Offset Error | ± 3 | $\mu\text{V typ}$ | |
| Offset Error Drift vs. Temperature | ± 10 | $\text{nV}/^{\circ}\text{C typ}$ | |
| Full-Scale Error ³ | ± 10 | $\mu\text{V typ}$ | |
| Gain Drift vs. Temperature | ± 0.5 | $\text{ppm}/^{\circ}\text{C typ}$ | |
| Power Supply Rejection | 90 | dB min | 100 dB typ, $A_{IN} = 1\text{ V}$ |
| ANALOG INPUTS | | | |
| Differential Input Voltage Ranges | $\pm REF_{IN}$ | V nom | $REF_{IN} = REF_{IN}(+) - REF_{IN}(-)$ |
| Absolute A_{IN} Voltage Limits ² | $GND - 30\text{ mV}$ | V min | |
| | $V_{DD} + 30\text{ mV}$ | V max | |
| Analogue Input Current | | | Input current varies with input voltage. |
| Average Input Current ² | ± 400 | nA/V typ | |
| Average Input Current Drift | ± 50 | $\text{pA}/^{\circ}\text{C typ}$ | |
| Normal Mode Rejection ² | | | |
| @ 50 Hz, 60 Hz | 65 | dB min | $50 \pm 1\text{ Hz}, 60 \pm 1\text{ Hz}$ |
| Common Mode Rejection | | | $A_{IN} = 1\text{ V}$ |
| @ DC | 90 | dB min | 100 dB typ |
| @ 50 Hz, 60 Hz ² | 100 | dB min | $50 \pm 1\text{ Hz}, 60 \pm 1\text{ Hz}$ |
| REFERENCE INPUT | | | |
| REF_{IN} Voltage | 2.5 | V nom | $REF_{IN} = REF_{IN}(+) - REF_{IN}(-)$ |
| Reference Voltage Range ² | 0.1 | V min | |
| | V_{DD} | V max | |
| Absolute REF_{IN} Voltage Limits ² | $GND - 30\text{ mV}$ | V min | |
| | $V_{DD} + 30\text{ mV}$ | V max | |
| Average Reference Input Current | 0.5 | $\mu\text{A/V typ}$ | |
| Average Reference Input Current Drift | ± 0.03 | $\text{nA}/^{\circ}\text{C typ}$ | |
| Normal Mode Rejection ² | | | |
| @ 50 Hz, 60 Hz | 65 | dB min | $50 \pm 1\text{ Hz}, 60 \pm 1\text{ Hz}$ |
| Common Mode Rejection | | | $A_{IN} = 1\text{ V}$ |
| @ DC | 110 | dB typ | |
| @ 50 Hz, 60 Hz | 110 | dB typ | $50 \pm 1\text{ Hz}, 60 \pm 1\text{ Hz}$ |

¹ Temperature Range -40°C to $+105^{\circ}\text{C}$.

² Specification is not production tested, but is supported by characterization data at initial product release.

³ Full-scale error applies to both positive and negative full scale and applies at the factory calibration conditions ($V_{DD} = 4\text{ V}$).

AD7788—SPECIFICATIONS¹

Table 2. ($V_{DD} = 2.5\text{ V to }5.25\text{ V}$ (B Grade); $V_{DD} = 2.7\text{ V to }5.25\text{ V}$ (A Grade); $REFIN(+)$ = 2.5 V; $REFIN(-)$ = GND; GND = 0 V; all specifications T_{MIN} to T_{MAX} , unless otherwise noted.)

| Parameter | AD7788A, B | Unit | Test Conditions/Comments |
|--|-------------------------|-----------------------------------|--|
| ADC CHANNEL SPECIFICATION | | | |
| Output Update Rate | 16.6 | Hz nom | |
| ADC CHANNEL | | | |
| No Missing Codes ² | 16 | Bits min | |
| Resolution | 16 | Bits p-p | |
| Output Noise | 1.5 | $\mu\text{V rms typ}$ | |
| Integral Nonlinearity | ± 15 | ppm of FSR max | B Grade |
| | ± 50 | ppm of FSR max | A Grade |
| Offset Error | ± 3 | $\mu\text{V typ}$ | |
| Offset Error Drift vs. Temperature | ± 10 | $\text{nV}/^{\circ}\text{C typ}$ | |
| Full-Scale Error ³ | ± 10 | $\mu\text{V typ}$ | |
| Gain Drift vs. Temperature | ± 0.5 | $\text{ppm}/^{\circ}\text{C typ}$ | |
| Power Supply Rejection | 90 | dB min | B Grade |
| | 90 | dB typ | A Grade |
| ANALOG INPUTS | | | |
| Differential Input Voltage Ranges | $\pm REFIN$ | V nom | $REFIN = REFIN(+) - REFIN(-)$ |
| Absolute AIN Voltage Limits ² | GND – 30 mV | V min | |
| | $V_{DD} + 30\text{ mV}$ | V max | |
| | | | Input current varies with input voltage. |
| Analogue Input Current | | | |
| Average Input Current ² | ± 400 | nA/V typ | |
| Average Input Current Drift | ± 50 | $\text{pA}/^{\circ}\text{C typ}$ | |
| Normal Mode Rejection ² | | | |
| @ 50 Hz, 60 Hz | 65 | dB min | B Grade, $50 \pm 1\text{ Hz}$, $60 \pm 1\text{ Hz}$ |
| | 60 | dB min | A Grade, $50 \pm 1\text{ Hz}$, $60 \pm 1\text{ Hz}$ |
| Common Mode Rejection | | | AIN = 1 V |
| @ DC | 90 | dB min | B Grade, 100 dB typ |
| | 90 | dB typ | A Grade |
| @ 50 Hz, 60 Hz ² | 100 | dB min | B Grade, $50 \pm 1\text{ Hz}$, $60 \pm 1\text{ Hz}$ |
| | 100 | dB typ | A Grade, $50 \pm 1\text{ Hz}$, $60 \pm 1\text{ Hz}$ |
| REFERENCE INPUT | | | |
| REFIN Voltage | 2.5 | V nom | $REFIN = REFIN(+) - REFIN(-)$ |
| Reference Voltage Range ² | 0.1 | V min | |
| | V_{DD} | V max | |
| | | | |
| Absolute REFIN Voltage Limits ² | GND – 30 mV | V min | |
| | $V_{DD} + 30\text{ mV}$ | V max | |
| | | | |
| Average Reference Input Current | 0.5 | $\mu\text{A/V typ}$ | |
| Average Reference Input Current Drift | ± 0.03 | $\text{nA}/^{\circ}\text{C typ}$ | |
| Normal Mode Rejection ² | | | |
| @ 50 Hz, 60 Hz | 65 | dB min | B Grade, $50 \pm 1\text{ Hz}$, $60 \pm 1\text{ Hz}$ |
| | 60 | dB min | A Grade |
| Common Mode Rejection | | | AIN = 1 V |
| @ DC | 100 | dB typ | |
| @ 50 Hz, 60 Hz | 110 | dB typ | $50 \pm 1\text{ Hz}$, $60 \pm 1\text{ Hz}$ |

¹ Temperature Range: B Grade, -40°C to $+105^{\circ}\text{C}$; A Grade, -40°C to $+85^{\circ}\text{C}$.

² Specification is not production tested but is supported by characterization data at initial product release.

³ Full-scale error applies to both positive and negative full scale and applies at the factory calibration conditions ($V_{DD} = 4\text{ V}$).

AD7788/AD7789 SPECIFICATIONS

Table 3.

| Parameter | AD7788A, B/ AD7789B | Unit | Test Conditions/Comments |
|--|------------------------|-------------------|---|
| LOGIC INPUTS | | | |
| All Inputs Except SCLK ¹ | | | |
| V_{INL} , Input Low Voltage | 0.8 | V max | $V_{DD} = 5\text{ V}$ |
| | 0.4 | V max | $V_{DD} = 3\text{ V}$ |
| V_{INH} , Input High Voltage | 2.0 | V min | $V_{DD} = 3\text{ V or } 5\text{ V}$ |
| SCLK Only (Schmitt-Triggered Input) ¹ | | | |
| $V_T(+)$ | 1.4/2 | V min/V max | $V_{DD} = 5\text{ V}$ |
| $V_T(-)$ | 0.8/1.4 | V min/V max | $V_{DD} = 5\text{ V}$ |
| $V_T(+)$ – $V_T(-)$ | 0.3/0.85 | V min/V max | $V_{DD} = 5\text{ V}$ |
| $V_T(+)$ | 0.9/2 | V min/V max | $V_{DD} = 3\text{ V}$ |
| $V_T(-)$ | 0.4/1.1 | V min/V max | $V_{DD} = 3\text{ V}$ |
| $V_T(+)$ – $V_T(-)$ | 0.3/0.85 | V min/V max | $V_{DD} = 3\text{ V}$ |
| Input Currents | ± 1 | $\mu\text{A max}$ | $V_{IN} = V_{DD}$ |
| Input Capacitance | 10 | pF typ | All Digital Inputs |
| LOGIC OUTPUTS | | | |
| V_{OH} , Output High Voltage ¹ | $V_{DD} - 0.6$ | V min | $V_{DD} = 3\text{ V}$, $I_{SOURCE} = 100\text{ }\mu\text{A}$ |
| V_{OL} , Output Low Voltage ¹ | 0.4 | V max | $V_{DD} = 3\text{ V}$, $I_{SINK} = 100\text{ }\mu\text{A}$ |
| V_{OH} , Output High Voltage ¹ | 4 | V min | $V_{DD} = 5\text{ V}$, $I_{SOURCE} = 200\text{ }\mu\text{A}$ |
| V_{OL} , Output Low Voltage ¹ | 0.4 | V max | $V_{DD} = 5\text{ V}$, $I_{SINK} = 1.6\text{ mA}$ |
| Floating-State Leakage Current | ± 1 | $\mu\text{A max}$ | |
| Floating-State Output Capacitance | 10 | pF typ | |
| Data Output Coding | Offset Binary | | |
| POWER REQUIREMENTS² | | | |
| Power Supply Voltage | | | |
| $V_{DD} - \text{GND}$ | 2.5/5.25 | V min/max | AD7789, AD7788B Grade |
| | 2.7/5.25 | V min/max | AD7788A Grade |
| Power Supply Currents | | | |
| I_{DD} Current | 75 | $\mu\text{A max}$ | 65 $\mu\text{A typ}$, $V_{DD} = 3.6\text{ V}$ |
| | 80 | $\mu\text{A max}$ | 73 $\mu\text{A typ}$, $V_{DD} = 5.25\text{ V}$ |
| I_{DD} (Power-Down Mode) | 1 | $\mu\text{A max}$ | |

¹ Specification is not production tested but is supported by characterization data at initial product release.² Digital inputs equal to V_{DD} or GND.

TIMING CHARACTERISTICS^{1, 2}

Table 4. ($V_{DD} = 2.5 \text{ V}$ to 5.25 V (AD7788B and AD7789), $V_{DD} = 2.7 \text{ V}$ to 5.25 V (AD7788A); $GND = 0 \text{ V}$, $REFIN(+) = 2.5 \text{ V}$, $REFIN(-) = GND$, Input Logic 0 = 0 V, Input Logic 1 = V_{DD} , unless otherwise noted.)

| Parameter | Limit at T_{MIN} , T_{MAX} (B Version) | Unit | Conditions/Comments |
|-----------------|---|--------|--|
| t_3 | 100 | ns min | SCLK High Pulsewidth |
| t_4 | 100 | ns min | SCLK Low Pulsewidth |
| Read Operation | | | |
| t_1 | 0 | ns min | \overline{CS} Falling Edge to DOUT/ \overline{RDY} Active Time |
| | 60 | ns max | $V_{DD} = 4.75 \text{ V}$ to 5.25 V |
| | 80 | ns max | $V_{DD} = 2.7 \text{ V}$ to 3.6 V |
| t_2^3 | 0 | ns min | SCLK Active Edge to Data Valid Delay ⁴ |
| | 60 | ns max | $V_{DD} = 4.75 \text{ V}$ to 5.25 V |
| | 80 | ns max | $V_{DD} = 2.7 \text{ V}$ to 3.6 V |
| $t_5^{5,6}$ | 10 | ns min | Bus Relinquish Time after \overline{CS} Inactive Edge |
| | 80 | ns max | |
| t_6 | 100 | ns max | SCLK Inactive Edge to \overline{CS} Inactive Edge |
| t_7 | 10 | ns min | SCLK Inactive Edge to DOUT/ \overline{RDY} High |
| Write Operation | | | |
| t_8 | 0 | ns min | \overline{CS} Falling Edge to SCLK Active Edge Setup Time ⁴ |
| t_9 | 30 | ns min | Data Valid to SCLK Edge Setup Time |
| t_{10} | 25 | ns min | Data Valid to SCLK Edge Hold Time |
| t_{11} | 0 | ns min | \overline{CS} Rising Edge to SCLK Edge Hold Time |

¹ Sample tested during initial release to ensure compliance. All input signals are specified with $t_R = t_F = 5 \text{ ns}$ (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V.

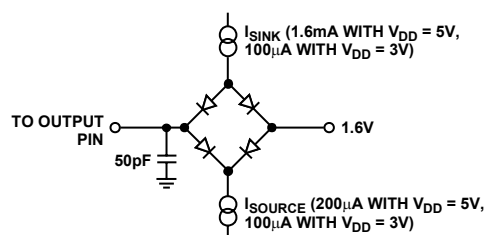
² See Figure 3 and Figure 4.

³ These numbers are measured with the load circuit of Figure 2 and defined as the time required for the output to cross the V_{OL} or V_{OH} limits.

⁴ SCLK active edge is falling edge of SCLK.

⁵ These numbers are derived from the measured time taken by the data output to change 0.5 V when loaded with the circuit of Figure 2. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the times quoted in the timing characteristics are the true bus relinquish times of the part and, as such, are independent of external bus loading capacitances.

⁶ \overline{RDY} returns high after a read of the ADC. In single conversion mode and continuous conversion mode, the same data can be read again, if required, while \overline{RDY} is high, although care should be taken to ensure that subsequent reads do not occur close to the next output update. In continuous read mode, the digital word can be read only once.



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Figure 2. Load Circuit for Timing Characterization

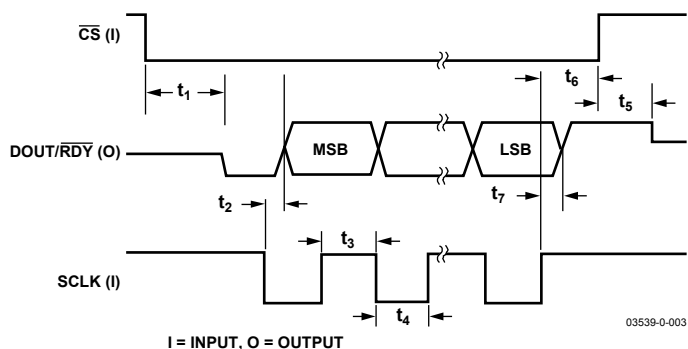


Figure 3. Read Cycle Timing Diagram

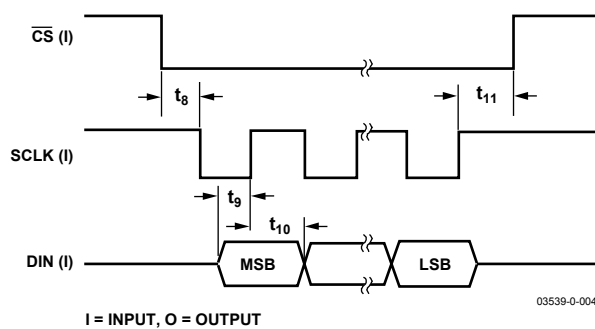


Figure 4. Write Cycle Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 5. ($T_A = 25^\circ\text{C}$, unless otherwise noted.)

| Parameter | Rating |
|--------------------------------------|----------------------------|
| V_{DD} to GND | −0.3 V to +7 V |
| Analog Input Voltage to GND | −0.3 V to $V_{DD} + 0.3$ V |
| Reference Input Voltage to GND | −0.3 V to $V_{DD} + 0.3$ V |
| Total AIN/REFIN Current (Indefinite) | 30 mA |
| Digital Input Voltage to GND | −0.3 V to $V_{DD} + 0.3$ V |
| Digital Output Voltage to GND | −0.3 V to $V_{DD} + 0.3$ V |
| Operating Temperature Range | |
| B Grade | −40°C to +105°C |
| A Grade | −40°C to +85°C |
| Storage Temperature Range | −65°C to +150°C |
| Maximum Junction Temperature | 150°C |
| MSOP | |
| θ_{JA} Thermal Impedance | 206°C/W |
| θ_{JC} Thermal Impedance | 44°C/W |
| Lead Temperature, Soldering (10 sec) | 300°C |
| IR Reflow, Peak Temperature | 220°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

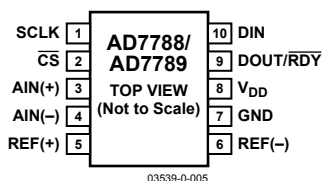


Figure 5. Pin Configuration

Table 6. Pin Function Descriptions

| Pin No. | Mnemonic | Function |
|---------|------------------------|---|
| 1 | SCLK | Serial Clock Input for Data Transfers to and from the ADC. The SCLK has a Schmitt-triggered input, making the interface suitable for opto-isolated applications. The serial clock can be continuous with all data transmitted in a continuous train of pulses. Alternatively, it can be a noncontinuous clock with the information being transmitted to or from the ADC in smaller batches of data. |
| 2 | $\overline{\text{CS}}$ | Chip Select Input. This is an active low logic input used to select the ADC. $\overline{\text{CS}}$ can be used to select the ADC in systems with more than one device on the serial bus or as a frame synchronization signal in communicating with the device. $\overline{\text{CS}}$ can be hardwired low, allowing the ADC to operate in 3-wire mode with SCLK, DIN, and DOUT used to interface with the device. |
| 3 | AIN(+) | Analog Input. AIN(+) is the positive terminal of the fully differential analog input. |
| 4 | AIN(-) | Analog Input. AIN(-) is the negative terminal of the fully differential analog input. |
| 5 | REFIN(+) | Positive Reference Input. REFIN(+) can lie anywhere between V_{DD} and GND + 0.1 V. The nominal reference voltage (REFIN(+) – REFIN(-)) is 2.5 V, but the part functions with a reference from 0.1 V to V_{DD} . |

| Pin No. | Mnemonic | Function |
|---------|-----------------|---|
| 6 | REFIN(-) | Negative Reference Input. This reference input can lie anywhere between GND and $V_{\text{DD}} - 0.1 \text{ V}$. |
| 7 | GND | Ground Reference Point. |
| 8 | V_{DD} | Supply Voltage, 3 V or 5 V Nominal. |
| 9 | DOUT/RDY | Serial Data Output/Data Ready Output. DOUT/RDY serves a dual purpose. It functions as a serial data output pin to access the output shift register of the ADC. The output shift register can contain data from any of the on-chip data or control registers. In addition, DOUT/RDY operates as a data ready pin, going low to indicate the completion of a conversion. If the data is not read after the conversion, the pin will go high before the next update occurs. The DOUT/ $\overline{\text{RDY}}$ falling edge can be used as an interrupt to a processor, indicating that valid data is available. With an external serial clock, the data can be read using the DOUT/RDY pin. With $\overline{\text{CS}}$ low, the data/control word information is placed on the DOUT/ $\overline{\text{RDY}}$ pin on the SCLK falling edge and is valid on the SCLK rising edge. The end of a conversion is also indicated by the RDY bit in the status register. When $\overline{\text{CS}}$ is high, the DOUT/ $\overline{\text{RDY}}$ pin is three-stated but the RDY bit remains active. |
| 10 | DIN | Serial Data Input to the Input Shift Register on the ADC. Data in this shift register is transferred to the control registers within the ADC, the register selection bits of the communications register identifying the appropriate register. |

TYPICAL PERFORMANCE CHARACTERISTICS

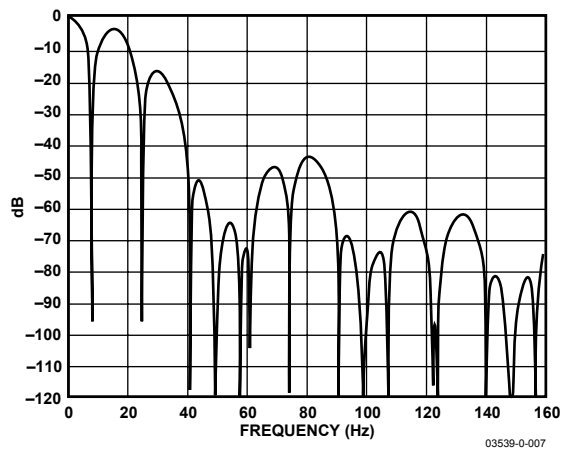


Figure 6. Frequency Response with 16.6 Hz Update Rate

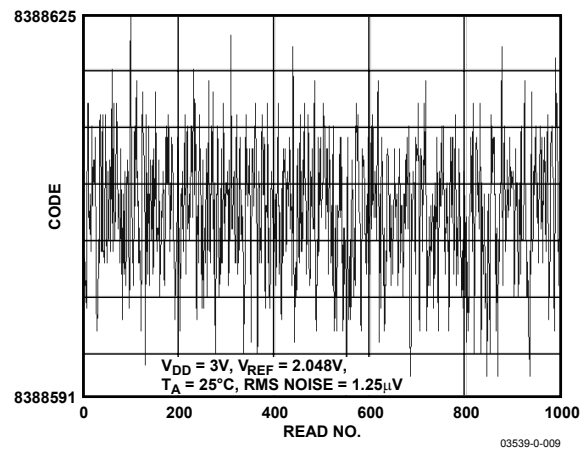


Figure 8. AD7789 Noise Plot

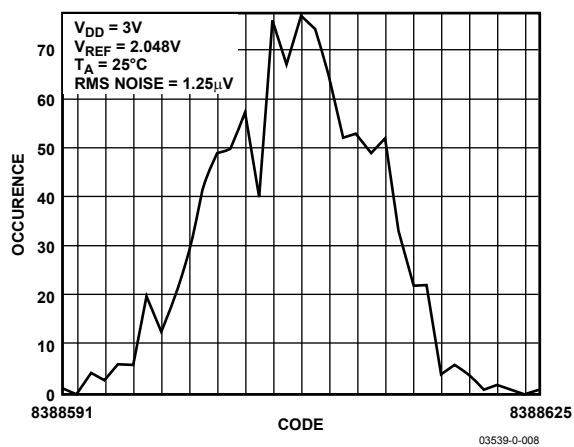


Figure 7. AD7789 Noise Histogram

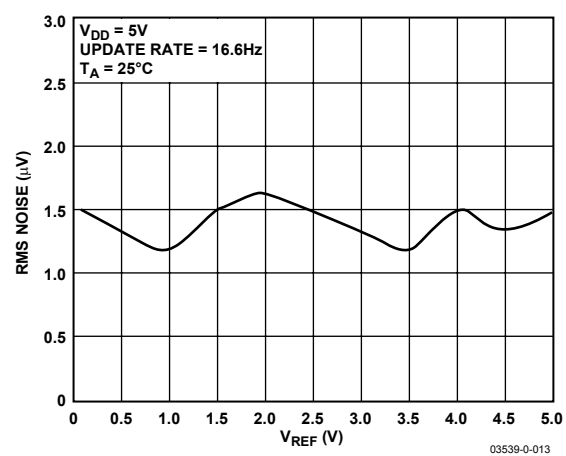


Figure 9. AD7788/AD7789 Noise vs. V_{REF}

ON-CHIP REGISTERS

The ADC is controlled and configured via a number of on-chip registers, which are described on the following pages. In the following descriptions, *set* implies a Logic 1 state and *cleared* implies a Logic 0 state, unless otherwise stated.

COMMUNICATIONS REGISTER (RS1, RS0 = 0, 0)

The communications register is an 8-bit write-only register. All communications to the part must start with a write operation to the communications register. The data written to the communications register determines whether the next operation is a read or write operation, and to which register this operation takes place. For read or write operations, once the subsequent read or write operation to the selected register is complete, the interface returns to where it expects a write operation to the communications register. This is the default state of the interface and, on power-up or after a reset, the ADC is in this default state waiting for a write operation to the communications register. In situations where the interface sequence is lost, a write operation of at least 32 serial clock cycles with DIN high returns the ADC to this default state by resetting the entire part. Table 7 outlines the bit designations for the communications register. CR0 through CR7 indicate the bit location, CR denoting the bits are in the communications register. CR7 denotes the first bit of the data stream. The number in brackets indicates the power-on/reset default status of that bit.

| CR7 | CR6 | CR5 | CR4 | CR3 | CR2 | CR1 | CR0 |
|--------|------|--------|--------|--------|----------|--------|--------|
| WEN(0) | 0(0) | RS1(0) | RS0(0) | R/W(0) | CREAD(0) | CH1(0) | CH0(0) |

Table 7. Communications Register Bit Designations

| Bit Location | Bit Name | Description |
|--------------|----------|--|
| CR7 | WEN | Write Enable Bit. A 0 must be written to this bit so that the write to the communications register actually occurs. If a 1 is the first bit written, the part will not clock on to subsequent bits in the register. It will stay at this bit location until a 0 is written to this bit. Once a 0 is written to the WEN bit, the next seven bits will be loaded to the communications register. |
| CR6 | 0 | This bit must be programmed with a Logic 0 for correct operation. |
| CR5–CR4 | RS1–RS0 | Register Address Bits. These address bits are used to select which of the ADC's registers are being selected during this serial interface communication. See Table 8. |
| CR3 | R/W | A 0 in this bit location indicates that the next operation will be a write to a specified register. A 1 in this position indicates that the next operation will be a read from the designated register. |
| CR2 | CREAD | Continuous Read of the Data Register. When this bit is set to 1 (and the data register is selected), the serial interface is configured so that the data register can be continuously read, i.e., the contents of the data register are placed on the DOUT pin automatically when the SCLK pulses are applied. The communications register does not have to be written to for data reads. To enable continuous read mode, the instruction 001111XX must be written to the communications register. To exit the continuous read mode, the instruction 001110XX must be written to the communications register while the RDY pin is low. While in continuous read mode, the ADC monitors activity on the DIN line so that it can receive the instruction to exit continuous read mode. Additionally, a reset will occur if 32 consecutive 1s are seen on DIN. Therefore, DIN should be held low in continuous read mode until an instruction is to be written to the device. |
| CR1–CR0 | CH1–CH0 | These bits are used to select the analog input channel. The differential channel can be selected (AIN(+)/AIN(–)) or an internal short (AIN(–)/AIN(–)) can be selected. Alternatively, the power supply can be selected, i.e., the ADC can measure the voltage on the power supply, which is useful for monitoring power supply variation. The power supply voltage is divided by 5 and then applied to the modulator for conversion. The ADC uses a $1.17\text{ V} \pm 5\%$ on-chip reference as the reference source for the analog to digital conversion. Any change in channel resets the filter and a new conversion is started. |

Table 8. Register Selection

| RS1 | RS0 | Register | Register Size |
|-----|-----|--|------------------------------------|
| 0 | 0 | Communications Register during a Write Operation | 8-Bit |
| 0 | 0 | Status Register during a Read Operation | 8-Bit |
| 0 | 1 | Mode Register | 8-Bit |
| 1 | 0 | Reserved | 8-Bit |
| 1 | 1 | Data Register | 16-Bit (AD7788) 24-Bit (AD7789) |

Table 9. Channel Selection

| CH1 | CH0 | Channel |
|-----|-----|-------------------------|
| 0 | 0 | AIN(+) – AIN(–) |
| 0 | 1 | Reserved |
| 1 | 0 | AIN(–) – AIN(–) |
| 1 | 1 | V _{DD} Monitor |

AD7788/AD7789

STATUS REGISTER (RS1, RS0 = 0, 0; POWER-ON/RESET = 0x88 [AD7788] AND 0x8C [AD7789])

The status register is an 8-bit read-only register. To access the ADC status register, the user must write to the communications register, select the next operation to be a read, and load bits RS1 and RS0 with 0. Table 10 outlines the bit designations for the status register. SR0 through SR7 indicate the bit locations, SR denoting the bits are in the status register. SR7 denotes the first bit of the data stream. The number in brackets indicates the power-on/reset default status of that bit.

| SR7 | SR6 | SR5 | SR4 | SR3 | SR2 | SR1 | SR0 |
|--------|--------|------|------|------|---------|--------|--------|
| RDY(1) | ERR(0) | 0(0) | 0(0) | 1(1) | WL(1/0) | CH1(0) | CH0(0) |

Table 10. Status Register Bit Designations

| Bit Location | Bit Name | Description |
|--------------|----------|---|
| SR7 | RDY | Ready bit for ADC. <i>Cleared</i> when data is written to the ADC data register. The RDY bit is <i>set</i> automatically after the ADC data register has been read or a period of time before the data register is updated with a new conversion result to indicate to the user not to read the conversion data. It is <i>also set</i> when the part is placed in power-down mode. The end of a conversion is indicated by the DOUT/RDY pin also. This pin can be used as an alternative to the status register for monitoring the ADC for conversion data. |
| SR6 | ERR | ADC Error Bit. This bit is written to at the same time as the RDY bit. <i>Set</i> to indicate that the result written to the ADC data register has been clamped to all 0s or all 1s. Error sources include overrange, underrange. <i>Cleared</i> by a write operation to start a conversion. |
| SR5 | 0 | This bit is automatically <i>cleared</i> . |
| SR4 | 0 | This bit is automatically <i>cleared</i> . |
| SR3 | 1 | This bit is automatically <i>set</i> . |
| SR2 | 1/0 | This bit is automatically <i>cleared</i> if the device is an AD7788 and it is automatically <i>set</i> if the device is an AD7789. This bit can be used to distinguish between the AD7788 and AD7789. |
| SR1–SR0 | CH1–CH0 | These bits indicate which channel is being converted by the ADC. |

MODE REGISTER (RS1, RS0 = 0, 1; POWER-ON/RESET = 0x02)

The mode register is an 8-bit register from which data can be read or to which data can be written. This register is used to configure the ADC for range, unipolar or bipolar mode, enable or disable the buffer, or place the device into power-down mode. Table 11 outlines the bit designations for the mode register. MR0 through MR7 indicate the bit locations, MR denoting the bits are in the mode register. MR7 denotes the first bit of the data stream. The number in brackets indicates the power-on/reset default status of that bit. Any write to the setup register resets the modulator and filter and sets the RDY bit.

| MR7 | MR6 | MR5 | MR4 | MR3 | MR2 | MR1 | MR0 |
|--------|--------|------|------|------|--------|------|------|
| MD1(0) | MD0(0) | 0(0) | 0(0) | 0(0) | U/B(0) | 1(1) | 0(0) |

Table 11. Mode Register Bit Designations

| Bit Location | Bit Name | Description |
|--------------|----------|--|
| MR7–MR6 | MD1–MD0 | Mode Select Bits. These bits select between continuous conversion mode, single conversion mode, and standby mode. In continuous conversion mode, the ADC continuously performs conversions and places the result in the data register. RDY goes low when a conversion is complete. The user can read these conversions by placing the device in continuous read mode whereby the conversions are automatically placed on the DOUT line when SCLK pulses are applied. Alternatively, the user can instruct the ADC to output the conversion by writing to the communications register. After power-on, the first conversion is available after a period $2/f_{ADC}$ while subsequent conversions are available at a frequency of f_{ADC} . In single conversion mode, the ADC is placed in power-down mode when conversions are not being performed. When single conversion mode is selected, the ADC powers up and performs a single conversion, which occurs after a period $2/f_{ADC}$. The conversion result is placed in the data register, RDY goes low, and the ADC returns to power-down mode. The conversion remains in the data register and RDY remains active (low) until the data is read or another conversion is performed. See Table 12. |

| Bit Location | Bit Name | Description |
|--------------|-------------------|---|
| MR5–MR3 | 0 | This bit must be programmed with a Logic 0 for correct operation. |
| MR2 | U/ \overline{B} | Unipolar/Bipolar Bit. <i>Set</i> by user to enable unipolar coding, i.e., zero differential input will result in 000...000 output and a full-scale differential input will result in 111...111 output. <i>Cleared</i> by the user to enable bipolar coding. Negative full-scale differential input will result in an output code of 000...000, zero differential input will result in an output code of 100...000, and a positive full-scale differential input will result in an output code of 111...111. |
| MR1 | 1 | This bit must be programmed with a Logic 1 for correct operation. |
| MR0 | 0 | This bit must be programmed with a Logic 0 for correct operation. |

Table 12. Operating Modes

| MD1 | MD0 | Mode |
|-----|-----|--------------------------------------|
| 0 | 0 | Continuous Conversion Mode (Default) |
| 0 | 1 | Reserved |
| 1 | 0 | Single Conversion Mode |
| 1 | 1 | Powerdown Mode |

DATA REGISTER (RS1, RS0 = 1, 1; POWER-ON/RESET = 0x0000 [AD7788] AND 0x000000 [AD7789])

The conversion result from the ADC is stored in this data register. This is a read-only register. On completion of a read operation from this register, the \overline{RDY} bit/pin is set.

ADC CIRCUIT INFORMATION

OVERVIEW

The AD7788/AD7789 is a low power ADC that incorporates a Σ - Δ modulator and on-chip digital filtering intended for the measurement of wide dynamic range, low frequency signals such as those in pressure transducers, weigh scales, and temperature measurement applications.

The part has one unbuffered differential input. The device requires an external reference voltage between 0.1 V and V_{DD} . Figure 10 shows the basic connections required to operate the part.

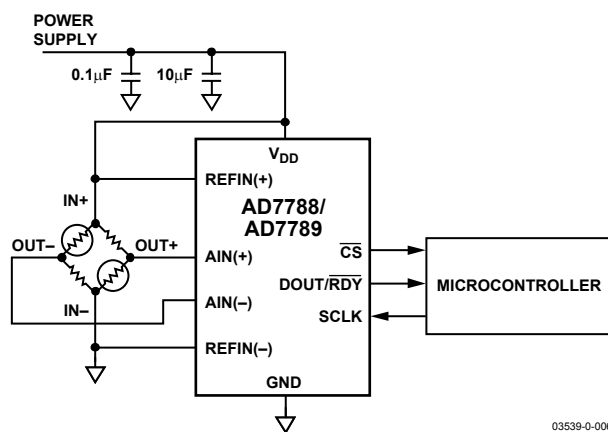


Figure 10. Basic Connection Diagram

The output rate of the AD7788/AD7789 (f_{ADC}) is 16.6 Hz with the settling time equal to $2 \times t_{ADC}$ (120.4 ms). Normal mode rejection is the major function of the digital filter. Simultaneous 50 Hz and 60 Hz rejection is optimized as notches are placed at both 50 Hz and 60 Hz with this update rate (see Figure 6).

NOISE PERFORMANCE

The AD7788/AD7789 has an rms noise of 1.5 μ V rms typically, which corresponds to a peak-to-peak resolution of 16 bits for the AD7788 and 19 bits (equivalent to an effective resolution of 21.5 bits) for the AD7789. The numbers given are for the bipolar input range with a reference of 2.5 V. The noise was measured with a differential input voltage of 0 V. The peak-to-peak resolution figures represent the resolution for which there will be no code flicker within a six-sigma limit. The output noise comes from two sources. The first is the electrical noise in the semiconductor devices (device noise) used in the implementation of the modulator. The second is quantization noise, which is added when the analog input is converted into the digital domain.

DIGITAL INTERFACE

As previously outlined, the AD7788/AD7789's programmable functions are controlled using a set of on-chip registers. Data is written to these registers via the part's serial interface and read access to the on-chip registers is also provided by this interface. All communications with the part must start with a write to the communications register. After power-on or reset, the device expects a write to its communications register. The data written to this register determines whether the next operation is a read operation or a write operation and also determines to which register this read or write operation occurs. Therefore, write access to any of the other registers on the part begins with a write operation to the communications register followed by a write to the selected register. A read operation from any other register (except when continuous read mode is selected) starts with a write to the communications register followed by a read operation from the selected register.

The AD7788/AD7789's serial interface consists of four signals: \overline{CS} , DIN, SCLK, and DOUT/RDY. The DIN line is used to transfer data into the on-chip registers while DOUT/RDY is used for accessing from the on-chip registers. SCLK is the serial clock input for the device and all data transfers (either on DIN or DOUT/RDY) occur with respect to the SCLK signal. The DOUT/RDY pin operates as a Data Ready signal also, the line going low when a new data-word is available in the output register. It is reset high when a read operation from the data register is complete. It also goes high prior to the updating of the data register to indicate when not to read from the device to ensure that a data read is not attempted while the register is being updated. \overline{CS} is used to select a device. It can be used to decode the AD7788/AD7789 in systems where several components are connected to the serial bus.

Figure 3 and Figure 4 show timing diagrams for interfacing to the AD7788/AD7789 with \overline{CS} being used to decode the part. Figure 3 shows the timing for a read operation from the AD7788/AD7789's output shift register while Figure 4 shows the timing for a write operation to the input shift register. In all modes except continuous read mode, it is possible to read the same word from the data register several times even though the DOUT/RDY line returns high after the first read operation. However, care must be taken to ensure that the read operations have been completed before the next output update occurs. In continuous read mode, the data register can be read only once.

The serial interface can operate in 3-wire mode by tying $\overline{\text{CS}}$ low. In this case, the SCLK, DIN, and DOUT/RDY lines are used to communicate with the AD7788/AD7789. The end of conversion can be monitored using the $\overline{\text{RDY}}$ bit in the status register. This scheme is suitable for interfacing to microcontrollers. If $\overline{\text{CS}}$ is required as a decoding signal, it can be generated from a port pin. For microcontroller interfaces, it is recommended that SCLK idles high between data transfers.

The AD7788/AD7789 can be operated with $\overline{\text{CS}}$ being used as a frame synchronization signal. This scheme is useful for DSP interfaces. In this case, the first bit (MSB) is effectively clocked out by $\overline{\text{CS}}$ since $\overline{\text{CS}}$ would normally occur after the falling edge of SCLK in DSPs. The SCLK can continue to run between data transfers, provided the timing numbers are obeyed.

The serial interface can be reset by writing a series of 1s on the DIN input. If a Logic 1 is written to the AD7788/AD7789 line for at least 32 serial clock cycles, the serial interface is reset. This ensures that in 3-wire systems, the interface can be reset to a known state if the interface gets lost due to a software error or some glitch in the system. Reset returns the interface to the state in which it is expecting a write to the communications register. This operation resets the contents of all registers to their power-on values.

The AD7788/AD7789 can be configured to continuously convert or to perform a single conversion. See Figure 11 through Figure 13.

Single Conversion Mode

In single conversion mode, the AD7788/AD7789 is placed in shutdown mode between conversions. When a single conversion is initiated by setting MD1 to 1 and MD0 to 0 in the mode register, the AD7788/AD7789 powers up, performs a single conversion, and then returns to shutdown mode. A conversion will require a time period of $2 \times t_{\text{ADC}}$. DOUT/ $\overline{\text{RDY}}$ goes low to indicate the completion of a conversion. When the data-word has been read from the data register, DOUT/ $\overline{\text{RDY}}$ will go high. If $\overline{\text{CS}}$ is low, DOUT/ $\overline{\text{RDY}}$ will remain high until another conversion is initiated and completed. The data register can be read several times, if required, even when DOUT/ $\overline{\text{RDY}}$ has gone high.

Continuous Conversion Mode

This is the default power-up mode. The AD7788/AD7789 will continuously convert, the $\overline{\text{RDY}}$ pin in the status register going low each time a conversion is complete. If $\overline{\text{CS}}$ is low, the DOUT/ $\overline{\text{RDY}}$ line will also go low when a conversion is complete. To read a conversion, the user can write to the communications register, indicating that the next operation is a read of the data register. The digital conversion will be placed on the DOUT/ $\overline{\text{RDY}}$ pin as soon as SCLK pulses are applied to the ADC. DOUT/ $\overline{\text{RDY}}$ will return high when the conversion is read. The user can read this register additional times, if required. However, the user must ensure that the data register is not being accessed at the completion of the next conversion or else the new conversion word will be lost.

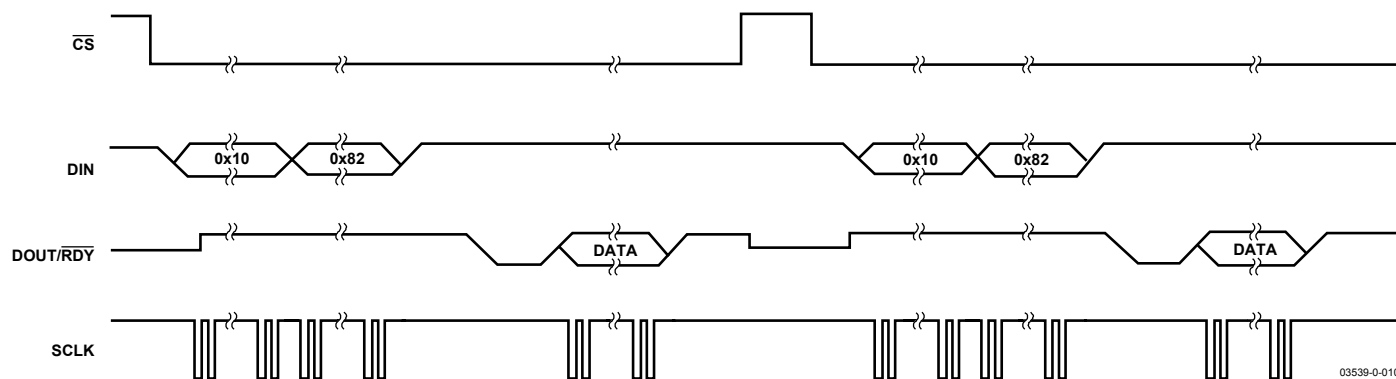


Figure 11. Single Conversion

Continuous Read Mode

Rather than write to the communications register each time a conversion is complete to access the data, the AD7788/AD7789 can be placed in continuous read mode. By writing 001111XX to the communications register, the user needs only to apply the appropriate number of SCLK cycles to the ADC and the data word will automatically be placed on the DOUT/RDY line when a conversion is complete.

When DOUT/RDY goes low to indicate the end of a conversion, sufficient SCLK cycles must be applied to the ADC and the data conversion will be placed on the DOUT/RDY line. When the conversion is read, DOUT/RDY will return high until the next conversion is available. In this mode, the data can be read only once. Also, the user must ensure that the data-word is read

before the next conversion is complete. If the user has not read the conversion before the completion of the next conversion or if insufficient serial clocks are applied to the AD7788/AD7789 to read the word, the serial output register is reset when the next conversion is complete and the new conversion is placed in the output serial register.

To exit the continuous read mode, the instruction 001110XX must be written to the communications register while the RDY pin is low. While in the continuous read mode, the ADC monitors activity on the DIN line so that it can receive the instruction to exit the continuous read mode. Additionally, a reset will occur if 32 consecutive 1s are seen on DIN. Therefore, DIN should be held low in continuous read mode until an instruction is to be written to the device.

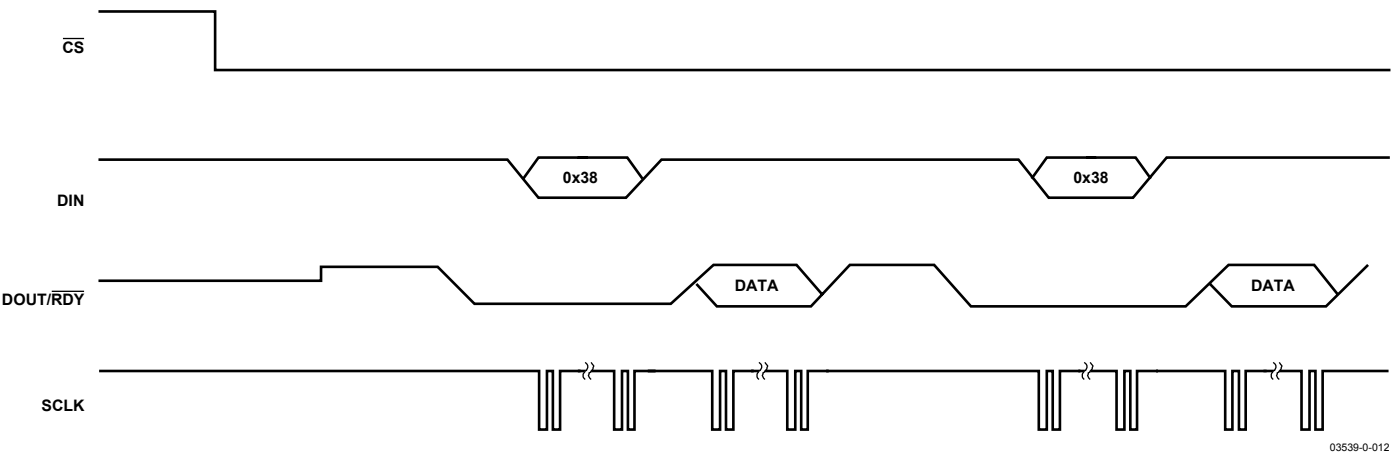


Figure 12. Continuous Conversion

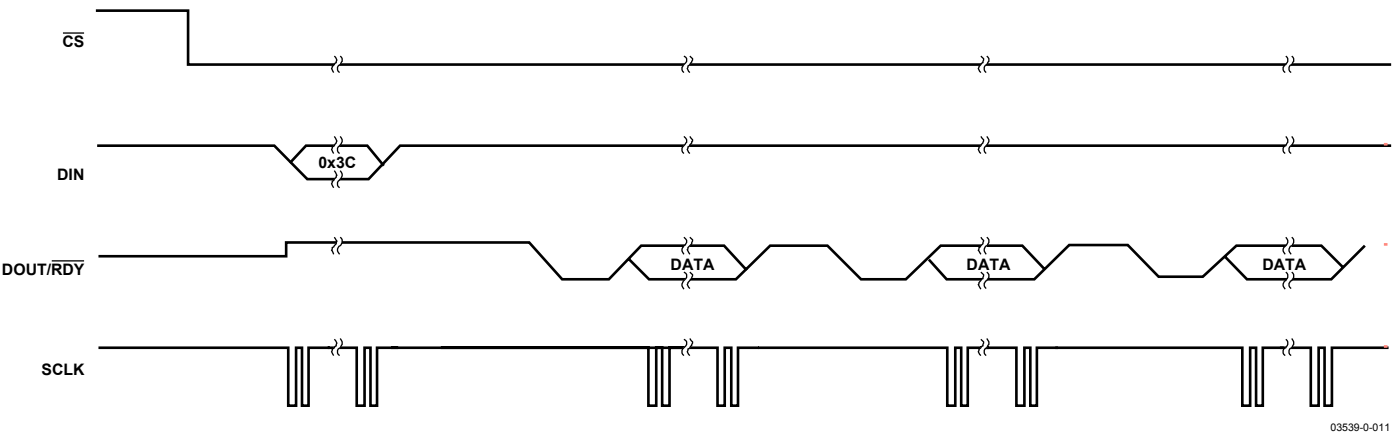


Figure 13. Continuous Read

CIRCUIT DESCRIPTION

ANALOG INPUT CHANNEL

The AD7788/AD7789 has one differential analog input channel that is connected to the modulator, i.e., the input is unbuffered. Note that this unbuffered input path provides a dynamic load to the driving source. Therefore, resistor/capacitor combinations on the input pins can cause dc gain errors, depending on the output impedance of the source that is driving the ADC input. Table 13 shows the allowable external resistance/capacitance values such that no gain error at the 16-bit level is introduced (AD7788), while Table 14 shows the allowable external resistance/capacitance values such that no gain error at the 20-bit level is introduced (AD7789).

Table 13. External R-C Combination for No 16-Bit Gain Error (AD7788)

| C (pF) | R (Ω) |
|--------|-------|
| 50 | 22.8K |
| 100 | 13.1K |
| 500 | 3.3K |
| 1000 | 1.8K |
| 5000 | 360 |

Table 14. External R-C Combination for No 20-Bit Gain Error (AD7789)

| C (pF) | R (Ω) |
|--------|-------|
| 50 | 16.7K |
| 100 | 9.6K |
| 500 | 2.2K |
| 1000 | 1.1K |
| 5000 | 160 |

The absolute input voltage includes the range between GND – 30 mV and $V_{DD} + 30$ mV. The negative absolute input voltage limit does allow the possibility of monitoring small true bipolar signals with respect to GND.

The absolute input voltage includes the range between GND – 30 mV and $V_{DD} + 30$ mV. The negative absolute input voltage limit does allow the possibility of monitoring small true bipolar signals with respect to GND.

BIPOLAR/UNIPOLAR CONFIGURATION

The analog input to the AD7788/AD7789 can accept either unipolar or bipolar input voltage ranges. A bipolar input range does not imply that the part can tolerate large negative voltages with respect to system GND. Unipolar and bipolar signals on the AIN(+) input are referenced to the voltage on the AIN(–) input. For example, if AIN(–) is 2.5 V and the ADC is configured for unipolar mode, the input voltage range on the AIN(+) pin is 2.5 V to 5 V. If the ADC is configured for bipolar mode,

the analog input range on the AIN(+) input is 0 V to 5 V. The bipolar/unipolar option is chosen by programming the B/U bit in the mode register.

DATA OUTPUT CODING

When the ADC is configured for unipolar operation, the output code is natural (straight) binary with a zero differential input voltage resulting in a code of 00...00, a midscale voltage resulting in a code of 100...000, and a full-scale input voltage resulting in a code of 111...111. The output code for any analog input voltage can be represented as

$$Code = 2^N \times (AIN/V_{REF})$$

When the ADC is configured for bipolar operation, the output code is offset binary with a negative full-scale voltage resulting in a code of 000...000, a zero differential input voltage resulting in a code of 100...000, and a positive full-scale input voltage resulting in a code of 111...111. The output code for any analog input voltage can be represented as

$$Code = 2^{N-1} \times [(AIN/V_{REF}) + 1]$$

where AIN is the analog input voltage and $N = 16$ for the AD7788 and 24 for the AD7789.

REFERENCE INPUT

The AD7788/AD7789 has a fully differential input capability for the channel. The common-mode range for these differential inputs is from GND to V_{DD} . The reference input is unbuffered and, therefore, excessive R-C source impedances will introduce gain errors. The reference voltage REFIN (REFIN(+) – REFIN(–)) is 2.5 V nominal, but the AD7788/AD7789 is functional with reference voltages from 0.1 V to V_{DD} . In applications where the excitation (voltage or current) for the transducer on the analog input also drives the reference voltage for the part, the effect of the low frequency noise in the excitation source will be removed because the application is ratiometric. If the AD7788/AD7789 is used in a nonratiometric application, a low noise reference should be used.

Recommended 2.5 V reference voltage sources for the AD7788/AD7789 include the ADR381 and ADR391, which are low noise, low power references. If the analog circuitry uses a 2.5 V power supply, the reference voltage source will require some headroom. In this case, a 2.048 V reference such as the ADR380 or ADR390 can be used. Again, these are low power, low noise references. Also note that the reference inputs provide a high impedance, dynamic load. Because the input impedance of each reference input is dynamic, resistor/capacitor combinations on these inputs can cause dc gain errors, depending on the output impedance of the source that is driving the reference inputs.

Reference voltage sources like those recommended above (e.g., ADR391) will typically have low output impedances and are, therefore, tolerant to having decoupling capacitors on REFIN(+) without introducing gain errors in the system. Deriving the reference input voltage across an external resistor will mean that the reference input sees a significant external source impedance. External decoupling on the REFIN pins would not be recommended in this type of circuit configuration.

V_{DD} MONITOR

Along with converting external voltages, the analog input channel can be used to monitor the voltage on the V_{DD} pin. When the CH1 and CH0 bits in the communications register are set to 1, the voltage on the V_{DD} pin is internally attenuated by 5 and the resultant voltage is applied to the Σ - Δ modulator using an internal 1.17 V reference for analog to digital conversion. This is useful because variations in the power supply voltage can be monitored.

GROUNDING AND LAYOUT

Since the analog inputs and reference inputs of the ADC are differential, most of the voltages in the analog modulator are common-mode voltages. The excellent common-mode rejection of the part will remove common-mode noise on these inputs. The digital filter will provide rejection of broadband noise on the power supply, except at integer multiples of the modulator sampling frequency. The digital filter also removes noise from the analog and reference inputs, provided that these noise sources do not saturate the analog modulator. As a result, the AD7788/AD7789 is more immune to noise interference than a conventional high resolution converter. However, because the resolution of the AD7788/AD7789 is so high, and the noise levels from the AD7788/AD7789 are so low, care must be taken with regard to grounding and layout.

The printed circuit board that houses the AD7788/AD7789 should be designed such that the analog and digital sections are separated and confined to certain areas of the board. A minimum etch technique is generally best for ground planes because it gives the best shielding.

It is recommended that the AD7788/AD7789's GND pin be tied to the AGND plane of the system. In any layout, it is important that the user keep in mind the flow of currents in the system, ensuring that the return paths for all currents are as close as possible to the paths the currents took to reach their destinations. Avoid forcing digital currents to flow through the AGND sections of the layout.

The AD7788/AD7789's ground plane should be allowed to run under the AD7788/AD7789 to prevent noise coupling. The power supply lines to the AD7788/AD7789 should use as wide a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals such as clocks should be shielded with digital ground to avoid radiating noise to other sections of the board, and clock signals should never be run near the analog inputs. Avoid cross-over of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This will reduce the effects of feedthrough through the board. A micro-strip technique is by far the best, but it is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes, while signals are placed on the solder side.

Good decoupling is important when using high resolution ADCs. V_{DD} should be decoupled with 10 μ F tantalum in parallel with 0.1 μ F capacitors to GND. To achieve the best from these decoupling components, they should be placed as close as possible to the device, ideally right up against the device. All logic chips should be decoupled with 0.1 μ F ceramic capacitors to DGND.

OUTLINE DIMENSIONS

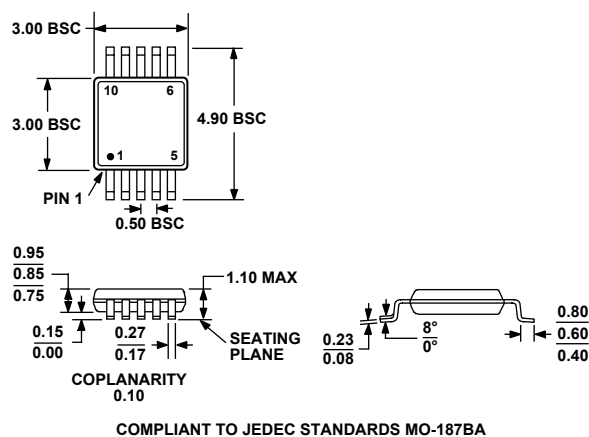


Figure 14. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)

Dimensions shown in millimeters

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



Table 15. Ordering Guide

| Model | Temperature Range | Package Description | Package Option | Branding |
|----------------|-------------------|---|----------------|----------|
| AD7788BRM | −40°C to +105°C | 10-Lead Mini Small Outline Package (MSOP) | RM-10 | COX |
| AD7788BRM-REEL | −40°C to +105°C | 10-Lead Mini Small Outline Package (MSOP) | RM-10 | COX |
| AD7788ARM | −40°C to +85°C | 10-Lead Mini Small Outline Package (MSOP) | RM-10 | COZ |
| AD7788ARM-REEL | −40°C to +85°C | 10-Lead Mini Small Outline Package (MSOP) | RM-10 | COZ |
| AD7789BRM | −40°C to +105°C | 10-Lead Mini Small Outline Package (MSOP) | RM-10 | COY |
| AD7789BRM-REEL | −40°C to +105°C | 10-Lead Mini Small Outline Package (MSOP) | RM-10 | COY |

NOTES