

## ADG811/ADG812/ADG813

### FEATURES

**0.5  $\Omega$  typ on resistance**  
**0.8  $\Omega$  max on resistance at 125°C**  
**1.65 V to 3.6 V operation**  
**Automotive temperature range: -40°C to +125°C**  
**High current carrying capability: 300 mA continuous**  
**Rail-to-rail switching operation**  
**Fast switching times: <25 ns**  
**Typical power consumption < 0.1  $\mu$ W**

### APPLICATIONS

**Cellular phones**  
**MP3 players**  
**Power routing**  
**Battery-powered systems**  
**PCMCIA cards**  
**Modems**  
**Audio and video signal routing**  
**Communications systems**

### GENERAL DESCRIPTION

The ADG811, ADG812, and ADG813 are low voltage CMOS devices containing four independently selectable switches. These switches offer ultralow on resistance of less than 0.8  $\Omega$  over the full temperature range. The digital inputs can handle 1.8 V logic with a 2.7 V to 3.6 V supply.

These devices contain four independent single-pole/single-throw (SPST) switches. The ADG811 and ADG812 differ only in that the digital control logic is inverted. The ADG811 switches are turned on with a logic low on the appropriate control input, while a logic high is required to turn on the switches of the ADG812. The ADG813 contains two switches whose digital control logic is similar to the ADG811, while the logic is inverted on the other two switches.

Each switch conducts equally well in both directions when on and has an input signal range that extends to the supplies. The ADG813 exhibits break-before-make switching action.

The ADG811, ADG812, and ADG813 are fully specified for 3.3 V, 2.5 V, and 1.8 V supply operation. They are available in a 16-lead TSSOP package.

#### Rev. A

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

### FUNCTIONAL BLOCK DIAGRAMS

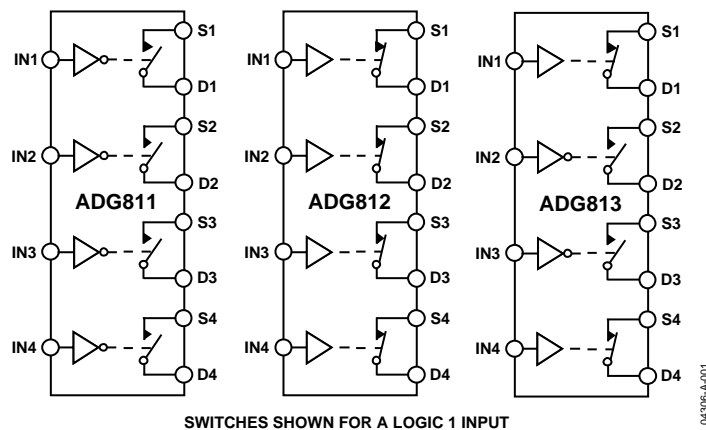


Figure 1.

### PRODUCT HIGHLIGHTS

1. <0.8  $\Omega$  over full temperature range of -40°C to +125°C.
2. Single 1.65 V to 3.6 V operation.
3. Operational with 1.8 V CMOS logic.
4. High current handling capability (300 mA continuous current at 3.3 V).
5. Low THD+N (0.02% typ).

TABLE OF CONTENTS

|  |   |   |    |
|--|---|---|----|
| ADG811/ADG812/ADG813—Specifications .....        | 3 | Typical Performance Characteristics ..... | 8  |
| Absolute Maximum Ratings.....                    | 6 | Test Circuits.....                        | 11 |
| ESD Caution.....                                 | 6 | Outline Dimensions .....                  | 13 |
| Pin Configuration and Function Descriptions..... | 7 | Ordering Guide .....                      | 13 |

REVISION HISTORY

5/04—Data Sheet Changed from Rev. 0 to Rev. A

|                              |           |
|------------------------------|-----------|
| Updated Format.....          | Universal |
| Updated Package Choices..... | Universal |

11/03—Revision 0: Initial Version

## ADG811/ADG812/ADG813—SPECIFICATIONS

Table 1.  $V_{DD} = 2.7\text{ V}$  to  $3.6\text{ V}$ ,  $GND = 0\text{ V}$ , unless otherwise noted<sup>1</sup>

| Parameter  | +25°C     | −40°C to +85°C | −40°C to +125°C | Unit              | Test Conditions/Comments  |
|--|-----------|----------------|-----------------|-------------------|---|
| <b>ANALOG SWITCH</b>                                     |           |                |                 |                   |   |
| Analog Signal Range                                      |           |                | 0 V to $V_{DD}$ | V                 |   |
| On Resistance ( $R_{ON}$ )                               | 0.5       |                |                 | $\Omega$ typ      | $V_{DD} = 2.7\text{ V}$ , $V_S = 0\text{ V}$ to $V_{DD}$ , $I_S = 10\text{ mA}$ ; |
|  | 0.65      | 0.75           | 0.8             | $\Omega$ max      | Figure 18   |
| On Resistance Match between Channels ( $\Delta R_{ON}$ ) | 0.04      |                |                 | $\Omega$ typ      | $V_{DD} = 2.7\text{ V}$ , $V_S = 0.5\text{ V}$ , $I_S = 10\text{ mA}$             |
|  |           | 0.075          | 0.08            | $\Omega$ max      |   |
| On Resistance Flatness ( $R_{FLAT(ON)}$ )                | 0.1       |                |                 | $\Omega$ typ      | $V_{DD} = 2.7\text{ V}$ , $V_S = 0\text{ V}$ to $V_{DD}$ , $I_S = 10\text{ mA}$   |
|  |           | 0.15           | 0.16            | $\Omega$ max      |   |
| <b>LEAKAGE CURRENTS</b>                                  |           |                |                 |                   |   |
| Source Off Leakage $I_S$ (OFF)                           | $\pm 0.2$ |                |                 | nA typ            | $V_{DD} = 3.6\text{ V}$   |
|  | $\pm 1$   | $\pm 8$        | $\pm 80$        | nA max            | $V_S = 0.6\text{ V}/3.3\text{ V}$ , $V_D = 3.3\text{ V}/0.6\text{ V}$ ;           |
| Drain Off Leakage $I_D$ (OFF)                            | $\pm 0.2$ |                |                 | nA typ            | Figure 19   |
|  | $\pm 1$   | $\pm 8$        | $\pm 80$        | nA max            | $V_S = 0.6\text{ V}/3.3\text{ V}$ , $V_D = 3.3\text{ V}/0.6\text{ V}$ ;           |
| Channel On Leakage $I_D$ , $I_S$ (ON)                    | $\pm 0.2$ |                |                 | nA typ            | Figure 19   |
|  | $\pm 1$   | $\pm 15$       | $\pm 90$        | nA max            | $V_S = V_D = 0.6\text{ V}$ or $3.3\text{ V}$ ; Figure 20                          |
| <b>DIGITAL INPUTS</b>                                    |           |                |                 |                   |   |
| Input High Voltage, $V_{INH}$                            |           |                | 2               | V min             |   |
| Input Low Voltage, $V_{INL}$                             |           |                | 0.8             | V max             |   |
| Input Current, $I_{INL}$ or $I_{INH}$                    | 0.005     |                |                 | $\mu\text{A}$ typ | $V_{IN} = V_{INL}$ or $V_{INH}$   |
|  |           |                | $\pm 0.1$       | $\mu\text{A}$ max |   |
| $C_{IN}$ , Digital Input Capacitance                     | 6         |                |                 | pF typ            |   |
| <b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>               |           |                |                 |                   |   |
| $t_{ON}$   | 21        |                |                 | ns typ            | $R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$   |
|  | 25        | 26             | 28              | ns max            | $V_S = 1.5\text{ V}/0\text{ V}$ ; Figure 21                                       |
| $t_{OFF}$  | 4         |                |                 | ns typ            | $R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$   |
|  | 5         | 6              | 7               | ns max            | $V_S = 1.5\text{ V}$ ; Figure 21  |
| Break-Before-Make Time Delay ( $t_{BBM}$ )               | 17        |                |                 | ns typ            | $R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$   |
| (ADG813 only)  |           |                | 5               | ns min            | $V_{S1} = V_{S2} = 1.5\text{ V}$ ; Figure 22                                      |
| Charge Injection   | 30        |                |                 | pC typ            | $V_S = 1.5\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ;                  |
|  |           |                |                 |                   | Figure 23   |
| Off Isolation  | −67       |                |                 | dB typ            | $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 100\text{ kHz}$ ;                 |
|  |           |                |                 |                   | Figure 24   |
| Channel-to-Channel Crosstalk                             | −90       |                |                 | dB typ            | $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 100\text{ kHz}$ ;                 |
|  |           |                |                 |                   | Figure 26   |
| Total Harmonic Distortion (THD + N)                      | 0.02      |                |                 | %                 | $R_L = 32\ \Omega$ , $f = 20\text{ Hz}$ to $20\text{ kHz}$ ,                      |
|  |           |                |                 |                   | $V_S = 2\text{ V p-p}$  |
| Insertion Loss   | −0.05     |                |                 | dB typ            | $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 100\text{ kHz}$                   |
| −3 dB Bandwidth  | 90        |                |                 | MHz typ           | $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; Figure 25                              |
| $C_S$ (OFF)  | 30        |                |                 | pF typ            |   |
| $C_D$ (OFF)  | 35        |                |                 | pF typ            |   |
| $C_D$ , $C_S$ (ON)                                       | 60        |                |                 | pF typ            |   |
| <b>POWER REQUIREMENTS</b>                                |           |                |                 |                   |   |
| $I_{DD}$   | 0.003     |                |                 | $\mu\text{A}$ typ | $V_{DD} = 3.6\text{ V}$   |
|  |           | 1.0            | 4               | $\mu\text{A}$ max | Digital inputs = 0 V or 3.6 V   |

<sup>1</sup>Temperature range for the Y version is −40°C to +125°C.<sup>2</sup>Guaranteed by design, not subject to production test.

# ADG811/ADG812/ADG813

**Table 2.**  $V_{DD} = 2.5 \text{ V} \pm 0.2 \text{ V}$ ,  $GND = 0 \text{ V}$ , unless otherwise noted<sup>1</sup>

| Parameter  | +25°C | –40°C to +85°C | –40°C to +125°C        | Unit    | Test Conditions/Comments   |
|--|-------|----------------|------------------------|---------|--|
| ANALOG SWITCH  |       |                |                        |         |  |
| Analog Signal Range                                      |       |                | 0 V to V <sub>DD</sub> | V       |  |
| On Resistance (R <sub>ON</sub> )                         | 0.65  |                |                        | Ω typ   | V <sub>DD</sub> = 2.3 V, V <sub>S</sub> = 0 V to V <sub>DD</sub> , I <sub>S</sub> = 10 mA; |
|  | 0.72  | 0.8            | 0.88                   | Ω max   | Figure 18  |
| On Resistance Match between Channels (ΔR <sub>ON</sub> ) | 0.04  |                |                        | Ω typ   | V <sub>DD</sub> = 2.3 V; V <sub>S</sub> = 0.55 V, I <sub>S</sub> = 10 mA                   |
|  |       | 0.08           | 0.085                  | Ω max   |  |
| On Resistance Flatness (R <sub>FLAT(ON)</sub> )          | 0.16  |                |                        | Ω typ   | V <sub>DD</sub> = 2.3 V; V <sub>S</sub> = 0 V to V <sub>DD</sub> , I <sub>S</sub> = 10 mA  |
|  |       | 0.23           | 0.24                   | Ω max   |  |
| LEAKAGE CURRENTS   |       |                |                        |         |  |
| Source Off Leakage I <sub>S</sub> (OFF)                  | ±0.2  |                |                        | nA typ  | V <sub>DD</sub> = 2.7 V  |
|  | ±1    | ±6             | ±35                    | nA max  | V <sub>S</sub> = 0.6 V/2.4 V, V <sub>D</sub> = 2.4 V/0.6 V;                                |
| Drain Off Leakage I <sub>D</sub> (OFF)                   | ±0.2  |                |                        | nA typ  | Figure 19  |
|  | ±1    | ±6             | ±35                    | nA max  | V <sub>S</sub> = 0.6 V/2.4 V, V <sub>D</sub> = 2.4 V/0.6 V;                                |
| Channel On Leakage I <sub>D</sub> , I <sub>S</sub> (ON)  | ±0.2  |                |                        | nA typ  | Figure 19  |
|  | ±1    | ±11            | ±70                    | nA max  | V <sub>S</sub> = V <sub>D</sub> = 0.6 V or 2.4 V; Figure 20                                |
| DIGITAL INPUTS   |       |                |                        |         |  |
| Input High Voltage, V <sub>INH</sub>                     |       |                | 1.7                    | V min   |  |
| Input Low Voltage, V <sub>INL</sub>                      |       |                | 0.7                    | V max   |  |
| Input Current, I <sub>INL</sub> or I <sub>INH</sub>      | 0.005 |                |                        | μA typ  | V <sub>IN</sub> = V <sub>INL</sub> or V <sub>INH</sub>                                     |
|  |       |                | ±0.1                   | μA max  |  |
| C <sub>IN</sub> , Digital Input Capacitance              | 6     |                |                        | pF typ  |  |
| DYNAMIC CHARACTERISTICS <sup>2</sup>                     |       |                |                        |         |  |
| t <sub>ON</sub>  | 22    |                |                        | ns typ  | R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 35 pF  |
|  | 27    | 29             | 30                     | ns max  | V <sub>S</sub> = 1.5 V/ 0 V; Figure 21   |
| t <sub>OFF</sub>   | 4     |                |                        | ns typ  | R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 35 pF  |
|  | 6     | 7              | 8                      | ns max  | V <sub>S</sub> = 1.5 V; Figure 21  |
| Break-Before-Make Time Delay (t <sub>BBM</sub> )         | 18    |                |                        | ns typ  | R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 35 pF  |
| (ADG813 only)  |       |                | 5                      | ns min  | V <sub>S1</sub> = V <sub>S2</sub> = 1.5 V; Figure 22                                       |
| Charge Injection   | 25    |                |                        | pC typ  | V <sub>S</sub> = 1.25 V, R <sub>S</sub> = 0 Ω, C <sub>L</sub> = 1 nF;                      |
|  |       |                |                        |         | Figure 23  |
| Off Isolation  | –67   |                |                        | dB typ  | R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 100 kHz;                                 |
|  |       |                |                        |         | Figure 24  |
| Channel-to-Channel Crosstalk                             | –90   |                |                        | dB typ  | R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 100 kHz;                                 |
|  |       |                |                        |         | Figure 26  |
| Total Harmonic Distortion (THD + N)                      | 0.022 |                |                        | %       | R <sub>L</sub> = 32 Ω, f = 20 Hz to 20 kHz,  |
|  |       |                |                        |         | V <sub>S</sub> = 1.5 V p-p   |
| Insertion Loss   | –0.06 |                |                        | dB typ  | R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 100 kHz                                  |
| –3 dB Bandwidth  | 90    |                |                        | MHz typ | R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF; Figure 25                                    |
| C <sub>S</sub> (OFF)                                     | 32    |                |                        | pF typ  |  |
| C <sub>D</sub> (OFF)                                     | 37    |                |                        | pF typ  |  |
| C <sub>D</sub> , C <sub>S</sub> (ON)                     | 60    |                |                        | pF typ  |  |
| POWER REQUIREMENTS                                       |       |                |                        |         |  |
| I <sub>DD</sub>  | 0.003 |                |                        | μA typ  | V <sub>DD</sub> = 2.7 V  |
|  |       | 1.0            | 4                      | μA max  | Digital inputs = 0 V or 2.7 V  |

<sup>1</sup> Temperature range for the Y version is –40°C to +125°C.

<sup>2</sup> Guaranteed by design, not subject to production test.

**Table 3.**  $V_{DD} = 1.65\text{ V to }1.95\text{ V}$ ,  $GND = 0\text{ V}$ , unless otherwise noted<sup>1</sup>

| Parameter  | +25°C     | –40°C to +85°C | –40°C to +125°C | Unit              | Test Conditions/Comments   |
|--|-----------|----------------|-----------------|-------------------|--|
| <b>ANALOG SWITCH</b>                                     |           |                |                 |                   |  |
| Analog Signal Range                                      |           |                | 0 V to $V_{DD}$ | V                 |  |
| On Resistance ( $R_{ON}$ )                               | 1         |                |                 | $\Omega$ typ      | $V_{DD} = 1.8\text{ V}$ , $V_S = 0\text{ V to }V_{DD}$ , $I_S = 10\text{ mA}$ ;<br>Figure 18 |
|  | 1.4       | 2.2            | 2.2             | $\Omega$ max      |  |
|  | 2.5       | 4              | 4               | $\Omega$ max      | $V_{DD} = 1.65\text{ V}$ , $V_S = 0\text{ V to }V_{DD}$ , $I_S = 10\text{ mA}$               |
| On Resistance Match between Channels ( $\Delta R_{ON}$ ) | 0.1       |                |                 | $\Omega$ typ      | $V_{DD} = 1.65\text{ V}$ , $V_S = 0.7\text{ V}$ , $I_S = 10\text{ mA}$                       |
| <b>LEAKAGE CURRENTS</b>                                  |           |                |                 |                   |  |
| Source Off Leakage $I_S$ (OFF)                           | $\pm 0.2$ |                |                 | nA typ            | $V_{DD} = 1.95\text{ V}$   |
|  | $\pm 1$   | $\pm 5$        | $\pm 30$        | nA max            | $V_S = 0.6\text{ V}/1.65\text{ V}$ , $V_D = 1.65\text{ V}/0.6\text{ V}$ ;<br>Figure 19       |
| Drain Off Leakage $I_D$ (OFF)                            | $\pm 0.2$ |                |                 | nA typ            | $V_S = 0.6\text{ V}/1.65\text{ V}$ , $V_D = 1.65\text{ V}/0.6\text{ V}$ ;                    |
|  | $\pm 1$   | $\pm 5$        | $\pm 30$        | nA max            | Figure 19  |
| Channel On Leakage $I_D$ , $I_S$ (ON)                    | $\pm 0.2$ |                |                 | nA typ            | $V_S = V_D = 0.6\text{ V or }1.65\text{ V}$ ; Figure 20                                      |
|  | $\pm 1$   | $\pm 9$        | $\pm 60$        | nA max            |  |
| <b>DIGITAL INPUTS</b>                                    |           |                |                 |                   |  |
| Input High Voltage, $V_{INH}$                            |           |                | $0.65V_{DD}$    | V min             |  |
| Input Low Voltage, $V_{INL}$                             |           |                | $0.35V_{DD}$    | V max             |  |
| Input Current, $I_{INL}$ or $I_{INH}$                    | 0.005     |                |                 | $\mu\text{A typ}$ | $V_{IN} = V_{INL}$ or $V_{INH}$  |
|  |           |                | $\pm 0.1$       | $\mu\text{A max}$ |  |
| CIN, Digital Input Capacitance                           | 6         |                |                 | pF typ            |  |
| <b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>               |           |                |                 |                   |  |
| $t_{ON}$   | 27        |                |                 | ns typ            | $R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$  |
|  | 35        | 36             | 37              | ns max            | $V_S = 1.5\text{ V}/0\text{ V}$ ; Figure 21  |
| $t_{OFF}$  | 6         |                |                 | ns typ            | $R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$  |
|  | 8         | 9              | 10              | ns max            | $V_S = 1.5\text{ V}$ ; Figure 21   |
| Break-Before-Make Time Delay ( $t_{BBM}$ )               | 20        |                |                 | ns typ            | $R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$  |
| (ADG813 only)  |           |                | 5               | ns min            | $V_{S1} = V_{S2} = 1\text{ V}$ ; Figure 22   |
| Charge Injection   | 15        |                |                 | pC typ            | $V_S = 1\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ;<br>Figure 23                  |
| Off Isolation  | –67       |                |                 | dB typ            | $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 100\text{ kHz}$ ;<br>Figure 24               |
| Channel-to-Channel Crosstalk                             | –90       |                |                 | dB typ            | $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 100\text{ kHz}$ ;<br>Figure 26               |
| Total Harmonic Distortion (THD + N)                      | 0.14      |                |                 | %                 | $R_L = 32\ \Omega$ , $f = 20\text{ Hz to }20\text{ kHz}$ ,<br>$V_S = 1.2\text{ V p-p}$       |
| Insertion Loss   | –0.08     |                |                 | dB typ            | $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 100\text{ kHz}$                              |
| –3 dB Bandwidth  | 90        |                |                 | MHz typ           | $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; Figure 25   |
| $C_S$ (OFF)  | 32        |                |                 | pF typ            |  |
| $C_D$ (OFF)  | 38        |                |                 | pF typ            |  |
| $C_D$ , $C_S$ (ON)                                       | 60        |                |                 | pF typ            |  |
| <b>POWER REQUIREMENTS</b>                                |           |                |                 |                   |  |
| $I_{DD}$   | 0.003     |                |                 | $\mu\text{A typ}$ | $V_{DD} = 1.95\text{ V}$   |
|  |           | 1.0            | 4               | $\mu\text{A max}$ | Digital inputs = 0 V or 1.95 V   |

<sup>1</sup>Temperature range for the Y version is –40°C to +125°C.

<sup>2</sup>Guaranteed by design, not subject to production test.

## ABSOLUTE MAXIMUM RATINGS

Table 4.  $T_A = 25^\circ\text{C}$ , unless otherwise noted

| Parameter  | Rating  |
|--|---|
| $V_{DD}$ to GND                                    | $-0.3\text{ V to }+4.6\text{ V}$                      |
| Analog Inputs <sup>1</sup>                         | $-0.3\text{ V to }V_{DD} + 0.3\text{ V}$              |
| Digital Inputs <sup>1</sup>                        | GND – 0.3 V to 4.6 V or 10 mA, whichever occurs first |
| Peak Current, S or D                               | (Pulsed at 1 ms, 10% Duty Cycle Max)                  |
| 3.3 V Operation                                    | 500 mA  |
| 2.5 V Operation                                    | 460 mA  |
| 1.8 V Operation                                    | 420 mA  |
| Continuous Current, S or D                         |   |
| 3.3 V Operation                                    | 300 mA  |
| 2.5 V Operation                                    | 275 mA  |
| 1.8 V Operation                                    | 250 mA  |
| Operating Temperature Range Automotive (Y Version) | $-40^\circ\text{C to }+125^\circ\text{C}$             |
| Storage Temperature Range                          | $-65^\circ\text{C to }+150^\circ\text{C}$             |
| Junction Temperature                               | $150^\circ\text{C}$                                   |
| TSSOP Package                                      |   |
| $\theta_{JA}$ Thermal Impedance                    | $150^\circ\text{C/W}$                                 |
| $\theta_{JC}$ Thermal Impedance                    | $27^\circ\text{C/W}$                                  |
| IR Reflow, Peak Temperature <20 sec                | $235^\circ\text{C}$                                   |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

<sup>1</sup> Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Table 5. ADG811/ADG812 Truth Table

| ADG811 IN | ADG812 IN | Switch Condition |
|-----------|-----------|------------------|
| 0         | 1         | On               |
| 1         | 0         | Off              |

Table 6. ADG813 Truth Table

| Logic | Switch 1, Switch 4 | Switch 2, Switch 3 |
|-------|--------------------|--------------------|
| 0     | Off                | On                 |
| 1     | On                 | Off                |

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

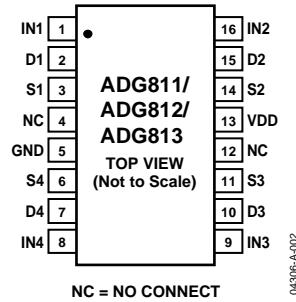


Figure 2.

Table 7. Terminology

| Term                | Definition   |
|---------------------|--|
| $V_{DD}$            | Most positive power supply potential.  |
| $I_{DD}$            | Positive supply current.   |
| GND                 | Ground (0 V) reference.  |
| S                   | Source terminal. May be an input or output.  |
| D                   | Drain terminal. May be an input or output.   |
| IN                  | Logic control input.   |
| $V_D, V_S$          | Analog voltage on Terminals D, S.  |
| $R_{ON}$            | Ohmic resistance between D and S.  |
| $R_{FLAT} (ON)$     | Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range. |
| $\Delta R_{ON}$     | On resistance match between any two channels, i.e., $R_{ON\ max} - R_{ON\ min}$ .  |
| $I_S (OFF)$         | Source leakage current with the switch off.  |
| $I_D (OFF)$         | Drain leakage current with the switch off.   |
| $I_D, I_S (ON)$     | Channel leakage current with the switch on.  |
| $V_{INL}$           | Maximum input voltage for Logic 0.   |
| $V_{INH}$           | Minimum input voltage for Logic 1.   |
| $I_{INL} (I_{INH})$ | Input current of the digital input.  |
| $C_S (OFF)$         | Off switch source capacitance. Measured with reference to ground.  |
| $C_D (OFF)$         | Off switch drain capacitance. Measured with reference to ground.   |
| $C_D, C_S (ON)$     | On switch capacitance. Measured with reference to ground.  |
| $C_{IN}$            | Digital input capacitance.   |
| $t_{ON}$            | Delay time between the 50% and the 90% points of the digital input and switch on condition.  |
| $t_{OFF}$           | Delay time between the 50% and the 90% points of the digital input and switch off condition.   |
| $t_{BBM}$           | On or off time measured between the 80% points of both switches, when switching from one to another.   |
| Charge Injection    | A measure of the glitch impulse transferred from the digital input to the analog output during on-to-off switching.                              |
| Off Isolation       | A measure of unwanted signal coupling through an off switch.   |
| Crosstalk           | A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.                           |
| -3 dB Bandwidth     | The frequency at which the output is attenuated by 3 dB.   |
| On Response         | The frequency response of the on switch.   |
| Insertion Loss      | The loss due to the on resistance of the switch.   |
| THD + N             | The ratio of the harmonic amplitudes plus noise of a signal to the fundamental.  |

## TYPICAL PERFORMANCE CHARACTERISTICS

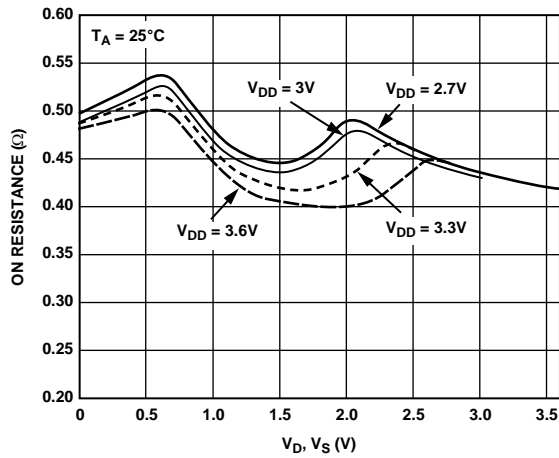


Figure 3. On Resistance vs.  $V_D$  ( $V_S$ ),  $V_{DD} = 2.7$  V to 3.6 V

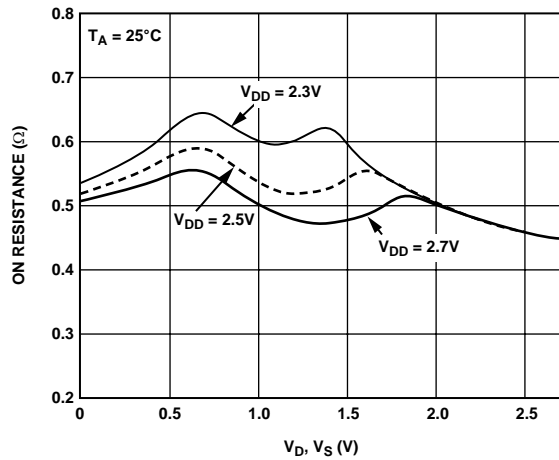


Figure 4. On Resistance vs.  $V_D$  ( $V_S$ ),  $V_{DD} = 2.5$  V  $\pm$  0.2 V

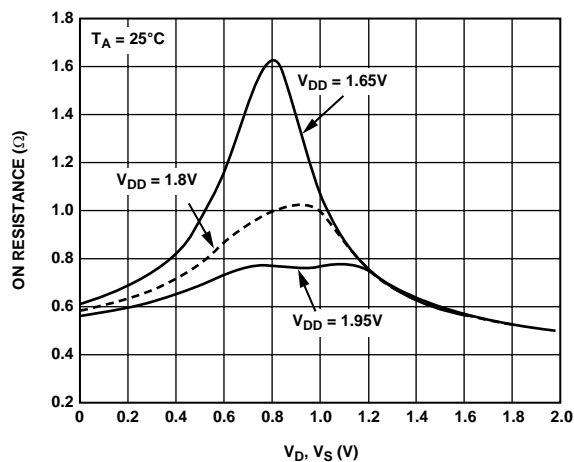


Figure 5. On Resistance vs.  $V_D$  ( $V_S$ ),  $V_{DD} = 1.8$  V  $\pm$  0.15 V

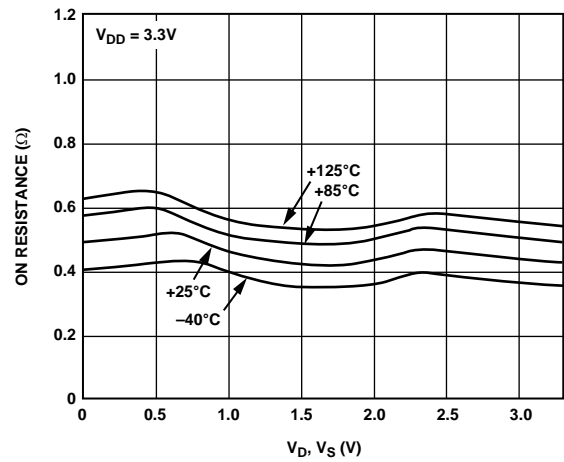


Figure 6. On Resistance vs.  $V_D$  ( $V_S$ ) for Different Temperatures,  $V_{DD} = 3.3$  V

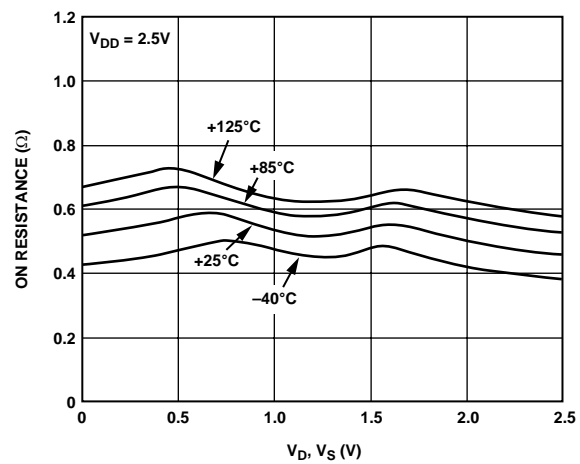


Figure 7. On Resistance vs.  $V_D$  ( $V_S$ ) for Different Temperatures,  $V_{DD} = 2.5$  V

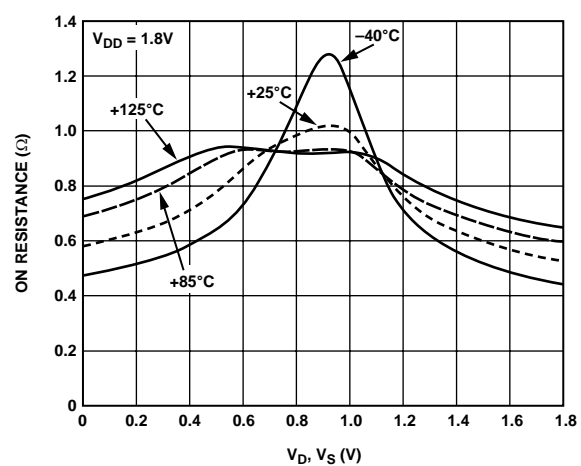


Figure 8. On Resistance vs.  $V_D$  ( $V_S$ ) for Different Temperatures,  $V_{DD} = 1.8$  V



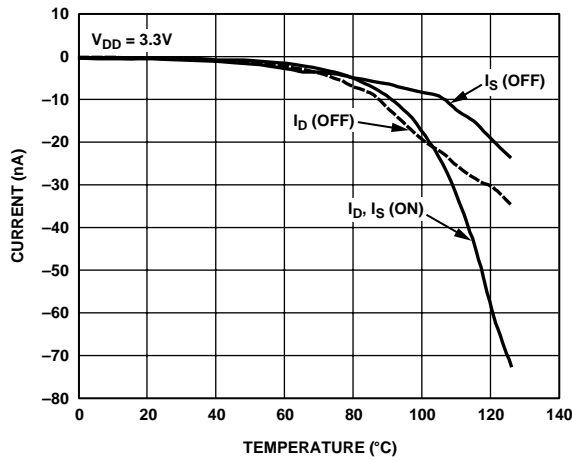


Figure 9. Leakage Currents vs. Temperature,  $V_{DD} = 3.3V$

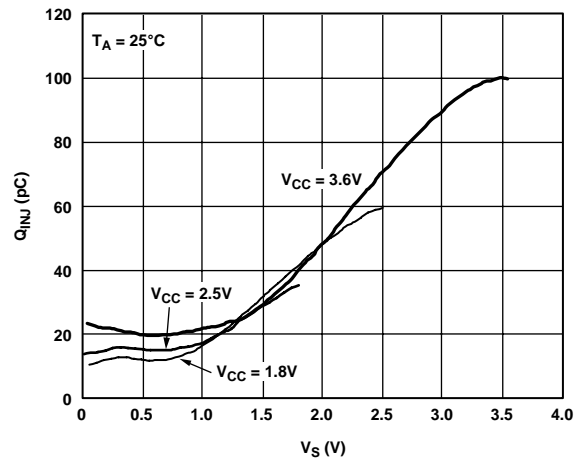


Figure 12. Charge Injection vs. Source Voltage

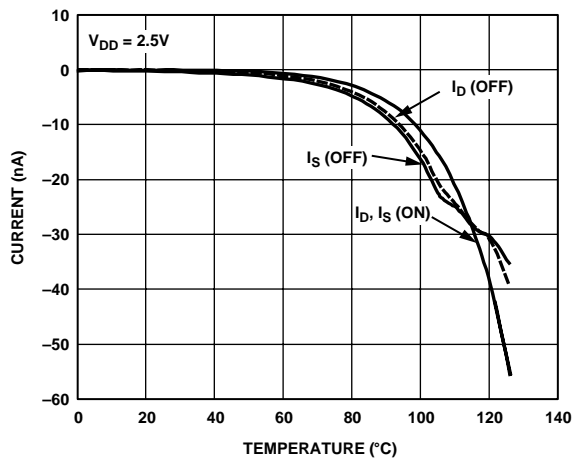


Figure 10. Leakage Currents vs. Temperature,  $V_{DD} = 2.5V$

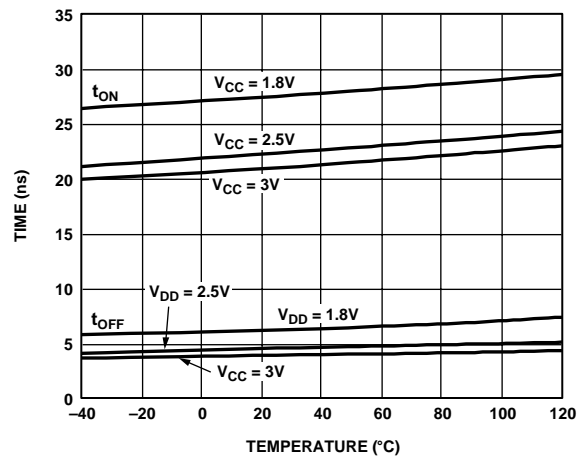


Figure 13.  $t_{ON}/t_{OFF}$  Times vs. Temperature

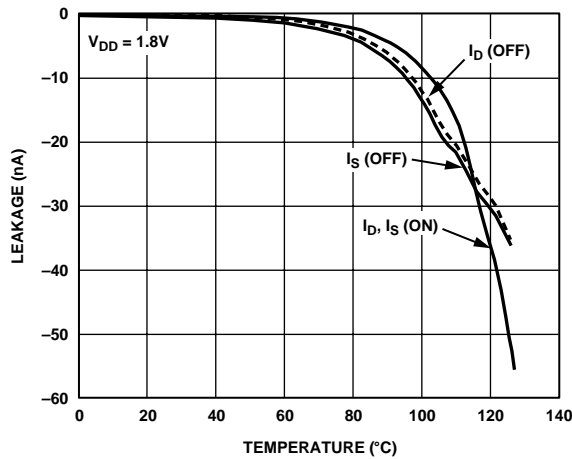


Figure 11. Leakage Currents vs. Temperature,  $V_{DD} = 1.8V$

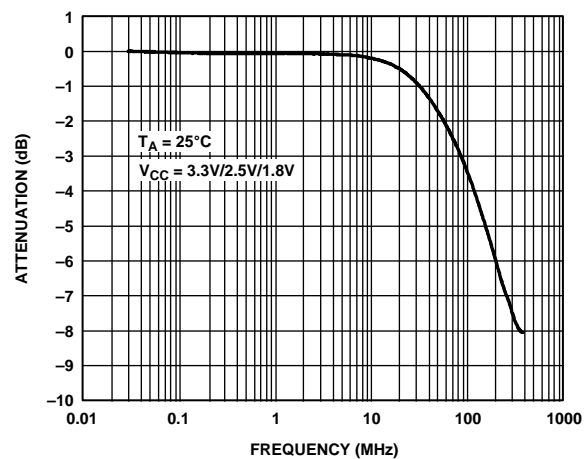


Figure 14. Bandwidth

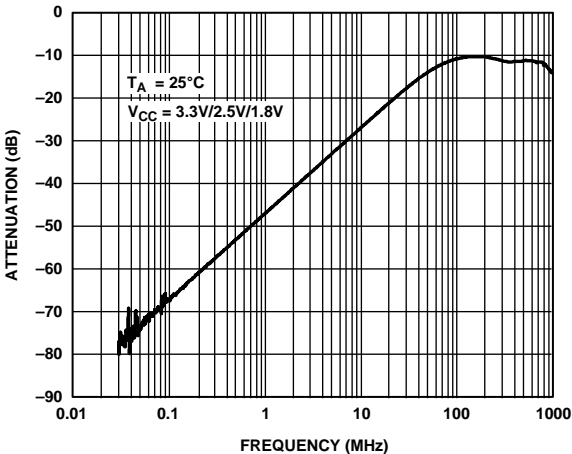


Figure 15. Crosstalk vs. Frequency

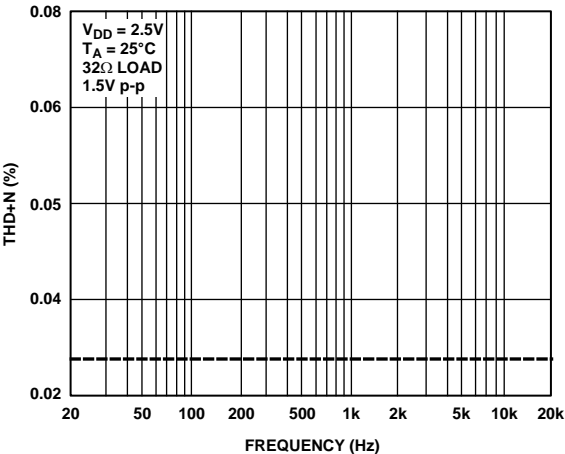


Figure 17. Total Harmonic Distortion

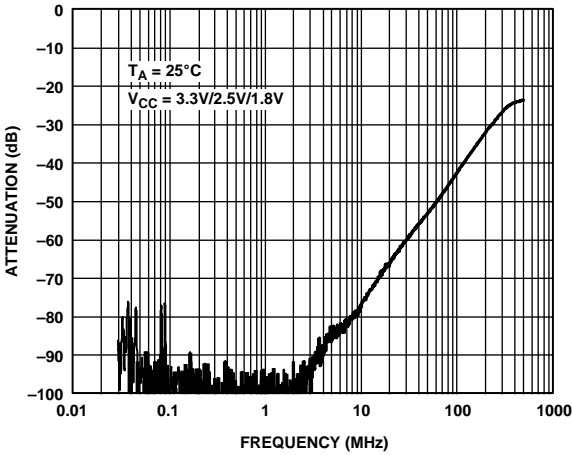


Figure 16. Off Isolation vs. Frequency

## TEST CIRCUITS

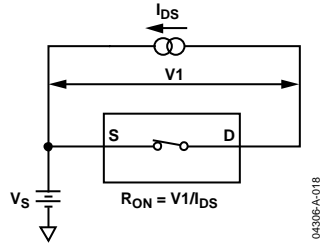


Figure 18. On Resistance

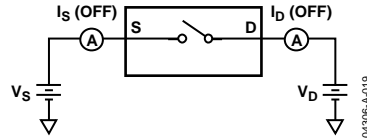


Figure 19. Off Leakage

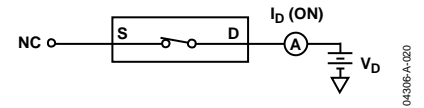


Figure 20. On Leakage

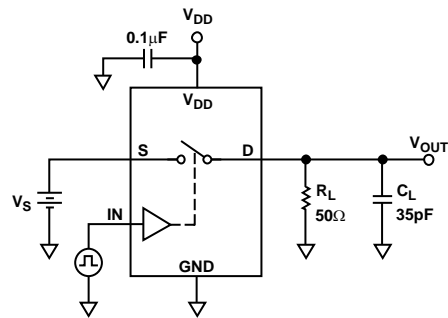


Figure 21. Switching Times

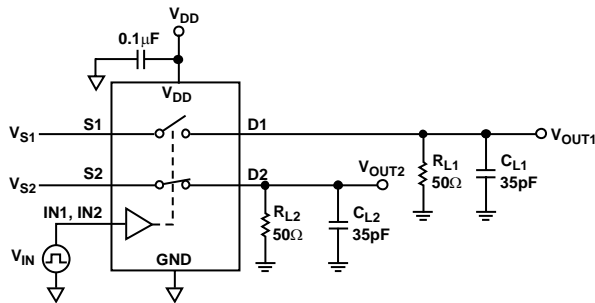
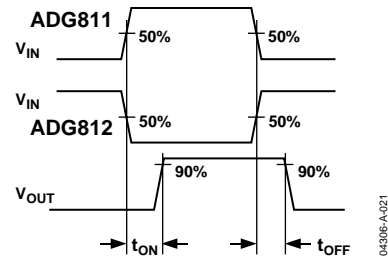


Figure 22. Break-Before-Make Time Delay,  $t_{BBM}$  (ADG813)

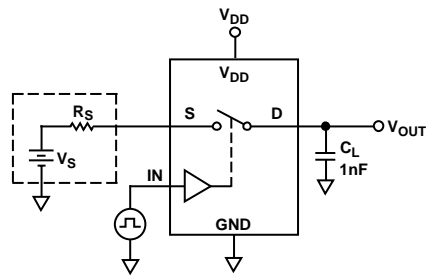
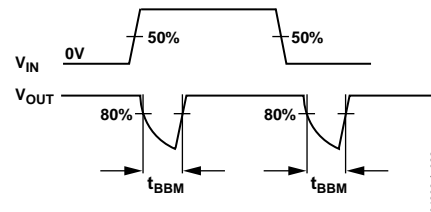
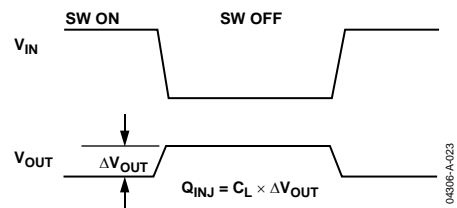


Figure 23. Charge Injection



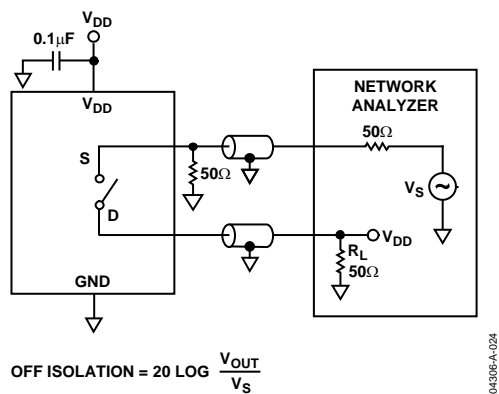


Figure 24. Off Isolation

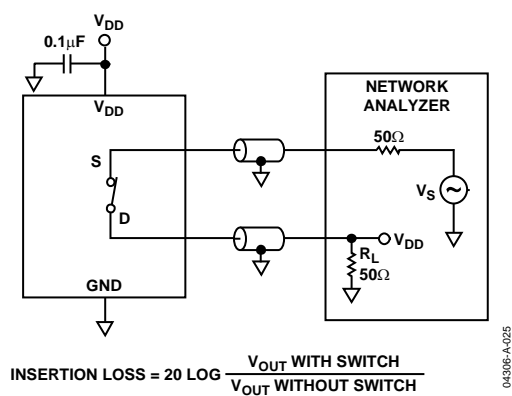


Figure 25. Bandwidth

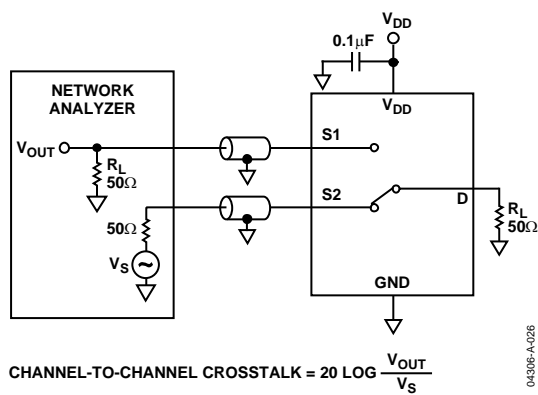


Figure 26. Channel-to-Channel Crosstalk



**NOTES**

## **NOTES**

## **NOTES**