

## OP-470

### FEATURES

- Very Low Noise .....  $5\text{nV}/\sqrt{\text{Hz}}$  @ 1kHz Max
- Excellent Input Offset Voltage ..... 0.4mV Max
- Low Offset Voltage Drift .....  $2\mu\text{V}/^\circ\text{C}$  Max
- Very High Gain ..... 1000V/mV Min
- Outstanding CMR ..... 110dB Min
- Slow Rate .....  $2\text{V}/\mu\text{s}$  Typ
- Gain-Bandwidth Product ..... 6MHz Typ
- Industry Standard Quad Pinouts
- Available in Die Form

### ORDERING INFORMATION †

$T_A = +25^\circ\text{C}$ $V_{OS}$ MAX ( $\mu\text{V}$ )	PACKAGE			OPERATING TEMPERATURE RANGE
	CERDIP 14-PIN	PLASTIC	LCC*	
400	-	-	OP470ARC/883	MIL
400	OP470AY*	-	OP470ATC/883	MIL
400	OP470EY	-	-	IND
800	OP470FY	-	-	IND
1000	-	OP470GP	-	XIND
1000	-	OP470GS††	-	XIND

\* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

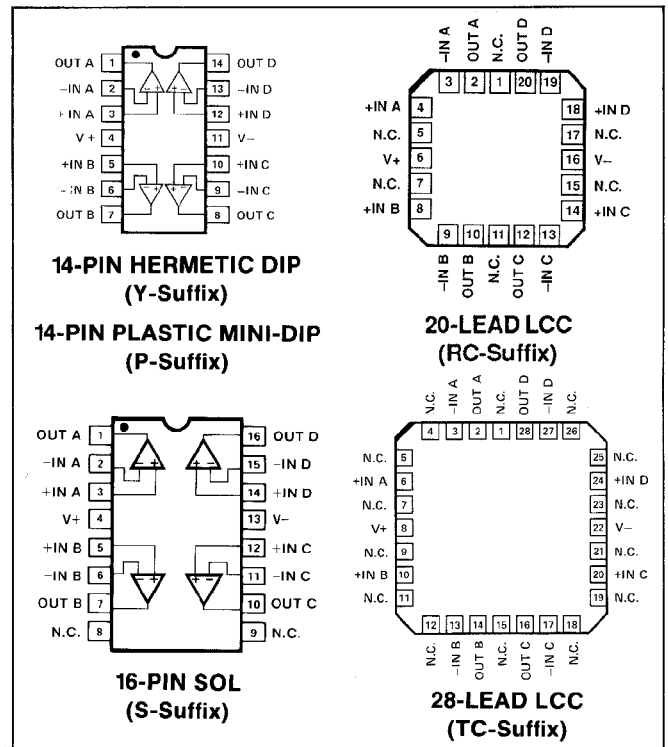
### GENERAL DESCRIPTION

The OP-470 is a high-performance monolithic quad operational amplifier with exceptionally low voltage noise,  $5\text{nV}/\sqrt{\text{Hz}}$  at 1kHz Max, offering comparable performance to PMI's industry standard OP-27.

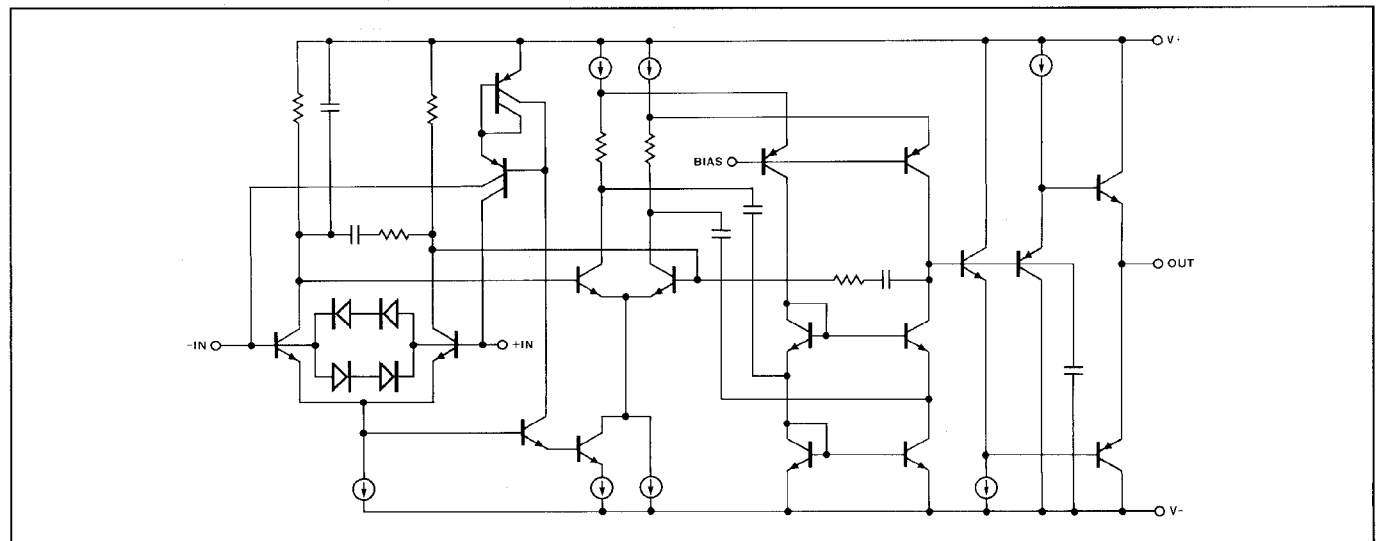
The OP-470 features an input offset voltage below 0.4mV, excellent for a quad op amp, and an offset drift under  $2\mu\text{V}/^\circ\text{C}$ , guaranteed over the full military temperature range. Open-loop gain of the OP-470 is over 1,000,000 into a  $10\text{k}\Omega$  load

insuring excellent gain accuracy and linearity, even in high-gain applications. Input bias current is under 25nA which reduces errors due to signal source resistance. The OP-470's CMR of over 110dB and PSRR of less than  $1.8\mu\text{V}/\text{V}$  significantly reduce errors due to ground noise and power supply fluctuations. Power consumption of the quad OP-470 is half that of four OP-27s, a significant advantage for power con-

### PIN CONNECTIONS



### SIMPLIFIED SCHEMATIC



# OP-470

scious applications. The OP-470 is unity-gain stable with a gain-bandwidth product of 6MHz and a slew rate of 2V/ $\mu$ s.

The OP-470 offers excellent amplifier matching which is important for applications such as multiple gain blocks, low-noise instrumentation amplifiers, quad buffers, and low-noise active filters.

The OP-470 conforms to the industry standard 14-pin DIP pinout. It is pin compatible with the OP-11, LM148/149, HA4741, HA5104, and RM4156 quad op amps and can be used to upgrade systems using these devices.

For higher speed applications the OP-471, with a slew rate of 8V/ $\mu$ s, is recommended.

## ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage	$\pm 18V$
Differential Input Voltage (Note 2)	$\pm 1.0V$
Differential Input Current (Note 2)	$\pm 25mA$
Input Voltage	Supply Voltage
Output Short-Circuit Duration	Continuous
Storage Temperature Range	
P, TC, Y-Package	$-65^{\circ}C$ to $+150^{\circ}C$

Lead Temperature Range (Soldering, 60 sec)	$300^{\circ}C$
Junction Temperature ( $T_j$ )	$-65^{\circ}C$ to $+150^{\circ}C$
Operating Temperature Range	
OP-470A	$-55^{\circ}C$ to $+125^{\circ}C$
OP-470E, OP-470F	$-25^{\circ}C$ to $+85^{\circ}C$
OP-470G	$-40^{\circ}C$ to $+85^{\circ}C$

PACKAGE TYPE	$\theta_{JA}$ (Note 3)	$\theta_{JC}$	UNITS
14-Pin Hermetic DIP (Y)	94	10	$^{\circ}C/W$
14-Pin Plastic DIP (P)	76	33	$^{\circ}C/W$
20-Contact LCC (RC)	78	30	$^{\circ}C/W$
28-Contact LCC (TC)	70	28	$^{\circ}C/W$
16-Pin SOL (S)	88	23	$^{\circ}C/W$

### NOTES:

- Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
- The OP-470's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise performance. If differential voltage exceeds  $\pm 1.0V$ , the input current should be limited to  $\pm 25mA$ .
- $\theta_{JA}$  is specified for worst case mounting conditions, i.e.,  $\theta_{JA}$  is specified for device in socket for TO, CerDIP, P-DIP, and LCC packages;  $\theta_{JA}$  is specified for device soldered to printed circuit board for SO and PLCC packages.

## ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ , $T_A = 25^{\circ}C$ , unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-470A/E			OP-470F			OP-470G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$V_{OS}$		—	0.1	0.4	—	0.2	0.8	—	0.4	1.0	mV
Input Offset Current	$I_{OS}$	$V_{CM} = 0V$	—	3	10	—	6	20	—	12	30	nA
Input Bias Current	$I_B$	$V_{CM} = 0V$	—	6	25	—	15	50	—	25	60	nA
Input Noise Voltage	$e_{np-p}$	0.1Hz to 10Hz (Note 1)	—	80	200	—	80	200	—	80	200	nV <sub>p-p</sub>
Input Noise Voltage Density	$e_n$	$f_O = 10Hz$	—	3.8	6.5	—	3.8	6.5	—	3.8	6.5	nV/ $\sqrt{Hz}$
		$f_O = 100Hz$	—	3.3	5.5	—	3.3	5.5	—	3.3	5.5	
		$f_O = 1kHz$ (Note 2)	—	3.2	5.0	—	3.2	5.0	—	3.2	5.0	
Input Noise Current Density	$i_n$	$f_O = 10Hz$	—	1.7	—	—	1.7	—	—	1.7	—	pA/ $\sqrt{Hz}$
		$f_O = 100Hz$	—	0.7	—	—	0.7	—	—	0.7	—	
		$f_O = 1kHz$	—	0.4	—	—	0.4	—	—	0.4	—	
Large-Signal Voltage Gain	$A_{VO}$	$V_O = \pm 10V$										V/mV
		$R_L = 10k\Omega$	1000	2300	—	800	1700	—	800	1700	—	
		$R_L = 2k\Omega$	500	1200	—	400	900	—	400	900	—	
Input Voltage Range	IVR	(Note 3)	$\pm 11$	$\pm 12$	—	$\pm 11$	$\pm 12$	—	$\pm 11$	$\pm 12$	—	V
Output Voltage Swing	$V_O$	$R_L \geq 2k\Omega$	$\pm 12$	$\pm 13$	—	$\pm 12$	$\pm 13$	—	$\pm 12$	$\pm 13$	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	110	125	—	100	120	—	100	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	0.56	1.8	—	1.0	5.6	—	1.0	5.6	$\mu V/V$
Slew Rate	SR		1.4	2	—	1.4	2	—	1.4	2	—	V/ $\mu s$

**ELECTRICAL CHARACTERISTICS** at  $V_S = \pm 15V$ ,  $T_A = 25^\circ C$ , unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-470A/E			OP-470F			OP-470G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Supply Current (All Amplifiers)	$I_{SY}$	No Load	—	9	11	—	9	11	—	9	11	mA
Gain Bandwidth Product	GBW	$A_V = +10$	—	6	—	—	6	—	—	6	—	MHz
Channel Separation	CS	$V_O = 20V_{p-p}$ $f_O = 10Hz$ (Note 1)	125	155	—	125	155	—	125	155	—	dB
Input Capacitance	$C_{IN}$		—	2	—	—	2	—	—	2	—	pF
Input Resistance Differential-Mode	$R_{IN}$		—	0.4	—	—	0.4	—	—	0.4	—	M $\Omega$
Input Resistance Common-Mode	$R_{INCM}$		—	11	—	—	11	—	—	11	—	G $\Omega$
Settling Time	$t_s$	$A_V = +1$ to 0.1%	—	5.5	—	—	5.5	—	—	5.5	—	$\mu s$
		to 0.01%	—	6.0	—	—	6.0	—	—	6.0	—	

**NOTES:**

1. Guaranteed but not 100% tested.
2. Sample tested.
3. Guaranteed by CMR test.

**ELECTRICAL CHARACTERISTICS** at  $V_S = \pm 15V$ ,  $-55^\circ C \leq T_A \leq 125^\circ C$  for OP-470A, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-470A			UNITS
			MIN	TYP	MAX	
Input Offset Voltage	$V_{OS}$		—	0.14	0.6	mV
Average Input Offset Voltage Drift	$TCV_{OS}$		—	0.4	2	$\mu V/^\circ C$
Input Offset Current	$I_{OS}$	$V_{CM} = 0V$	—	5	20	nA
Input Bias Current	$I_B$	$V_{CM} = 0V$	—	15	50	nA
Large-Signal Voltage Gain	$A_{VO}$	$V_O = \pm 10V$ $R_L = 10k\Omega$	750	1600	—	V/mV
		$R_L = 2k\Omega$	400	800	—	
Input Voltage Range	IVR	(Note 1)	$\pm 11$	$\pm 12$	—	V
Output Voltage Swing	$V_O$	$R_L \geq 2k\Omega$	$\pm 12$	$\pm 13$	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	100	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	1.0	5.6	$\mu V/V$
Supply Current (All Amplifiers)	$I_{SY}$	No Load	—	9.2	11	mA

**NOTE:**

1. Guaranteed by CMR test.

# OP-470

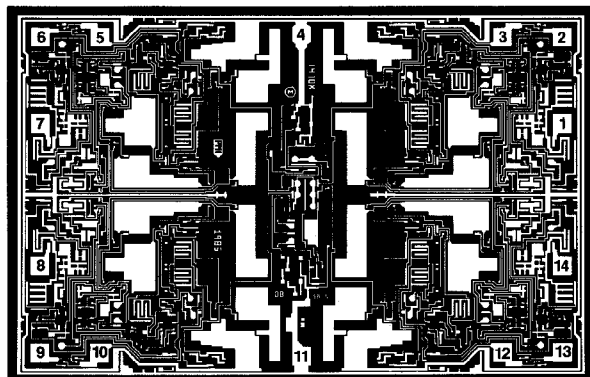
**ELECTRICAL CHARACTERISTICS** at  $V_S = \pm 15V$ ,  $-25^\circ C \leq T_A \leq +85^\circ C$  for OP-470E/F,  $-40^\circ C \leq T_A \leq +85^\circ C$  for OP-470G, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-470E			OP-470F			OP-470G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$V_{OS}$		—	0.12	0.5	—	0.24	1.0	—	0.5	1.5	mV
Average Input Offset Voltage Drift	$TCV_{OS}$		—	0.4	2	—	0.6	4	—	2	—	$\mu V/^\circ C$
Input Offset Current	$I_{OS}$	$V_{CM} = 0V$	—	4	20	—	7	40	—	20	50	nA
Input Bias Current	$I_B$	$V_{CM} = 0V$	—	11	50	—	20	70	—	40	75	nA
Large-Signal Voltage Gain	$A_{VO}$	$V_O = \pm 10V$	800	1800	—	600	1400	—	600	1500	—	V/mV
		$R_L = 10k\Omega$ $R_L = 2k\Omega$	400	900	—	300	700	—	300	800	—	
Input Voltage Range	IVR	(Note 1)	$\pm 11$	$\pm 12$	—	$\pm 11$	$\pm 12$	—	$\pm 11$	$\pm 12$	—	V
Output Voltage Swing	$V_O$	$R_L \geq 2k\Omega$	$\pm 12$	$\pm 13$	—	$\pm 12$	$\pm 13$	—	$\pm 12$	$\pm 13$	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	100	120	—	90	115	—	90	110	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	0.7	5.6	—	1.8	10	—	1.8	10	$\mu V/V$
Supply Current (All Amplifiers)	$I_{SY}$	No Load	—	9.2	11	—	9.2	11	—	9.3	11	mA

**NOTE:**

1. Guaranteed by CMR test.

DICE CHARACTERISTICS



- 1. OUT A
- 2. -IN A
- 3. +IN A
- 4. V+
- 5. +IN B
- 6. -IN B
- 7. OUT B
- 8. OUT C
- 9. -IN C
- 10. +IN C
- 11. V-
- 12. +IN D
- 13. -IN D
- 14. OUT D

DIE SIZE 0.163 × 0.106 inch, 17,278 sq. mils  
(4.14 × 2.69 mm, 11.14 sq. mm)

WAFER TEST LIMITS at  $V_S = \pm 15V$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-470GBC LIMIT	UNITS
Input Offset Voltage	$V_{OS}$		0.8	mV MAX
Input Offset Current	$I_{OS}$	$V_{CM} = 0V$	20	nA MAX
Input Bias Current	$I_B$	$V_{CM} = 0V$	50	nA MAX
Large-Signal Voltage Gain	$A_{VO}$	$V_O = \pm 10V$	800	V/mV MIN
		$R_L = 10k\Omega$ $R_L = 2k\Omega$	400	
Input Voltage Range	IVR	(Note 1)	$\pm 11$	V MIN
Output Voltage Swing	$V_O$	$R_L \geq 2k\Omega$	$\pm 12$	V MIN
Common Mode Rejection	CMR	$V_{CM} = \pm 11V$	100	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	5.6	$\mu V/V$ MAX
Slew Rate	SR		1.4	V/ $\mu s$ MIN
Supply Current (All Amplifiers)	$I_{SY}$	No Load	11	mA MAX

NOTE:

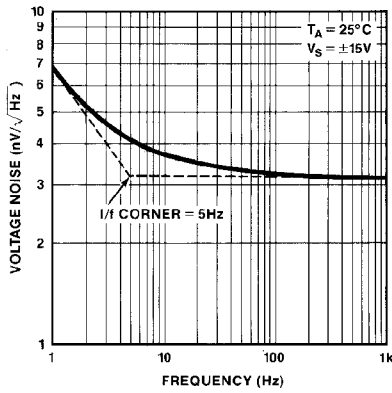
- 1. Guaranteed by CMR test.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

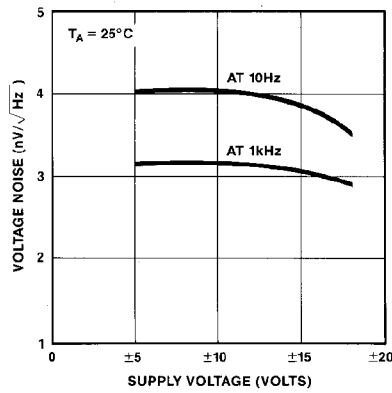
# OP-470

## TYPICAL PERFORMANCE CHARACTERISTICS

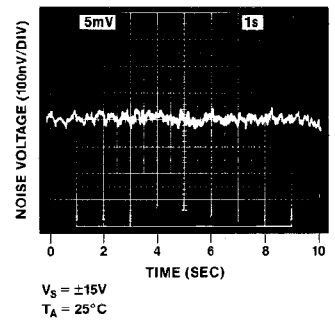
**VOLTAGE NOISE DENSITY vs FREQUENCY**



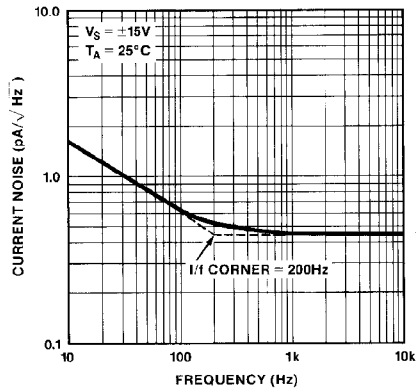
**VOLTAGE NOISE DENSITY vs SUPPLY VOLTAGE**



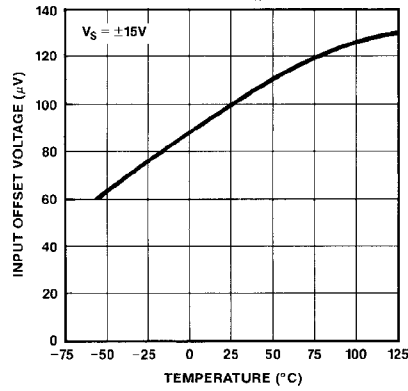
**0.1Hz TO 10Hz NOISE**



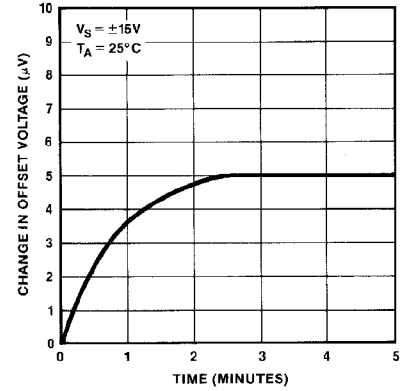
**CURRENT NOISE DENSITY vs FREQUENCY**



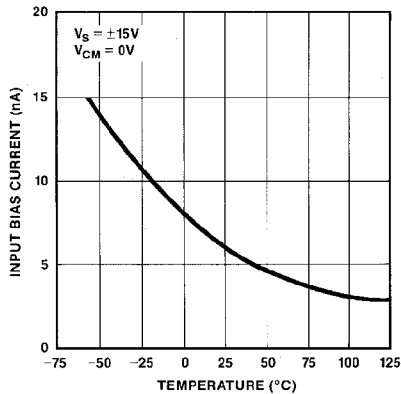
**INPUT OFFSET VOLTAGE vs TEMPERATURE**



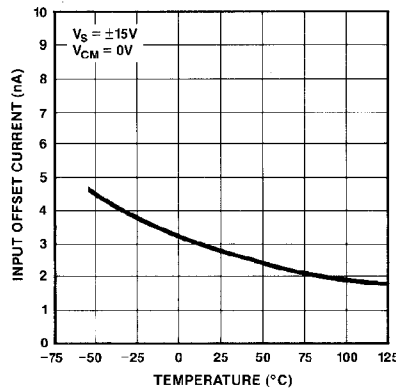
**WARM-UP OFFSET VOLTAGE DRIFT**



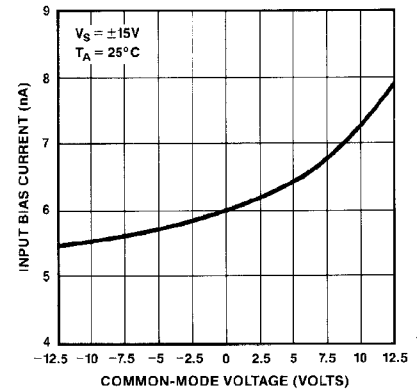
**INPUT BIAS CURRENT vs TEMPERATURE**



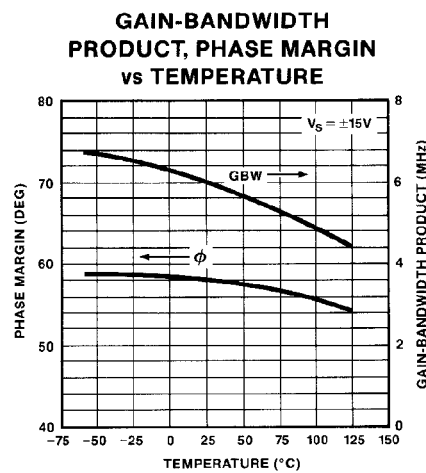
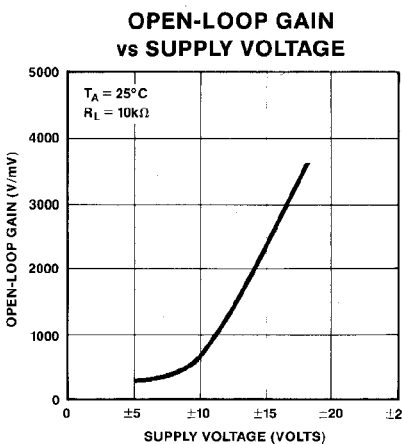
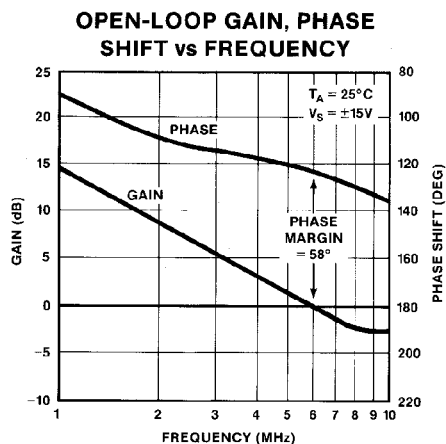
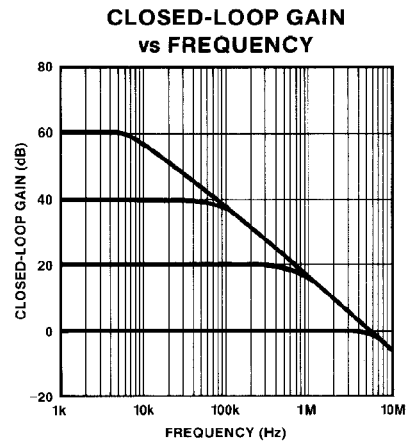
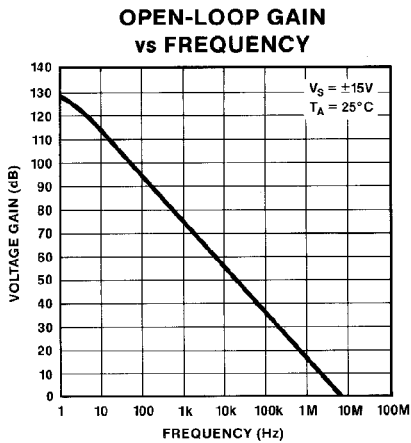
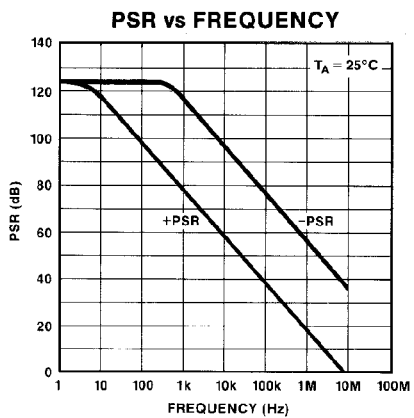
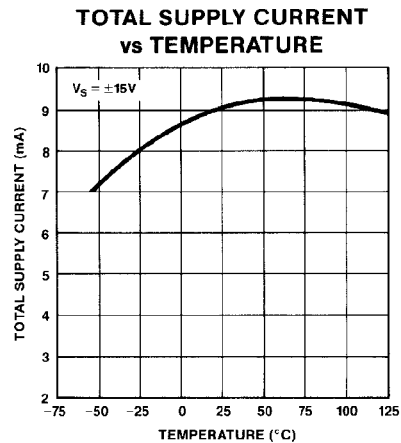
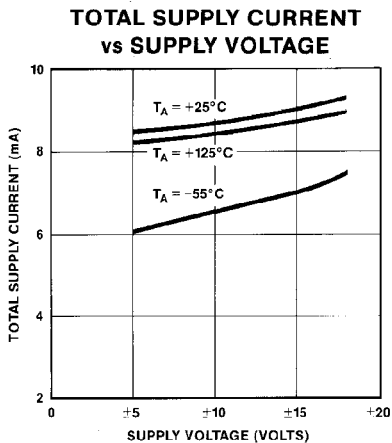
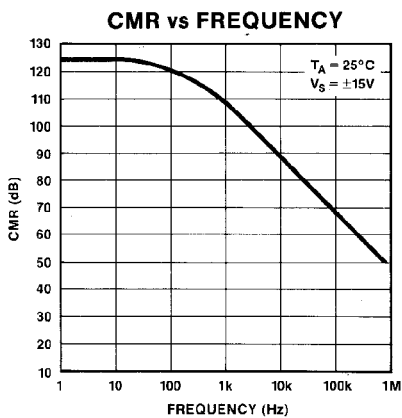
**INPUT OFFSET CURRENT vs TEMPERATURE**



**INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE**



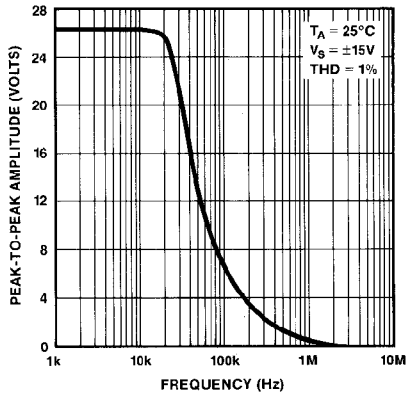
TYPICAL PERFORMANCE CHARACTERISTICS



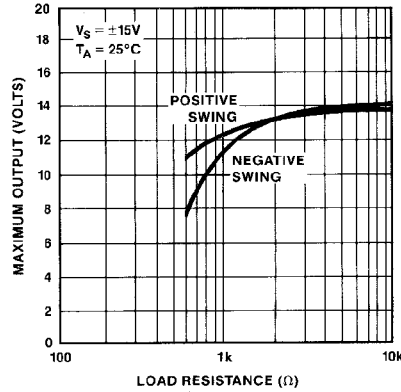
# OP-470

## TYPICAL PERFORMANCE CHARACTERISTICS

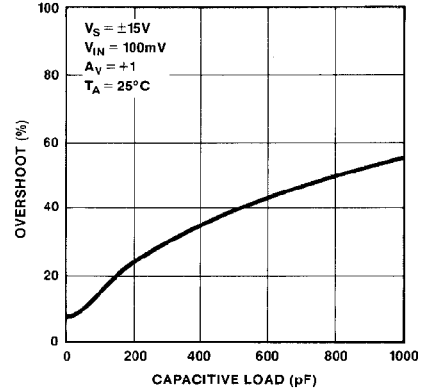
**MAXIMUM OUTPUT SWING vs FREQUENCY**



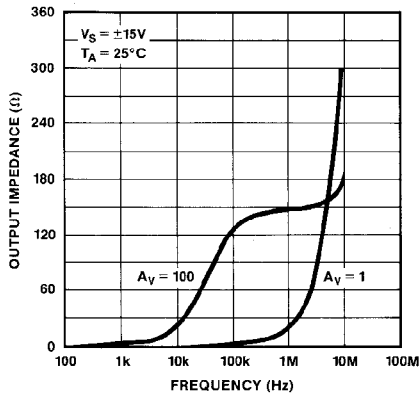
**MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE**



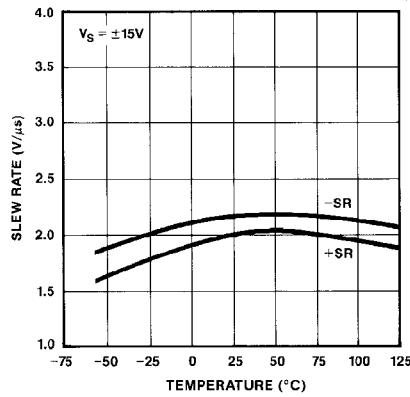
**SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD**



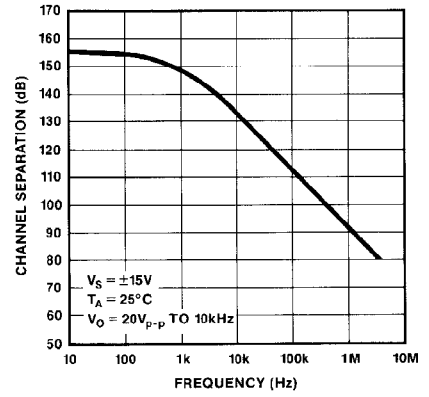
**OUTPUT IMPEDANCE vs FREQUENCY**



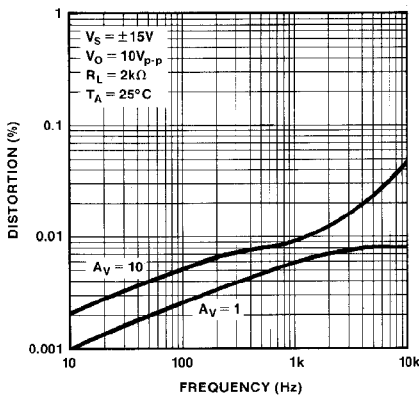
**SLEW RATE vs TEMPERATURE**



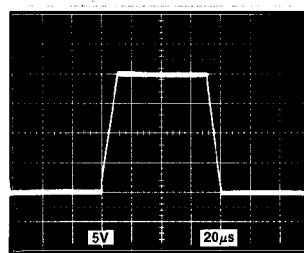
**CHANNEL SEPARATION vs FREQUENCY**



**TOTAL HARMONIC DISTORTION vs FREQUENCY**

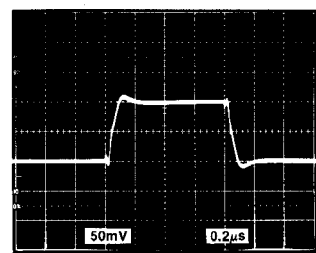


**LARGE-SIGNAL TRANSIENT RESPONSE**



TA = 25°C  
VS = ±15V  
AV = +1

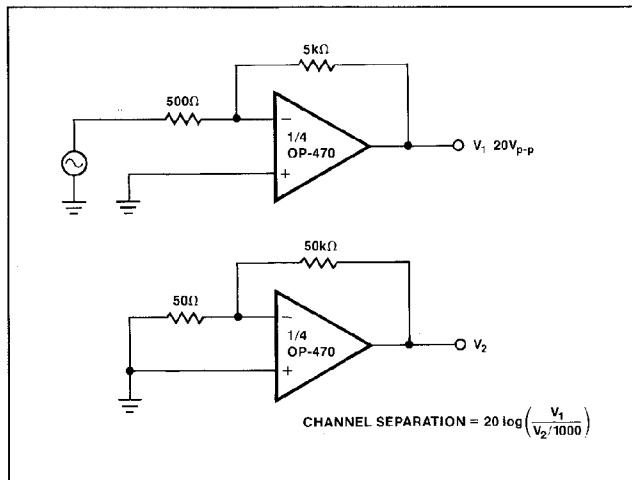
**SMALL-SIGNAL TRANSIENT RESPONSE**



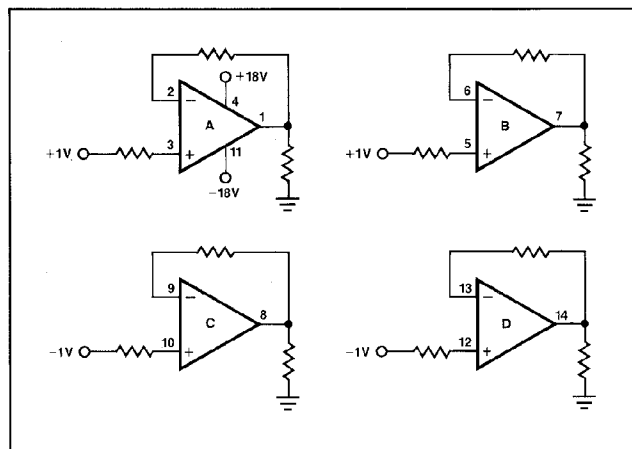
TA = 25°C  
VS = ±15V  
AV = +1



**CHANNEL SEPARATION TEST CIRCUIT**



**BURN-IN CIRCUIT**



**APPLICATIONS INFORMATION**

**VOLTAGE AND CURRENT NOISE**

The OP-470 is a very low-noise quad op amp, exhibiting a typical voltage noise of only  $3.2\text{nV}/\sqrt{\text{Hz}}$  @ 1kHz. The exceptionally low noise characteristics of the OP-470 is in part achieved by operating the input transistors at high collector currents since the voltage noise is inversely proportional to the square root of the collector current. Current noise, however, is directly proportional to the square root of the collector current. As a result, the outstanding voltage noise performance of the OP-470 is gained at the expense of current noise performance, which is typical for low noise amplifiers.

To obtain the best noise performance in a circuit it is vital to understand the relationship between voltage noise ( $e_n$ ), current noise ( $i_n$ ), and resistor noise ( $e_t$ ).

**TOTAL NOISE AND SOURCE RESISTANCE**

The total noise of an op amp can be calculated by:

$$E_n = \sqrt{(e_n)^2 + (i_n R_S)^2 + (e_t)^2}$$

where:

$E_n$  = total input referred noise

$e_n$  = op amp voltage noise

$i_n$  = op amp current noise

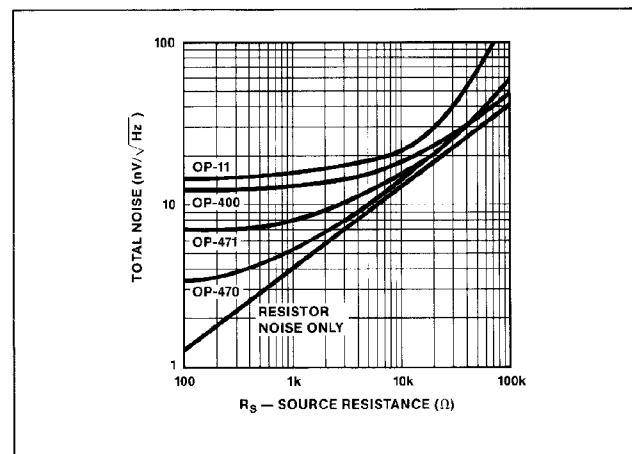
$e_t$  = source resistance thermal noise

$R_S$  = source resistance

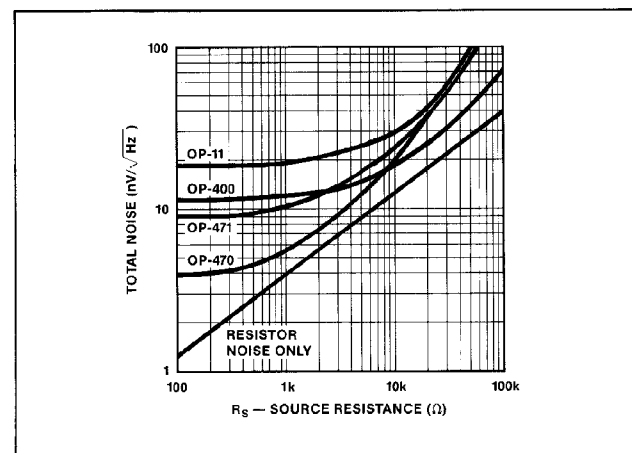
The total noise is referred to the input and at the output would be amplified by the circuit gain.

Figure 1 shows the relationship between total noise at 1kHz and source resistance. For  $R_S < 1\text{k}\Omega$  the total noise is dominated by the voltage noise of the OP-470. As  $R_S$  rises above

**FIGURE 1:** Total Noise vs Source Resistance (Including Resistor Noise) at 1kHz



**FIGURE 2:** Total Noise vs Source Resistance (Including Resistor Noise) at 10Hz



# OP-470

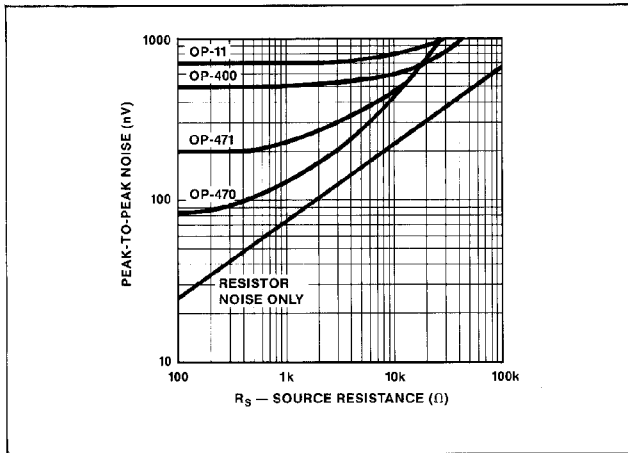
1kΩ, total noise increases and is dominated by resistor noise rather than by voltage or current noise of the OP-470. When  $R_S$  exceeds 20kΩ, current noise of the OP-470 becomes the major contributor to total noise.

Figure 2 also shows the relationship between total noise and source resistance, but at 10Hz. Total noise increases more quickly than shown in Figure 1 because current noise is inversely proportional to the square root of frequency. In Figure 2, current noise of the OP-470 dominates the total noise when  $R_S > 5kΩ$ .

From Figures 1 and 2 it can be seen that to reduce total noise, source resistance must be kept to a minimum. In applications with a high source resistance, the OP-400, with lower current noise than the OP-470, will provide lower total noise.

Figure 3 shows peak-to-peak noise versus source resistance over the 0.1Hz to 10Hz range. Once again, at low values of  $R_S$ ,

**FIGURE 3: Peak-To-Peak Noise (0.1Hz To 10Hz) vs Source Resistance (Includes Resistor Noise)**



the voltage noise of the OP-470 is the major contributor to peak-to-peak noise with current noise the major contributor as  $R_S$  increases. The crossover point between the OP-470 and the OP-400 for peak-to-peak noise is at  $R_S = 17kΩ$ .

The OP-471 is a higher speed version of the OP-470, with a slew rate of 8V/μs. Noise of the OP-471 is only slightly higher than the OP-470. Like the OP-470, the OP-471 is unity-gain stable.

For reference, typical source resistances of some signal sources are listed in Table I.

**TABLE I**

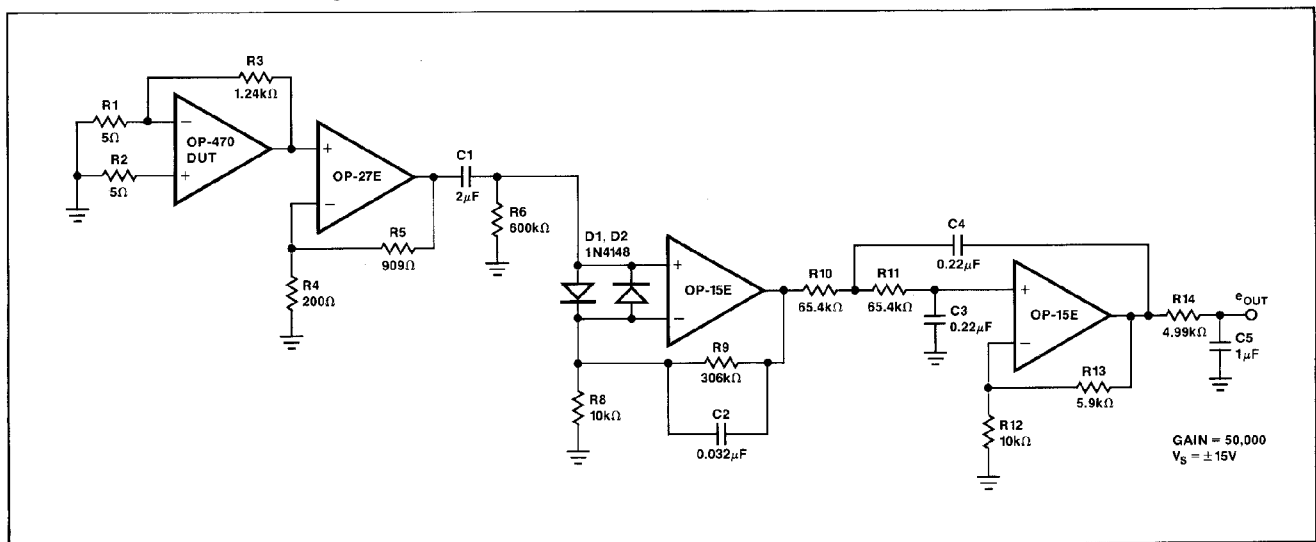
DEVICE	SOURCE IMPEDANCE	COMMENTS
Strain gauge	<500Ω	Typically used in low-frequency applications.
Magnetic tapehead	<1500Ω	Low $I_B$ very important to reduce self-magnetization problems when direct coupling is used. OP-470 $I_B$ can be neglected.
Magnetic phonograph cartridges	<1500Ω	Similar need for low $I_B$ in direct coupled applications. OP-470 will not introduce any self-magnetization problem.
Linear variable differential transformer	<1500Ω	Used in rugged servo-feedback applications. Bandwidth of interest is 400Hz to 5kHz.

For further information regarding noise calculations, see "Minimization of Noise in Op-Amp Applications," Application Note AN-15.

## NOISE MEASUREMENTS — PEAK-TO-PEAK VOLTAGE NOISE

The circuit of Figure 4 is a test setup for measuring peak-to-peak voltage noise. To measure the 200nV peak-to-peak

**FIGURE 4: Peak-To-Peak Voltage Noise Test Circuit (0.1Hz To 10Hz)**

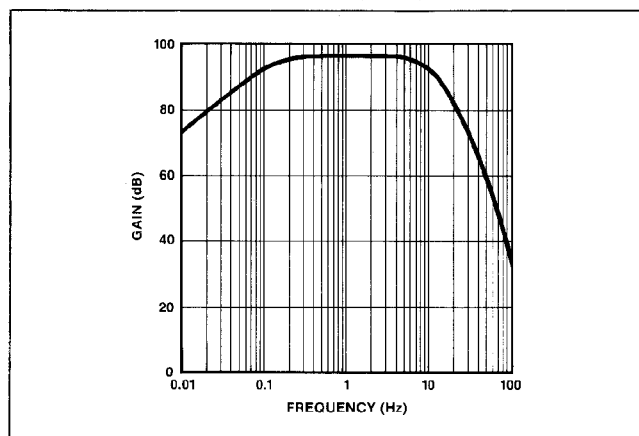


noise specification of the OP-470 in the 0.1Hz to 10Hz range, the following precautions must be observed:

1. The device has to be warmed-up for at least five minutes. As shown in the warm-up drift curve, the offset voltage typically changes  $5\mu V$  due to increasing chip temperature after power-up. In the 10-second measurement interval, these temperature-induced effects can exceed tens-of-nanovolts.
2. For similar reasons, the device has to be well-shielded from air currents. Shielding also minimizes thermocouple effects.
3. Sudden motion in the vicinity of the device can also "feed-through" to increase the observed noise.

4. The test time to measure 0.1Hz-to-10Hz noise should not exceed 10 seconds. As shown in the noise-tester frequency-response curve of Figure 5, the 0.1Hz corner is defined by only one pole. The test time of 10 seconds acts as an additional pole to eliminate noise contribution from the frequency band below 0.1Hz.
5. A noise-voltage-density test is recommended when measuring noise on a large number of units. A 10Hz noise-voltage-density measurement will correlate well with a 0.1Hz-to-10Hz peak-to-peak noise reading, since both results are determined by the white noise and the location of the  $1/f$  corner frequency.
6. Power should be supplied to the test circuit by well bypassed low-noise supplies, e.g. batteries. These will minimize output noise introduced via the amplifier supply pins.

**FIGURE 5:** 0.1Hz To 10Hz Peak-To-Peak Voltage Noise Test Circuit Frequency Response



**NOISE MEASUREMENT — NOISE VOLTAGE DENSITY**

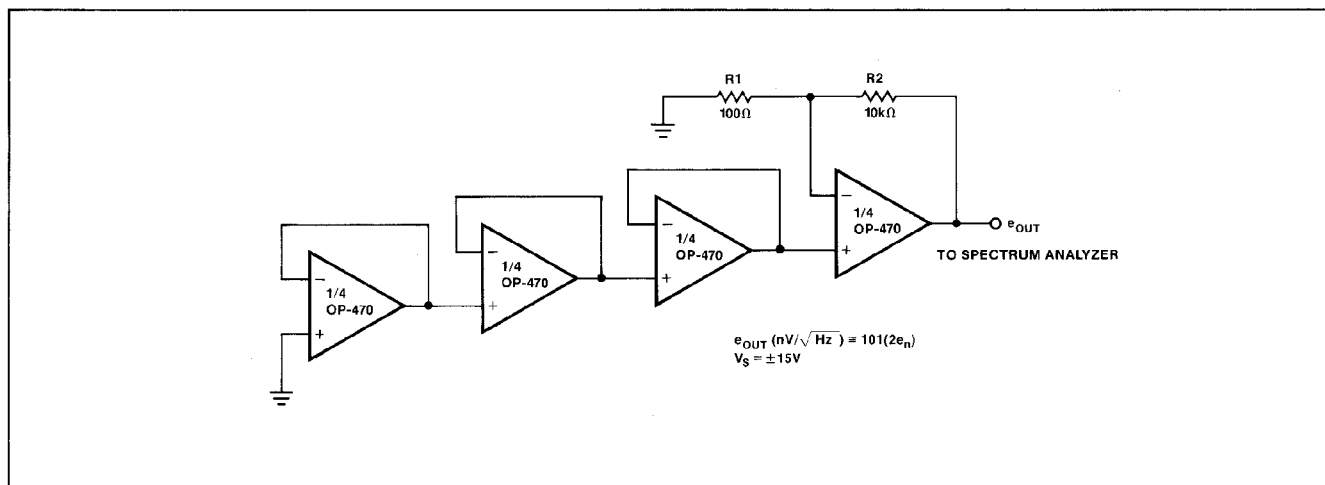
The circuit of Figure 6 shows a quick and reliable method of measuring the noise voltage density of quad op amps. Each individual amplifier is series-connected and is in unity-gain, save the final amplifier which is in a noninverting gain of 101. Since the ac noise voltages of each amplifier are uncorrelated, they add in rms fashion to yield:

$$e_{OUT} = 101 \left( \sqrt{e_{nA}^2 + e_{nB}^2 + e_{nC}^2 + e_{nD}^2} \right)$$

The OP-470 is a monolithic device with four identical amplifiers. The noise voltage density of each individual amplifier will match, giving:

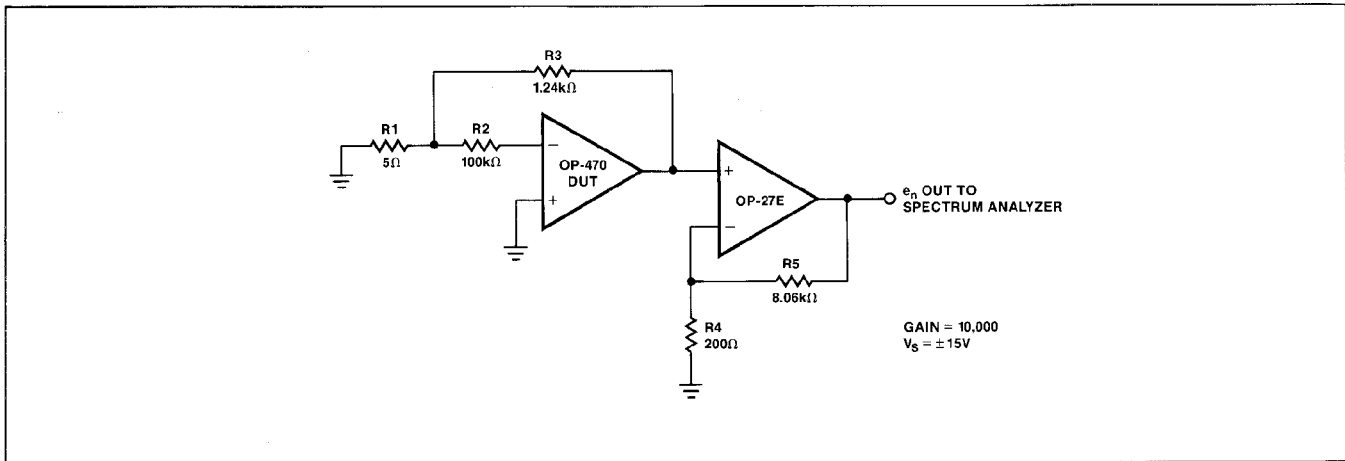
$$e_{OUT} = 101 \left( \sqrt{4e_n^2} \right) = 101 (2e_n)$$

**FIGURE 6:** Noise Voltage Density Test Circuit



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**FIGURE 7: Current Noise Density Test Circuit**



## NOISE MEASUREMENT — CURRENT NOISE DENSITY

The test circuit shown in Figure 7 can be used to measure current noise density. The formula relating the voltage output to current noise density is:

$$i_n = \frac{\sqrt{\left(\frac{e_{nOUT}}{G}\right)^2 - \left(40nV/\sqrt{Hz}\right)^2}}{R_S}$$

where:

G = gain of 10000

R<sub>S</sub> = 100kΩ source resistance

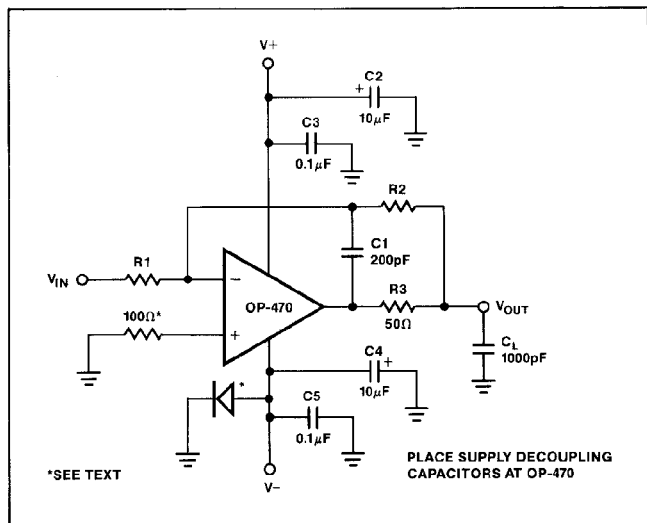
## CAPACITIVE LOAD DRIVING AND POWER SUPPLY CONSIDERATIONS

The OP-470 is unity-gain stable and is capable of driving large capacitive loads without oscillating. Nonetheless, good supply bypassing is highly recommended. Proper supply bypassing reduces problems caused by supply line noise and improves the capacitive load driving capability of the OP-470.

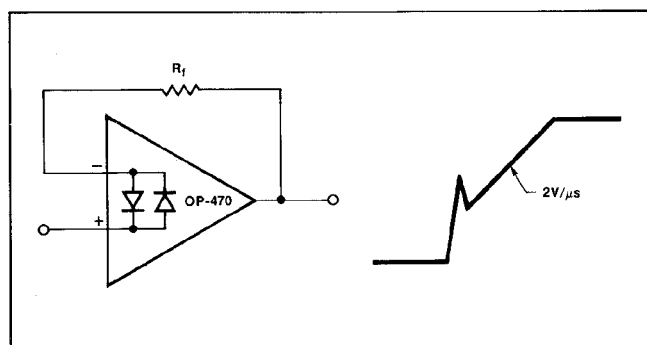
In the standard feedback amplifier, the op amp's output resistance combines with the load capacitance to form a low-pass filter that adds phase shift in the feedback network and reduces stability. A simple circuit to eliminate this effect is shown in Figure 8. The added components, C1 and R3, decouple the amplifier from the load capacitance and provide additional stability. The values of C1 and R3 shown in Figure 8 are for a load capacitance of up to 1000pF when used with the OP-470.

In applications where the OP-470's inverting or noninverting inputs are driven by a low source impedance (under 100Ω) or connected to ground, if V+ is applied before V-, or when V- is disconnected, excessive parasitic currents will flow. Most

**FIGURE 8: Driving Large Capacitive Loads**



**FIGURE 9: Pulsed Operation**



applications use dual tracking supplies and with the device supply pins properly bypassed, power-up will not present a problem. A source resistance of at least 100Ω in series with all inputs (Figure 8) will limit the parasitic currents to a safe level if V<sub>-</sub> is disconnected. It should be noted that any source resistance, even 100Ω, adds noise to the circuit. Where noise is required to be kept at a minimum, a germanium or Schottky diode can be used to clamp the V<sub>-</sub> pin and eliminate the parasitic current flow instead of using series limiting resistors. For most applications, only one diode clamp is required per board or system.

**UNITY-GAIN BUFFER APPLICATIONS**

When R<sub>f</sub> ≤ 100Ω and the input is driven with a fast, large-signal pulse (>1V), the output waveform will look as shown in Figure 9.

During the fast feedthrough-like portion of the output, the input protection diodes effectively short the output to the input, and a current, limited only by the output short-circuit protection, will be drawn by the signal generator. With R<sub>f</sub> ≥ 500Ω, the output is capable of handling the current requirements (I<sub>L</sub> ≤ 20mA at 10V); the amplifier will stay in its active mode and a smooth transition will occur.

When R<sub>f</sub> > 3kΩ, a pole created by R<sub>f</sub> and the amplifier's input capacitance (2pF) creates additional phase shift and reduces phase margin. A small capacitor (20 to 50pF) in parallel with R<sub>f</sub> helps eliminate this problem.

**APPLICATIONS**

**LOW NOISE AMPLIFIER**

A simple method of reducing amplifier noise by paralleling amplifiers is shown in Figure 10. Amplifier noise, depicted in Figure 11, is around 2nV/√Hz @ 1kHz (R.T.I.). Gain for each paralleled amplifier and the entire circuit is 1000. The 200Ω resistors limit circulating currents and provide an effective output resistance of 50Ω. The amplifier is stable with a 10nF capacitive load and can supply up to 30mA of output drive.

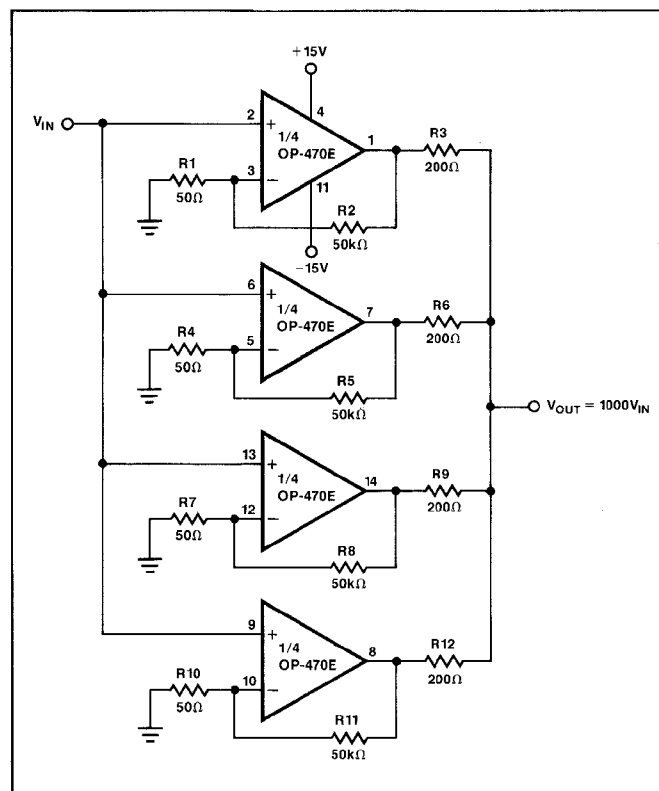
**DIGITAL PANNING CONTROL**

Figure 12 uses a DAC-8408, a quad 8-bit DAC, to pan a signal between two channels. The complementary DAC current outputs of two of the DAC-8408's four DACs drive current-to-voltage converters built from a single quad OP-470. The amplifiers have complementary outputs with the amplitudes dependent upon the digital code applied to the DAC. Figure 13 shows the complementary outputs for a 1kHz input signal and digital ramp applied to the DAC data inputs. Distortion of the digital panning control is less than 0.01%.

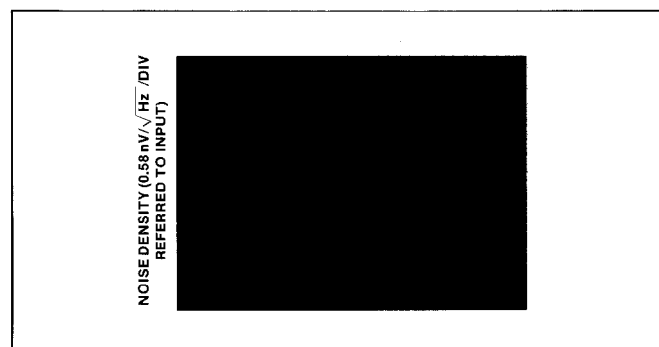
Gain error due to the mismatching between the internal DAC ladder resistors and the current-to-voltage feedback resis-

tors is eliminated by using feedback resistors internal to the DAC. Of the four DACs available in the DAC-8408, only two, DACs A and C, actually pass a signal. DACs B and D are used to provide the additional feedback resistors needed in the circuit. If the V<sub>REFB</sub> and V<sub>REFD</sub> inputs remain unconnected the current-to-voltage converters using R<sub>FBB</sub> and R<sub>FBD</sub> are unaffected by digital data reaching DACs B and D.

**FIGURE 10: Low Noise Amplifier**



**FIGURE 11: Noise Density of Low Noise Amplifier, G = 1000**



# OP-470

FIGURE 12: Digital Panning Control Circuit

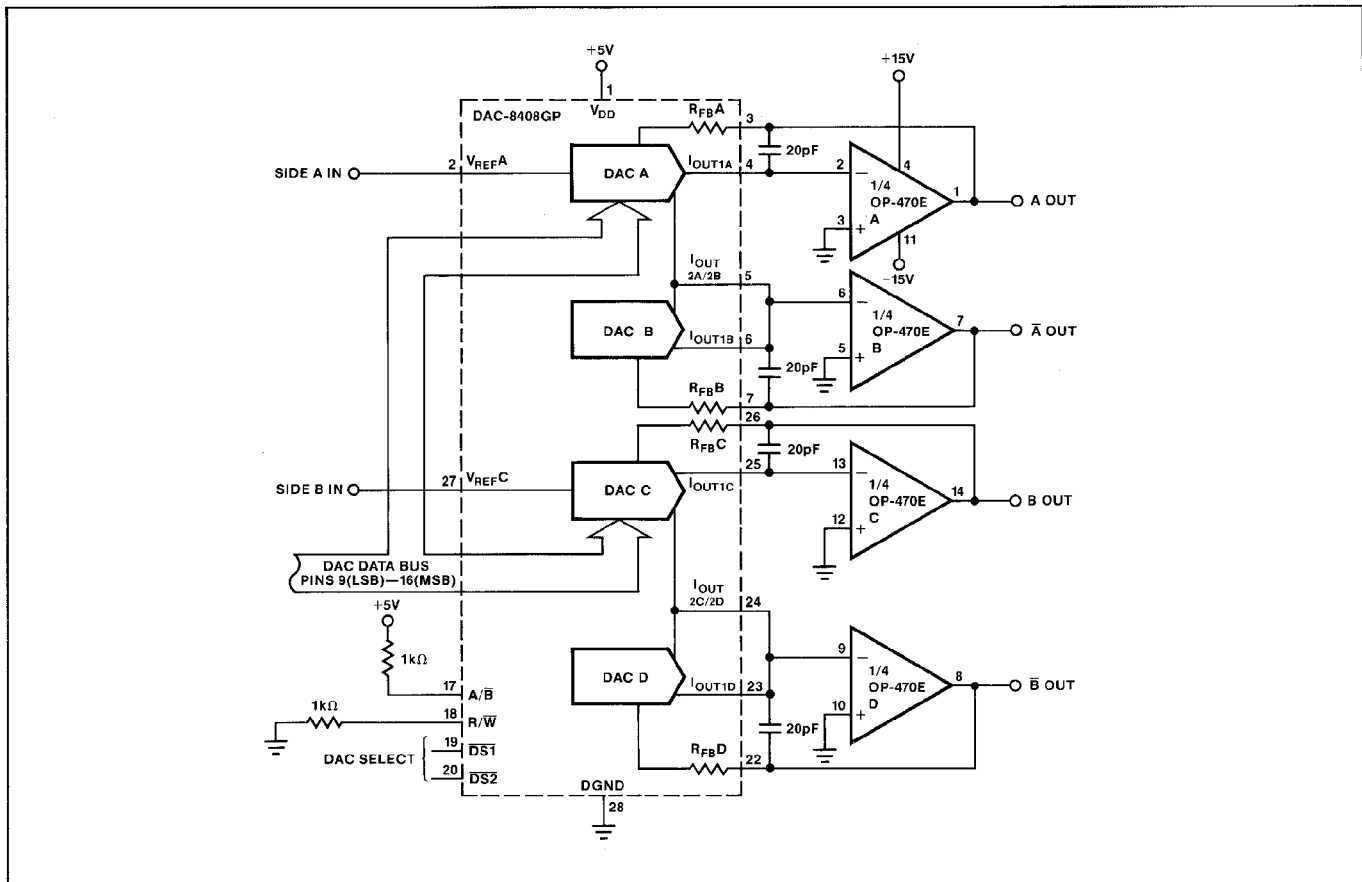
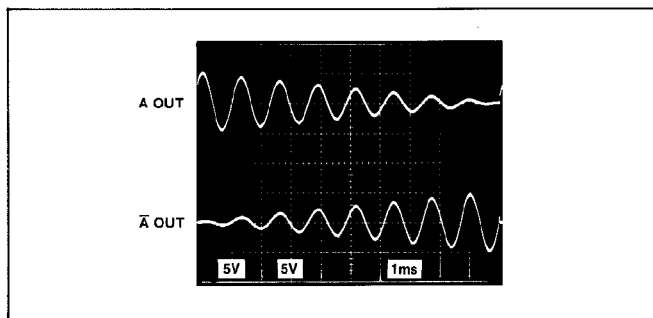


FIGURE 13: Digital Panning Control Output

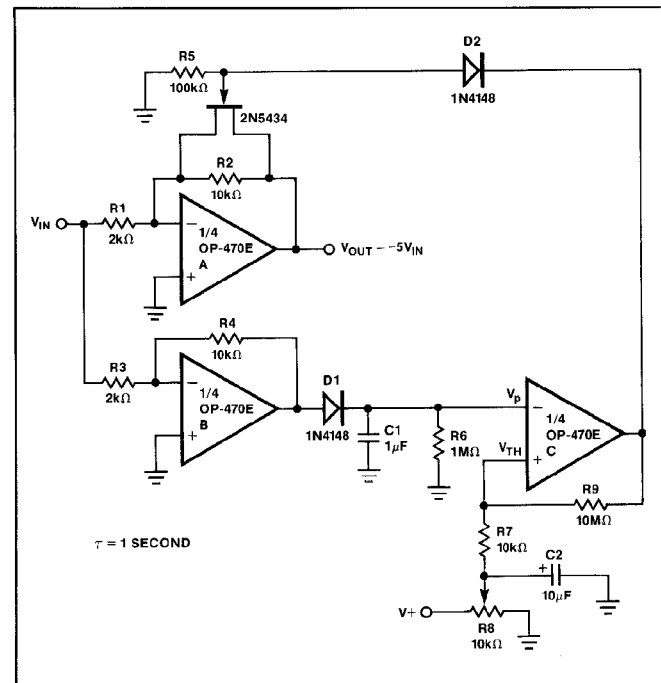


## SQUELCH AMPLIFIER

The circuit of Figure 14 is a simple squelch amplifier that uses a FET switch to cut off the output when the input signal falls below a preset limit.

The input signal is sampled by a peak detector with a time constant set by C1 and R6. When the output of the peak detector,  $V_p$ , falls below the threshold voltage,  $V_{TH}$ , set by R8, the comparator formed by op amp C switches from  $V^-$  to  $V^+$ . This drives the gate of the N-channel FET high, turning it ON, reducing the gain of the inverting amplifier formed by op amp A to zero.

FIGURE 14: Squelch Amplifier



**FIVE-BAND LOW NOISE STEREO GRAPHIC EQUALIZER**

The graphic equalizer circuit shown in Figure 15 provides 15dB of boost or cut over a 5-band range. Signal-to-noise

ratio over a 20kHz bandwidth is better than 100dB referred to a 3V rms input. Larger inductors can be replaced by active inductors but this reduces the signal-to-noise ratio.

**FIGURE 15:** 5-Band Low Noise Graphic Equalizer

