Thermoelectric Cooler Controller

ADN8830

FEATURES

High Efficiency
Small Size: 5 mm × 5 mm LFCSP
Low Noise: <0.5% TEC Current Ripple
Long-Term Temperature Stability: ±0.01°C
Temperature Lock Indication
Temperature Monitoring Output
Oscillator Synchronization with an External Signal
Clock Phase Adjustment for Multiple Controllers
Programmable Switching Frequency up to 1 MHz
Thermistor Failure Alarm
Maximum TEC Voltage Programmability

APPLICATIONS

Thermoelectric Cooler (TEC) Temperature Control
Resistive Heating Element Control
Temperature Stabilization Substrate (TSS) Control

GENERAL DESCRIPTION

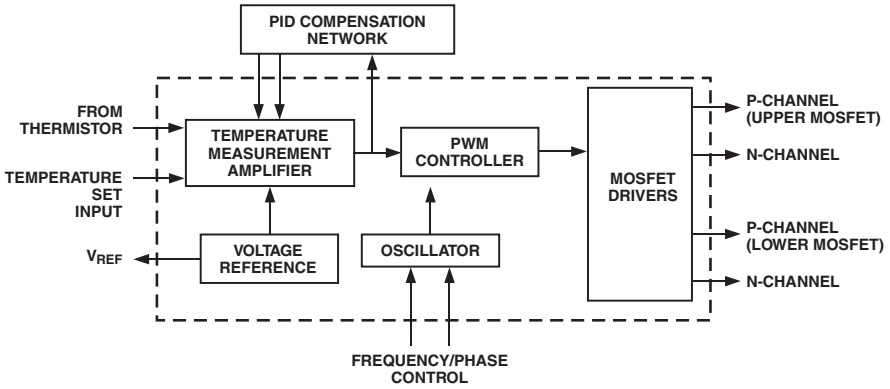
The ADN8830 is a monolithic controller that drives a thermoelectric cooler (TEC) to stabilize the temperature of a laser diode or a passive component used in telecommunications equipment.

This device relies on a negative temperature coefficient (NTC) thermistor to sense the temperature of the object attached to the TEC. The target temperature is set with an analog input voltage either from a DAC or an external resistor divider.

The loop is stabilized by a PID compensation amplifier with high stability and low noise. The compensation network can be adjusted by the user to optimize temperature settling time. The component values for this network can be calculated based on the thermal transfer function of the laser diode or obtained from the lookup table given in the Application Notes section.

Voltage outputs are provided to monitor both the temperature of the object and the voltage across the TEC. A voltage reference of 2.5 V is also provided.

FUNCTIONAL BLOCK DIAGRAM



REV. C

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ADN8830–SPECIFICATIONS

(@ V_{DD} = 3.3 V to 5.0 V, V_{GND} = 0 V, T_A = 25°C, T_{SET} = 25°C, using typical application configuration as shown in Figure 1, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
TEMPERATURE STABILITY						
Long-Term Stability		Using 10 kΩ thermistor with α = –4.4% at 25°C			0.01	°C
PWM OUTPUT DRIVERS						
Output Transition Time	t_R, t_F	C_L = 3,300 pF		20		ns
Nonoverlapping Clock Delay			50	65		ns
Output Resistance	R_O (N1, P1)	I_L = 50 mA		6		Ω
Output Voltage Swing	OUT A	V_{LIM} = 0 V	0		V_{DD}	V
Output Voltage Ripple	ΔOUT A	f_{CLK} = 1 MHz		0.2		%
Output Current Ripple	ΔI_{TEC}	f_{CLK} = 1 MHz		0.2		%
LINEAR OUTPUT AMPLIFIER						
Output Resistance	$R_{O, P2}$	I_{OUT} = 2 mA		85		Ω
	$R_{O, N2}$	I_{OUT} = 2 mA		178		Ω
Output Voltage Swing	OUT B		0		V_{DD}	V
POWER SUPPLY						
Power Supply Voltage	V_{DD}		3.0		5.5	V
Power Supply Rejection Ratio	PSRR	V_{DD} = 3.3 V to 5 V, V_{TEC} = 0 V	80	92		dB
		–40°C ≤ T_A ≤ +85°C	60			dB
Supply Current	I_{SY}	PWM not switching		8	12	mA
		–40°C ≤ T_A ≤ +85°C			15	mA
Shutdown Current	I_{SD}	Pin 10 = 0 V		5		μA
Soft-Start Charging Current	I_{SS}			15		μA
Undervoltage Lockout	V_{OLOCK}	Low-to-high threshold		2.0	2.7	V
ERROR AMPLIFIER						
Input Offset Voltage	V_{OS}	V_{CM} = 1.5 V		50	250	μV
Gain	$A_{V, IN}$			20		V/V
Input Voltage Range	V_{CM}		0.2		2.0	V
Common-Mode Rejection Ratio	CMRR	0.2 V < V_{CM} < 2.0 V	58	68		dB
		–40°C ≤ T_A ≤ +85°C	55			dB
Open-Loop Input Impedance	R_{IN}			1		GΩ
Gain-Bandwidth Product	GBW			2		MHz
REFERENCE VOLTAGE						
Reference Voltage	V_{REF}	I_{REF} < 2 mA	2.37	2.47	2.57	V
OSCILLATOR						
Synchronization Range	f_{CLK}	Pin 25 connected to external clock	200		1,000	kHz
Oscillator Frequency	f_{CLK}	Pin 24 = V_{DD}; (R = 150 kΩ; Pin 25 = GND)	800	1,000	1,250	kHz
LOGIC CONTROL*						
Logic Low Input Threshold					0.2	V
Logic High Input Threshold			3			V
Logic Low Output Level					0.2	V
Logic High Output Threshold			V_{DD} – 0.2			V

*Logic inputs meet typical CMOS I/O conditions for source/sink current (~1 μA).

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . 6 V
Input Voltage . . . . . GND to V_S + 0.3 V
Storage Temperature Range . . . . . –65°C to +150°C
Operating Temperature Range . . . . . –40°C to +85°C
Operating Junction Temperature . . . . . 125°C
Lead Temperature Range (Soldering, 10 sec) . . . . . 300°C

ESD RATINGS

883 (Human Body) Model . . . . . 1.0 kV

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

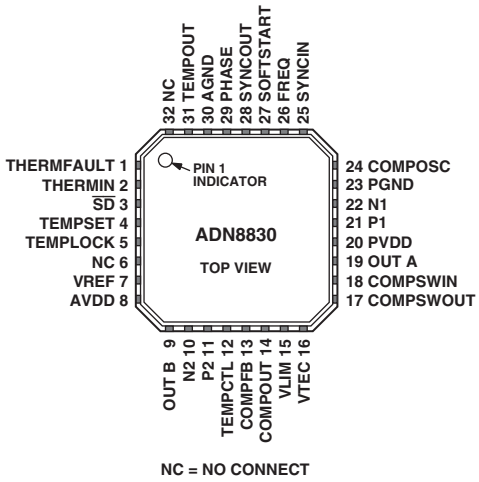
Package Type	θ_{JA}*	θ_{JC}	Unit
32-Lead LFCSP (ACP)	35	10	°C/W

*θ_{JA} is specified for worst-case conditions, i.e., θ_{JA} is specified for a device soldered in a 4-layer circuit board for surface-mount packages.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADN8830ACP	–40°C to +85°C	32-Lead Lead Frame Chip Scale Package (LFCSP)	CP-32-1
ADN8830ACP-REEL	–40°C to +85°C	32-Lead Lead Frame Chip Scale Package (LFCSP)	CP-32-1
ADN8830ACP-REEL7	–40°C to +85°C	32-Lead Lead Frame Chip Scale Package (LFCSP)	CP-32-1
ADN8830-EVAL		Evaluation Board	

PIN CONFIGURATION

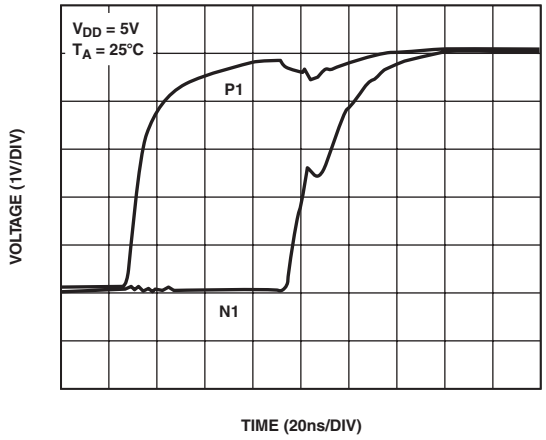


CAUTION

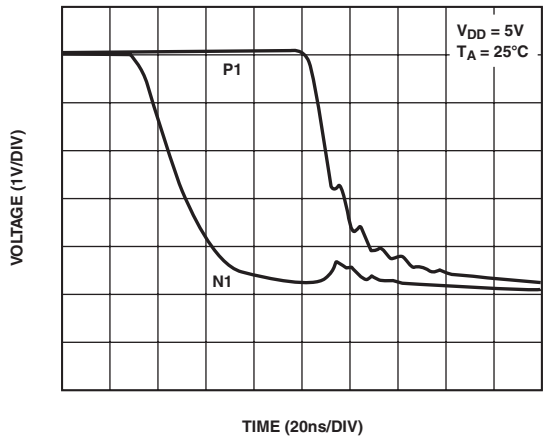
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADN8830 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTIONS

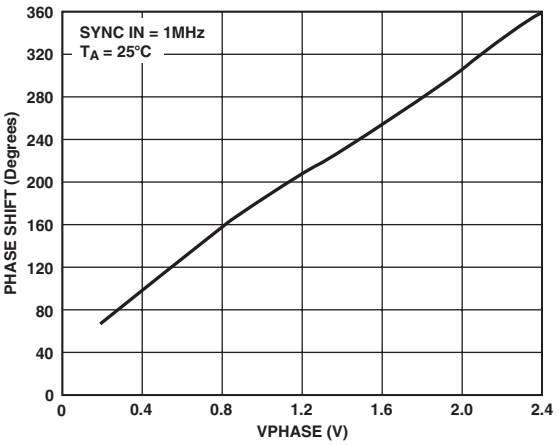
Pin No.	Mnemonic	Type	Description
1	THERMFAULT	Digital Output	Indicates an Open or Short-Circuit Condition from Thermistor.
2	THERMIN	Analog Input	Thermistor Feedback Input.
3	$\overline{SD}$	Digital Input	Puts Device into Low Current Shutdown Mode. Active low.
4	TEMPSET	Analog Input	Target Temperature Input.
5	TEMPLOCK	Digital Output	Indicates when Thermistor Temperature is within ±0.1°C of Target Temperature as Set by TEMPSET Voltage.
6	NC		No Connection, except as Noted in the Application Notes Section.
7	VREF	Analog Output	2.5 V Reference Voltage.
8	AVDD	Power	Power for Nondriver Sections. 3.0 V min; 5.5 V max.
9	OUT B	Analog Input	Linear Output Feedback. Will typically connect to TEC+ pin of TEC.
10	N2	Analog Output	Drives Linear Output External NMOS Gate.
11	P2	Analog Output	Drives Linear Output External PMOS Gate.
12	TEMPCTL	Analog Output	Output of Error Amplifier. Connects to COMPFB through feedforward section of compensation network.
13	COMPFB	Analog Input	Feedback Summing Node of Compensation Amplifier. Connects to TEMPCTL and COMPOUT through compensation network.
14	COMPOUT	Analog Output	Output of Compensation Amplifier. Connects to COMPFB through feedback section of compensation network.
15	VLIM	Analog Input	Sets Maximum Voltage across TEC.
16	VTEC	Analog Output	Indicates Relative Voltage across the TEC. The 1.5 V corresponds to 0 V across TEC. The 3.0 V indicates maximum output voltage, maximum heat transfer through TEC.
17	COMPSWOUT	Analog Output	Compensation for Switching Amplifier.
18	COMPSWIN	Analog Input	Compensation for Switching Amplifier. Capacitor connected between COMPSWIN and COMPSWOUT.
19	OUT A	Analog Input	PWM Output Feedback. Will typically connect to TEC– pin of TEC.
20	PVDD	Power	Power for Output Driver Sections. 3.0 V min; 5.5 V max.
21	P1	Digital Output	Drives PWM Output External PMOS Gate.
22	N1	Digital Output	Drives PWM Output External NMOS Gate.
23	PGND	Ground	Power Ground. External NMOS devices connect to PGND. Can be connected to digital ground as noise sensitivity at this node is not critical.
24	COMPOSC	Analog Input	Connect as Indicated in the Application Notes Section.
25	SYNCIN	Digital Input	Optional Clock Input. If not connected, clock frequency set by FREQ pin.
26	FREQ	Analog Input	Sets Switching Frequency.
27	SOFTSTART	Analog Input	Controls Initialization Time for ADN8830 with Capacitor to Ground.
28	SYNCOUT	Digital Output	Phase Adjusted Clock Output. Phase set from PHASE pin. Can be used to drive SYNCIN of other ADN8830 devices.
29	PHASE	Analog Input	Sets Switching and SYNCOUT Clock Phase Relative to SYNCIN Clock.
30	AGND	Ground	Analog Ground. Should be low noise for highest accuracy.
31	TEMPOUT	Analog Output	Indication of Thermistor Temperature.
32	NC		No Connection.



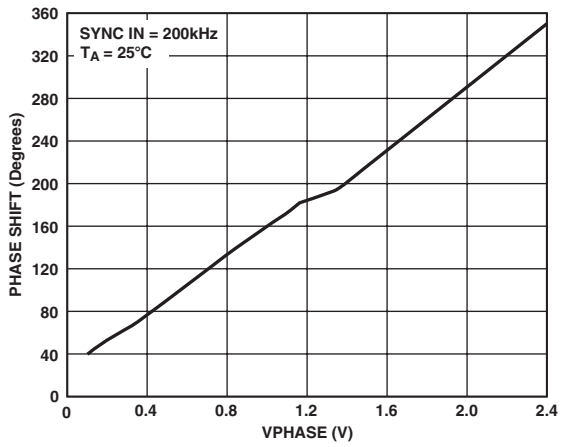
TPC 1. N1 and P1 Rise Time



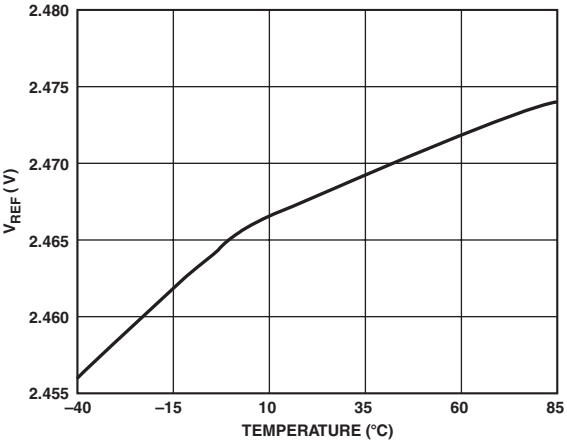
TPC 2. N1 and P1 Fall Time



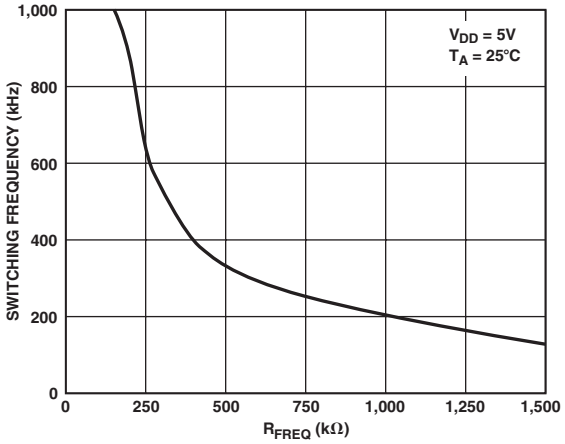
TPC 3. Clock Phase Shift vs. Phase Voltage



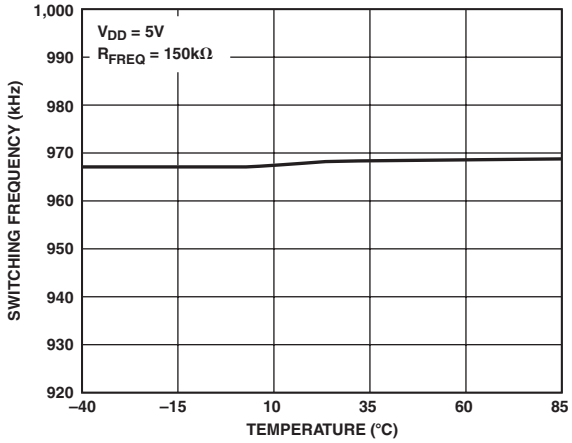
TPC 4. Clock Phase Shift vs. Phase Voltage



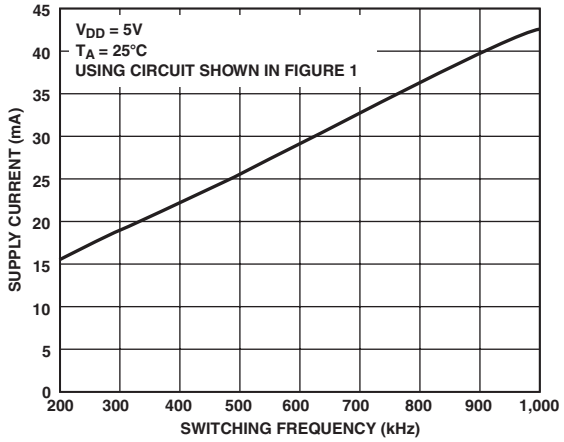
TPC 5. V_{REF} vs. Temperature



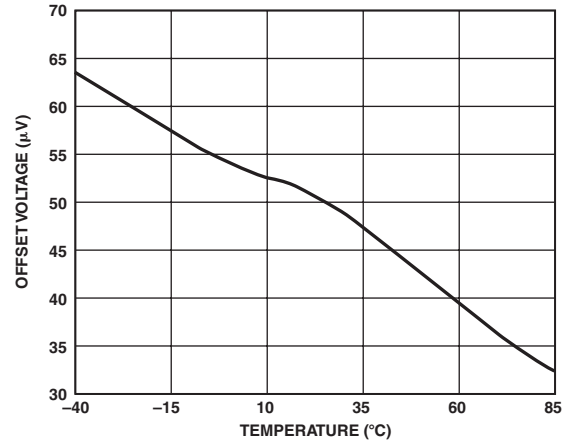
TPC 6. Switching Frequency vs. R_{FREQ}



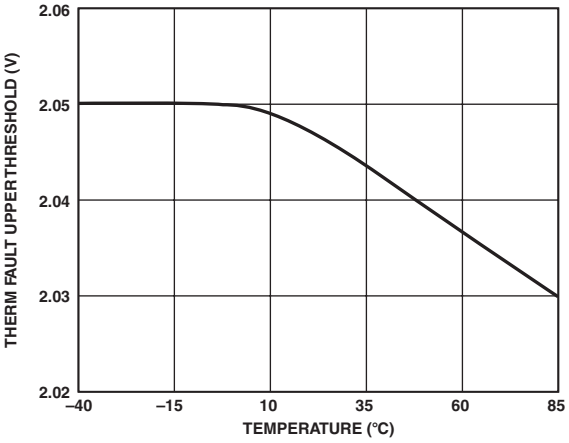
TPC 7. Switching Frequency vs. Temperature



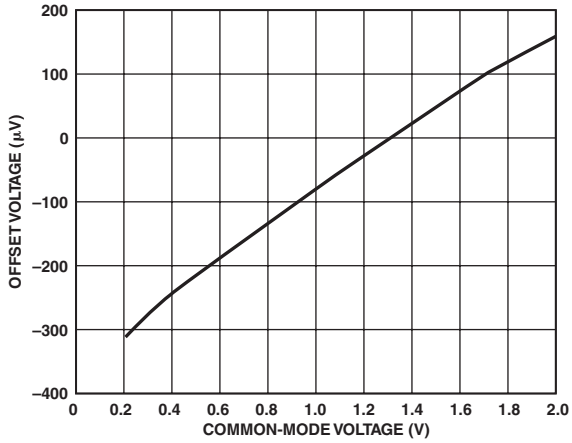
TPC 10. Supply Current vs. Switching Frequency



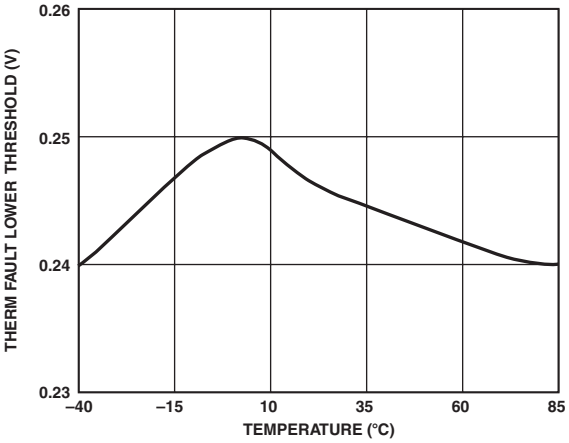
TPC 8. Offset Voltage vs. Temperature



TPC 11. Open Thermistor Fault Threshold vs. Temperature



TPC 9. Offset Voltage vs. Common-Mode Voltage



TPC 12. Short Thermistor Fault Threshold vs. Temperature

APPLICATION NOTES

Principle of Operation

The ADN8830 is a controller for a TEC and is used to set and stabilize the temperature of the TEC. A voltage applied to the input of the ADN8830 corresponds to a target temperature setpoint. The appropriate current is then applied to the TEC to pump heat either to or away from the object whose temperature is being regulated. The temperature of the object is measured by a thermistor and is fed back to the ADN8830 to correct the loop and settle the TEC to the appropriate final temperature. For best stability, the thermistor should be mounted in close proximity to the object. In most laser diode modules, the TEC and thermistor are already mounted in the unit and are used to regulate the temperature of the laser diode.

A complete TEC controller solution requires:

- A precision input amplifier stage to accurately measure the difference between the target and object temperatures.
- A compensation amplifier to optimize the stability and temperature settling time.
- A high output current stage. Because of the high output currents involved, a TEC controller should operate with high efficiency to minimize the heat generated from power dissipation.

In addition, an effective controller should operate down to 3.3 V and have an indication of when the target temperature has been reached. The ADN8830 accomplishes all of these requirements with a minimum of external components. Figure 1 shows a reference design for a typical application.

Temperature is monitored by connecting the measurement thermistor to a precision amplifier, called the error amplifier, with a simple resistor divider. This voltage is compared against the temperature set input voltage, creating an error voltage that is proportional to their difference. To maintain accurate wavelength and power from the laser diode, this difference voltage must be as accurate as possible. For this reason, self-correction auto-zero amplifiers are used in the input stage of the ADN8830, providing a maximum offset voltage of 250 μV over time and temperature. This results in final temperature accuracy within ±0.01°C in typical applications, eliminating the ADN8830 as an error source in the temperature control loop. A logic output is provided at TEMPLOCK to indicate when the target temperature has been reached.

The output of the error amplifier is then fed into a compensation amplifier. An external network consisting of a few resistors and capacitors is connected around the compensation amplifier. This network can be adjusted by the user to optimize the step

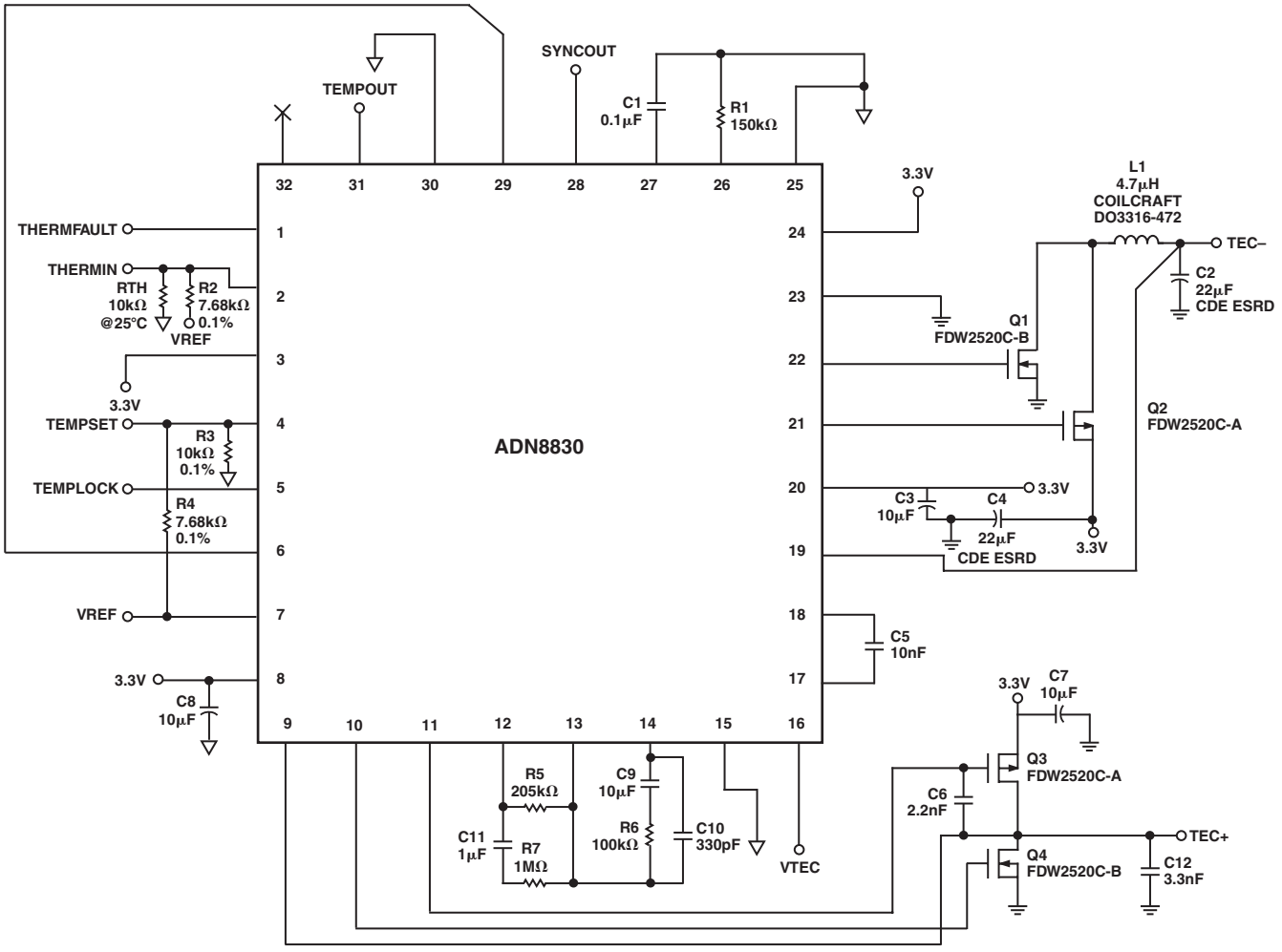


Figure 1. Typical Application Schematic

response of the TEC's temperature either in terms of settling time or maximum current change. Details of how to adjust the compensation network are given in the Compensation Loop section.

The ADN8830 can be easily integrated with a wavelength locker for fine-tune temperature adjustment of the laser diode for a specific wavelength. This is a useful topology for tunable wavelength lasers. Details are highlighted in the Using the TEC Controller ADN8830 with a Wave Locker section.

The TEC is driven differentially using an H-bridge configuration to maximize the output voltage swing. The ADN8830 drives external transistors that are used to provide current to the TEC. These transistors can be selected by the user based on the maximum output current required for the TEC. The maximum voltage across the TEC can be set through use of the VLIM pin on the ADN8830.

To further improve the power efficiency of the system, one side of the H-bridge uses a switched output. Only one inductor and one capacitor are required to filter out the switching frequency. The output voltage ripple is a function of the output inductor and capacitor and the switching frequency. For most applications, a 4.7 μH inductor, 22 μF capacitor, and switching frequency of 1 MHz maintains less than ±0.5% worst-case output voltage ripple across the TEC. The other side of the H-bridge does not require any additional circuitry.

The oscillator section of the ADN8830 controls the switched output section. A single resistor sets the switching frequency from 100 kHz to 1 MHz. The clock output is available at the SYNCOUT pin and can be used to drive another ADN8830 device by connecting to its SYNCIN pin. The phase of the clock is adjusted by a voltage applied to the PHASE pin, which can be set by a simple resistor divider. Phase adjustment allows two or more ADN8830 devices to operate from the same clock frequency and not have all outputs switch simultaneously, which could create an excessive power supply ripple. Details of how to adjust the clock frequency and phase are given in the Setting the Switching Frequency section.

For effective indication of a catastrophic system failure, the ADN8830 alerts to open-circuit or short-circuit conditions from the thermistor, preventing an erroneous and potentially damaging temperature correction from occurring. With some additional external circuitry, output overcurrent detection can be implemented to provide warning in the event of a TEC short-circuit failure. This circuit is highlighted in the Setting Maximum Output Current and Short-Circuit Protection section.

Signal Flow Diagram

Figure 2 shows the signal flow diagram through the ADN8830. The input amplifier is fixed with a gain of 20. The voltage at *TEMPCTL* can be expressed as

$$TEMPCTL = 20 \times \left(TEMPSET - THERMIN\right) + 1.5 \quad (1)$$

When the temperature is settled, the thermistor voltage will be equal to the *TEMPSET* voltage, and the output of the input amplifier will be 1.5 V.

The voltage at TEMPCTL is then fed into the compensation amplifier whose frequency response is dictated by the compensation network. Details on the compensation amplifier can be found in the Compensation Loop section. When configured as a simple integrator or PID loop, the dc forward gain of the compensation section is equal to the open-loop gain of the compensation amplifier, which is over 80 dB or 10,000. The output from the compensation loop at COMPOUT is then fed to the linear amplifier. The output of the linear amplifier at OUT B is fed with COMPOUT into the PWM amplifier whose output is OUT A. These two outputs provide the voltage drive directly to the TEC. Including the external transistors, the gain of the differential output section is fixed at 4. Details on the output amplifiers can be found in the Output Driver Amplifiers section.

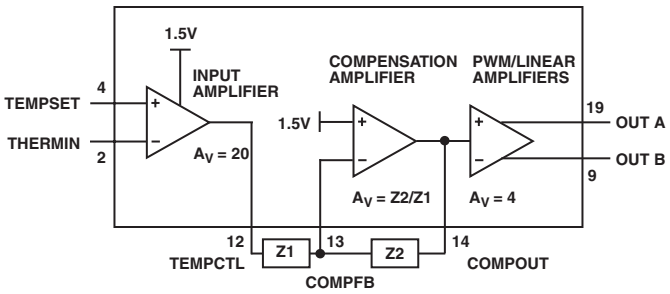


Figure 2. Signal Flow Block Diagram of the ADN8830

Thermistor Setup

The temperature of the thermal object, such as a laser diode, is detected with a negative temperature coefficient (NTC) thermistor. The thermistor's resistance exhibits an exponential relationship to the inverse of temperature, meaning the resistance decreases at higher temperatures. Thus, by measuring the thermistor resistance, temperature can be ascertained. Betatherm is a leading supplier of NTC thermistors. Thermistor information and details can be found at www.betatherm.com.

For this application, the resistance is measured using a voltage divider. The thermistor is connected between THERMIN (Pin 2) and AGND (Pin 30). Another resistor (R_X) is connected between VREF (Pin 7) and THERMIN (Pin 2), creating a voltage divider for the VREF voltage. Figure 3 shows the schematic for this configuration.

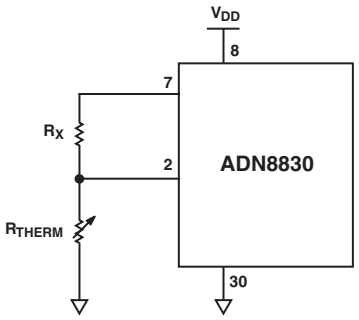


Figure 3. Connecting a Thermistor to the ADN8830

With the thermistor connected from THERMIN to AGND, the voltage at THERMIN will decrease as temperature increases. To maintain the proper input-to-output polarity in this configuration, OUT A (Pin 19) should connect to the TEC– pin on the TEC, and OUT B (Pin 9) should connect to the VTEC+ pin.

The thermistor can also be connected from VREF to THERMIN with R_X connecting to ground. In this case, OUT A must connect to TEC+ with OUT B connected to TEC– for proper operation.

Although the thermistor has a nonlinear relationship to temperature, near optimal linearity over a specified temperature range can be achieved with the proper value of R_X. First, the resistance of the thermistor must be known, where

$$\begin{aligned} R_{THERM} &= R_{T1} @ T = T_{LOW} \\ &= R_{T2} @ T = T_{MID} \\ &= R_{T3} @ T = T_{HIGH} \end{aligned} \quad (2)$$

T_{LOW} and T_{HIGH} are the endpoints of the temperature range and T_{MID} is the average. These resistances can be found in most thermistor data sheets. In some cases, only the coefficients corresponding to the Steinhart-Hart equation are given. The Steinhart-Hart equation is

$$\frac{1}{T} = a + b1n\left(R\right) + c\left[1n\left(R\right)\right]^3 \quad (3)$$

where T is the absolute temperature of the thermistor in Kelvin (K = °C + 273.15), and R is the resistance of the thermistor at that temperature. Based on the coefficients a, b, and c, R_{THERM} can be calculated for a given T, albeit somewhat tediously, by solving the cubic roots of this equation

$$R_{THERM} = \exp\left[\left(-\frac{\chi}{2} + \left(\frac{\chi^2}{4} + \frac{\psi^3}{27}\right)^{\frac{1}{2}}\right)^{\frac{1}{3}} + \left(-\frac{\chi}{2} - \left(\frac{\chi^2}{4} + \frac{\psi^3}{27}\right)^{\frac{1}{2}}\right)^{\frac{1}{3}}\right] \quad (4)$$

where

$$X = \frac{a - \frac{1}{T}}{c} \text{ and } \psi = \frac{b}{c}$$

R_X is then found as

$$R_X = \frac{R_{T1}R_{T2} + R_{T2}R_{T3} - 2R_{T1}R_{T3}}{R_{T1} + R_{T3} - 2R_{T2}} \quad (5)$$

For the best accuracy as well as the widest selection range for resistances, R_X should be 0.1% tolerance. Naturally, the smaller the temperature range required for control, the more linear the voltage divider will be with respect to temperature. The voltage at THERMIN is

$$V_X = VREF\frac{R_{THERM}}{R_{THERM} + R_X} \quad (6)$$

where $VREF$ has a typical value of 2.47 V.

The ADN8830 control loop will adjust the temperature of the TEC until V_X equals the voltage at TEMPSET (Pin 4), which we define as V_{SET}. Target temperature can be set by

$$V_{SET} = m\left(T - T_{MID}\right) + V_{XMID} \quad (7)$$

where T equals the target temperature, and

$$m = \frac{V_{X,\,HIGH} - V_{X,\,LOW}}{T_{HIGH} - T_{LOW}} \quad (8)$$

V_X for high, mid, and low are found by using Equation 6 and substituting R_{T3}, R_{T2}, and R_{T1}, respectively, for R_{THERM}. The variable m is the change in V_X with respect to temperature and is expressed in V/°C.

The setpoint voltage can be driven from a DAC or another voltage source, as shown in Figure 4. The reference voltage for the DAC should be connected to VREF (Pin 7) on the ADN8830 to ensure best accuracy from device to device.

For a fixed target temperature, a voltage divider network can be used as shown in Figure 5. R1 is set equal to R_X, and R2 is equal to the value of R_{THERM} at the target temperature.

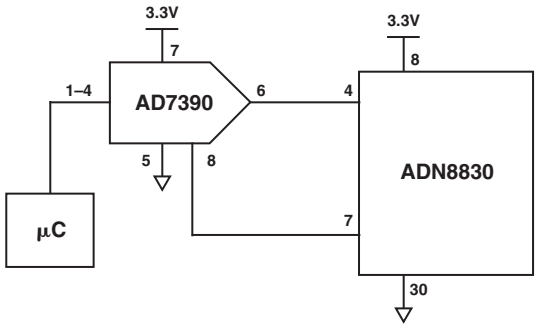


Figure 4. Using a DAC to Control the Temperature Setpoint

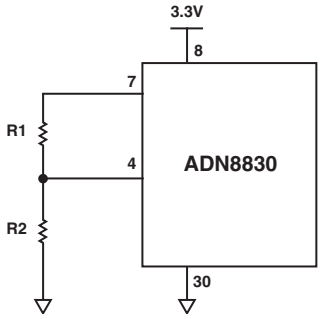


Figure 5. Using a Voltage Divider to Set a Fixed Temperature Setpoint

Design Example 1

A laser module requires a constant temperature of 25°C. From the manufacturer's data sheet, we find the thermistor in the laser module has a value of 10 kΩ at 25°C. Because the laser is not required to operate at a range of temperatures, the value of R_X can be set to 10 kΩ. TEMPSET can be set by a simple resistor divider as shown in Figure 5, with R1 and R2 both equal to 10 kΩ.

Design Example 2

A laser module requires a continuous temperature control from 5°C to 45°C. The manufacturer's data sheet shows the thermistor has a value of 10 kΩ at 25°C, 25.4 kΩ at 5°C, and 4.37 kΩ at 45°C. Using Equation 5, R_X is calculated to be 7.68 kΩ to yield the most linear temperature-to-voltage conversion. A DAC will be used to set the TEMPSET voltage.

DAC Resolution for TEMPSET

The temperature setpoint voltage to THERMIN can be set from a DAC. The DAC must have a sufficient number of bits to achieve adequate temperature resolution from the system. The voltage range for THERMIN is found by multiplying the variable m from Equation 8 by the temperature range.

$$THERMIN\ Voltage\ Range = m \times \left(T_{MAX} - T_{MIN}\right) \quad (9)$$

From Design Example 2, 40°C of the control temperature range is achieved with a voltage range of only 1 V.

To eliminate the resolution of the DAC as the principal source of system error, the step size of each bit, V_{STEP}, should be lower than the desired system resolution. A practical value for absolute DAC resolution is the equivalent of 0.05°C. The value of V_{STEP} should be less than the value of m from Equation 8 multiplied by the desired temperature resolution, or

$$V_{STEP} < 0.05°C \times m \tag{10}$$

where m is the slope of the voltage-to-temperature conversion line, as found from Equation 8. From Design Example 2, where m = 25 mV/°C, we see the DAC should have resolution better than 1.25 mV per step.

The minimum number of bits required is then given as

$$Number\ of\ Bits = \frac{\log(V_{FS}) - \log(V_{STEP})}{\log(2)} \tag{11}$$

where V_{FS} is the full-scale output voltage from the DAC, which should be equal to the reference voltage from the ADN8830, VREF = 2.47 V as given in the Specifications table for the Reference Voltage. In this example, the minimum resolution is 11 bits. A 12-bit DAC, such as the AD7390, can be readily found.

It is important that the full-scale voltage input to the DAC is tied to the ADN8830 reference voltage, as shown in Figure 4. This eliminates errors from slight variances of VREF.

Thermistor Fault and Temperature Lock Indications

Both the THERMFAULT (Pin 1) and TEMPLOCK (Pin 5) outputs are CMOS compatible outputs that are active high. THERMFAULT will be a logic low while the thermistor is operating normally and will go to a logic high if a short or open is detected at THERMIN (Pin 2). The trip voltage for THERMFAULT is when THERMIN falls below 0.2 V or exceeds 2.0 V. THERMFAULT provides only an indication of a fault condition and does not activate any shutdown or protection circuitry on the ADN8830. To shut down the ADN8830, a logic low voltage must be asserted on Pin 3, as described in the Shutdown Mode section.

TEMPLOCK will output a logic high when the voltage at THERMIN is within 2.5 mV of TEMPSET. This voltage can be related to temperature by solving for m from Equation 8. For most laser diode applications, 2.5 mV is equivalent to ±0.1°C. If the voltage difference between THERMIN and TEMPSET is greater than 2.5 mV, then TEMPLOCK will output a logic low. The input offset voltage of the ADN8830 is guaranteed to within 250 µV, which for most applications is within ±0.01°C.

Setting the Switching Frequency

The ADN8830 has an internal oscillator to generate the switching frequency for the output stage. This oscillator can be either set in free-run mode or synchronized to an external clock signal. For free-run operation, SYNCIN (Pin 25) should be connected to ground and COMPOSC (Pin 24) should be connected to AVDD. The switching frequency is then set by a single resistor connected from FREQ (Pin 26) to ground. Table I shows R_{FREQ} for some common switching frequencies.

Table I. Switching Frequencies vs. R_{FREQ}

f_{SWITCH}	R_{FREQ}
100 kHz	1.5 MΩ
250 kHz	600 kΩ
500 kHz	300 kΩ
750 kHz	200 kΩ
1 MHz	150 kΩ

For other frequencies, the value for this resistor, R_{FREQ}, should be set to

$$R_{FREQ} = \frac{150 \times 10^9}{f_{SWITCH}} \tag{12}$$

where f_{SWITCH} is the switching frequency in Hz.

Higher switching frequencies reduce the voltage ripple across the TEC. However, high switch frequencies will create more power dissipation in the external transistors. This is due to the more frequent charging and discharging of the transistors' gate capacitances. If large transistors are needed for a high output current application, faster switching frequencies could reduce the overall power efficiency of the circuit. This is covered in detail in the Calculating Power Dissipation and Efficiency section.

The switching frequency of the ADN8830 can be synchronized with an external clock by connecting the clock signal to SYNCIN (Pin 25). Pin 24 should also be connected to an R-C network, as shown in Figure 6. This network is simply used to compensate a PLL to lock on to the external clock. To ensure the quickest synchronization lock-in time, R_{FREQ} should be set to 1.5 MΩ.

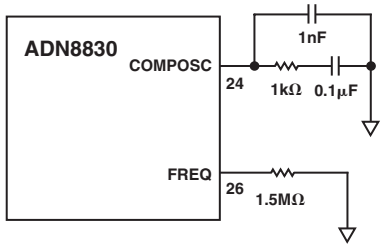


Figure 6. Using an R-C Network on Pin 24 with an External Clock

The relative phase of the ADN8830 internal oscillator compared to the external clock signal can be adjusted. This is accomplished by adjusting the voltage to PHASE (Pin 29) according to TPCs 3 and 4. The phase shift versus voltage can be approximated as

$$Phase\ Shift° = 360° \times \frac{V_{PHASE}}{VREF} \tag{13}$$

where V_{PHASE} is the voltage at Pin 29, and $VREF$ has a typical value of 2.47 V.

To ensure the oscillator operates correctly, V_{PHASE} should remain higher than 100 mV and lower than 2.3 V. This is required for either internal clock or external synchronization operation. A resistor divider from $VREF$ to ground can establish this voltage easily, although any voltage source, such as a DAC, could be used as well. If phase is not a consideration, for example with a single ADN8830 being used, Pin 29 can be tied to Pin 6, which provides a 1.5 V reference voltage.

The phase adjusted output from the ADN8830 is available at SYNCOUT (Pin 28). This pin can be used as a master clock signal for driving other ADN8830 devices. Multiple ADN8830 devices can be either driven from a single master ADN8830 device by connecting its SYNCOUT pin to each slave's SYNCIN pin or daisy-chained by connecting each device's SYNCOUT to the next device's SYNCIN pin.

Phase shifting is useful in systems that use more than one ADN8830 TEC controller. It ensures the ADN8830 devices will not switch at the same time, which could create excessive ripple on the power supply voltage. By adjusting the phase of each device, the switching transients can be spaced equally over the clock period, reducing potential supply ripple and easing the instantaneous current demand from the supply.

Using a single master clock, each slave ADN8830 should have a different value phase shift. For example, with four TEC controllers, one slave device should be set for 90° of phase shift, another for 180°, and the last for 270°. In a daisy-chain configuration, each slave device would be set with equal phase. Using the previous example, each slave would be set to 90° with its SYNCOUT pin connected to the next device's SYNCIN pin. Examples are shown in Figures 7 and 8.

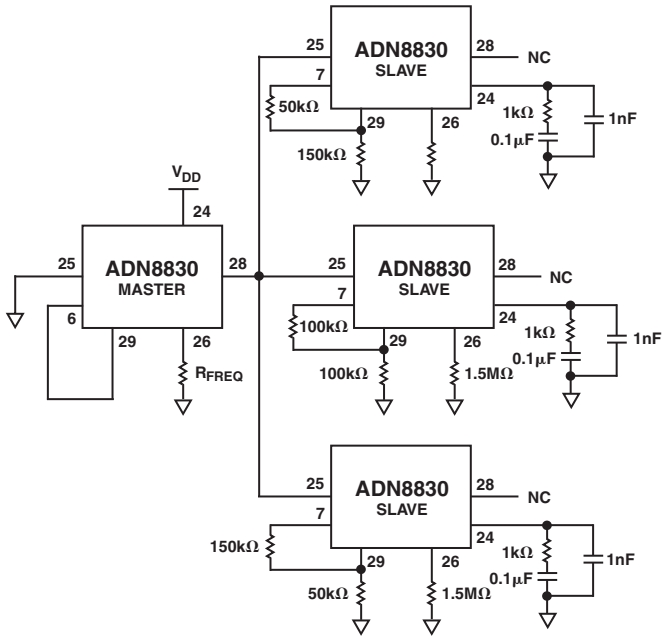


Figure 7. Multiple ADN8830 Devices Driven from a Master Clock

Soft Start on Power-Up

The ADN8830 can be programmed to ramp up for a specified time after the power supply is applied or after shutdown is de-asserted. This feature, known as soft start, is useful for gradually increasing the duty cycle of the PWM amplifier. The soft start time is set with a single capacitor connected from Pin 27 to ground according to Equation 14.

$$\tau_{SS} = 150 \times C_{SS} \quad (14)$$

where C_{SS} is the value of the capacitor in microfarads, and τ_{SS} is the soft start time in milliseconds. To set a soft start time of 15 ms, C_{SS} should equal 0.1 µF. A minimum soft start time of 10 ms is recommended to ensure proper initialization of the ADN8830 on power-up.

Shutdown Mode

The ADN8830 has a shutdown mode that deactivates the output stage and puts the device into a low current standby state. The current draw for the ADN8830 in shutdown is less than 100 µA. The shutdown input, Pin 3, is active low. To shut down the device, Pin 3 should be driven to logic low. Once a logic high is applied, the ADN8830 will reactivate after the delay set by the soft start circuitry. Refer to the Soft Start on Power-Up section for more details on this feature.

Pin 3 should not be left floating as there are no internal pull-up or pull-down resistors. If the shutdown function is not required, Pin 3 should be tied to V_{DD} to ensure the device is always active.

Compensation Loop

The ADN8830 TEC controller has a built-in amplifier dedicated for loop compensation. The exact compensation network is set by the user and can vary from a simple integrator to PI, PID, or any other type of network. The type of compensation and component values should be determined by the user since it will depend on the thermal response of the object and the TEC. One method for determining these values empirically is to input a step function to TEMPSET, thus changing the target temperature, and adjusting the compensation network to minimize the settling time of the object's temperature.

A typical compensation network used for temperature control of a laser module is a PID loop, which consists of a very low frequency pole and two separate zeros at higher frequencies. Figure 9 shows a simple network for implementing PID compensation. An additional pole is added at a higher frequency than the zeros to reduce the noise sensitivity of the control loop. The bode plot of the magnitude is shown in Figure 10.

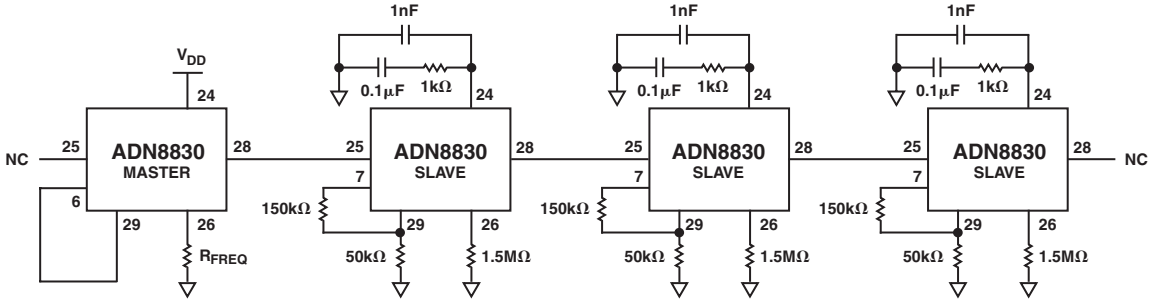


Figure 8. Multiple ADN8830 Devices Using a Daisy Chain

The unity-gain crossover frequency of the feedforward amplifier is given as

$$f_{0dB} = \frac{1}{2\pi R3C1} \times 80 \times TEC\ GAIN \quad (15)$$

To ensure stability, the unity-gain crossover frequency should be lower than the thermal time constant of the TEC and thermistor. However, this thermal time constant may not be specified and can be difficult to characterize.

There are many texts written on loop stabilization, and it is beyond the scope of this data sheet to discuss all methods and trade-offs in optimizing compensation networks. A simple method that can be used to empirically determine a PID compensation loop as shown in Figure 9 involves the following procedure:

1. Connect thermistor and TEC to the ADN8830 application circuit. Power does not need to be applied to the laser diode for this procedure. Monitor output voltage across the TEC with an oscilloscope.
2. Short C1 and open C2, leaving just R1 and R3 as a simple proportional-only compensation loop.
3. While maintaining a constant TEMPSET voltage, increase the ratio of R1/R3, thus increasing the gain until loop oscillation starts to occur. Decrease this ratio by a factor of 2 from the point of oscillation. The R1/R3 ratio will likely be less than unity for most laser modules.
4. Add C1 capacitor and decrease value until oscillation starts, then increase by a factor of 2. A good initial starting value for C1 is to create a unity-gain crossover of 0.1 Hz based on Equation 15.
5. Short R2 and increase C2 until oscillation starts. At this point, either C2 can be decreased or R2 can be added to regain stability. Generally speaking, R2 will be greater than R3 and C2 will be one or more orders of magnitude less than C1.
6. TEMPSET should be adjusted with a step change while observing the output voltage settling time. A step change of 100 mV should suffice. From here, C2, R2, and even C1 can be decreased to minimize settling time at the expense of additional output voltage overshoot.
7. An additional feedback capacitor, CF, in parallel with R1 and C1, can be added to add another high frequency pole. In many cases, this improves the stability of the system without increasing the settling time as out-of-band noise is filtered out of the control signal. A 330 pF to 1 nF capacitor should suffice, if required.

The typical values shown in the typical application circuit in Figure 1 have R1 = 100 kΩ, R2 = 1 MΩ, R3 = 205 kΩ, C1 = 10 µF, C2 = 1 µF, and an additional feedback capacitor of 330 pF. For most pump laser modules, this results in a 10°C TEMPSET step settling time to within 0.1°C in less than 5 seconds.

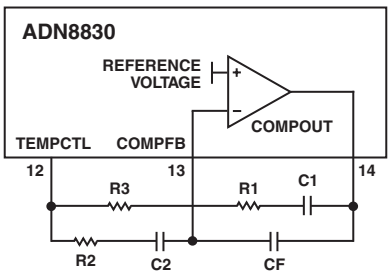


Figure 9. Implementing a PID Compensation Loop

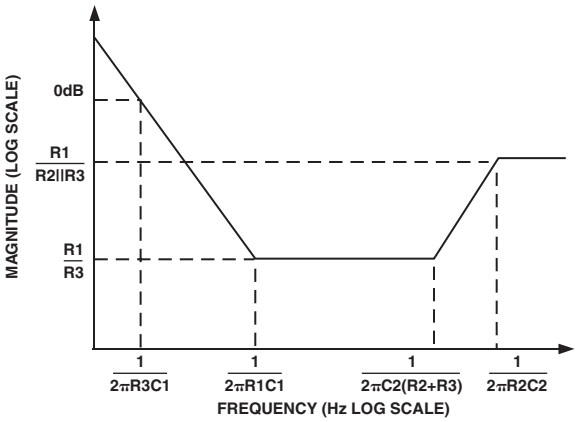


Figure 10. Bode Plot for PID Compensation

Using the TEC Controller ADN8830 with a Wave Locker

Many optical applications require precision control of laser wavelength. The wavelength of the laser diode can be adjusted by changing its temperature, which is done through temperature control of the TEC. Wavelength control can be done by feeding a wave locker or etalon output back to the microprocessor and using the microprocessor to calculate and reinstruct the TEC controller with a new target temperature. However, this method is computationally expensive and has time delays before the adjustment is done. A faster responding and simpler method is to feed the wave locker signal back to the TEC controller for direct temperature control.

The ADN8830 is designed to be compatible with a wave locker controller. Figure 11 shows the basic schematic. The TEMPCTL output from ADN8830 is proportional to the object's actual temperature. This voltage is fed to the wave locker controller. Also fed to the wave locker controller are the photodiode outputs from the wave locker, as well as the laser diode power and a digital signal indicating a functional laser diode, both of which come from the CW controller. The output of the wave locker controller is then connected to the input of the compensation network. This allows the wave locker controller to adjust the TEC temperature based on the current temperature of the object, the current wavelength of the laser diode, and the target wavelength. Once the target wavelength is reached, the wave locker controller sends a signal to the microcontroller indicating that the laser signal is good.

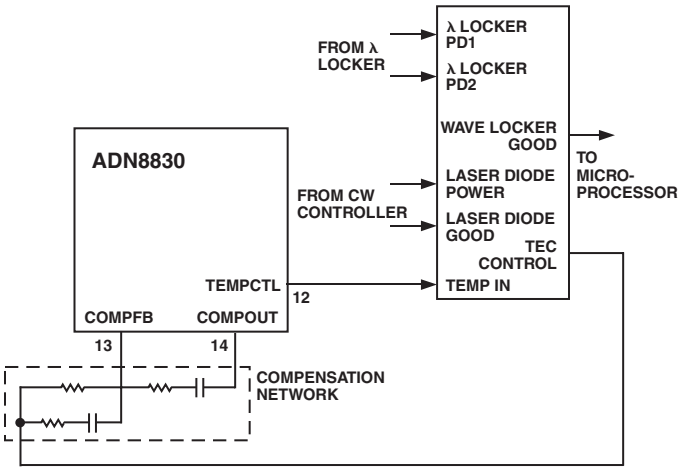


Figure 11. Using the ADN8830 with a Wave Locker

Using TEMPOUT to Measure Temperature

The TEMPOUT pin is a voltage that is proportional to the difference between the target temperature and the measured thermistor temperature. The full equation for the voltage at *TEMPOUT* is

$$TEMPOUT = 1.5 + 3 \times \left(THERMIN - TEMPSET\right) \quad (16)$$

The voltage range of *TEMPOUT* is 0 V to 3.0 V and is independent of power supply voltage.

Setting the Maximum TEC Voltage and Current

The ADN8830 can be programmed for a maximum output voltage to protect the TEC. A voltage from 0 V to 1.5 V applied to the VLIM (Pin 15) input to the ADN8830 sets the maximum TEC voltage, $V_{TEC, MAX}$. This voltage can be set with either a resistor divider or from a DAC. Because the output of the ADN8830 is bidirectional, this voltage sets both the upper and lower limits of the TEC voltage. The equation governing $V_{TEC, MAX}$ is given in Equation 17 and the graph of this equation is shown in Figure 12.

$$V_{TEC, MAX} = \left(1.5V - VLIM\right) \times 4 \quad (17)$$

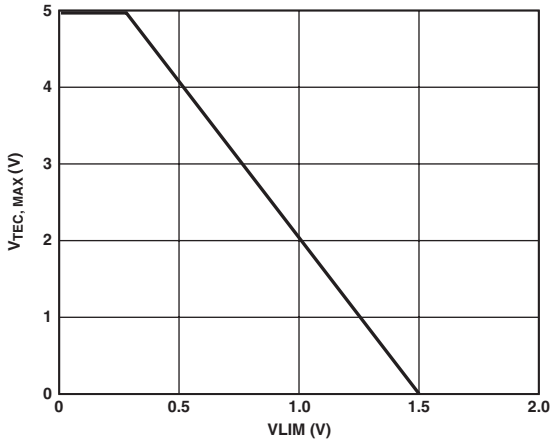


Figure 12. VLIM Voltage vs. Maximum TEC Voltage

If the supply voltage is lower than $V_{TEC, MAX}$, the maximum TEC voltage will obviously be equal to the supply voltage. The voltage to VLIM should not exceed 1.5 V since this causes improper operation of the output voltage limiting circuitry. Setting VLIM to 1.5 V can be used to deactivate the TEC current without shutting down the ADN8830 in the event of a system failure. If a maximum TEC voltage is not required, VLIM should be connected to ground. It is not advisable to leave VLIM floating as this would cause unpredictable output behavior.

This feature should be used to limit the maximum output current to the TEC as specified in the TEC data sheet. For example, if the maximum TEC voltage is specified at 2 V, VLIM should be set to 1 V. The maximum output voltage is then set to ±2 V.

Output Driver Amplifiers

The output voltage across the TEC as measured from Pin 19 to Pin 9 can be monitored at Pin 16. This is labeled as VTEC in the typical application schematic in Figure 1. The voltage at VTEC can vary from 0 V to 3 V independent of the power supply voltage. Its equation is given as

$$VTEC = 0.25 \times \left(V_{OUT\,A} - V_{OUT\,B}\right) + 1.5 \quad (18)$$

where $V_{OUT\,A}$ and $V_{OUT\,B}$ are the voltages at Pins 19 and 9, respectively. The ripple voltage at Pin 19 is filtered out internally and does not appear at VTEC, leaving it as an accurate dc output of the TEC voltage.

The TEC is driven with a differential voltage, allowing current to flow in either direction through the TEC. This can provide heat transfer either to or from the object being regulated without the use of a negative voltage rail. The maximum output voltage across the TEC is set by the voltage at VLIM (Pin 15). Refer to the Setting the Maximum TEC Voltage and Current section for details on this operation. With VLIM set to ground, the maximum output voltage is the power supply voltage, V_{DD}.

To achieve a differential output, the ADN8830 has two separate output stages. OUT A is a switched output or pulse-width modulated (PWM) amplifier, and OUT B is a high gain linear amplifier. Although they achieve the same result, to provide constant voltage and high current, their operation is different. The exact equations for the two outputs are

$$OUT\ A = 4 \times \left(COMPOUT - 1.5\right) + OUT\ B \quad (19)$$

$$OUT\ B = -14 \times \left(COMPOUT - 1.5\right) + 1.5 \quad (20)$$

where *COMPOUT* is the voltage at Pin 13. The voltage at *COMPOUT* is determined by the compensation network that is fed by the input amplifier, which receives its input voltage from TEMPSET and THERMIN. Equation 20 is valid only in the linear region of the linear amplifier. OUT B has a lower limit of 0 V and an upper limit of the power supply.

Because the COMPOUT voltage is not readily known, Equation 20 can be rewritten in terms of the TEC voltage, VTEC, which is defined as OUT B – OUT A.

$$OUT\ B = 4 \times VTEC + 1.5 \quad (21)$$

In Figure 1, Pins 10 and 11 provide the gate drive for Q3 and Q4, which complete the linear output amplifier. This output voltage is fed back to Pin 9 (OUT B) to close its loop. The gate-to-drain capacitance of Q3 and Q4 provide the compensation for the linear amplifier. If using the recommended FDW2520C transistors, it will be necessary to add an additional 2.2 nF of capacitance from the gate to the drain of the PMOS transistor to maintain stability. A 3.3 nF capacitor should also be connected from the drain to ground to prevent small oscillations when there is very little or no current through the TEC.

These extra capacitors are specified only when using FDW2520C transistors in the linear amplifier. If other transistors are used, these values may need to be adjusted. To ensure the linear amplifier is stable, the total gate-to-source capacitance for both Q3 and Q4 should be at least 2.5 nF. Refer to the transistor's data sheet for its typical gate-to-drain capacitance values.

The output of the linear amplifier is proportional to the voltage at Pin 13 (COMPOUT). Because the linear amplifier operates with a gain of 14, its output will typically be at either ground or V_{DD} if there is more than about 100 mA of current flowing through the TEC. This ensures Q3 and Q4 will not be a dominant source of power dissipation at high output currents.

Inductor Selection

In addition to the external transistors, the PWM amplifier requires an inductor and a capacitor at its output to filter the switched output waveform. Proper inductor selection is important to achieve the best efficiency. The duty cycle of the PWM sets the OUT A output voltage and is

$$D = \frac{OUT\ A}{V_{DD}} \tag{22}$$

The average current through the inductor is equal to the TEC current. The ripple current through the inductor, ΔI_L, varies with the duty cycle and is equal to

$$\Delta I_L = \frac{V_{DD} \times D \times (1 - D)}{L \times f_{CLK}} \tag{23}$$

where f_{CLK} is the clock frequency as set by the resistor R_{FREQ} at Pin 26 or an external clock frequency. Refer to the Setting the Switching Frequency section for more information. Selecting a faster switching frequency or a larger value inductor will reduce the ripple current through the inductor. The waveform of the inductor current is shown in Figure 13.

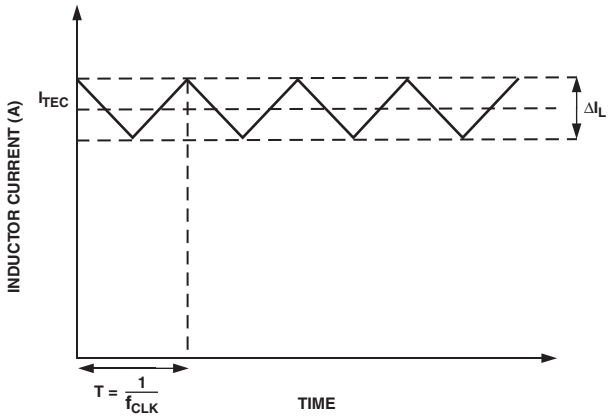


Figure 13. Current Waveform Through Inductor

It is important to select an inductor that can tolerate the maximum possible current that could pass through it. Most TECs are specified with a maximum voltage and current for proper and reliable operation. The maximum instantaneous inductor current can be found as

$$I_{L,MAX} = I_{TEC,MAX} + 0.5 \times \Delta I_L \tag{24}$$

where ΔI_L can be found from Equation 23 with the appropriate duty cycle calculated from Equation 22 with OUT A = $V_{TEC, MAX}$.

Design Example 3

A TEC is specified with a maximum current of 1.5 A and maximum voltage of 2.5 V. The ADN8830 will be operating from a 3.3 V supply voltage with a 200 kHz clock and a 4.7 µH inductor. The duty cycle of the PWM amplifier at 2.5 V is calculated to be 75.8%. Using Equation 23, the inductor ripple current is found to be 664 mA. From Equation 24, the maximum inductor current will be 1.82 A and should be considered when selecting the inductor. Notice that increasing the clock frequency to 1 MHz would reduce $I_{L, MAX}$ to 1.56 A.

Design Example 4

Using the same TEC as above, the ADN8830 will be powered from 5.0 V instead. Here, the duty cycle is 50%, which happens to be the worst-case duty cycle for inductor current ripple. Now DIL equals 1.33 A with a 200 kHz clock, and $I_{L, MAX}$ is 2.83 A. Reducing the inductor ripple current is another compelling reason to operate the ADN8830 from a 3.3 V supply instead.

Table II lists some inductor manufacturers and part numbers along with some key specifications. The column I_{MAX} refers to the maximum current at which the inductor is rated to remain linear. Although higher currents can be pushed through the inductor, efficiency and ripple voltage will be dramatically degraded.

This is by no means a complete list of manufacturers or inductors that can be used in the application. More information on these inductors is available at their websites. Note the trade-offs between inductor height, maximum current, and series resistance. Smaller inductors cannot handle as muèH current and therefore require higher clock speeds to reduce their ripple current. They also have higher series resistance, which can lower the overall efficiency of the ADN8830.

PWM Output Filter Requirements

The switching of Q1 and Q2 creates a pulse width modulated (PWM) square wave from 0 V to V_{DD}. This square wave must be filtered sufficiently to create a steady voltage that will drive the TEC. The ripple voltage across the TEC is a function of the inductor ripple current, the L-C filter cutoff frequency, and the equivalent series resistance (ESR) of the filter capacitor. The equivalent circuit for the PWM side is given in Figure 14.

Table II. Partial List of Inductors and Key Specifications

Inductance (µH)	I_{MAX} (A)	$R_{S, TYP}$ (mΩ)	Height (mm)	Part Number	Manufacturer	Website
4.7	1.1	200	1	LPO1704-472M	Coilcraft	www.coilcraft.com
4.7	1.59	55	2	A918CY-4R7M	Toko	www.toko.com
4.7	3.9	48	2.8	UP2.8B-4R7	Cooper	www.cooperet.com
4.7	1.5	90	3	DO1608C-472	Coilcraft	www.coilcraft.com
4.7	1.32	56	3	CDRH4D28 4R7	Sumida	www.sumida.com
4.7	7.5	12	4.5	892NAS-4R7M	Toko	www.toko.com
4.7*	5.4	18	5.2	DO3316P-472	Coilcraft	www.coilcraft.com
10	2.7	80	2.8	UP2.8B-100	Cooper	www.cooperet.com
15	8	32	8	DO5022P-153HC	Coilcraft	www.coilcraft.com
47	4.5	86	7.1	DO5022P-473	Coilcraft	www.coilcraft.com

*Recommend inductor in typical application circuit Figure 1.

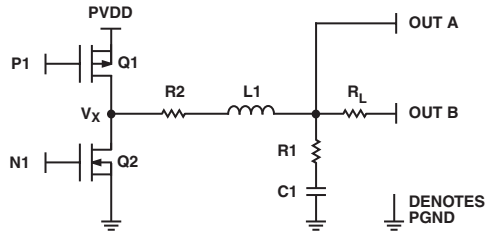


Figure 14. Equivalent Circuit for PWM Amplifier and Filter

In this circuit, R_L is the TEC resistance, R2 is the parasitic resistance of the inductor combined with the equivalent $r_{DS, ON}$ of Q1 and Q2, and R1 is the ESR of C1. The voltage, V_X, is the pulse-width modulated waveform that switches between PVDD and ground. This is a second-order low-pass filter with an exact cutoff frequency of

$$f_C = \frac{1}{2\pi}\sqrt{\frac{R2 + R_L}{(R1 + R_L)C1L1}} \quad (25)$$

Practically speaking, R1 and R2 are several tens of milliohms and are much smaller than the TEC resistance, which can be a few ohms. The cutoff frequency can be roughly approximated as

$$f_C = \frac{1}{2\pi}\sqrt{\frac{1}{C1L1}} \quad (26)$$

This cutoff frequency should be much lower than the clock frequency to achieve adequate filtering of the switched output waveform. Also of importance is the damping factor, ζ, of the L-C filter. Too low a damping factor will result in a longer settling time and could potentially cause stability problems for the temperature control loop. Neglecting R1 and R2 again, the damping factor is simply

$$\zeta = \frac{1}{2R_L}\sqrt{\frac{L1}{C1}} \quad (27)$$

Using the recommended values of L1 = 4.7 µH and C1 = 22 µF results in a cutoff frequency of 15.7 kHz. With a TEC resistance of 2 Ω, the damping factor is 0.12. The cutoff frequency can be decreased to lower the output voltage ripple with slower clock frequencies by increasing L1 or C1. Increasing C1 may appear to be a simpler approach as it would not increase the physical size of the inductor, but there is a potential stability danger in lowering the damping factor too far. It is recommended that ζ remain greater than 0.05 to provide a reasonable settling time for the TEC. Increasing ζ also makes finding the proper PID compensation easier as there is less ringing in the L-C output filter. To allow adequate phase and gain margin for the PWM amplifier, Table III should be used to find the lower limit of cutoff frequency for a given damping factor.

Table III. Minimum L-C Filter Cutoff Frequency vs. Damping Factor

ζ	$f_{C, MIN}$ (kHz)
0.05	8
0.1	4
0.2	2
0.3	1.9
0.5	1.6
> 0.707	1.5

Calculating PWM Output Ripple Voltage

Although it may seem that f_C can be arbitrarily lowered to reduce output ripple, the ripple voltage is also dependent on the ESR of C1, shown as R1 in Figure 14. This resistance creates a zero that turns the second-order filter into a first-order filter at high frequencies. The location of this zero is

$$Z1 = \frac{1}{2\pi R1C1} \quad (28)$$

With a clock frequency greater than Z1, and presumably greater than f_C, the output voltage ripple is

$$\Delta OUT\ A = \Delta I_L \times R1 \quad (29)$$

$$\Delta OUT\ A = \frac{V_{DD}D(1-D)R1}{L1f_{CLK}}\ for\ (f_{CLK} > Z1) \quad (30)$$

The worst-case voltage ripple occurs when the duty cycle of the PWM output is exactly 50%, or when OUT A = 0.5 × V_{DD}. As shown in Equation 31

$$\Delta OUT\ A_{MAX} \approx \frac{V_{DD}R1}{4f_{CLK}L1}\ for\ (f_{CLK} > Z1) \quad (31)$$

Here it can be directly seen that increasing the inductor value or clock frequency will reduce the ripple. Choosing a low ESR capacitor will ensure R1 remains low. Operating from a lower supply voltage will also help reduce the output ripple voltage from the L-C filter. With a clock frequency equal to *Z*1 but presumably greater than f_C, the worst-case output voltage ripple is

$$\Delta OUT\ A_{MAX} = V_{DD}\frac{\left(16R1^2C1^2 f_{CLK}{}^2 + 1\right)}{32L1C1f_{CLK}}\ for\ (f_{CLK} = Z1) \quad (32)$$

Which, if $f_{CLK} < Z1$, can be further simplified to

$$\Delta OUT\ A_{MAX} = \frac{V_{DD}}{32L1C1f_{CLK}{}^2}\ for\ (f_{CLK} < Z1) \quad (33)$$

A typical 100 µF surface-mount electrolytic capacitor can have an ESR of over 100 mΩ, pulling this zero to below 16 kHz, and resulting in an excess of ripple voltage across the TEC. Low ESR capacitors, such as ceramic or polymer aluminum capacitors, are recommended instead. Polymer aluminum capacitors can provide more bulk capacitance per unit area over ceramic ones, saving board space. Table IV shows a limited list of capacitors with their equivalent series resistances.

This is by no means a complete list of all capacitor manufacturers or capacitor types that can be used in the application. The 22 µF capacitor recommended has a maximum ESR of 35 mΩ, which puts Z1 at 207 kHz. Using a 3.3 V supply with the recommended inductor and capacitor listed with a 1 MHz clock frequency will yield a worst-case ripple voltage at OUT A of about 6 mV.

External FET Requirements

External FETs are required for both the PWM and linear amplifiers that drive OUT A and OUT B from the ADN8830. Although it is important to select FETs that can supply the maximum current required to the TEC, they should also have a low enough resistance ($r_{DS, ON}$) to prevent excessive power dissipation and improve efficiency. Other key requirements from these FET pairs are slightly different for the PWM and linear outputs.

The gate drive outputs for the PWM amplifier at P1 (Pin 21) and N1 (Pin 22) have a typical nonoverlap delay of 65 ns. This is done to ensure that one FET is completely off before the other FET is turned on, preventing current from shooting through both simultaneously.

The input capacitance (C_{ISS}) of the FET should not exceed 5 nF. The P1 and N1 outputs from the ADN8830 have a typical output impedance of 6 Ω. This creates a time constant in combination with C_{ISS} of the external FETs equal to 6 Ω × C_{ISS}. To ensure shoot-through does not occur through these FETs, this time constant should remain less than 30 ns.

The linear output from the ADN8830 uses N2 (Pin 10) and P2 (Pin 11) to drive the gates of the linear side FETs, shown as Q3 and Q4 in Figure 1. Local compensation for the linear amplifier is achieved through the gate-to-drain capacitances (C_{GD}) of Q3 and Q4. The value of C_{GD}, which can be determined from the data sheet, is usually referred to as C_{RSS}, the reverse transfer capacitance. The exact C_{RSS} value should be determined from a graph that shows capacitance versus drain-to-source voltage, using the power supply voltage as the appropriate V_{DS}.

To ensure stability of the linear amplifier, the total C_{GD} of the PMOS device, Q3, should be greater than 2.5 nF and the total C_{GD} of the NMOS should be greater than 150 pF. External capacitance can be added around the FET to increase the effective C_{GD} of the transistor. This is the function of C6 in the typical application schematic shown in Figure 1. If external capacitance must be added, it will generally only be required around the PMOS transistor.

In the event of zero output current through the TEC, there will be no current flowing through Q3 and Q4. In this condition, these FETs will not provide any small signal gain and thus no negative feedback for the linear amplifier. This leaves only a feedforward signal path through C_{GD}, which could cause a settling problem at OUT B. This is often seen as a small signal oscillation at OUT B, but only when the TEC is at or very near zero current.

The remedy for this potential minor instability is to add capacitance from OUT B to ground. This may need to be determined empirically, but a good starting point is 1.5 times the total C_{GD}. This is the function of C12 in Figure 1. Note that while adding more C_{GD} around Q3 and Q4 will help to ensure stability, it could potentially increase instability in the zero current dead band region, requiring additional capacitance from OUT B to ground.

Bear in mind that the addition of these capacitors is only for local stabilization. The stability of the entire TEC application may need adjustment, which should be done around the compensation amplifier. This is covered in the Compensation Loop section.

There is one additional consideration for selecting both the linear output FETs; they must have a minimum threshold voltage (V_T) of 0.6 V. Lower threshold voltages could cause shoot-through current in the linear output transistors.

Table V shows the recommended FETs that can be used for the linear output in the ADN8830 application. Table V includes the appropriate external gate-to-drain capacitance (external C_{GD}) and snubber capacitor value (C_{SNUB}) connected from OUT B to ground that should be added to ensure local stability. Table VI shows the recommended PWM output FETs. Although other transistors can be used, these combinations have been tested and are proved stable and reliable for typical applications.

Data sheets for these devices can be found at their respective websites:

Fairchild – www.fairchildsemi.com
Vishay Siliconix – www.vishay.com
International Rectifier – www.irf.com

Calculating Power Dissipation and Efficiency

The total efficiency of the ADN8830 application circuit is simply the ratio of the output power to the TEC divided by the total power delivered from the supply. The idea in minimizing power dissipation is to avoid both drawing additional power and reducing heat generated from the circuit. The dominant sources of power dissipation will include resistive losses, gate charge loss, core loss from the inductor, and the current used by the ADN8830 itself.

The on-channel resistance of both the linear and PWM output FETs will affect efficiency primarily at high output currents. Because the linear amplifier operates in a high gain configuration, it will be at either ground or V_{DD} when significant current is flowing through the TEC. In this condition, the power dissipation through the linear output FET will be

$$P_{FET,LIN} = r_{DS,ON} \times I_{TEC}^{2} \quad (34)$$

using either the $r_{DS,ON}$ for the NMOS or the PMOS depending on the direction of the current flow. In the typical application setup in Figure 2, if the TEC is cooling the target object, the PMOS is sourcing the current. If the TEC is heating the object, the NMOS will be sinking current.

Table IV. Partial List of Capacitors and Key Specifications

Value (μF)	ESR (mΩ)	Voltage Rating (V)	Part Number	Manufacturer	Website
10	60	6.3	NSP100M6.3D2TR	NIC Components	www.niccomp.com
22*	35	8	ESRD220M08B	Cornell Dubilier	www.cornell-dubilier.com
22	35	8	NSP220M8D5TR	NIC Components	www.niccomp.com
22	35	8	EEFFD0K220R	Panasonic	www.maco.panasonic.co.jp
47	25	6.3	NSP470M6.3D2TR	NIC Components	www.niccomp.com
68	18	8	ESRD680M08B	Cornell Dubilier	www.cornell-dubilier.com
100	95	10	594D107X_010C2T	Vishay	www.vishay.com

*Recommend capacitor in typical application circuit Figure 1.

Although the FETs that drive OUT A alternate between Q1 and Q2 being on, they have an equivalent series resistance that is equal to a weighted average of their $r_{DS, ON}$ values.

$$R_{EQIV} = D \times r_{DS, P1} + (1 - D) \times r_{DS, N1} \quad (35)$$

The resistive power loss from the PWM transistors is then

$$P_{FET, PWM} = R_{EQIV} \times I_{TEC}^{2} \quad (36)$$

There is also a power loss from the continuing charging and discharging of the gate capacitances on Q1 and Q2. The power dissipated due to gate charge loss (P_{GCL}) is

$$P_{GCL} = \frac{1}{2} C_{ISS} V_{DD}^{2} f_{CLK} \quad (37)$$

using the appropriate input capacitance (C_{ISS}) for the NMOS and PMOS. Both transistors are switching, so P_{GCL} should be calculated for each one and will be added to find the total power dissipated from the circuit.

The series resistance of the inductor, *R*2 from Figure 14, will also exhibit a power dissipation equal to

$$P_{R2} = R2 \times I_{TEC}^{2} \quad (38)$$

Core loss from the inductor arises as a result of nonidealities of the inductor. Although this is difficult to calculate explicitly, it can be estimated as 80% of P_{RLS} at 1 MHz switching frequencies and 50% of P_{RL} at 100 kHz. Judging conservatively

$$P_{LOSS} = 0.8 \times P_{RL} \quad (39)$$

Finally, the power dissipated by the ADN8830 is equal to the current used by the device multiplied by the supply voltage. Again, this exact equation is difficult to determine as we have already taken into account some of the current while finding the gate charge loss. A reasonable estimate is to use 40 mA as the total current used by the ADN8830. The power dissipated from the device itself is

$$P_{ADN8830} = V_{DD} \times 10\ mA \quad (40)$$

There are certainly other minor mechanisms for power dissipation in the circuit. However, a rough estimate of the total power dissipated can be found by summing the preceding power dissipation equations. *Efficiency* is then found by comparing the power dissipated with the required output power to the load.

$$Efficiency = \frac{P_{LOAD}}{P_{LOAD} + P_{DISS, TOT}} \quad (41)$$

where

$$P_{LOAD} = I_{LOAD} \times V_{LOAD}$$

The measured efficiency of the system will likely be less than the calculated efficiency. Measuring the efficiency of the application circuit is fairly simple but must be done in an exact manner to ensure the correct numbers are being measured. Using two high current, low impedance ammeters and two voltmeters, the circuit should be set up as shown in Figure 15.

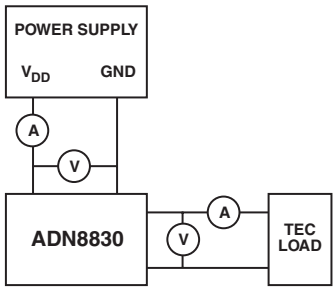


Figure 15. Measuring Efficiency of the ADN8830 Circuit

Table V. Recommended FETs for Linear Output Amplifier

Part Number	Type	C_{GD} (nF)	Ext. C_{GD} (nF)	C_{SNUB} (nF)	$r_{DS, ON}$ (mΩ)	I_{MAX} (A)	Manufacturer
FDW2520C*	NMOS	0.17			18	6.0	Fairchild
	PMOS	0.15	2.2	3.3	35	4.5	Fairchild
IRF7401	NMOS	0.5			22	8.7	International Rectifier
IRF7233	PMOS	2.2	1.0	3.3	20	9.5	International Rectifier
FDR6674A	NMOS	0.23			9.5	11.5	Fairchild
FDR840P	PMOS	0.6	1.0	3.3	12	10	Fairchild

*Recommend transistors in typical application circuit Figure 1.

Table VI. Recommended FETs for PWM Output Amplifier

Part Number	Type	C_{ISS} (nF)	$r_{DS,ON}$ (mΩ)	Continuous I_{MAX} (A)	Manufacturer
FDW2520C*	NMOS	1.33	18	6.0	Fairchild
	PMOS	1.33	35	4.5	Fairchild
Si7904DN	NMOS	1.0	30	5.3	Vishay Siliconix
Si7401DN	PMOS	3.5	17	7.3	Vishay Siliconix
IRF7401	NMOS	1.6	22	8.7	International Rectifier
IRF7404	PMOS	1.5	40	6.7	International Rectifier

*Recommend transistors in typical application circuit Figure 1.

The voltmeter to the TEC or output load should include the series ammeter since the power delivered to the ammeter is considered part of the total output power. However, the voltmeter measuring the voltage delivered to the ADN8830 circuit should not include the series ammeter from the power supply. This prevents a false supply voltage power measurement since we are interested only in the supply voltage power delivered to the ADN8830 circuit. Figures 16 and 17 show some efficiency measurements using the typical application circuit shown in Figure 1.

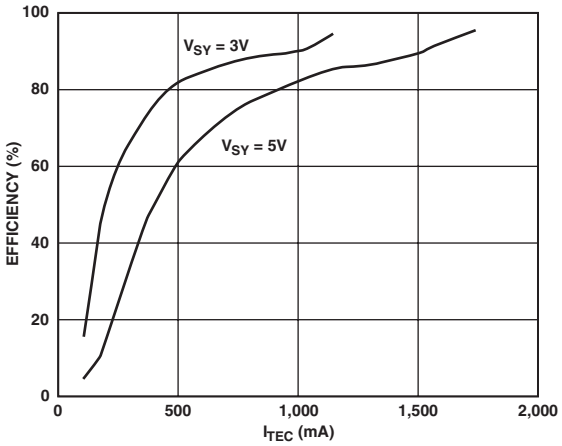


Figure 16. Efficiency with f_{CLK} = 1 MHz

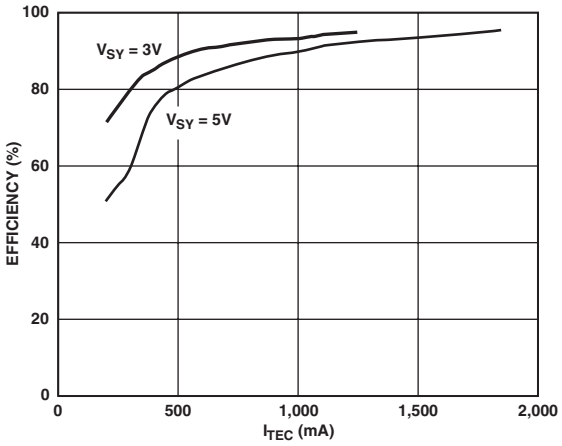


Figure 17. Efficiency with f_{CLK} = 200 kHz

Note that higher efficiency can be achieved using a lower supply voltage or a slower clock frequency. This is due to the fact that the dominant source of power dissipation at high clock frequencies is the gate charge loss on the PWM transistors.

Layout Considerations

The two key considerations for laying out the board for the ADN8830 are to minimize both the series resistance in the output and the potential noise pickup in the precision input section. The best way to accomplish both of these objectives is to divide the layout into two sections, one for the output components and the other for the remainder of the circuit. These sections should have independent power supply and ground current paths that are each connected together at a single point near the power supply. This is used to minimize power supply and ground voltage bounce on the more sensitive input stages to the ADN8830 caused by the switching of the PWM output. Such a layout technique is referred to as a "star" ground and supply connection. Figure 18 shows a block diagram of the concept.

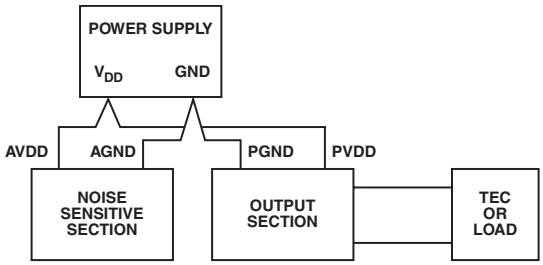


Figure 18. Using Star Connections to Minimize Noise Pickup from Switched Output

The low noise power and ground are referred to as AVDD and AGND, with the output supply and ground paths labeled PVDD and PGND. These pins are labeled on the ADN8830 and should be connected appropriately. Both sets of external FETs should be connected to PVDD and PGND. All output filtering and PVDD supply bypass capacitors should be connected to PGND.

All remaining connections to ground and power supply should be done through AVDD and AGND. A 4-layer board layout is recommended for best performance with split power and ground planes between the top and bottom layers. This provides the lowest impedance for both supply and ground points. Setting the ADN8830 above the AGND plane will reduce the potential noise injection into the device. Figure 19 shows the top layer of the layout used for the ADN8830 evaluation boards, highlighting the power and ground split planes.

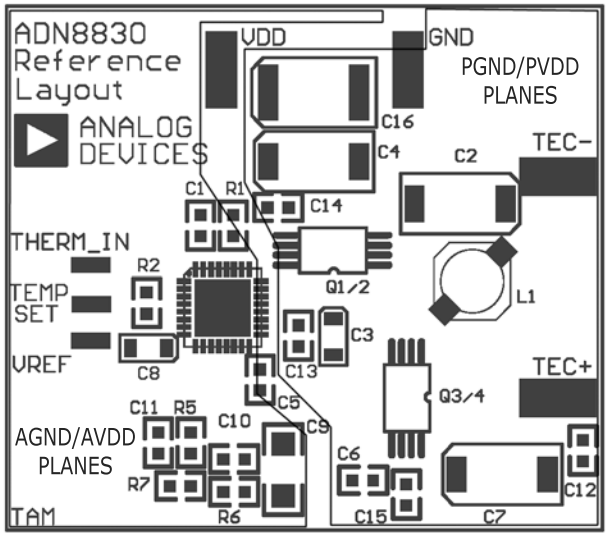


Figure 19. Top Layer Reference Layout for ADN8830

Proper supply voltage bypassing should also be taken into consideration to minimize the ripple voltage on the power supply. A minimum bypass capacitance of 10 µF should be placed in close proximity to each component connected to the power supply. This includes Pins 8 and 20 on the ADN8830 and both external PMOS transistors. An additional 0.1 µF capacitor should be placed in parallel to each 10 µF capacitor to provide bypass for high frequency noise. Using a large bulk capacitor, 100 µF or greater, in parallel with a low ESR capacitor where AVDD and PVDD connect will further improve voltage supply ripple. This is covered in more detail in the Power Supply Ripple section.

Power Supply Ripple

Minimizing ripple on the power supply voltage can be an important consideration, particularly in signal source laser applications. If the laser diode is operated from the same supply rail as the TEC controller, ripple on the supply voltage could cause inadvertent modulation of the laser frequency. As most laser diodes are driven from a 5 V supply, it is recommended the ADN8830 be operated from a separate 3.3 V regulated supply unless higher TEC voltages are required. Operation from 3.3 V also improves efficiency, thus minimizing power dissipation.

The power supply ripple is primarily a function of the supply bypass capacitance, also called bulk capacitance, and the inductor ripple current. Similar to the L-C filter at the PWM amplifier output, using more capacitance with low equivalent series resistance (ESR) will lower the supply ripple. A larger inductor value will reduce the inductor ripple current, but this may not be practical in the application. A recommended approach is to use a standard electrolytic capacitor in parallel with a low ESR capacitor. A surface-mount 220 µF electrolytic in parallel with a 22 µF polymer aluminum low ESR capacitor can occupy an approximate total board area of only 0.94 square inches or 61 square millimeters. Using these capacitors along with a 4.7 µH inductor can yield a supply ripple of less than 5 mV.

High frequency transient spikes may appear on the supply voltage as well. This is due to the fast switching times on the PWM transistors and the sharp edges of their gate voltages. Although these transient spikes can reach several tens of millivolts at their peak, they typically last for less than 20 ns and have a resonance greater than 100 MHz. Additional bulk capacitance will not appreciably affect the level of these spikes as such capacitance is not reactive at these frequencies. Adding 0.01 µF ceramic capacitors on the supply line near the PWM PMOS transistor can reduce this switching noise. Inserting an RF inductor with a High-Q around 100 MHz in series with PVDD will also block this noise from traveling back to the power supply.

Setting Maximum Output Current and Short-Circuit Protection

Although the maximum output voltage can be programmed through VLIM to protect the TEC from overvoltage damage, the user may wish to protect the ADN8830 circuit from a possible short circuit at the output. Such a short could quickly damage the external FETs or even the power supply since they would attempt to drive excessive current. Figure 20 shows a simple modification that will protect the system from an output short circuit.

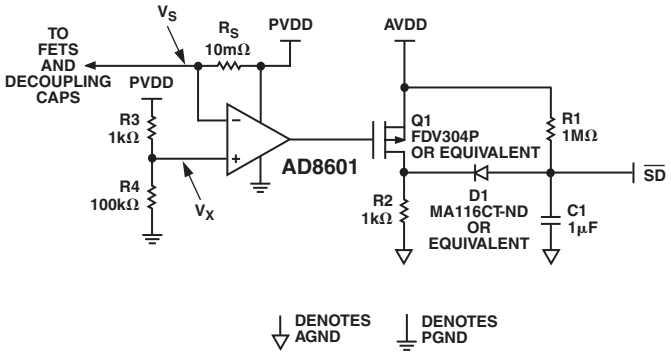


Figure 20. Implementing Output Short-Circuit Protection

A 10 mΩ resistor placed in series with the PVDD supply line creates a voltage drop proportional to the absolute value of the output current. The AD8601 is a CMOS amplifier that is configured as a comparator. As long as the voltage at its inverting input (V_S) exceeds the voltage set by the resistor divider at the noninverting input (V_X), the gate of Q1 will remain at ground. This leaves Q1 on, effectively connecting D1 to the positive rail and leaving the voltage on C1 at V_{DD}. Should enough current flow through R_S to drop V_S below V_X, Q1 will turn off and C1 will discharge through R2 down to a logic low to activate the ADN8830 shutdown. Once V_S returns to a voltage greater than V_X, Q1 will turn back on and C1 will charge back to V_{DD} through R1. The shutdown and reactivation time constants are approximately

$$\tau_{SD} = C1 \times R1$$
$$\tau_{ON} = C1 \times R1 \quad (42)$$

The shutdown time constant should be a minimum of 10 clock cycles to ensure high current switching transients do not trigger a false activation. If powered from 5 V, the circuit shown will shut down the ADN8830 should PVDD deliver over 5 A for more than 1 ms. After shutdown, the circuit will reactivate the ADN8830 in about 1 second.

The voltage drop across R_S is found as

$$V_{R_S} = \frac{I_{OUT}{}^2 R_L R_S}{\eta V_{DD}} \quad (43)$$

where R_L is the load resistance or resistance of the TEC and η is the efficiency of the system. An estimate of efficiency can be calculated either from the Calculating Power Dissipation and Efficiency section or from Figures 16 and 17. A reasonable approximation is η = 0.85. Although the exact resistance of a TEC varies with temperature, an estimation can be made by dividing the maximum voltage rating of the TEC by its maximum current rating.

In addition to providing protection against a short at the output, this circuit will also protect the FETs against shoot-through current. Shoot-through will not occur when using the recommended transistors and additional capacitance shown in Tables V and VI. However, if different transistors are used where their shoot-through potential is unknown, implementing the short-circuit protection circuit will unconditionally protect these transistors.

To set a maximum output current limit, use the circuit in Figure 21. This circuit can share the 10 mΩ power supply shunt resistor as the short-circuit protection circuit to sense the output current. In normal operation Q1 is on, pulling the ADN8830 VLIM pin down to the voltage set by VLIMIT. This sets the maximum output voltage limit as described in the Setting the Maximum TEC Voltage and Current section.

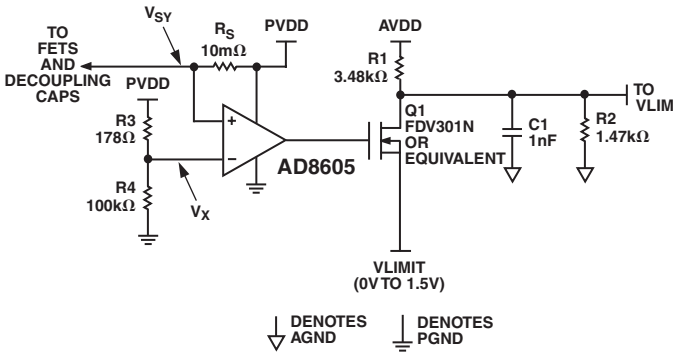


Figure 21. Setting a Maximum Output Current Limit

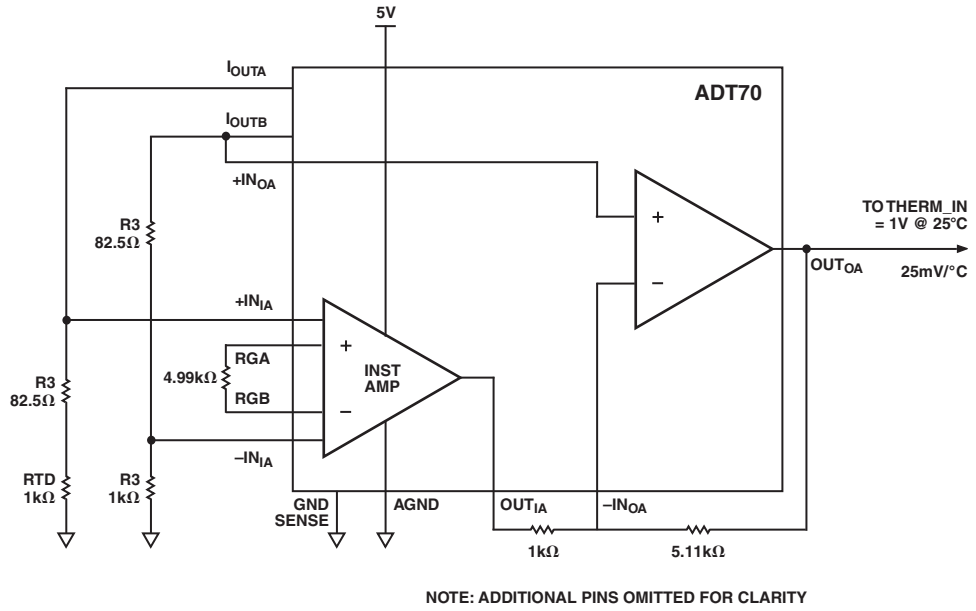


Figure 22. Using an RTD for Temperature Feedback to the ADN8830

If the voltage at V_{SY} drops below V_X, Q1 is turned off and the VLIM pin will be set to 1.5 V, effectively setting the maximum voltage across the outputs to 0 V. The voltage divider for V_X is calculated from Equation 43.

Design Example 5

A maximum output current limit needs to be set at 1.5 A for a TEC with a maximum voltage rating of 2.5 V. The ADN8830 is powered from 5 V. The TEC resistance is estimated at 1.67 Ω and efficiency at 85%. Using Equation 43, the voltage drop across R_S will be 8.8 mV when 1.5 A is delivered to the TEC. The trip voltage V_X is set to 4.991 V with R3 = 178 Ω and R4 = 100 kΩ as shown in Figure 21. To set the output voltage limit to 2.5 V, the voltage at VLIMIT should be set to 0.875 V according to Equation 17.

The C1 capacitor is added to smooth the voltage transitions at VLIM. Once an overcurrent condition is detected, the output voltage will turn down to 0 V within 30 ms.

For a more exact measurement of the output current, place a sense resistor in series with the output load, as shown in Figure 23. The AD626 instrumentation amplifier is set for a gain of 100 with a reference voltage of 2.47 V from VREF. The output of the AD626 is equal to $100 \times R_S \times I_L$ and is fed to the AD8602, which is set up as a window comparator. With V_X greater than VLO but less than VHI, VLIM will be pulled down to the voltage at VLIMIT. Should V_X fall outside the voltage window, VLIM will be pulled to 1.5 V as in Figure 21. The trip points should be set according to

$$VHI = VREF + 100 \times R_S I_{LIMIT+}$$
$$VLO = VREF - 100 \times R_S I_{LIMIT-} \quad (44)$$

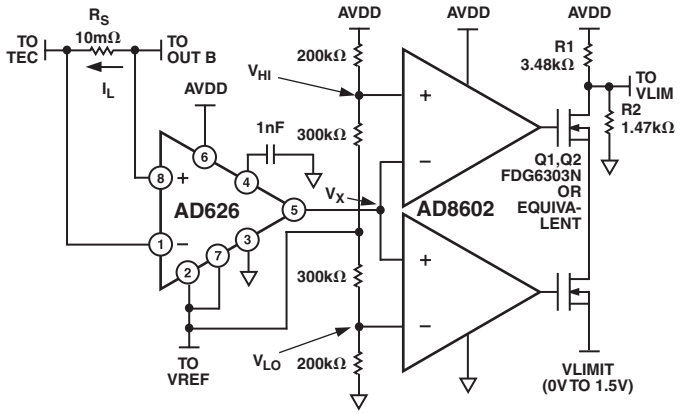


Figure 23. High Accuracy Output Current Limit

The upper and lower trip point voltages can be set independently, allowing different maximum output current limits depending on the direction of the current. The resistor divider for VHI and VLO is tapped to VREF to maintain window accuracy with any changes in VREF. Using the values from Figure 23 with a 5 V supply, the output current will not exceed 1.5 A in either direction.

Adding the current sensing resistor will slightly reduce efficiency. The power dissipated by this resistor is $D \times ITEC2 \times R_S$ if the TEC is heating, or $(1–D) \times ITEC2 \times R_S$ if the TEC is cooling. Include this when calculating efficiency as described in the Calculating Power Dissipation and Efficiency section.

Using an RTD for Temperature Sensing

The ADN8830 can be used with a resistive temperature device (RTD) as the temperature feedback sensor. The resistance of an RTD is linear with respect to temperature, offering an advantage over thermistors that have an exponential relationship to temperature. A constant current applied through an RTD will yield a voltage proportional to temperature. However, this voltage could be on the order of only 0.5 mV/°C, thus requiring the use of additional amplification to achieve a usable signal level.

The ADT70 from Analog Devices can be used to bias and amplify the voltage across an RTD, which can then be fed directly to the THERMIN pin on the ADN8830 to provide temperature feedback for the TEC controller. The ADT70 uses a 0.9 mA current source to drive the RTD and an instrumentation amplifier with adjustable gain to boost the RTD voltage. Application notes and typical schematics for this device can be found in the ADT70 Data Sheet.

Most RTDs have a positive temperature coefficient, also called tempco, as opposed to thermistors, which have a negative tempco. For the OUT A output to drive the TEC– input as shown in Figure 1, the signal from an RTD must be conditioned to create a negative tempco. This can be easily done using an inverting amplifier. Alternately, OUT A can be connected to drive TEC+ with OUT B driving TEC– with a positive tempco at THERMIN. This is highlighted in the Output Driver Amplifiers section.

For the ADN8830, proper operation care should be taken to ensure the voltage at THERMIN remains within 0.4 V and 2.0 V. Using a 1 kΩ RTD with the ADT70 will yield a THERMIN voltage of 0.9 V at 25°C. Using the application circuit shown in Figure 22 will provide a nominal output voltage of 1.0 V at 25°C and a total gain of 66.7 mV/Ω. Using an RTD with a temperature coefficient of 0.375 Ω/°C will give a THERMIN voltage swing from 1.5 V at 5°C to 0.5 V at 45°C, well within the input range of the ADN8830.

Using a Resistive Load as a Heating Element

The ADN8830 can be used in applications that do not necessarily drive a TEC but require only a high current output into a load resistance. Such applications generally only require heating above ambient temperature and simply use the power dissipated by the load element to accomplish this. Because the power dissipated by such an element is proportional to the square of the output voltage, the ADN8830 application circuit must be modified. Figure 24 shows the preferred method for driving a heating element load.

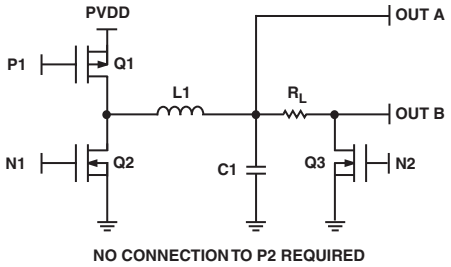
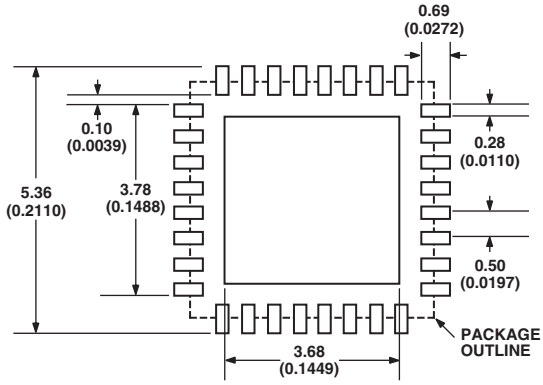


Figure 24. Using the ADN8830 to Drive a Heating Element

Current is delivered from the PWM amplifier through Q3 when the voltage at THERMIN is lower than TEMPSET. If the object temperature is greater than the target temperature, Q3 will turn off and the current through the load goes to zero, allowing the object to cool back toward the ambient temperature. As the target temperature is approached, a steady output current should be reached. Naturally, a proper compensation network must be found to ensure stability and adequate temperature settling time. The P2 output from the ADN8830 should be left unconnected.

Suggested Pad Layout for CP-32 Package

Figure 25 shows the dimensions for the PC board pad layout for the ADN8830, which is a 5 × 5, 32-lead lead frame chipscale package. This package has a metallic heat slug that should be soldered to a copper pad on the PC board. Although the package slug is electrically connected to the substrate of the IC, the copper pad should be left electrically floating. This prevents potential noise injection into the substrate while maintaining good thermal conduction to the PC board.



CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

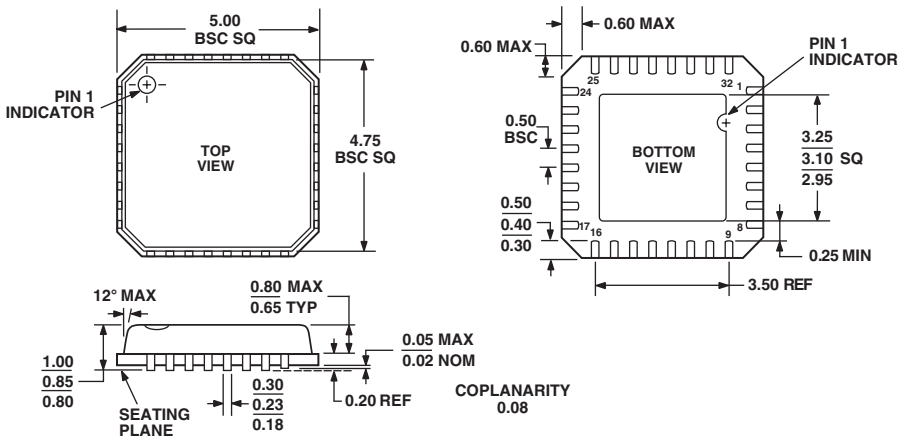
THERMAL PAD SHOULD BE SOLDERED TO AN ELECTRICALLY FLOATING PAD ON THE PC BOARD

Figure 25. Suggested PC Board Layout for CP-32 Pad Landing

OUTLINE DIMENSIONS

32-Lead Lead Frame Chip Scale Package [LFCSP]
(CP-32-1)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VHHD-2

Revision History

Location	Page
11/03—Data Sheet Changed from REV. B to REV. C.	
Changes to ORDERING GUIDE	3
Deleted Figure 24	21
Deleted Boosting the Output Voltage section	22
Deleted Figure 26	22
Deleted Equations 45, 46 and 47	22
Updated OUTLINE DIMENSIONS	23
8/03—Data Sheet Changed from REV. A to REV. B.	
Updated ORDERING GUIDE	3
Updated Thermistor Setup section	8
Updated OUTLINE DIMENSIONS	23
2/03—Data Sheet changed from REV. 0 to REV. A.	
Renumbered Figures	Universal
Change to Thermistor Setup section	8
Change to Figure 14	15
Change to Figure 23	20
Change to Figure 25	21
Update OUTLINE DIMENSIONS	23