480 MHz Single-Supply (5 V) Triple 2:1 Multiplexers

AD8186/AD8187

FEATURES

- Fully Buffered Inputs and Outputs
- Fast Channel-to-Channel Switching: 4 ns
- Single-Supply Operation (5 V)
- High Speed:
  - 480 MHz Bandwidth (–3 dB) 2 V p-p
  - >1600 V/μs (G = +1)
  - >1500 V/μs (G = +2)
- Fast Settling Time of 7 ns to 0.1%
- Low Current: 19 mA/20 mA
- Excellent Video Specifications (R_L = 150 Ω)
- 0.05% Differential Gain Error
- 0.05° Differential Phase Error
- Low Glitch
- All Hostile Crosstalk
  - –84 dB @ 5 MHz
  - –52 dB @ 100 MHz
- High Off Isolation of –95 dB @ 5 MHz
- Low Cost
- Fast, High Impedance Disable Feature for Connecting Multiple Outputs
- Logic-Shifted Outputs

APPLICATIONS

- Switching RGB in LCD and Plasma Displays
- RGB Video Switchers and Routers

GENERAL DESCRIPTION

The AD8186 (G = +1) and AD8187 (G = +2) are high speed, single-supply, triple 2-to-1 multiplexers. They offer –3 dB large signal bandwidth of over 480 MHz along with a slew rate in excess of 1500 V/μs. With better than –80 dB of all hostile crosstalk and –95 dB OFF isolation, they are suited for many high speed applications. The differential gain and differential phase error of 0.05% and 0.05°, along with 0.1 dB flatness to 85 MHz, make the AD8186 and AD8187 ideal for professional and component video multiplexing. They offer 4 ns switching time, making them an excellent choice for switching video signals while consuming less than 20 mA on a single 5 V supply (100 mW). Both devices have a high speed disable feature that sets the outputs into a high impedance state. This allows the building of larger input arrays while minimizing OFF channel output loading. The devices are offered in a 24-lead TSSOP package.

FUNCTIONAL BLOCK DIAGRAM

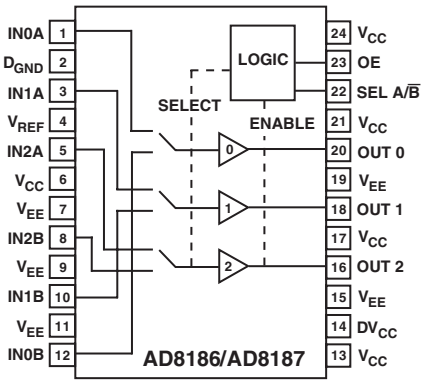

Table I. Truth Table

SEL A/$\overline{B}$	OE	OUT
0	0	High Z
1	0	High Z
1	1	IN A
0	1	IN B

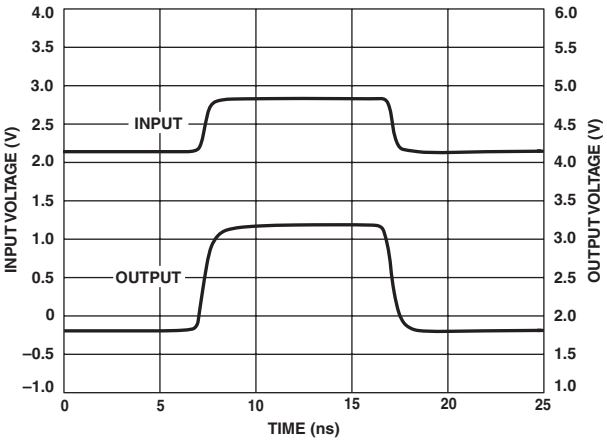

Figure 1. AD8187 Video Amplitude Pulse Response, V_{OUT} = 1.4 V p-p, R_L = 150 Ω

REV. A

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AD8186/AD8187–SPECIFICATIONS

(T_A = 25°C; AD8186: V_S = 5 V, R_L = 1 kΩ to 2.5 V; AD8187: V_S = 5 V, V_{REF} = 2.5 V, R_L = 150 Ω to 2.5 V; unless otherwise noted.)

Parameter	Conditions	AD8186/AD8187 Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Bandwidth (Small Signal)	V_{OUT} = 200 mV p-p		1000/1000		MHz
–3 dB Bandwidth (Large Signal)	V_{OUT} = 2 V p-p		450/480		MHz
0.1 dB Flatness	V_{OUT} = 200 mV p-p		90/85		MHz
Slew Rate (10% to 90% Rise Time)	V_{OUT} = 2 V p-p, R_L = 150 Ω		1600/1500		V/µs
Settling Time to 0.1%	V_{IN} = 1 V Step, R_L = 150 Ω		6/7.5		ns
NOISE/DISTORTION PERFORMANCE					
Differential Gain	3.58 MHz, R_L = 150 Ω		0.05/0.05		%
Differential Phase	3.58 MHz, R_L = 150 Ω		0.05/0.05		Degrees
All Hostile Crosstalk	5 MHz		–84/–78		dB
	100 MHz		–52/–48		dB
Channel-to-Channel Crosstalk, RTI	5 MHz		–90/–85		dB
OFF Isolation	5 MHz		–84/–95		dB
Voltage Noise, RTI	f = 100 kHz to 100 MHz		7/9		nV/√Hz
DC PERFORMANCE					
Voltage Gain Error	No Load		0.1/0.1	±0.3/0.6	%
Voltage Gain Error Matching	Channel A to Channel B		0.04/0.04	±0.2/0.2	%
V_{REF} Gain Error	1 kΩ Load		0.04	±0.6	%
Input Offset Voltage			0.2/0.5	±6.5/7.0	mV
	T_{MIN} to T_{MAX}		±8.0		mV
Input Offset Voltage Matching	Channel A to Channel B		0.2/0.2	±5.0/5.5	mV
Input Offset Drift			10/5		µV/°C
Input Bias Current			1.5/1.5	4/4	µA
V_{REF} Bias Current (for AD8187 only)			1.0		µA
INPUT CHARACTERISTICS					
Input Resistance	@100 kHz		1.8/1.3		MΩ
Input Capacitance			0.9/1.0		pF
Input Voltage Range (About Midsupply)	IN0A, IN0B, IN1A, IN1B, IN2A, IN2B		±1.2/±1.2		V
	V_{REF}		+0.9, –1.2		V
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 1 kΩ	3.1/2.8	3.2/3.0		V p-p
	R_L = 150 Ω	2.8/2.5	3.0/2.7		V p-p
Short Circuit Current			85		mA
Output Resistance	Enabled @ 100 kHz		0.2/0.35		Ω
	Disabled @ 100 kHz		1000/600		kΩ
Output Capacitance	Disabled		1.5/2.0		pF
POWER SUPPLY					
Operating Range		3.5		5.5	V
Power Supply Rejection Ratio	+PSRR, V_{CC} = 4.5 V to 5.5 V, V_{EE} = 0 V		–72/–61		dB
	–PSRR, V_{EE} = –0.5 V to +0.5 V, V_{CC} = 5.0 V		–76/–72		dB
Quiescent Current	All Channels ON		18.5/19.5	21.5/22.5	mA
	All Channels OFF		3.5/4.5	4.5/5.5	mA
	T_{MIN} to T_{MAX}, All Channels ON	15		23	mA

Parameter	Conditions	AD8186/AD8187 Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS					
Channel-to-Channel Switching Time	50% Logic to 50% Output Settling, INA = +1 V, INB = –1 V		3.6/4		ns
ENABLE to Channel ON Time	50% Logic to 50% Output Settling, INPUT = 1 V		4/3.8		ns
DISABLE to Channel OFF Time	50% Logic to 50% Output Settling, INPUT = 1 V		17/5		ns
Channel Switching Transient (Glitch)	All Channels Grounded		21/45		mV
Output Enable Transient (Glitch)	All Channels Grounded		64/118		mV
DIGITAL INPUTS					
Logic 1 Voltage	SEL A/$\overline{B}$, OE Inputs	1.6			V
Logic 0 Voltage	SEL A/$\overline{B}$, OE Inputs			0.6	V
Logic 1 Input Current	SEL A/$\overline{B}$, OE = 2.0 V		45		nA
Logic 0 Input Current	SEL A/$\overline{B}$, OE = 0.5 V		2		μA
OPERATING TEMPERATURE RANGE					
Temperature Range	Operating (Still Air)	–40		+85	°C
θ_{JA}	Operating (Still Air)		85		°C/W
θ_{JC}	Operating		20		°C/W

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1, 2, 3, 4]

Supply Voltage	5.5 V
DV_{CC} to D_{GND}	5.5 V
DV_{CC} to V_{EE}	8.0 V
V_{CC} to D_{GND}	8.0 V
IN0A, IN0B, IN1A, IN1B, IN2A, IN2B, V_{REF}	$V_{EE} \le V_{IN} \le V_{CC}$
SEL A/$\overline{B}$, OE	$D_{GND} \le V_{IN} \le DV_{CC}$
Output Short Circuit Operation	Indefinite
Storage Temperature Range	–65°C to +150°C
Lead Temperature Range (Soldering 10 sec)	300°C

NOTES

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the Theory of Operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2] Specification is for device in free air (T_A = 25°C).

[3] 24-lead TSSOP; T_{JA}= 85°C/W. Maximum internal power dissipation (PD) should be derated for ambient temperature (T_A) such that PD < (150°C T_A)/T_{JA}.

[4] T_{JA} of 85°C/W is on a 4-layer board (2s 2p).

MAXIMUM POWER DISSIPATION

The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately 150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure.

While the AD8186/AD8187 is internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature (150°C) is not exceeded under all conditions. To ensure proper operation, it is necessary to observe the maximum power derating curves shown in Figure 2.

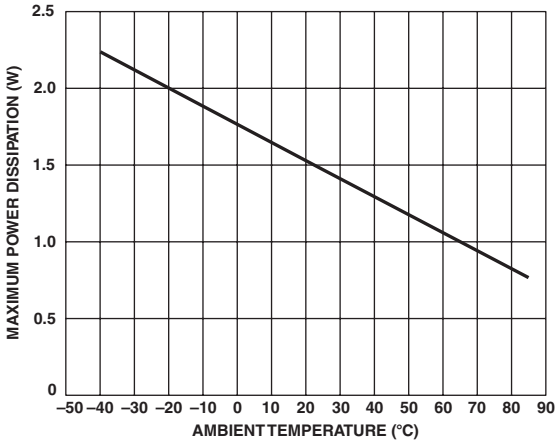
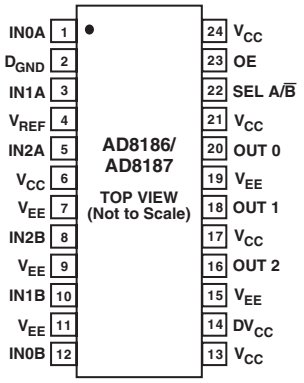


Figure 2. Maximum Power Dissipation vs. Temperature

PIN CONFIGURATION

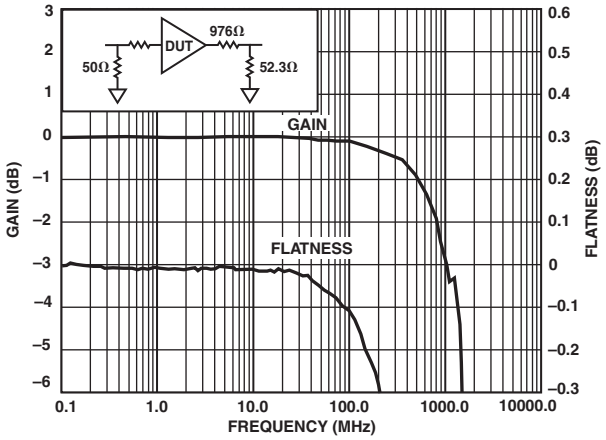


ORDERING GUIDE

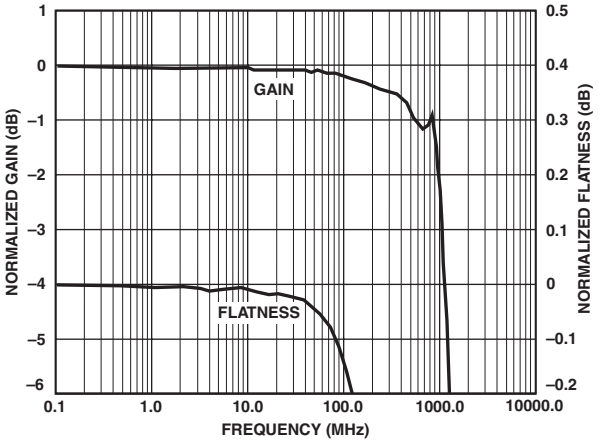
Model	Temperature Range	Package Description	Package Option
AD8186ARU	–40°C to +85°C	24-Lead Thin Shrink Small Outline Package (TSSOP)	RU-24
AD8186ARU-REEL	–40°C to +85°C	13" Reel TSSOP	RU-24
AD8186ARU-REEL 7	–40°C to +85°C	7" Reel TSSOP	RU-24
AD8187ARU	–40°C to +85°C	24-Lead Thin Shrink Small Outline Package (TSSOP)	RU-24
AD8187ARU-REEL	–40°C to +85°C	13" Reel TSSOP	RU-24
AD8187ARU-REEL 7	–40°C to +85°C	7" Reel TSSOP	RU-24
AD8186-EVAL		Evaluation Board	
AD8187-EVAL		Evaluation Board	

CAUTION

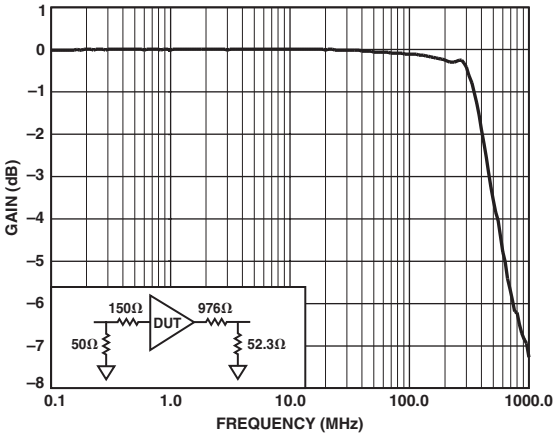
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8186/AD8187 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



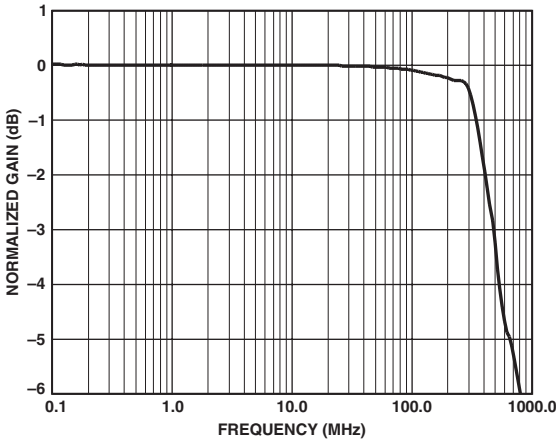
TPC 1. AD8186 Frequency Response, V_{OUT} = 200 mV p-p, R_L = 1 kΩ



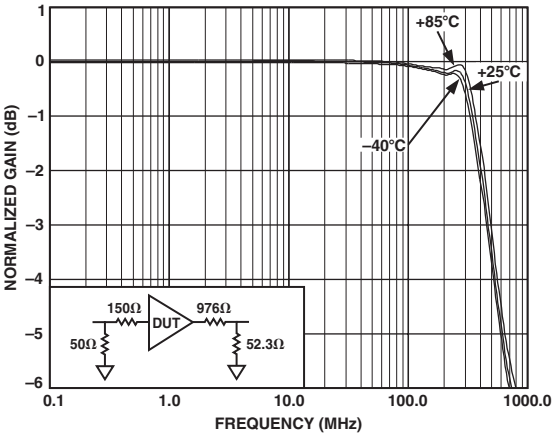
TPC 4. AD8187 Frequency Response, V_{OUT} = 200 mV p-p, R_L = 150 Ω



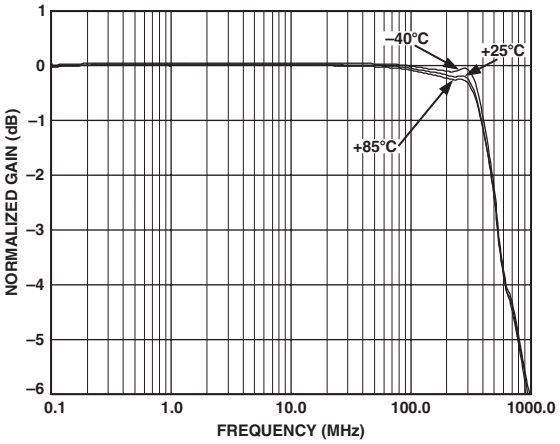
TPC 2. AD8186 Frequency Response, V_{OUT} = 2 V p-p, R_L = 1 kΩ



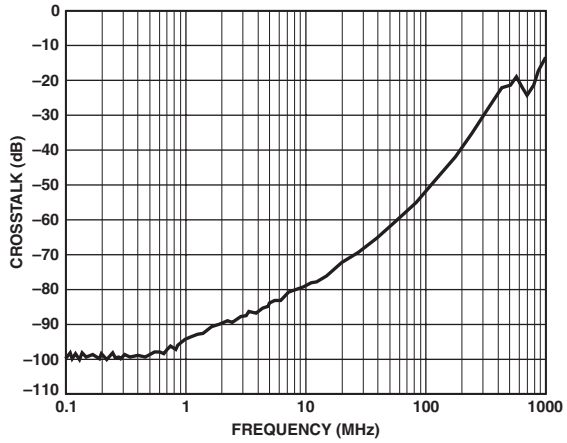
TPC 5. AD8187 Frequency Response, V_{OUT} = 2 V p-p, R_L = 150 Ω



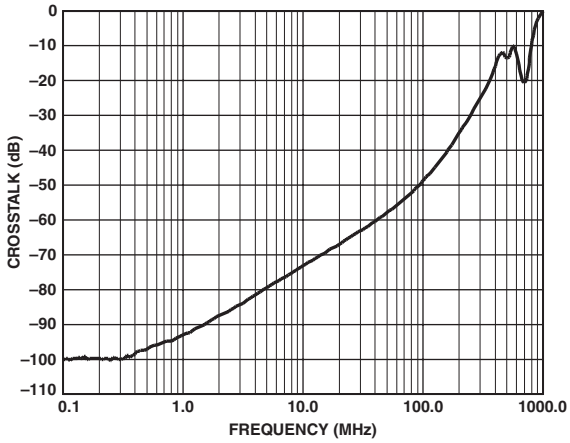
TPC 3. AD8186 Large Signal Bandwidth vs. Temperature, V_{OUT} = 2 V p-p, R_L = 1 kΩ



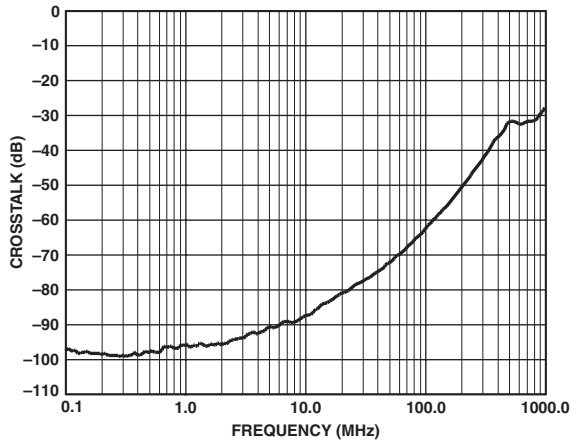
TPC 6. AD8187 Large Signal Bandwidth vs. Temperature, V_{OUT} = 2 V p-p, R_L = 150 Ω



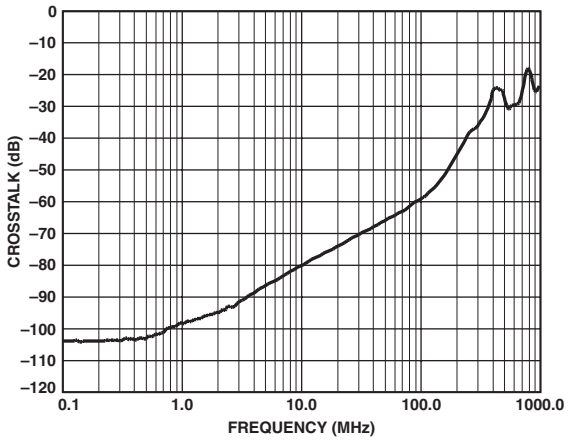
TPC 7. AD8186 All Hostile Crosstalk vs. Frequency*



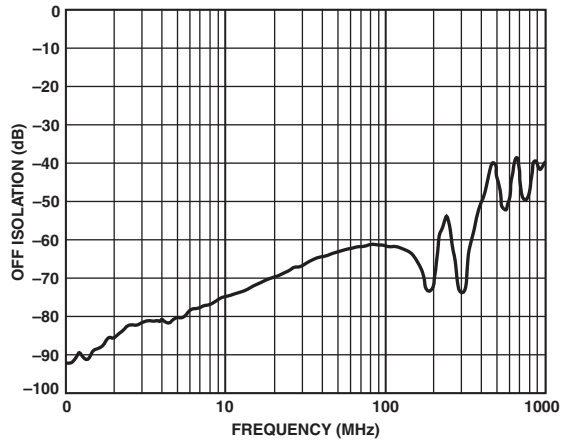
TPC 10. AD8187 All Hostile Crosstalk vs. Frequency*



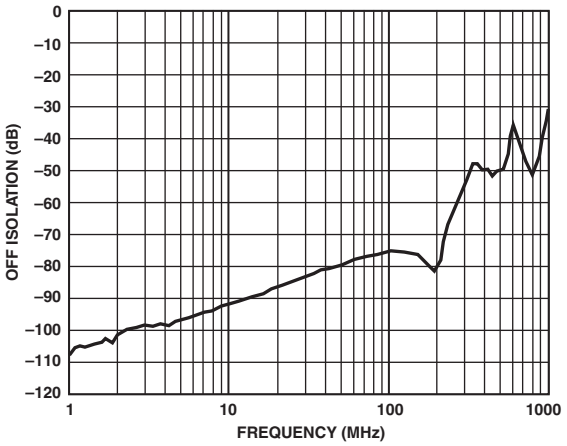
TPC 8. AD8186 Adjacent Channel Crosstalk vs. Frequency*



TPC 11. AD8187 Adjacent Channel Crosstalk vs. Frequency*

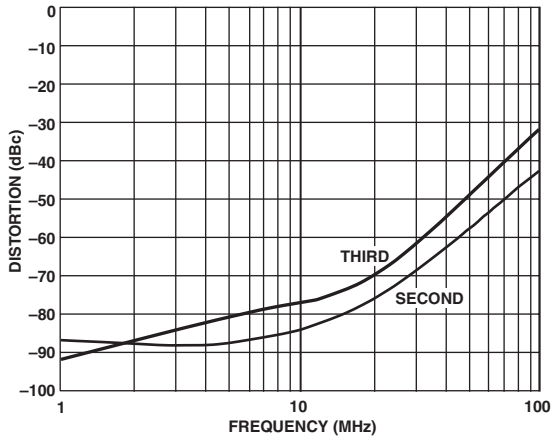


TPC 9. AD8186 OFF Isolation vs. Frequency*

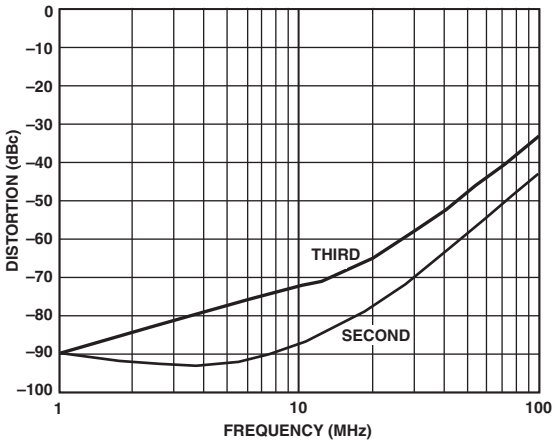


TPC 12. AD8187 OFF Isolation vs. Frequency*

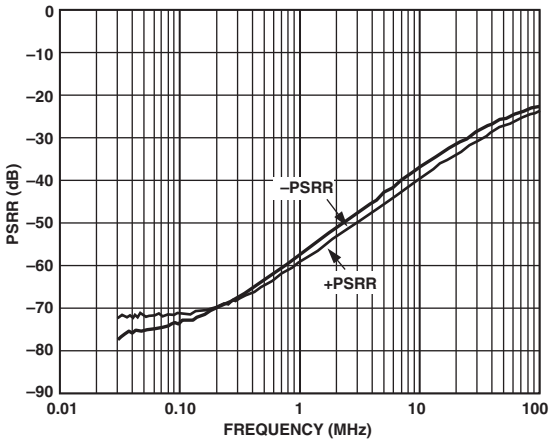
* All hostile crosstalk—Drive all INA, listen to output with INB selected.
Adjacent channel crosstalk—Drive one INA, listen to an adjacent output with INB selected.
Off isolation—Drive inputs with OE tied low.



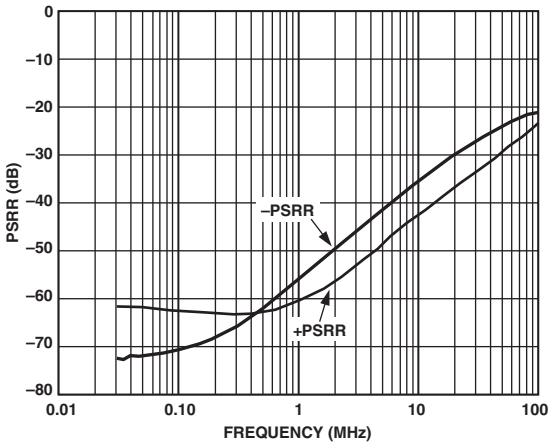
TPC 13. AD8186 Harmonic Distortion vs. Frequency V_{OUT} = 2 V p-p, R_L = 150 Ω



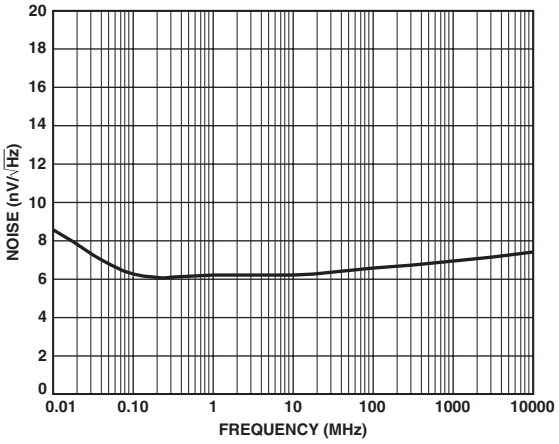
TPC 16. AD8187 Harmonic Distortion vs. Frequency V_{OUT} = 2 V p-p, R_L = 150 Ω



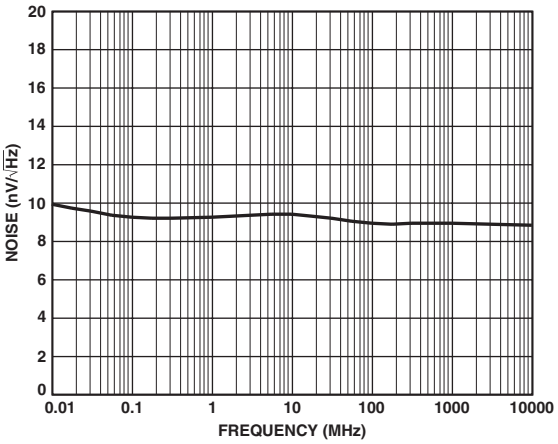
TPC 14. AD8186 PSRR vs. Frequency, R_L = 150 Ω



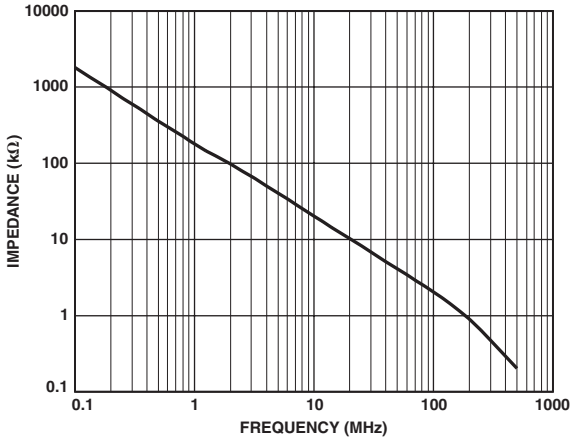
TPC 17. AD8187 PSRR vs. Frequency, R_L = 150 Ω



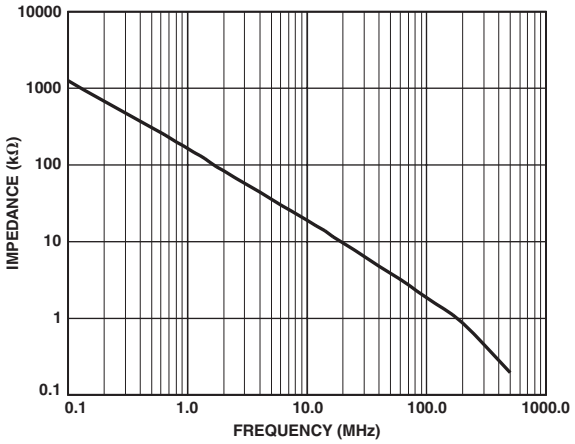
TPC 15. AD8186 Input Voltage Noise vs. Frequency



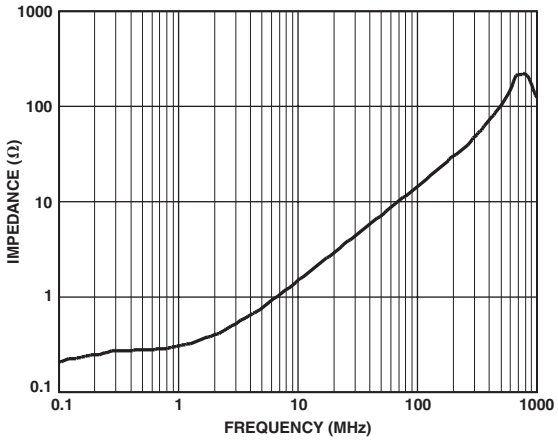
TPC 18. AD8187 Input Voltage Noise vs. Frequency



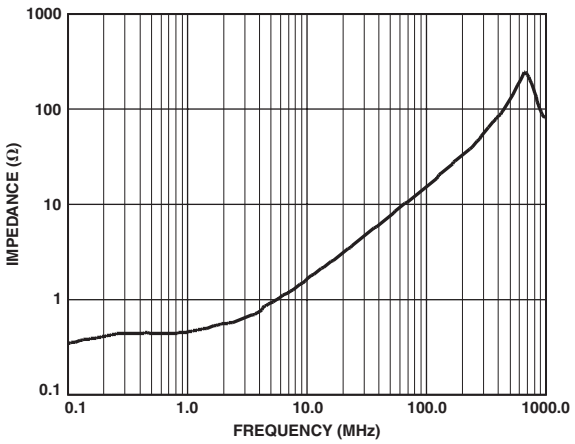
TPC 19. AD8186 Input Impedance vs. Frequency



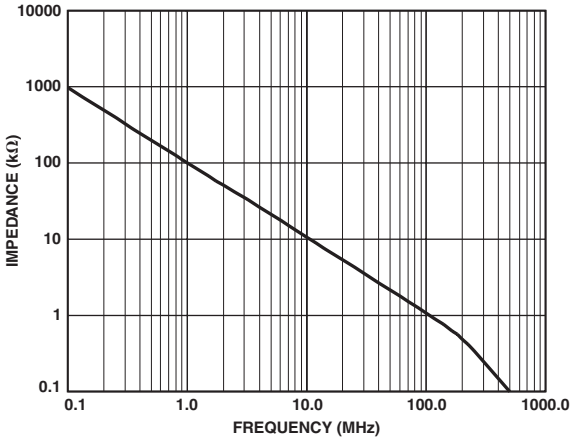
TPC 22. AD8187 Input Impedance vs. Frequency



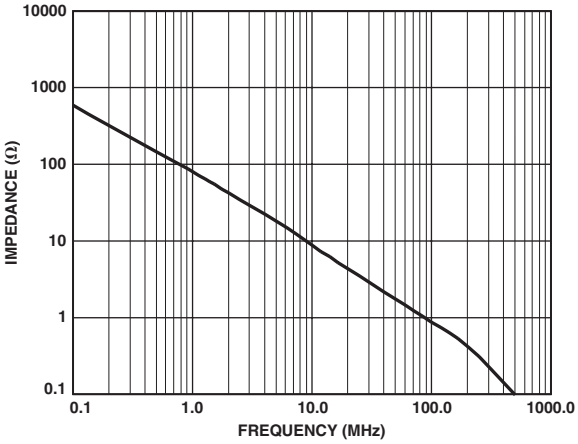
TPC 20. AD8186 Enabled Output Impedance vs. Frequency



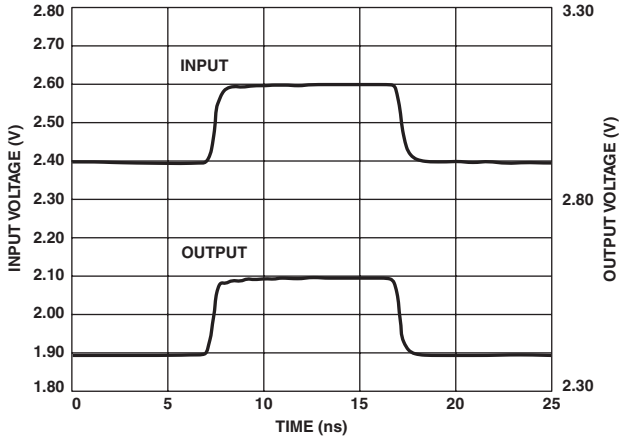
TPC 23. AD8187 Enabled Output Impedance vs. Frequency



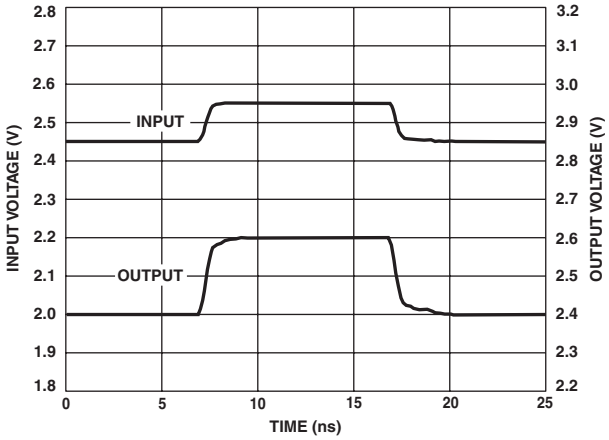
TPC 21. AD8186 Disabled Output Impedance vs. Frequency



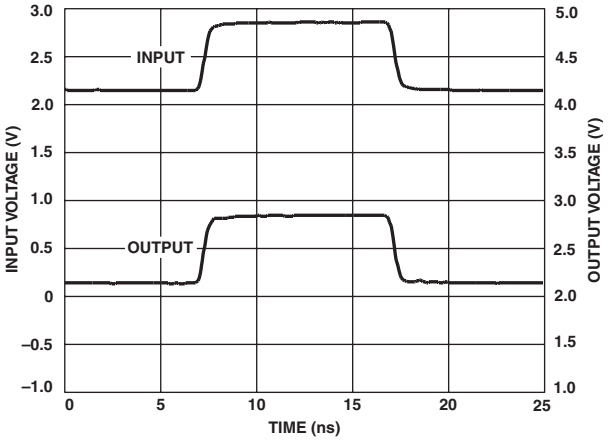
TPC 24. AD8187 Disabled Output Impedance vs. Frequency



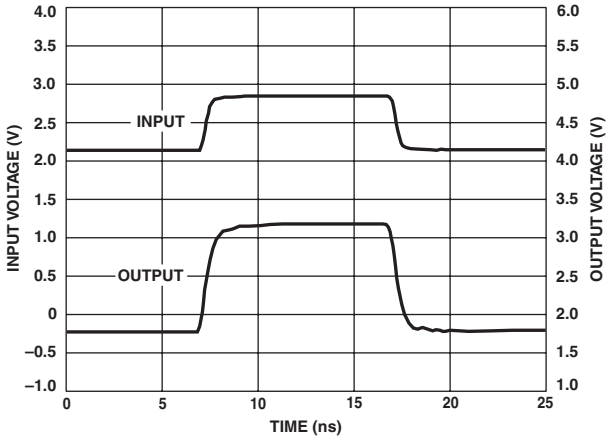
TPC 25. AD8186 Small Signal Pulse Response, V_{OUT} = 200 mV p-p, R_L = 1 kΩ



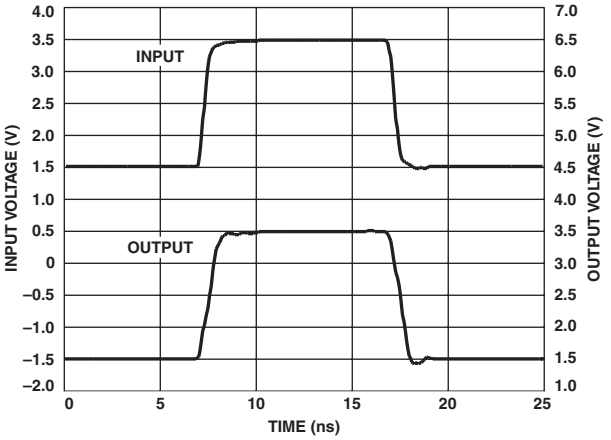
TPC 28. AD8187 Small Signal Pulse Response, V_{OUT} = 200 mV p-p, R_L = 150 kΩ



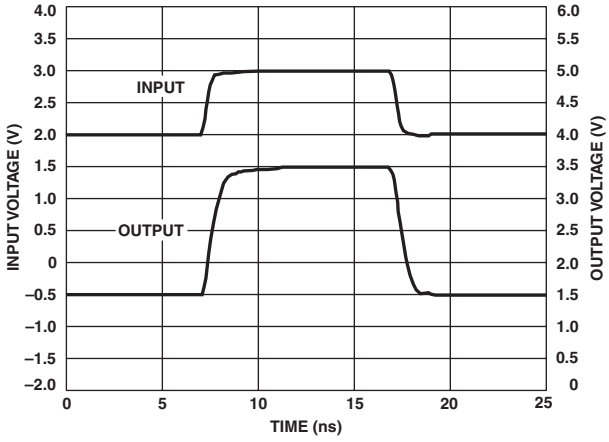
TPC 26. AD8186 Video Signal Pulse Response, V_{OUT} = 700 mV p-p, R_L = 1 kΩ



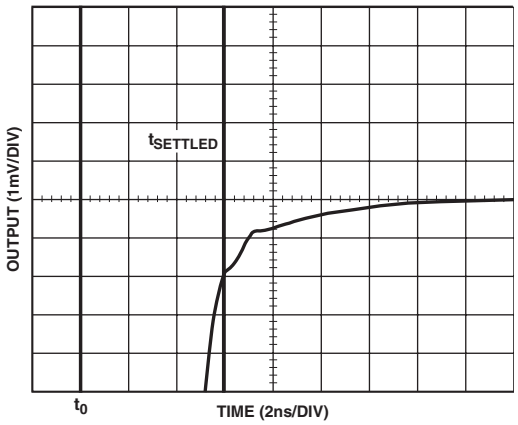
TPC 29. AD8187 Video Amplitude Pulse Response, V_{OUT} = 1.4 V p-p, R_L = 150 kΩ



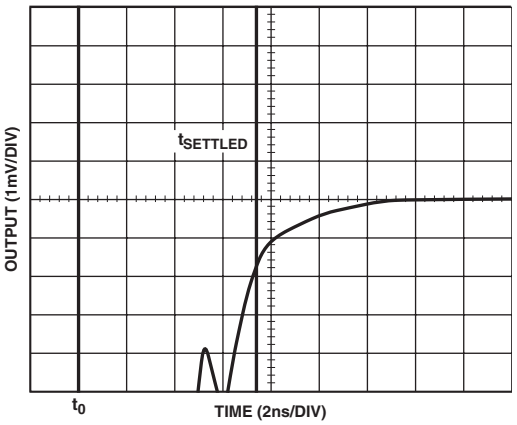
TPC 27. AD8186 Large Signal Pulse Response, V_{OUT} = 2 V p-p, R_L = 1 kΩ



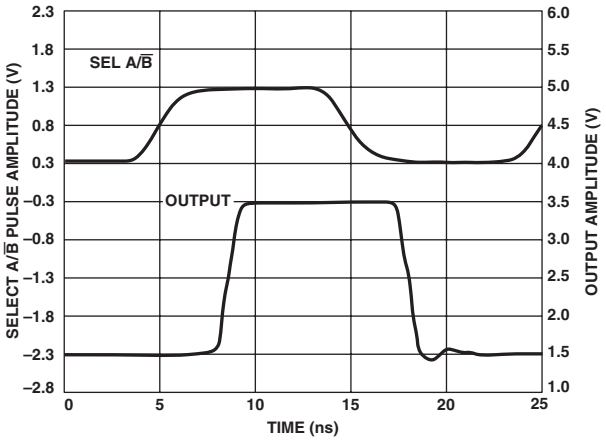
TPC 30. AD8187 Large Signal Pulse Response, V_{OUT} = 2 V p-p, R_L = 150 kΩ



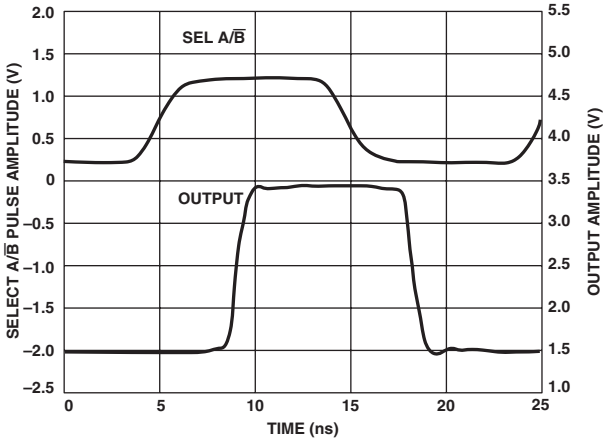
TPC 31. AD8186 Settling Time (0.1%), V_{OUT} = 2 V Step, R_L = 1 kΩ



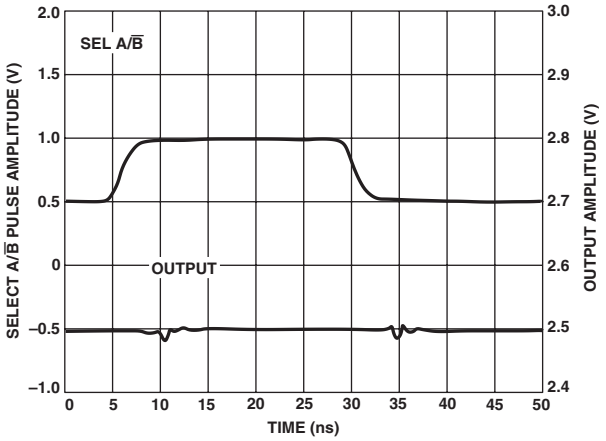
TPC 34. AD8187 Settling Time (0.1%), V_{OUT} = 2 V Step, R_L = 150 Ω



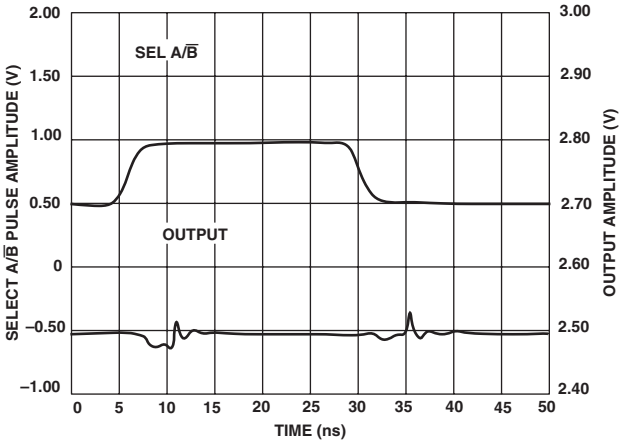
TPC 32. AD8186 Channel-to-Channel Switching Time, V_{OUT} = 2 V p-p, INA = 3.5 V, INB = 1.5 V



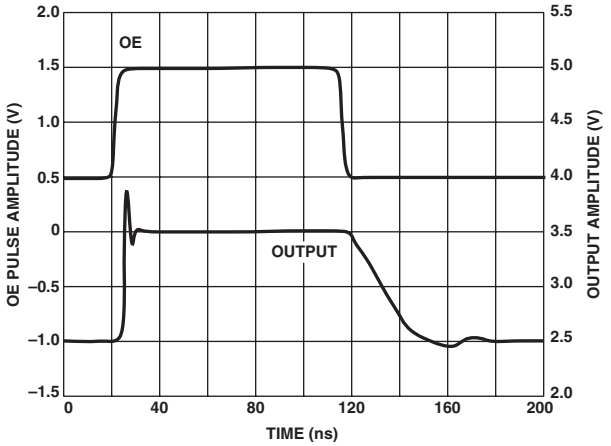
TPC 35. AD8187 Channel-to-Channel Switching Time, V_{OUT} = 2 V p-p, INA = 3.0 V, INB = 2.0 V



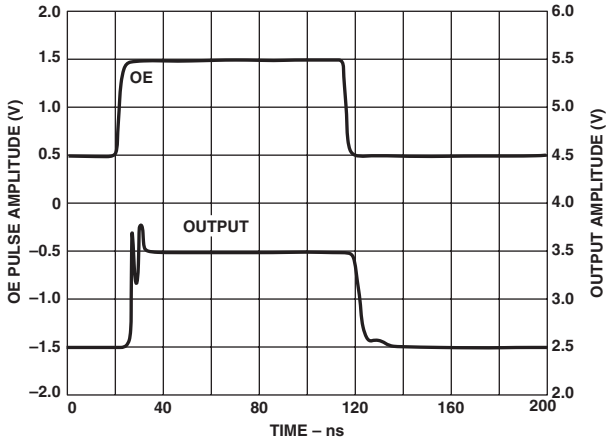
TPC 33. AD8186 Channel Switching Transient (Glitch), INA = INB = 0 V



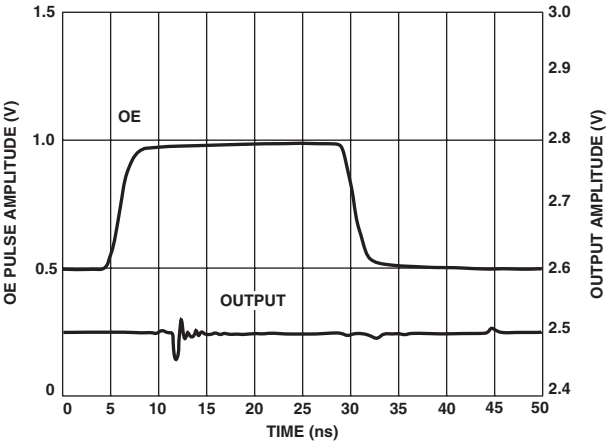
TPC 36. AD8187 Channel Switching Transient (Glitch), INA = INB = V_{REF} = 0 V



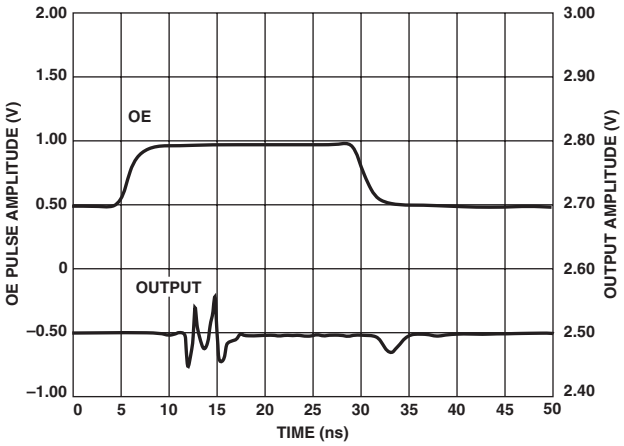
TPC 37. AD8186 Enable ON/OFF Time, V_{OUT} = 0 V to 1 V



TPC 39. AD8187 Enable ON/OFF Time, V_{OUT} = 0 V to 1 V



TPC 38. AD8186 Channel Enable/Disable Transient (Glitch)



TPC 40. AD8187 Channel Enable/Disable Transient (Glitch)

THEORY OF OPERATION

The AD8186 (G = +1) and AD8187 (G = +2) are single-supply, triple 2:1 multiplexers with TTL compatible global input switching and output-enable control. Optimized for selecting between two RGB (red, green, blue) video sources, the devices have high peak slew rates, maintaining their bandwidth for large signals. Additionally, the multiplexers are compensated for high phase margin, minimizing overshoot for good pixel resolution. The multiplexers also have respectable video specifications and are superior for switching NTSC or PAL composite signals.

The multiplexers are organized as three independent channels, each with two input transconductance stages and one output transimpedance stage. The appropriate input transconductance stages are selected via one logic pin (SEL A/$\overline{B}$) such that all three outputs switch input connections simultaneously. The unused input stages are disabled with a proprietary clamp circuit to provide excellent crosstalk isolation between "on" and "off" inputs while protecting the disabled devices from damaging reverse base-emitter voltage stress. No additional input buffering is necessary, resulting in low input capacitance and high input impedance without additional signal degradation.

The transconductance stage, a high slew rate, class AB circuit, sources signal current into a high impedance node. Each output stage contains a compensation network and is buffered to the output by a complementary emitter-follower stage. Voltage feedback sets the gain, with the AD8186 configured as a unity gain follower and the AD8187 as a gain-of-two amplifier with a feedback network. This architecture provides drive for a reverse-terminated video load (150 Ω) with low differential gain and phase errors while consuming relatively little power. Careful chip layout and biasing result in excellent crosstalk isolation between channels.

High Impedance, Output Disable Feature, and Off Isolation

The output-enable logic pin (OE) controls whether the three outputs are enabled or disabled to a high impedance state. The high impedance disable allows larger matrices to be built by busing the outputs together. In the case of the AD8187 (G = +2), a feedback isolation scheme is used so that the impedance of the gain-of-two feedback network does not load the output. When not in use, the outputs can be disabled to reduce power consumption.

The reader may have noticed that the off isolation performance of the signal path is dependent upon the value of the load resistor, R_L. For calculating off isolation, the signal path may be modeled as a simple high-pass network with an effective capacitance of 3 fF. Off isolation will improve as the load resistance is decreased. In the case of the AD8186, off isolation is specified with a 1 kΩ load. However, a practical application would likely gang the outputs of multiple muxes. In this case, the proper load resistance for the off isolation calculation is the output impedance of an enabled AD8186, typically less than a 10th of an ohm.

Full Power Bandwidth vs. –3 dB Large Signal Bandwidth

Note that full power bandwidth for an undistorted sinusoidal signal is often calculated using the peak slew rate from the equation

$$Full\ Power\ Bandwidth = \frac{Peak\ Slew\ Rate}{2\pi \times Sinusoid\ Amplitude}$$

The peak slew rate is not the same as the average slew rate. The average slew rate is typically specified as the ratio

$$\frac{\Delta V_{OUT}}{\Delta t}$$

measured between the 20% to 80% output levels of a sufficiently large output pulse. For a natural response, the peak slew rate may be 2.7 times larger than the average slew rate. Therefore, calculating a full power bandwidth with a specified average slew rate will give a pessimistic result. In specifying the large signal performance of these multiplexers, we've published the large-signal bandwidth, the average slew rate, and the measurements of the total harmonic distortion. (Large signal bandwidth is defined as the –3 dB point measured on a 2 V p-p output sine wave.) Specifying these three aspects of the signal path's large signal dynamics allows the user to predict system behavior for either pulse or sinusoid waveforms.

Single-Supply Considerations

DC-Coupled Inputs, Integrated Reference Buffers, and Selecting the V_{REF} Level on the AD8187, (G = +2)

The AD8186 and AD8187 offer superior large signal dynamics. The trade-off is that the input and output compliance is limited to ~1.3 V from either rail when driving a 150 Ω load. These sections address some challenges of designing video systems within a single 5 V supply.

The AD8186

The AD8186 is internally wired as a unity-gain follower. Its inputs and outputs can both swing to within ~1.3 V of either rail. This affords the user 2.4 V of dynamic range at input and output, which should be enough for most video signals, whether the inputs are ac- or dc-coupled. In both cases, the choice of output termination voltage will determine the quiescent load current.

For improved supply rejection, the V_{REF} pin should be tied to an ac ground (the more quiet supply is a good bet). Internally, the V_{REF} pin connects to one terminal of an on-chip capacitor. The capacitor's other terminal connects to an internal node. The consequence of building this bypass capacitor on-chip is twofold. First, the V_{REF} pin on the AD8186 draws no input bias current. (Contrast this to the case of the AD8187, where the V_{REF} pin typically draws 2 μA of input bias current). Second, on the AD8186, the V_{REF} pin may be tied to any voltage within the supply range.

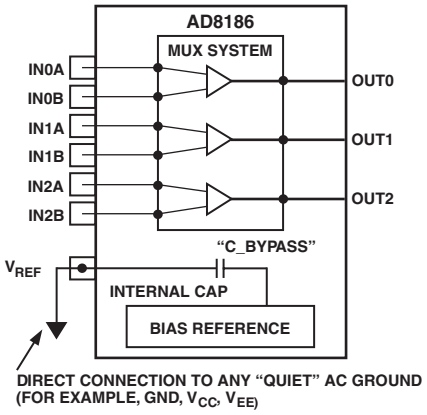


Figure 3. V_{REF} Pin Connection for AD8186 (Differs from AD8187)

The AD8187

The AD8187 uses on-chip feedback resistors to realize the gain-of-two function. To provide low crosstalk and a high output impedance when disabled, each set of 500 Ω feedback resistors is terminated by a dedicated reference buffer. A reference buffer is a high speed op amp configured as a unity-gain follower. The three reference buffers, one for each channel, share a single, high impedance input, the V_{REF} pin (see Figure 4). V_{REF} input bias current is typically less than 2 μA.

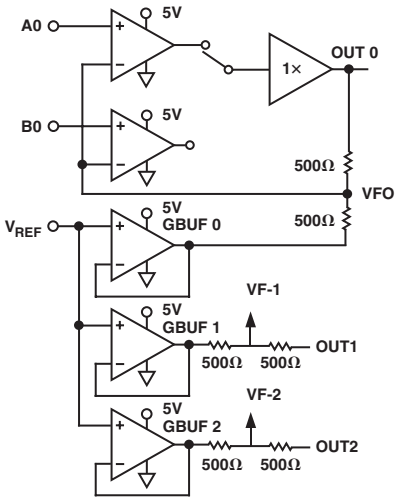


Figure 4. Conceptual Diagram of a Single Multiplexer Channel, G = +2

This configuration has a few implications for single-supply operation:

1) On the AD8187, V_{REF} may not be tied to the most negative analog supply, V_{EE}.

   Limits on Reference Voltage (AD8187, see Figure 5):

$$V_{EE} + 1.3\,V < V_{REF} < V_{CC} - 1.6\,V$$

$$1.3\,V < V_{REF} < 3.4\,V \text{ on } 0\ V/5\ V \text{ Supplies}$$

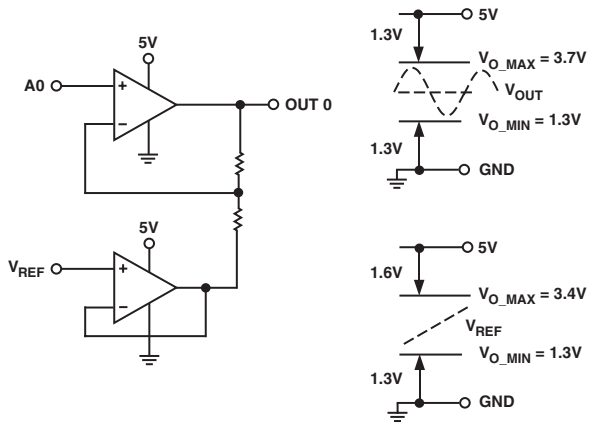


Figure 5. Output Compliance of Main Amplifier Channel and Ground Buffer

2) Signal at the V_{REF} pin appears at each output. Therefore, V_{REF} should be tied to a well bypassed, low impedance source. Using superposition, it is easily shown that

$$V_{OUT} = 2 \times V_{IN} - V_{REF}$$

3) To maximize the output dynamic range, the reference voltage should be chosen with some care.

For example, consider amplifying a 700 mV video signal with a sync pulse 300 mV below black level. The user might decide to set V_{REF} at black level to preferentially run video signals on the faster NPN transistor path. The AD8186 would, in this case, allow a reference voltage as low as 1.3 V + 300 mV = 1.6 V. If the AD8187 is used, the sync pulse would be amplified to 600 mV. Therefore, the lower limit on V_{REF} becomes 1.3 V + 600 mV = 1.9 V. For routing RGB video, an advantageous configuration would be to employ +3 V and –2 V supplies, in which case V_{REF} could be tied to ground.

If system considerations prevent running the multiplexer on split supplies, a false ground reference should be employed. A low impedance reference may be synthesized with a second operational amplifier. Alternately, a well bypassed resistor divider may serve. Refer to the Application section for further explanation and more examples.

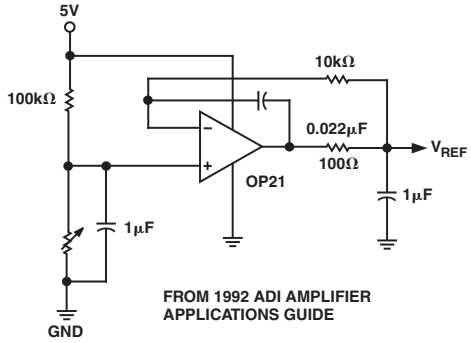


Figure 6a. Synthesis of a False Ground Reference

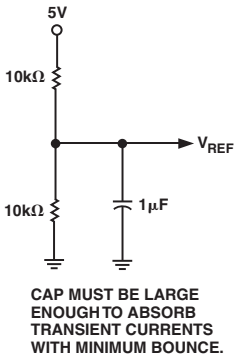


Figure 6b. Alternate Method for Synthesis of a False Ground Reference

High Impedance Disable

Both the AD8186 and the AD8187 may have their outputs disabled to a high impedance state. In the case of the AD8187, the reference buffers also disable to a state of high output impedance. This feature prevents the feedback network of a disabled channel from loading the output, which is valuable when busing together the outputs of several muxes.

AC-Coupled Inputs (DC Restore before Mux Input)
Using ac-coupled inputs presents an interesting challenge for video systems operating from a single 5 V supply. In NTSC and PAL video systems, 700 mV is the approximate difference between the maximum signal voltage and black level. It is assumed that sync has been stripped. However, given the two pathological cases shown in Figure 7, a dynamic range of twice the maximum signal swing is required if the inputs are to be ac-coupled. A possible solution would be to use a dc restore circuit before the mux.

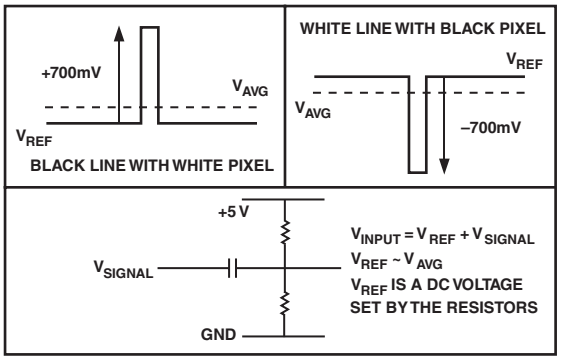


Figure 7. Pathological Case for Input Dynamic Range

Tolerance to Capacitive Load
Op amps are sensitive to reactive loads. A capacitive load at the output appears in parallel with an effective resistance of $R_{EFF} = (R_L \| r_O)$, where R_L is the discrete resistive load, and r_O is the open-loop output impedance, approximately 15 Ω for these muxes.

The load pole, at $f_{LOAD} = 1/(2\pi\ R_{EFF}\ C_L)$, can seriously degrade phase margin and therefore stability. The old workaround is to place a small series resistance directly at the output to isolate the load pole. While effective, this ruse also affects the dc and termination characteristics of a 75 Ω system. The AD8186 and AD8187 are built with a variable compensation scheme that senses the output reactance and trades bandwidth for phase margin, ensuring faster settling and lower overshoot at higher capacitive loads.

Secondary Supplies and Supply Bypassing
The high current output transistors are given their own supply pins (Pins 15, 17, 19, and 21) to reduce supply noise on-chip and to improve output isolation. Since these secondary, high current supply pins are not connected on-chip to the primary analog supplies (V_{CC}/V_{EE}, Pins 6, 7, 9, 11, 13, and 24), some care should be taken to ensure that the supply bypass capacitors are connected to the correct pins. At a minimum, the primary supplies should be bypassed. Pin 6 and Pin 7 may be a convenient place to accomplish this. Stacked power and ground planes could be a convenient way to bypass the high current supply pins.

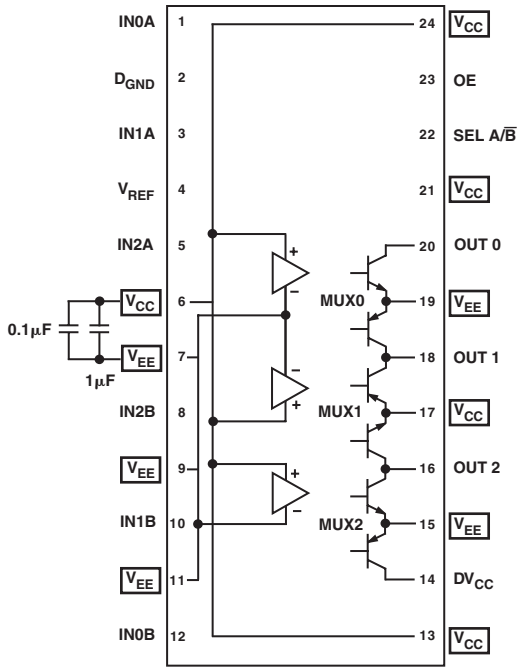


Figure 8. Detail of Primary and Secondary Supplies

Split-Supply Operation
Operating from split supplies (e.g., +3 V/–2 V or ±2.5 V) simplifies the selection of the V_{REF} voltage and load resistor termination voltage. In this case, it is convenient to tie V_{REF} to ground. The logic inputs are level shifted internally to allow the digital supplies and logic inputs to operate from 0 V and 5 V when powering the analog circuits from split supplies. The maximum voltage difference between DV_{CC} and V_{EE} must not exceed 8 V (see Figure 9).

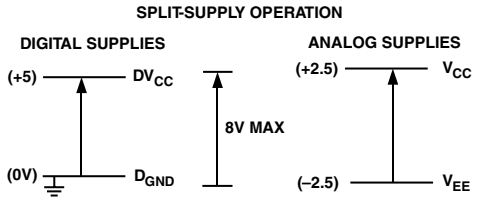


Figure 9. Split-Supply Operation

APPLICATION

Single-Supply Operation

The AD8186/AD8187 are targeted mainly for use in single-supply 5 V systems. For operating on these supplies, both V_{EE} and D_{GND} should be tied to ground. The control logic pins will be referenced to ground. Normally, the DV_{CC} supply should be set to the same positive supply as the driving logic.

For dc-coupled single-supply operation, it is necessary to set an appropriate input dc level that is within the specified range of the amplifier. For the unity-gain AD8186, the output dc level will be the same as the input, while for the gain-of-two AD8187, the V_{REF} input can be biased to obtain an appropriate output dc level.

Figure 10 shows a circuit that provides a gain-of-two and is dc-coupled. The video input signals must have a dc bias from their source of approximately 1.5 V. This same voltage is applied to V_{REF} of the AD8187. The result is that when the video signal is at 1.5 V, the output will also be at the same voltage. This is close to the lower dynamic range of both the input and the output.

When the input goes most positive, which is 700 mV above the black level for a standard video signal, it reaches a value of 2.2 V and there is enough headroom for the signal. On the output side, the magnitude of the signal will change by 1.4 V, which will make the maximum output voltage 2.2 V + 1.4 V = 3.6 V. This is just within the dynamic range of the output of the part.

AC Coupling

When a video signal is ac-coupled, the amount of dynamic range required to handle the signal can potentially be double that required for dc-coupled operation. For the unity-gain AD8186, there is still enough dynamic range to handle an ac-coupled, standard video signal with 700 mV p-p amplitude.

If the input is biased at 2.5 V dc, the input signal can potentially go 700 mV both above and below this point. The resulting 1.8 V and 2.2 V are within the input signal range for single 5 V operation. Since the part is unity-gain, the outputs will follow the inputs, and there will be adequate range at the output as well.

When using the gain-of-two AD8187 in a simple ac-coupled application, there will be a dynamic range limitation at the output caused by its higher gain. At the output, the gain-of-two will produce a signal swing of 1.4 V, but the ac coupling will double this required amount to 2.8 V. The AD8187 outputs can only swing from 1.4 V to 3.6 V on a 5 V supply, so there are only 2.2 V of dynamic signal swing available at the output.

A standard means for reducing the dynamic range requirements of an ac-coupled video signal is to use a dc restore. This circuit works to limit the dynamic range requirements by clamping the black level of the video signal to a fixed level at the input to the amplifier. This prevents the video content of the signal from varying the black level as happens in a simple ac-coupled circuit.

After ac coupling a video signal, it is always necessary to use a dc restore to establish where the black level is. Usually, this appears at the end of a video signal chain. This dc restore circuit needs to have the required accuracy for the system. It compensates for all the offsets of the preceding stages. Therefore, if a dc restore circuit is to be used only for dynamic-range limiting, it does not require great dc accuracy.

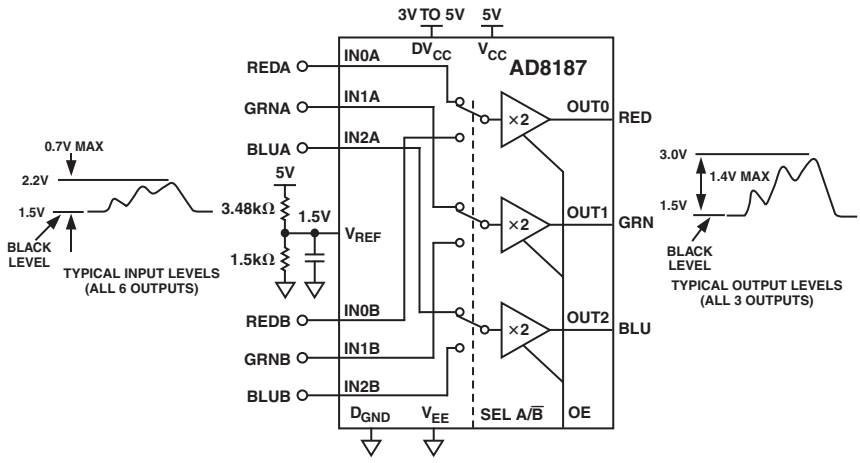


Figure 10. DC-Coupled (Bypassing and Logic Not Shown)

A dc restore circuit using the AD8187 is shown in Figure 11. Two separate sources of RGB video are ac-coupled to the 0.1 µF input capacitors of the AD8187. The input points of the AD8187 are switched to a 1.5 V reference by the ADG786, which works in the following manner:

The SEL A/$\overline{B}$ signal selects the A or B inputs to the AD8187. It also selects the switch positions in the ADG786 such that the same selected inputs will be connected to V_{REF} when $\overline{EN}$ is low.

During the horizontal interval, all of the RGB input signals are at a flat black level. A logic signal that is low during $\overline{HSYNC}$ is applied to the $\overline{EN}$ of the ADG786. This closes the switches and clamps the black level to 1.5 V. At all other times, the switches are off and the node at the inputs to the AD8187 floats.

There are two considerations for sizing the input coupling capacitors. One is the time constant during the H-pulse clamping. The other is the droop associated with the capacitor discharge due to the input bias current of the AD8187. For the former, it is better to have a small capacitor; but for the latter, a larger capacitor is better.

The ON resistance of the ADG786 and the coupling capacitor forms the time constant of the input clamp. The ADG786 ON resistance is 5 Ω max. With a 0.1 µF capacitor, a time constant of 0.5 µs is created. Thus, a sync pulse of greater than 2.5 µs will cause less than 1% error. This is not critical because the black level from successive lines is very close and the voltage changes little from line to line.

A rough approximation for the horizontal line time for a graphics system is 30 µs. This will vary depending on the resolution and the vertical rate. The coupling capacitor needs to hold the voltage relatively constant during this time while the input bias current of the AD8187 is discharging it.

The change in voltage is I_{BIAS} times the line time divided by the capacitance. With an I_{BIAS} of 2.5 µA, a line time of 30 µs, and a 0.1 µF coupling capacitor, the amount of droop is 0.75 mV. This is roughly 0.1% of the full video amplitude and will not be observable in the video display.

High Speed Design Considerations

The AD8186/AD8187 are extremely high speed switching amplifiers for routing the highest resolution graphic signals. Extra care is required in the circuit design and layout to ensure that the full resolution of the video is realized.

First, the board should have at least one layer of a solid ground plane. Long signal paths should be referenced to a ground plane as controlled-impedance traces. All bypass capacitors should be very close to the pins of the part with absolutely minimum extra circuit length in the path. It is also helpful to have a large V_{CC} plane on a circuit board layer that is closely spaced to the ground plane. This creates a low inductance interplane capacitance, which is very helpful in supplying the fast transient currents that the part demands during high resolution signal transitions.

Evaluation Board

An evaluation board has been designed and is offered for running the AD8186/AD8187 on a single supply. The inputs and outputs are ac-coupled and terminated with 75 Ω resistors. For the AD8187, a potentiometer is provided to allow setting V_{REF} at any value between V_{CC} and ground.

The logic control signals can be statically set by adding or removing a jumper. If it is required to drive the logic pins with a fast signal, an SMA connector can be used to deliver the signal, and a place for a termination resistor is provided.

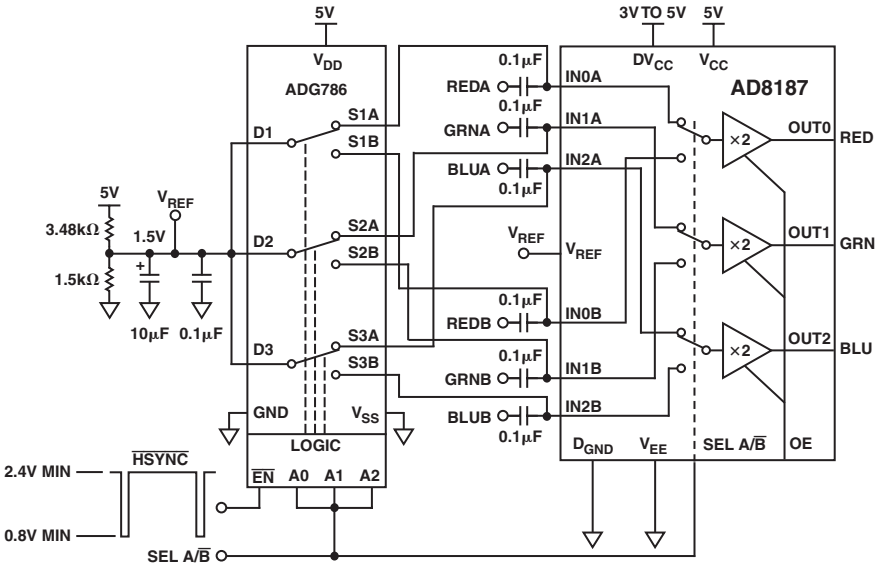


Figure 11. AD8187 AC-Coupled with DC Restore

EVALUATION BOARD

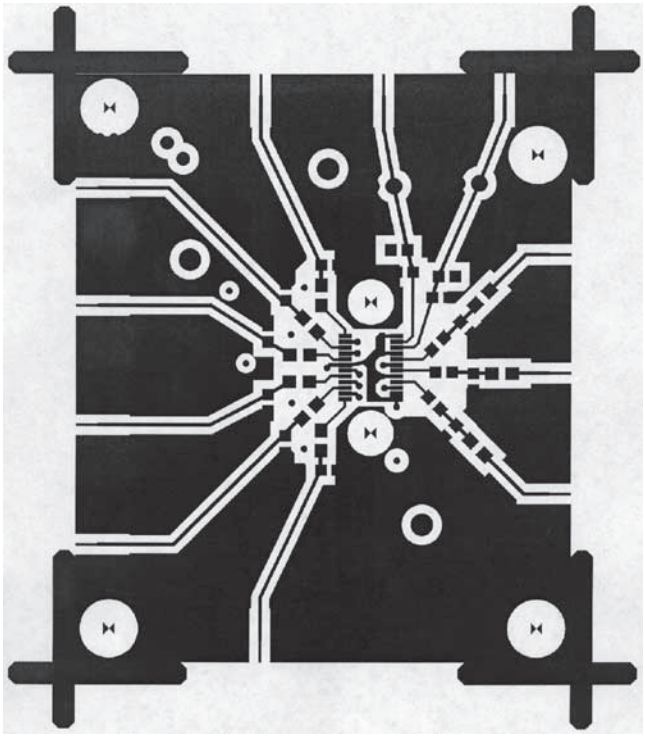


Figure 12. Component Side Board Layout

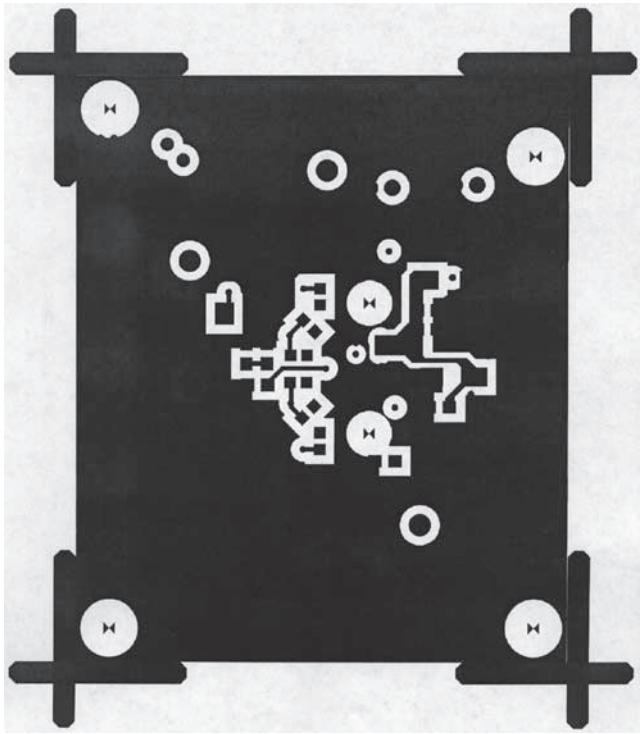


Figure 13. Circuit Side Board Layout

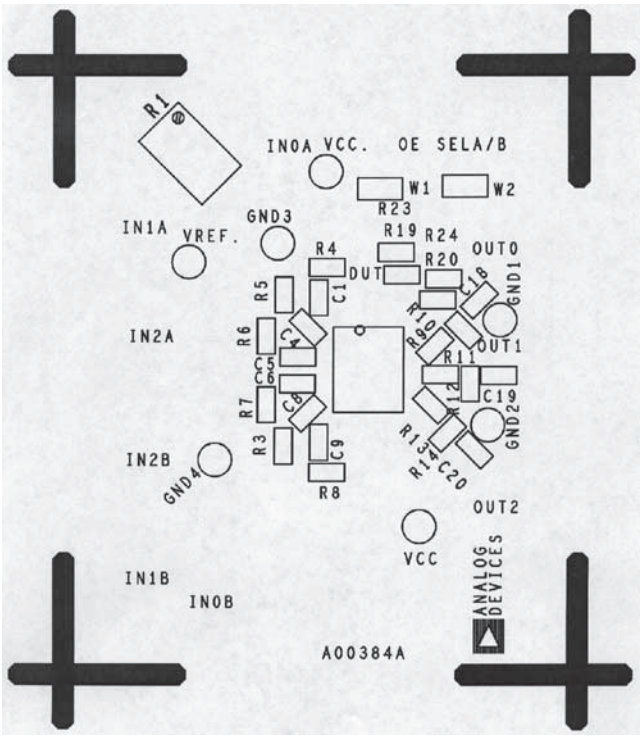


Figure 14. Component Side Silkscreen

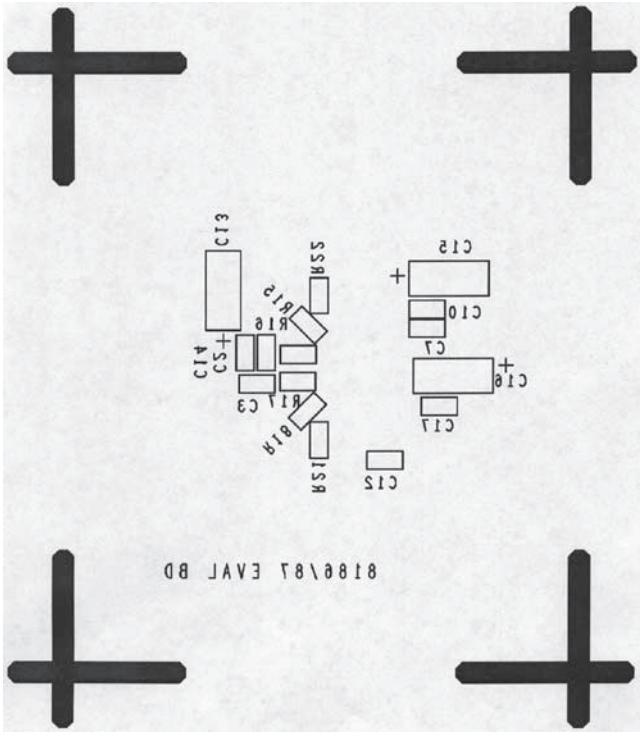


Figure 15. Circuit Side Silkscreen

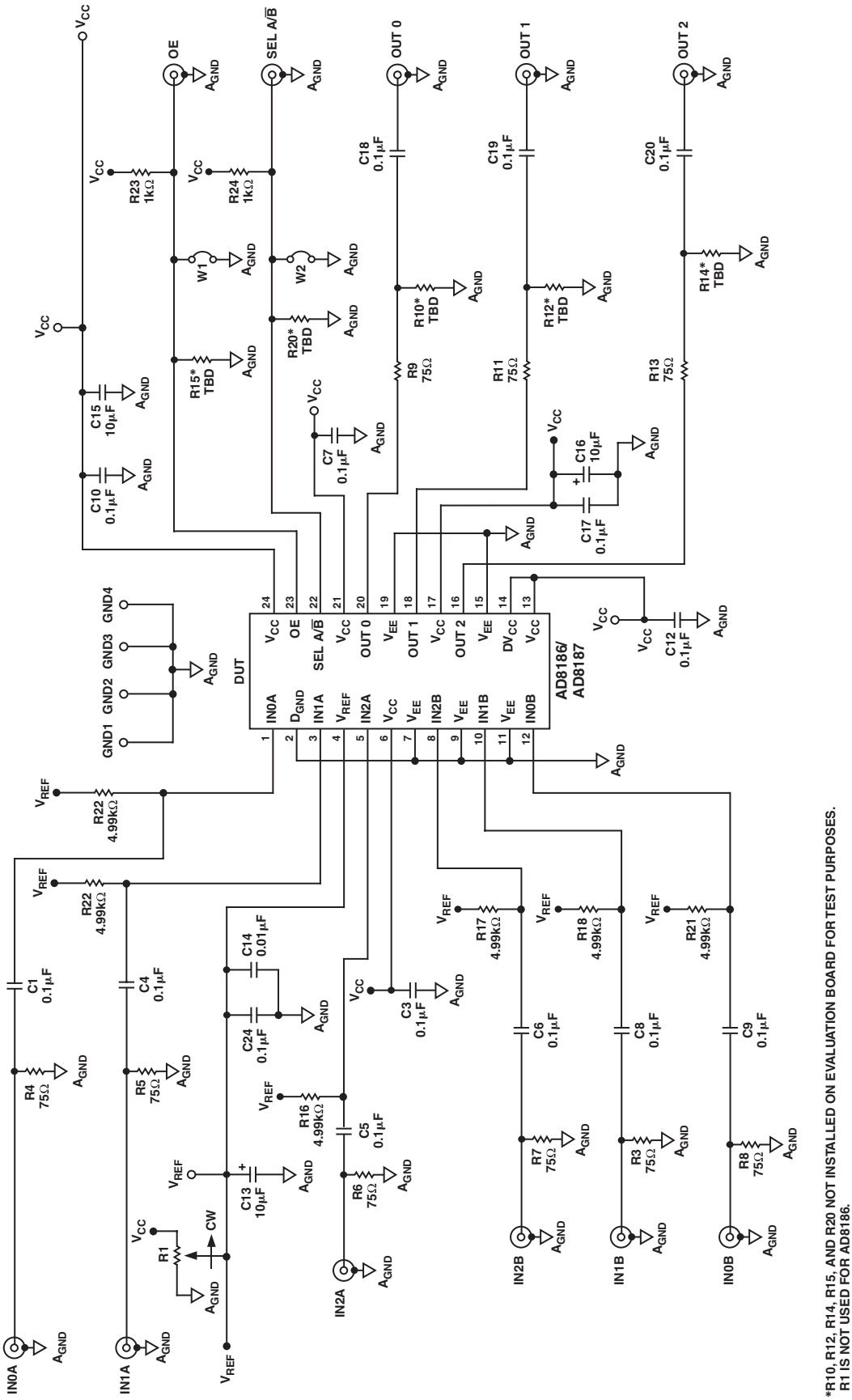
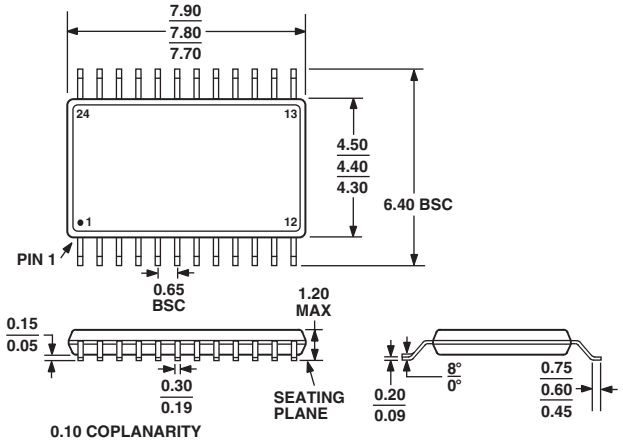


Figure 16. Single-Supply Evaluation Board

OUTLINE DIMENSIONS

24-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-24)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153AD

C02985–0–6/03(A)

Revision History

Location	Page
6/03—Data Sheet changed from REV. 0 to REV. A.	
Changes to SPECIFICATIONS	2
Edits to TPCs 32, 35, and 40	10
Updated OUTLINE DIMENSIONS	20