3.3 V, 50 Mbps to 3.3 Gbps Single-Loop Laser Diode Driver

Preliminary Technical Data

ADN2871

FEATURES

SFP/SFF and SFF-8472 MSA-compliant
SFP reference design available
50 Mbps to 4.25 Gbps operation
Multirate 155 Mbps to 4.25 Gbps operation
Automatic average power control
Typical rise/fall time 60 ps
Bias current range 2 mA to 100 mA
Modulation current range 5 mA to 90 mA
Laser fail alarm and automatic laser shutdown (ALS)
Bias and modulation current monitoring
3.3 V operation
4 mm × 4 mm LFCSP package
Voltage setpoint control
Resistor setpoint control
Pin-compatible with ADN2870

APPLICATIONS

Multirate OC3 to OC48-FEC SFP/SFF modules
1×/2×/4× Fibre channel SFP/SFF modules
LX-4 modules
DWDM/CWDM SFP modules
1GE SFP/SFF transceiver modules

GENERAL DESCRIPTION

The ADN2871 laser diode driver is designed for advanced SFP and SFF modules, using SFF-8472 digital diagnostics. The ADN2871 supports single-rate or multi-rate operation from 50 Mbps to 4.25 Gbps.

Average power and extinction ratio can be set with a voltage provided by a microcontroller DAC or by a trimmable resistor or digipot. Average power control-loop is implemented using feedback from a monitor photodiode. The part provides bias and modulation current monitoring as well as fail alarms and automatic laser shutdown. The device interfaces easily with the ADI ADuC70xx family of microconverters and with the ADN289x family of limiting amplifiers to make a complete SFP/SFF transceiver solution. An SFP reference design is available. The product is pin compatible with the ADN2870 Dual Loop LDD allowing one PC board layout to work with either device. For dual loop applications, refer to the ADN2870 datasheet.

The product is available in a space-saving 4 mm ×4 mm LFCSP package specified over the −40°C to +85°C temperature range.

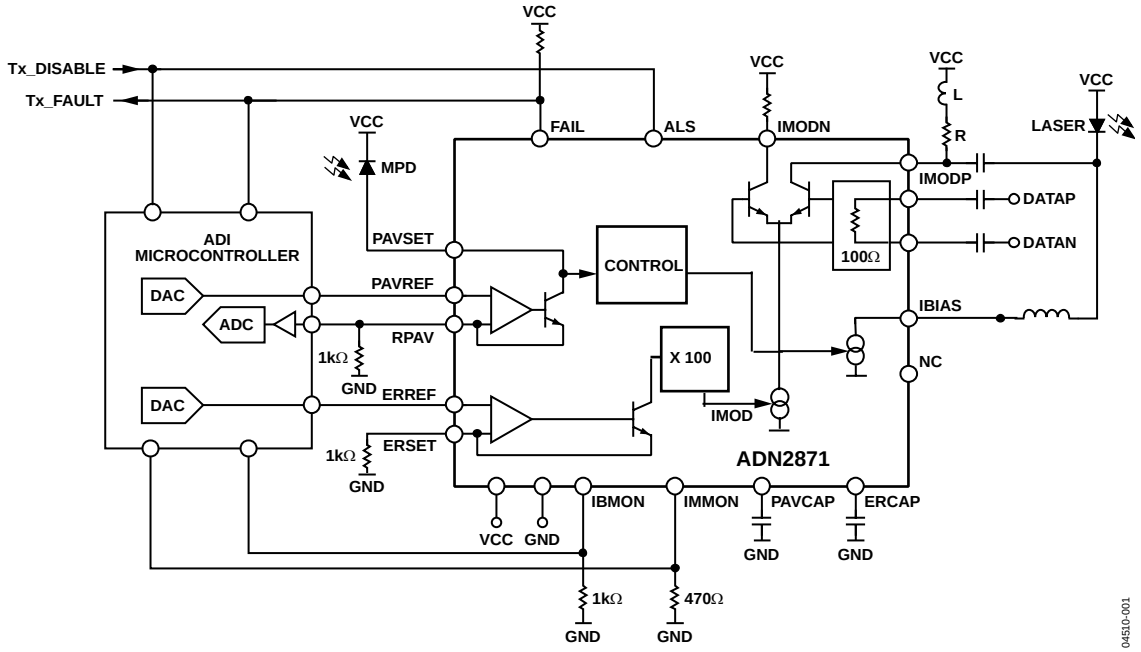

Figure 1. Application Diagram Showing Microcontroller Interface

Protected by US patent: US6414974

Rev. PrA

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REVISION HISTORY

Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 3.0 V to 3.6 V. All specifications T_{MIN} to T_{MAX},[1] unless otherwise noted. Typical values as specified at 25°C.

Table 1.

Parameter	Min	Typ	Max	Unit	Conditions/Comments
LASER BIAS CURRENT (IBIAS)					
Output Current IBIAS	2		100	mA	
Compliance Voltage	1.2		V_{CC}	V	
IBIAS when ALS is High			0.2	mA	
CCBIAS Compliance Voltage	1.2			V	
MODULATION CURRENT (IMODP, IMODN)[2]					
Output Current IMOD	5		90	mA	
Compliance Voltage	1.5		V_{CC}	V	
IMOD when ALS is High			0.05	mA	
Rise Time[2, 3]		60	104	ps	
Fall Time[2, 3]		60	96	ps	
Random Jitter[2, 3]		0.8	1.1	ps	rms
Deterministic Jitter[2, 3]			35	ps	20 mA < IMOD < 90 mA
Pulse-Width Distortion[2, 3]			30	ps	20 mA < IMOD < 90 mA
AVERAGE POWER SET (PAVSET)					
Pin Capacitance			80	pF	
Voltage	1.1	1.2	1.35	V	
Photodiode Monitor Current (Average Current)	50		1200	µA	Resistor setpoint mode
EXTINCTION RATIO SET INPUT (ERSET)					
Resistance Range	1.49		25	kΩ	Resistor setpoint mode
Resistance Range	0.99	1.0	1.01	kΩ	Voltage setpoint mode
AVERAGE POWER REFERENCE VOLTAGE INPUT (PAVREF)					
Voltage Range	0.12		1	V	Voltage setpoint mode (RPAV fixed at 1 kΩ)
Photodiode Monitor Current (Average Current)	120		1000	µA	Voltage setpoint mode (RPAV fixed at 1 kΩ)
EXTINCTION RATIO REFERENCE VOLTAGE INPUT (ERREF)					
Voltage Range	0.05		0.9	V	Voltage setpoint mode (RERSET fixed at 1 kΩ)
DATA INPUTS (DATAP, DATAN)[4]					
V p-p (Differential)	0.4		2.4	V	AC-coupled
Input Impedance (Single-Ended)		50		Ω	
LOGIC INPUTS (ALS)					
V_{IH}	2			V	
V_{IL}			0.8	V	
ALARM OUTPUT (FAIL)[5]					
V_{OFF}		> 1.8		V	Voltage required at FAIL for Ibias and Imod to turn off when FAIL asserted
V_{ON}		< 1.3		V	Voltage required at FAIL for Ibias and Imod to stay on when FAIL asserted

Parameter	Min	Typ	Max	Unit	Conditions/Comments
IBMON, IMMON DIVISION RATIO					
IBIAS/IBMON[3]	85	100	115	A/A	11 mA < IBIAS < 50 mA
IBIAS/IBMON[3]	92	100	108	A/A	50 mA < IBIAS < 100 mA
IBIAS/IBMON STABILITY[3, 6]			±5	%	10 mA < IBIAS < 100 mA
IMOD/IMMON		50		A/A	
IBMON Compliance Voltage	0		1.3	V	
SUPPLY					
I_{CC}[7]		30		mA	When IBIAS = IMOD = 0
V_{CC} (w.r.t. GND)[8]	3.0	3.3	3.6	V	

[1] Temperature range: –40°C to +85°C.
[2] Measured into a 15 Ω load (22 Ω resistor in parallel with digital scope 50 Ω input) using a 11110000 pattern at 2.5 Gbps, shown in Figure 2.
[3] Guaranteed by design and characterization. Not production tested.
[4] When the voltage on DATAP is greater than the voltage on DATAN, the modulation current flows in the IMODP pin.
[5] Guaranteed by design. Not production tested.
[6] IBIAS/IBMON ratio stability is defined in SFF-8472 revision 9 over temperature and supply variation.
[7] I_{CC} min for power calculation in the Power Consumption section.
[8] All VCC pins should be shorted together.

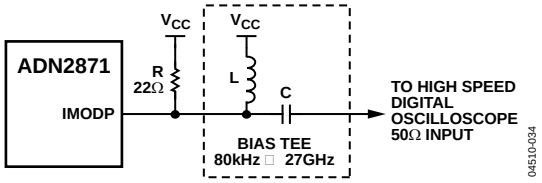

Figure 2. High Speed Electrical Test Output Circuit

SFP TIMING SPECIFICATIONS

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Conditions/Comments
ALS Assert Time	t_off		1	5	µs	Time for the rising edge of ALS (TX_DISABLE) to when the bias current falls below 10% of nominal.
ALS Negate Time[1]	t_on		0.83	0.95	ms	Time for the falling edge of ALS to when the modulation current rises above 90% of nominal.
Time to Initialize, Including Reset of FAIL[1]	t_init		25	275	ms	From power-on or negation of FAIL using ALS.
FAIL Assert Time	t_fault			100	µs	Time to fault to FAIL on.
ALS to Reset time	t_reset			5	µs	Time TX_DISABLE must be held high to reset TX_FAULT.

[1] Guaranteed by design and characterization. Not production tested.

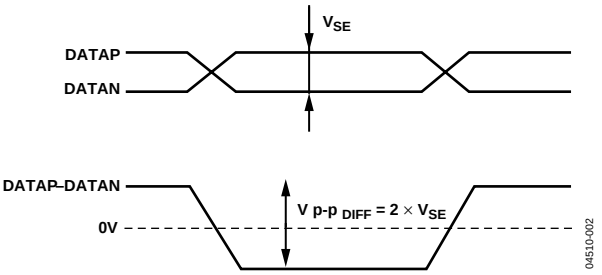

Figure 3. Signal Level Definition

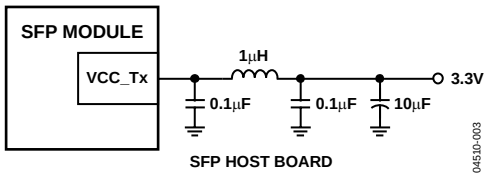

Figure 4. Recommended SFP Supply

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
VCC to GND	4. 2 V
IMODN, IMODP	–0.3 V to +4.8 V
PAVCAP	–0.3 V to +3.9 V
ERCAP	–0.3 V to +3.9 V
PAVSET	–0.3 V to +3.9 V
PAVREF	–0.3 V to +3.9 V
ERREF	–0.3 V to +3.9 V
IBIAS	–0.3 V to +3.9 V
IBMON	–0.3 V to +3.9 V
IMMON	–0.3 V to +3.9 V
ALS	–0.3 V to +3.9 V
CCBIAS	–0.3 V to +3.9 V
RPAV	–0.3 V to +3.9 V
ERSET	–0.3 V to +3.9 V
FAIL	–0.3 V to +3.9 V
DATAP, DATAN (single-ended differential)	1.5 V
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TEMPERATURE SPECIFICATIONS

TEMPERATURE SPECIFICATIONS	
Operating Temperature Range	
Industrial	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	125°C
LFCSP Package	
Power Dissipation[1]	(T_J max − T_A)/θ_{JA} W
θ_{JA} Thermal Impedance[2]	30°C/W
θ_{JC}Thermal Impedance	29.5°C/W
Lead Temperature (Soldering 10 s)	300°C

[1] Power consumption equations are provided in the Power Consumption section.

[2] θ_{JA} is defined when part is soldered on a 4-layer board.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

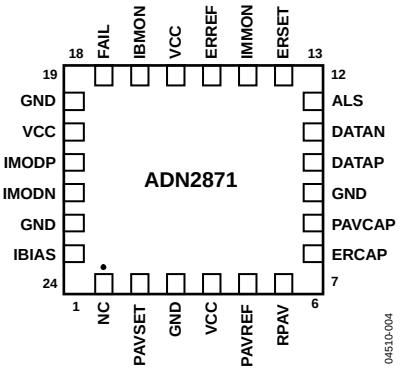

Figure 5. Pin Configuration- Top View

Table 4. Pin Fuction Descriptions

Pin No.	Mnemonic	Description
1	NC	No Connect
2	PAVSET	Average Optical Power Set Pin
3	GND	Supply Ground
4	VCC	Supply Voltage
5	PAVREF	Reference Voltage Input for Average Optical Power Control
6	RPAV	Average Power Resistor when Using PAVREF
7	ERCAP	TBD
8	PAVCAP	Average Power Loop Capacitor
9	GND	Supply Ground
10	DATAP	Data, Positive Differential Input
11	DATAN	Data, Negative Differential Input
12	ALS	Automatic Laser Shutdown
13	ERSET	Extinction Ratio Set Pin
14	IMMON	Modulation Current Monitor Current Source
15	ERREF	Reference Voltage Input for Extinction Ratio Control
16	VCC	Supply Voltage
17	IBMON	Bias Current Monitor Current Source
18	FAIL	FAIL Alarm Output
19	GND	Supply Ground
20	VCC	Supply Voltage
21	IMODP	Modulation Current Positive Output, Connect to Laser Diode
22	IMODN	Modulation Current Negative Output
23	GND	Supply Ground
24	IBIAS	Laser Diode Bias (Current Sink to Ground)

Note: The LFCSP package has an exposed paddle that must be connected to ground.

TYPICAL OPERATING CHARACTERISTICS

V_{CC} = 3.3 V and T_A = 25°C, unless otherwise noted.

OPTICAL WAVEFORMS SHOWING MULTIRATE PERFORMANCE USING LOW COST FABRY PEROT TOSA NEC NX7315UA

Note: No change to PAVCAP and ERCAP values

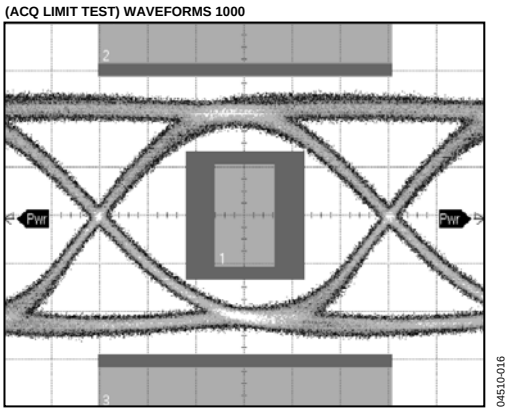

Figure 6. Optical Eye 2.488 Gbps,65 ps/div, PRBS 2^{31-1} PAV = −4.5 dBm, ER = 9 dB, Mask Margin 25%

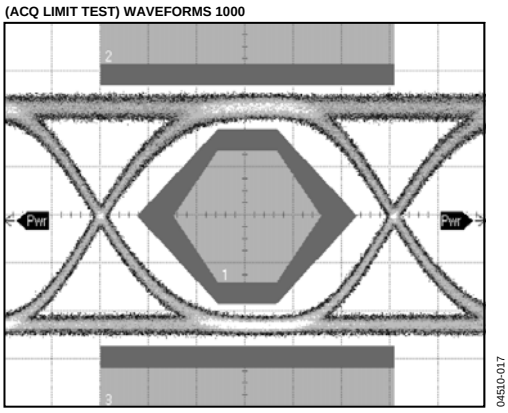

Figure 7. Optical Eye 622 Mbps, 264 ps/div, PRBS 2^{31-1} PAV = −4.5 dBm, ER = 9 dB, Mask Margin 50%

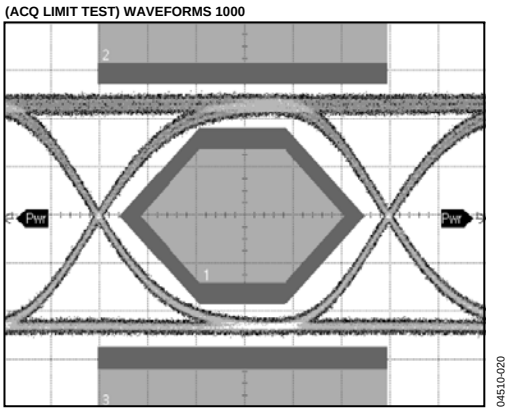

Figure 8. Optical Eye 155 Mbps,1.078 ns/div, PRBS 2^{31-1} PAV = −4.5 dBm, ER = 9 dB, Mask Margin 50%

EXTINCTION RATIO PERFORMANCE OVER TEMPERATURE USING DFB TOSA ?????

Figure 9. Drift of Imod versus Temperature

Figure 10. Honeywekk VCSEL eye

PERFORMANCE CHARACTERISTICS

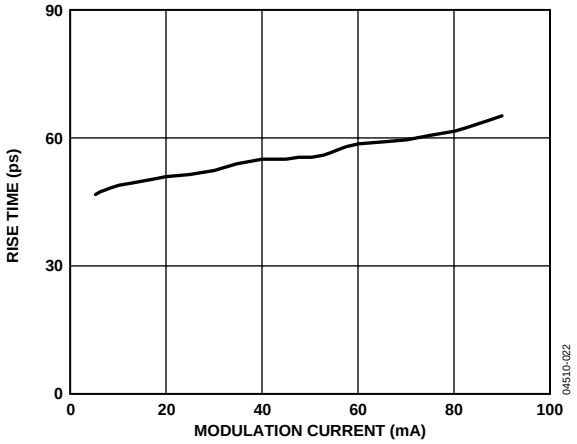

Figure 11. Rise Time vs. Modulation Current, Ibias = 20 mA

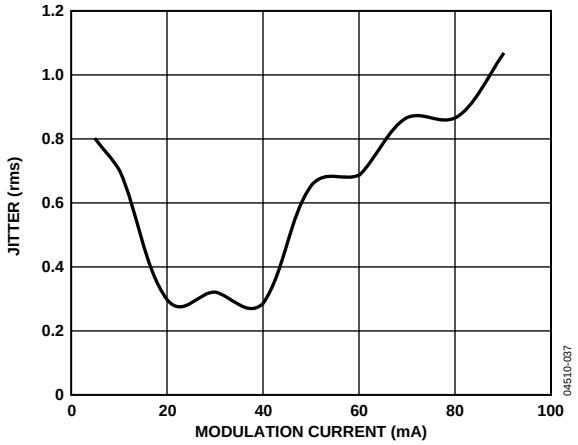

Figure 14. Random Jitter vs. Modulation Current, Ibias = 20 mA

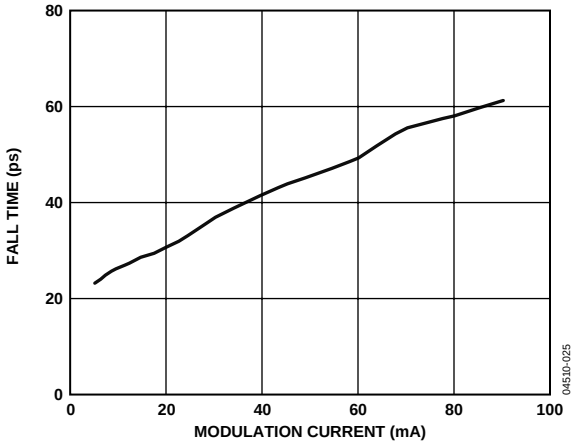

Figure 12. Fall Time vs. Modulation Current, Ibias = 20 mA

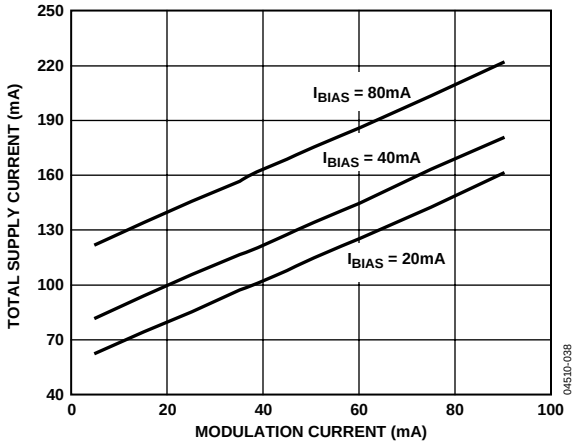

Figure 15. Total Supply Current vs. Modulation Current
Total Supply Current = I_{CC} + Ibias + Imod

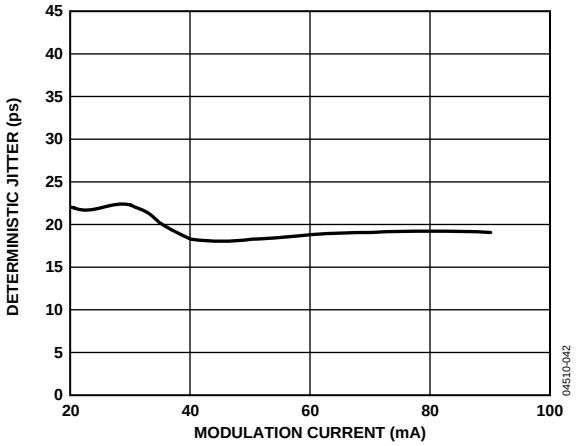

Figure 13. Deterministic Jitter vs. Modulation Current, Ibias = 20 mA

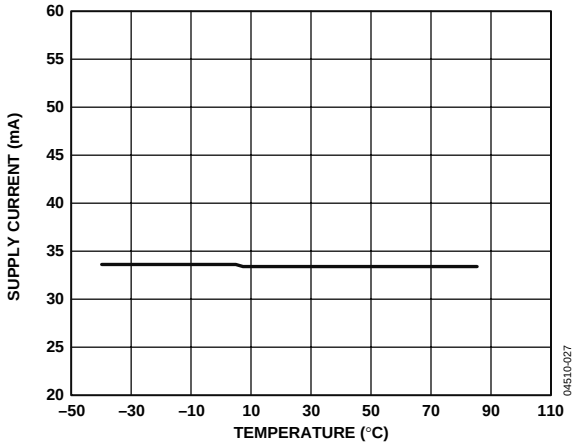

Figure 16. Supply Current (I_{CC}) vs. Temperature with ALS Asserted, Ibias = 20 mA

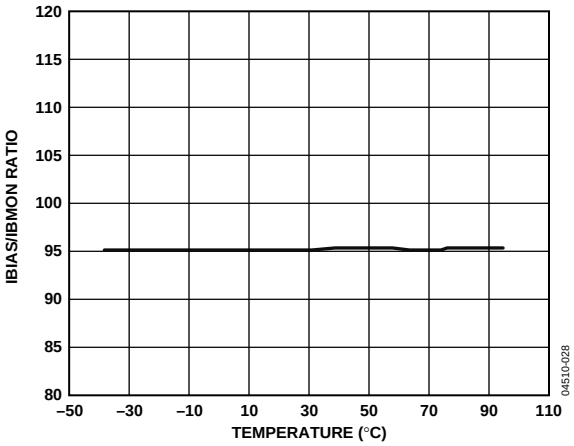

Figure 17. IBIAS/IBMON Gain vs. Temperature, Ibias = 20 mA

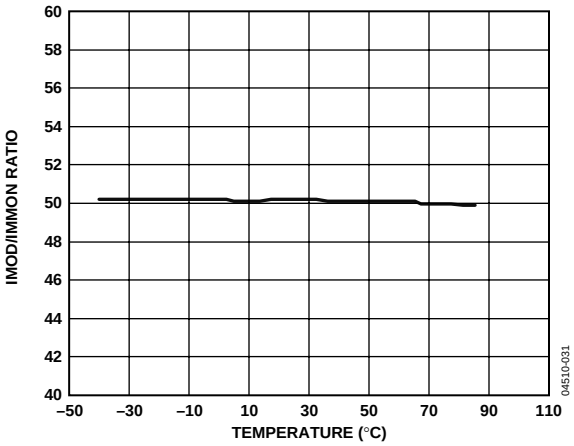

Figure 20. IMOD/IMMON Gain vs. Temperature, Imod = 30 mA

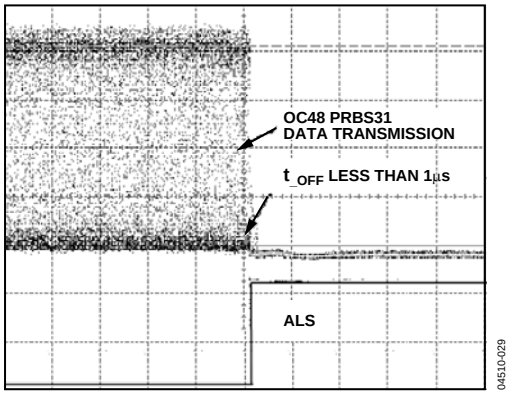

Figure 18. ALS Assert Time, 5 µs/div

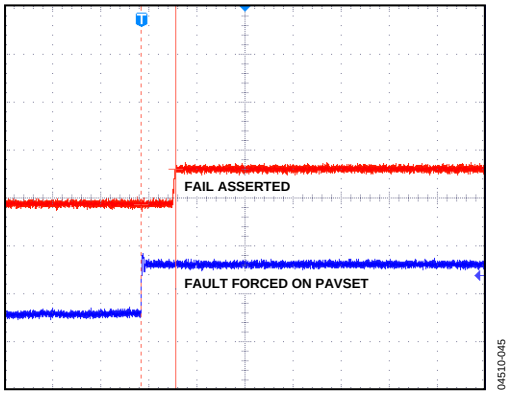

Figure 21. FAIL Assert Time,1 µs/div

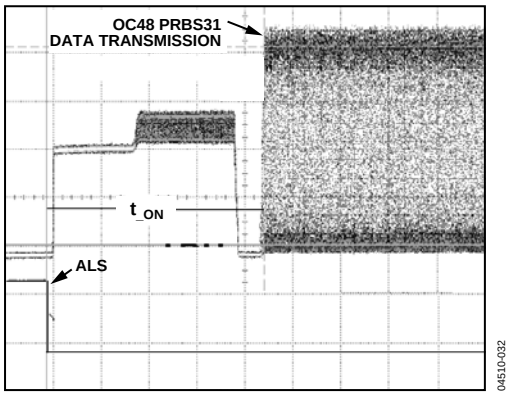

Figure 19. ALS Negate Time, 200 µs/div

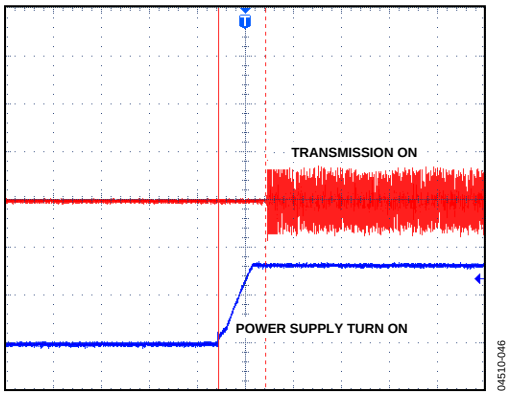

Figure 22. Time to Initialize, Including Reset, 40 ms/div

THEORY OF OPERATION

Laser diodes have a current-in to light-out transfer function as shown in Figure 23. Two key characteristics of this transfer function are the threshold current, Ith, and slope in the linear region beyond the threshold current, referred to as slope efficiency, LI.

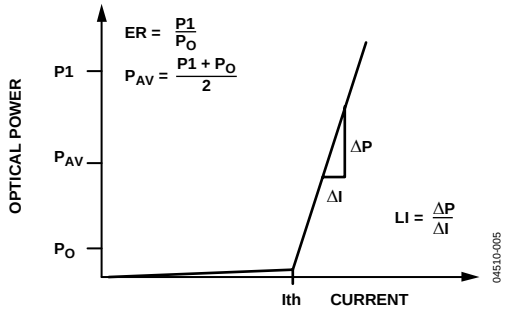

Figure 23. Laser Transfer Function

LASER CONTROL

Typically laser threshold current and slope efficiency are both functions of temperature. For FP and DFB type lasers the threshold current increases and the slope efficiency decreases with increasing temperature. In addition, these parameters vary as the laser ages. To maintain a constant optical average power and a constant optical extinction ratio over temperature and laser lifetime, it is necessary to vary the applied electrical bias current and modulation current to compensate for the lasers changing LI characteristics.

Average Power Control Loop (APCL)

The APCL compensates for changes in Ith and LI by varying Ibias. Average power control is performed by measuring MPD current, Impd. This current is bandwidth-limited by the MPD. This is not a problem because the APCL is required to respond to the average current from the MPD.

Extinction Ratio (ER) Control

ER control is implemented by adjusting the Modulation current. Temperature-calibration is required in order to adjust the Modulation current to compensate for variation of the laser characteristics with temperature.

CONTROL METHODS

The ADN2871 has two methods for setting the average power (PAV) and extinction ratio (ER). The average power and extinction ratio can be voltage-set using a microcontroller's voltage DACs outputs to provide controlled reference voltages PAVREF and ERREF. Alternatively, the average power and extinction ratio can be resistor-set using potentiometers at the PAVSET and ERSET pins, respectively.

VOLTAGE SETPOINT CALIBRATION

The ADN2871 allows interface to a microcontroller for both control and monitoring (see Figure 24). The average power and extinction ratio can be set using the microcontroller's DACs to provide controlled reference voltages PAVREF and ERREF.

$$PAVREF = P_{AV} \times R_{SP} \times RPAV \text{ (Volts)}$$

$$ERREF = \frac{IMOD \times R_{ERSET}}{100} \text{ (Volts)}$$

where:
R_{SP} = Impd/(Laser output power)

P_{AV} is the average power required.

RPAV = R_{ERSET} = 1kOhm

IMOD = Modulation current

In voltage setpoint mode, RPAV and R_{ERSET} must be 1 kΩ resistors with a 1% tolerance and a temperature coefficient of 50 ppm/°C.

Note that during power up, there is an internal sequence that allows 25 ms before enabling the alarms; therefore the customer must ensure that the voltage for PAVREF and ERREF are active within 20 ms after ramp-up of the power supply.

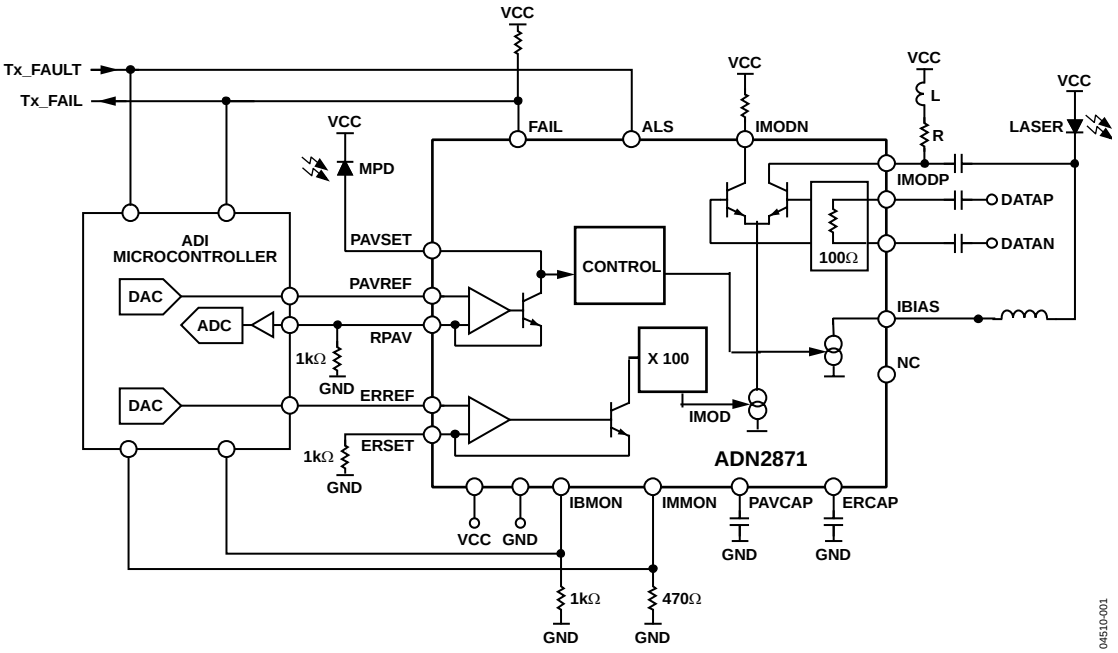

Figure 24. ADN2871 Using Microconverter Calibration and Monitoring

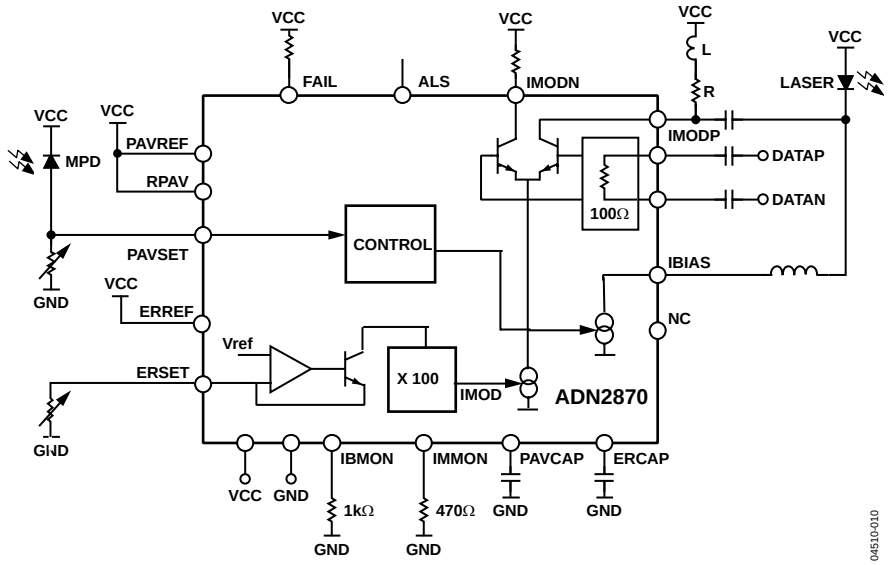

Figure 25. ADN2871 Using Resistor Setpoint Calibration of Average Power and Extinction Ratio

RESISTOR SETPOINT CALIBRATION

In resistor setpoint calibration. PAVREF, ERREF, and RPAV must all be tied to VCC. Average power and extinction ratio can be set using the PAVSET and ERSET pins, respectively. A resistor is placed between the pin and GND to set the current flowing in each pin as shown in Figure 25. The ADN2871 ensures that both PAVSET and ERSET are kept 1.23 V above GND. The PAVSET and ERSET resistors are given by the following:

$$R_{PAVSET} = \frac{1.23\ \text{V}}{P_{AV} \times R_{SP}}\ (\Omega)$$

$$R_{ERSET} = \frac{1.23\ \text{V} \times 100}{IMOD}\ \ (\Omega)$$

where:
R_{SP} = Impd/(Laser output power)
IMOD is the modulation current required.

P_{AV} is the average power required

IMPD MONITORING

IMPD monitoring can be implemented for voltage setpoint and resistor setpoint as follows.

Voltage Setpoint

In voltage setpoint calibration, the following methods may be used for IMPD monitoring.

Method 1: Measuring Voltage at RPAV

The IMPD current is equal to the voltage at RPAV divided by the value of RPAV (see Figure 26) as long as the laser is on and is being controlled by the control loop. This method does not provide a valid IMPD reading when the laser is in shut-down or fail mode. A microconverter buffered A/D input may be connected to RPAV to make this measurement. No decoupling or filter capacitors should be placed on the RPAV node because this can disturb the control loop.

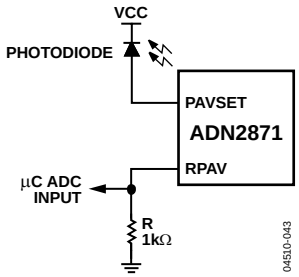

Figure 26. Single Measurement of IMPD RPAV in Voltage Setpoint Mode

Method 2: Measuring IMPD Across a Sense Resistor

The second method has the advantage of providing a valid IMPD reading at all times, but has the disadvantage of requiring a differential measurement across a sense resistor directly in series with the IMPD. As shown in Figure 27, a small resistor, Rx, is placed in series with the IMPD. If the laser used in the design has a pinout where the monitor photodiode cathode and the lasers anode are not connected, a sense resistor can be placed in series with the photodiode cathode and VCC as shown in Figure 28. When choosing the value of the resistor, the user must take into account the expected IMPD value in normal operation. The resistor must be large enough to make a significant signal for the buffered A/Ds to read, but small enough so as not to cause a significant voltage reduction across the IMPD. The voltage across the sense resistor should not exceed 250 mV when the laser is in normal operation. It is recommended that a 10 pF capacitor be placed in parallel with the sense resistor.

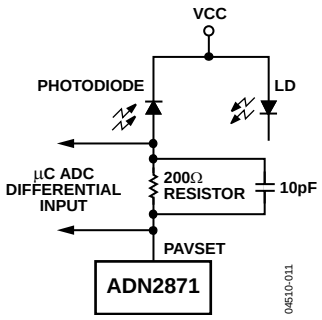

Figure 27. Differential Measurement of IMPD Across a Sense Resistor

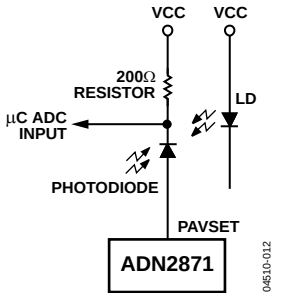

Figure 28. Single Measurement of IMPD Across a Sense Resistor

Resistor Setpoint

In resistor setpoint calibration, the current through the resistor from PAVSET to ground is the IMPD current. The recommended method for measuring the IMPD current is to place a small resistor in series with PAVSET resistor (or potentiometer) and measure the voltage across this resistor as shown in Figure 29. The IMPD current is then equal to this voltage divided by the value of resistor used. In resistor setpoint, PAVSET is held to 1.2 V nominal; it is recommended that the sense resistor should be selected so that the voltage across the sense resistor does not exceed 250 mV.

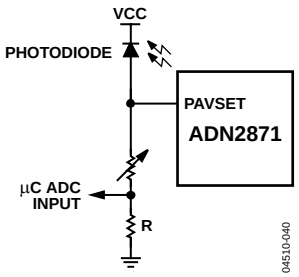

Figure 29. Single Measurement of IMPD Across a Sense Resistor in Resistor Setpoint IMPD Monitoring

LOOP BANDWIDTH SELECTION

To ensure that the ADN2871 control loop has sufficient bandwidth, the average power loop capacitor (PAVCAP) is calculated using the lasers slope efficiency (watts/amps) and the average power required.

For resistor setpoint control:

$$PAVCAP = 3.2E-6 \times \frac{LI}{PAV}(Farad)$$

For voltage setpoint control:

$$PAVCAP = 1.28E-6 \times \frac{LI}{PAV}(Farad)$$

where *PAV* is the average power required and *LI* (mW/mA) is the typical slope efficiency at 25°C of a batch of lasers that are used in a design. The capacitor value equation is used to get a centered value for the particular type of laser that is used in a design and average power setting. The laser LI can vary by a factor of 7 between different physical lasers of the same type and across temperature without the need to recalculate the PAVCAP and ERCAP values. In ac coupling configuration the LI can be calculated as follows:

$$LI = \frac{P1-P0}{Imod}\ (\text{mW/mA})$$

where *P1* is the optical power (mW) at the one level, and *P0* is the optical power (mW) at the zero level.

This capacitor is placed between the PAVCAP pin and ground. It is important that the capacitor is a low leakage multilayer ceramic with an insulation resistance greater than 100 GΩ or a time constant of 1000 sec, whichever is less. Pick a standard off-the-shelf capacitor value such that the actual capacitance is within +/-30% of the calculated value after the capacitors own tolerance is taken into account.

POWER CONSUMPTION

The ADN2871 die temperature must be kept below 125°C. The LFCSP package has an exposed paddle, which should be connected such that is at the same potential as the ADN2871 ground pins. Power consumption can be calculated as follows:

$$I_{CC} = I_{CC}\ min + 0.3\ I_{MOD}$$

$$P = V_{CC} \times I_{CC} + (I_{BIAS} \times V_{BIAS\_PIN}) + I_{MOD}\ (V_{MODP\_PIN} + V_{MODN\_PIN})/2$$

$$T_{DIE} = T_{AMBIENT} + \theta_{JA} \times P$$

Thus, the maximum combination of $I_{BIAS} + I_{MOD}$ must be calculated.

where:

$I_{CC}\ min$ = 30 mA, the typical value of I_{CC} provided in the Specifications with $I_{BIAS} = I_{MOD} = 0$.
T_{DIE} is the die temperature.
$T_{AMBIENT}$ is the ambient temperature.
V_{BIAS_PIN} is the voltage at the IBIAS pin.
V_{MODP_PIN} is the voltage at the IMODP pin.
V_{MODN_PIN} is the voltage at the IMODN pin.

AUTOMATIC LASER SHUTDOWN (TX_DISABLE)

ALS (TX disable) is an input that is used to shut down the transmitter optical output. The ALS pin is pulled up internally with a 6 kΩ resistor, and conforms to SFP MSA specification. When ALS is logic high or when open, both the bias and modulation currents are turned off.

BIAS AND MODULATION MONITOR CURRENTS

IBMON and IMMON are current-controlled current sources that mirror a ratio of the bias and modulation current. The monitor bias current, IBMON, and the monitor modulation current, IMMON, should both be connected to ground through a resistor to provide a voltage proportional to the bias current and modulation current, respectively. When using a micro-controller, the voltage developed across these resistors can be connected to two of the ADC channels, making available a digital representation of the bias and modulation current.

DATA INPUTS

Data inputs should be ac-coupled (10 nF capacitors are recommended) and are terminated via a 100 Ω internal resistor between the DATAP and DATAN pins. A high impedance circuit sets the common-mode voltage and is designed to allow maximum input voltage headroom over temperature. It is necessary to use ac coupling to eliminate the need for matching between common-mode voltages.

LASER DIODE INTERFACING

The schematic in Figure 30 describes the recommended circuit for interfacing the ADN2871 to most TO-Can or Coax lasers. These lasers typically have impedances of 5 Ω to 7 Ω, and have axial leads. The circuit shown works over the full range of data rates from 155 Mbps to 3.3 Gbps including multirate operation (with no change to PAVCAP and ERCAP values); see the Typical Operating Characteristics for multirate performance examples. Coax lasers have special characteristics that make them difficult to interface to. They tend to have higher inductance, and their impedance is not well controlled. The circuit in Figure 30 operates by deliberately misterminating the transmission line on the laser side, while providing a very high quality matching network on the driver side. The impedance of the driver side matching network is very flat versus frequency and enables multirate operation. A series damping resistor should not be used.

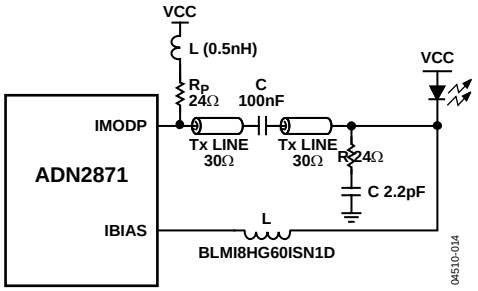

Figure 30. Recommended Interface for ADN2871 AC Coupling

The 30 Ω transmission line used is a compromise between drive current required and total power consumed. Other transmission line values can be used, with some modification of the component values. The R and C snubber values in Figure 30, 24 Ω and 2.2 pF, respectively, represent a starting point and must be tuned for the particular model of laser being used. R_P, the pull-up resistor is in series with a very small (0.5 nH) inductor. In some cases, an inductor is not required or can be accommodated with deliberate parasitic inductance, such as a thin trace or a via, placed on the PC board.

Care should be taken to mount the laser as close as possible to the PC board, minimizing the exposed lead length between the laser can and the edge of the board. The axial lead of a coax laser are very inductive (approximately 1 nH per mm). Long exposed leads result in slower edge rates and reduced eye margin.

Recommended component layouts and gerber files are available by contacting the factory. Note that the circuit in Figure 30 can supply up to 56 mA of modulation current to the laser, sufficient for most lasers available today. Higher currents can be accommodated by changing transmission lines and backmatch values; contact factory for recommendations. This interface circuit is not recommended for butterfly-style lasers or other lasers with 25 Ω characteristic impedance. Instead, a 25 Ω transmission line and inductive (instead of resistive) pull-up is recommended; contact the factory for recommendations.

The ADN2871 also supports differential drive schemes. These can be particularly useful when driving VCSELs or other lasers with slow fall times. Differential drive can be implemented by adding a few extra components. A possible implementation is shown in Figure 31.

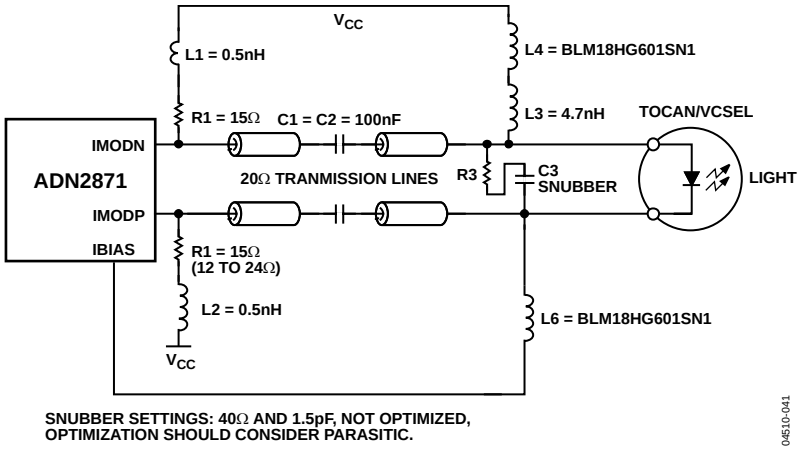

Figure 31. Recommended Differential Drive Circuit

ALARMS

The ADN2871 has a latched active high monitoring alarm (FAIL). The FAIL alarm output is an open drain in conformance to SFP MSA specification requirements.

The ADN2871 has a 3-fold alarm system that covers

- Use of a bias current higher than expected, probably as a result of laser aging.
- Out-of-bounds average voltage at the monitor photodiode (MPD) input, indicating an indicating an excessive amount of laser power or a broken loop.
- Undervoltage in IBIAS node (laser diode cathode) that would increase the laser power.

The bias current alarm trip point is set by selecting the value of resistor on the IBMON pin to GND. The alarm is triggered when the voltage on the IBMON pin goes above 1.2 V.

FAIL is activated when the single-point faults in Table 5 occur.

Table 5. ADN2871 Single-Point Alarms

Alarm Type	Pin Name	Over Voltage or Short to VCC Condition	Under Voltage or Short to GND Condition
1. Bias Current	IBMON	Alarm if > 1.2 V	Ignore
2. MPD Current	PAVSET	Alarm if > 1.7 V	Alarm if < 0.9 V
3. Crucial Nodes	ERREF	Alarm if shorted to VCC	Alarm if shorted to GND
	IBIAS	Ignore	Alarm if < 400 mV

Table 6. ADN2871 Response to Various Single-Point Faults in AC-Coupled Configuration as Shown in Figure 30

Pin	Short to VCC	Short to GND	Open
CCBIAS	Fault state occurs	Fault state occurs	Does not increase laser average power
PAVSET	Fault state occurs	Fault state occurs	Fault state occurs
PAVREF	Voltage mode: Fault state occurs Resistor mode: Tied to VCC	Fault state occurs	Fault state occurs
RPAV	Voltage mode: Fault state occurs Resistor mode: Tied to VCC	Fault state occurs	Voltage mode: Fault state occurs Resistor mode: Does not increase average power
ERCAP	Does not increase laser average power	Does not increase laser average power	Does not increase laser average power
PAVCAP	Fault state occurs	Fault state occurs	Fault state occurs
DATAP	Does not increase laser average power	Does not increase laser average power	Does not increase laser average power
DATAN	Does not increase laser average power	Does not increase laser average power	Does not increase laser average power
ALS	Output currents shut off	Normal currents	Output currents shut off
ERSET	Does not increase laser average power	Does not increase laser average power	Does not increase laser average power
IMMON	Does not affect laser power	Does not increase laser average power	Does not increase laser average power
ERREF	Voltage mode: Fault state occurs Resistor mode: Tied to VCC	Voltage mode: Does not increase average power Resistor mode: Fault state occurs	Does not increase laser average power
IBMON	Fault state occurs	Does not increase laser average power	Does not increase laser average power
FAIL	Fault state occurs	Does not increase laser average power	Does not increase laser average power
IMODP	Does not increase laser average power	Does not increase laser average power	Does not increase laser average power
IMODN	Does not increase laser average power	Does not increase laser average power	Does not increase laser power
IBIAS	Fault state occurs	Fault state occurs	Fault state occurs

OUTLINE DIMENSIONS

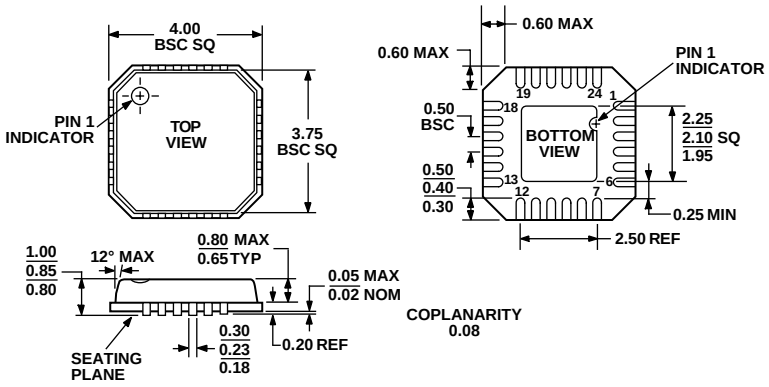

Figure 32. 24-Lead Lead Frame Chip Scale Package [LFCSP]
(CP-24)
Dimensions shown in millimeters

Note: The LFCSP package has an exposed paddle that must be connected to ground.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADN2871ACPZ[1]	–40°C to +85°C	24-Lead Lead Frame Chip Scale Package	CP-24
ADN2871ACPZ-RL[1]	–40°C to +85°C	24-Lead Lead Frame Chip Scale Package	CP-24
ADN2871ACPZ-RL7[1]	–40°C to +85°C	24-Lead Lead Frame Chip Scale Package	CP-24

[1] Z = Pb-free part.

NOTES

PR05228-0-10/04(PrA)