CCD Signal Processor with Precision Timing™ Generator

AD9929

FEATURES

36 MSPS correlated double sampler (CDS)
12-bit 36 MHz A/D converter
On-chip vertical driver for CCD image sensor
On-chip horizontal driver for CCD image sensor
6 dB to 40 dB variable gain amplifier (VGA)
Black level clamp with variable level control
Complete on-chip timing generator
Precision Timing core with 0.58 ns resolution
2-phase H-clock modes
4-phase vertical transfer clocks
Electronic and mechanical shutter modes
On-chip sync generator with external sync option
64-lead, plastic ball, 9 × 9 grid array Pb-free package

APPLICATION

Digital still cameras
Digital video camcorders

PRODUCT DESCRIPTION

The AD9929 is a highly integrated CCD signal processor for digital still camera and digital video camera applications. It includes a complete analog front end with A/D conversion, combined with a full-function, programmable timing generator. The AD9929 also includes horizontal and vertical clock drivers, which allow direct connection to the CCD image sensor.

The AD9929 is specified at pixel rates of up to 36 MHz. The analog front end includes black level clamping, a CDS, a VGA, and a 12-bit A/D converter. The timing generator provides all the necessary CCD clocks: RG-clock, H-clocks, V-clocks, sensor gate pulses, a substrate clock, and a substrate bias pulse. Operation is programmed using a 3-wire serial interface.

The AD9929 is packaged in a 64-lead CSPBGA. It is specified over an operating temperature range of −25°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

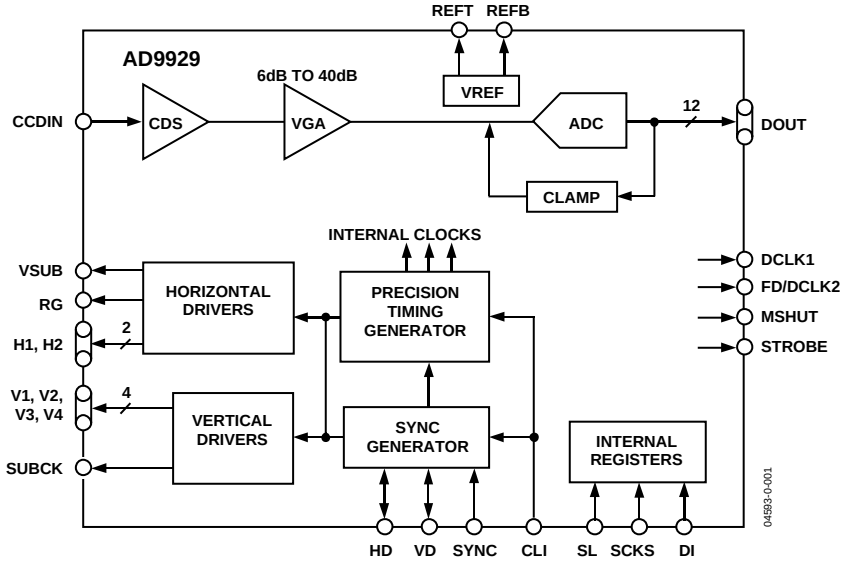

Figure 1.

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REVISION HISTORY

Revision A

2/04—Data Sheet Changed from Rev. 0 to Rev. A

Replaced Figure ... 21

1/04—Revision 0: Initial Version

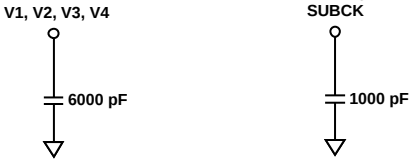
SPECIFICATIONS

Table 1.

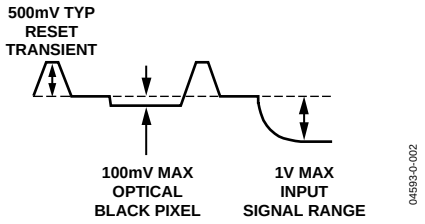
Parameter	Min	Typ	Max	Unit
TEMPERATURE RANGE				
Operating	−25		+85	°C
Storage	−65		+150	°C
POWER SUPPLY VOLTAGE				
AVDD (AFE Analog Supply)	2.7	3.0	3.6	V
TCVDD (Timing Core Analog Supply)	2.7	3.0	3.6	V
RGVDD (RG Driver)	2.7	3.0	3.6	V
HVDD (H1 to H2 Drivers)	2.7	3.0	3.6	V
DRVDD (Data Output Drivers)	2.7	3.0	3.6	V
DVDD (Digital)	2.7	3.0	3.6	V
VERTICAL DRIVER SUPPLY VOLTAGE				
VDD (Vertical Driver Input Logic Supply)	2.7	3.0	3.6	V
VH1, VH2 (Vertical Driver High Supply)	11.5	15.0	16.0	V
VM1, VM2 (Vertical Driver Mid Supply)	−1.0	0.0	1.0	V
VL (Vertical Driver Low Supply for 3 Level and 2 Level)	−9.0	−7.5	−5.0	V
AFETG POWER DISSIPATION				
36 MHz, Typ Supply Levels, 100 pF H1 to H2 Loading		180		mW
Power from HVDD Only[1]		36		mW
Power-down Mode (AFE and Digital in Standby Operation)		1		mW
VERTICAL DRIVER POWER DISSIPATION[2] (6000 pF V1 to V4 Loading, 1000 pF SUBCK Loading)				
Power from VDD		<1.0		mW
Power from VH1		23.0		mW
Power from VH2		15.0		mW
Power from VL		42.0		mW
MAXIMUM CLOCK RATE (CLI) AD9929	36			MHz

[1] The total power dissipated by the HVDD supply may be approximated by using the equation:
Total HVDD Power = [C_{LOAD} × *HVDD* × *Pixel Frequency*] × *HVDD* × *Number of H-Outputs Used*.
Actual HVDD power may be slightly different than the calculated value because of the stray capacitance inherent in the PCB layout/routing.

[2] Vertical driver loads used when characterizing power consumption. Note: actual power depends on the V1 to V4 timing and number of SUBCKs.



INPUT SIGNAL CHARACTERISTICS DEFINED AS FOLLOWS:



DIGITAL SPECIFICATIONS

Table 2. RGVDD = HVDD = 2.7 V to 3.6 V, DVDD = DRVDD = 2.7 V to 3.6 V, C_L = 20 pF, T_{MIN} to T_{MAX}, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit
LOGIC INPUTS					
High Level Input Voltage	V_{IH}	2.1			V
Low Level Input Voltage	V_{IL}			0.6	V
High Level Input Current	I_{IH}		10		µA
Low Level Input Current	I_{IL}		10		µA
Input Capacitance	C_{IN}		10		pF
LOGIC OUTPUTS (Except H and RG)					
High Level Output Voltage @ I_{OH} = 2 mA	V_{OH}	2.2			V
Low Level Output Voltage @ I_{OL} = 2 mA	V_{OL}			0.5	V
RG and H-DRIVER OUTPUTS (H1 to H2)					
High Level Output Voltage @ Max Current	V_{OH}	VDD − 0.5			V
Low Level Output Voltage @ Max Current	V_{OL}			0.5	V
RG Maximum Output Current (Programmable)				15	mA
H1 and H2 Maximum Output Current (Programmable)				30	mA
Maximum Load Capacitance		100			pF

ANALOG SPECIFICATIONS

Table 3. AVDD = 3.0 V, f_{CLI} = 36 MHz, T_{MIN} to T_{MAX}, unless otherwise noted.

Parameter	Min	Typ	Max	Unit	Notes
CDS					
Allowable CCD Reset Transient		500		mV	See input signal characteristics in Table 1.
Max Input Range before Saturation	1.0			V p–p	
Max CCD Black Pixel Amplitude		±100		mV	
VARIABLE GAIN AMPLIFIER (VGA)					
Max Output Range	2.0			V p–p	
Gain Control Resolution		1024		Steps	
Gain Monotonicity		Guaranteed			
Gain Range					
Low Gain		6		dB	
Max Gain		40		dB	
BLACK LEVEL CLAMP					
Clamp Level Resolution		255		Steps	
Clamp Level				LSB	LSB measured at ADC output.
Min Clamp Level		0		LSB	
Max Clamp Level		255		LSB	
A/D CONVERTER					
Resolution	10			Bits	
Differential Nonlinearity (DNL)		±0.5		LSB	
No Missing Codes		Guaranteed			
Full-Scale Input Voltage		2.0		V	
VOLTAGE REFERENCE					
Reference Top Voltage (REFT)		2.0		V	
Reference Bottom Voltage (REFB)		1.0		V	
SYSTEM PERFORMANCE					Includes entire signal chain.
Gain Accuracy					
Low Gain (VGA Code = 22)		6		dB	Gain = (0.035 × Code) + 5.2 dB.
Max Gain (VGA Code = 994)		40		dB	
Peak Nonlinearity, 500 mV Input Signal		0.1		%	12 dB gain applied.
Total Output Noise		0.3		LSB rms	AC grounded input, 6 dB gain applied.
Power Supply Rejection (PSR)		40		dB	Measured with step change on supply.

TIMING SPECIFICATIONS

Table 4. C_L = 20 pF, AVDD = DVDD = DRVDD = 3.0 V, f_{CLI} = 36 MHz, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit
MASTER CLOCK, CLI					
CLI Clock Period	t_{CONV}	27.8			ns
CLI High/Low Pulse Width			13.9		ns
Delay from CLI Rising Edge to Internal Pixel Position 0	t_{CLIDLY}		6		ns
AFE CLAMP PULSES[1]					
CLPOB Pulse Width		4	10		Pixels
AFE SAMPLE LOCATION[1] (See Figure 17)					
SHP Sample Edge to SHD Sample Edge	T_{S1}	20	25		Pixels
DATA OUTPUTS					
Output Delay from DCLK1 Rising Edge (See Figure 19)	t_{OD}		9		ns
Pipeline Delay from SHP/SHD Sampling (See Figure 70)				9	Cycles
SERIAL INTERFACE (See Figure 10 and Figure 11)	t_{DV}				
Maximum SCK Frequency	f_{SCLK}	10			MHz
SL to SCK Setup Time	t_{LS}	10			ns
SCK to SL Hold Time	t_{LH}	10			ns
SDATA Valid to SCK Rising Edge Setup	t_{DS}	10			ns
SCK Falling Edge to SDATA Valid Hold	t_{DH}	10			ns
SCK Falling Edge to SDATA Valid Read	t_{OD}	10			ns

[1] Parameter is programmable.

VERTICAL DRIVER SPECIFICATIONS

Table 5. V1 to V4 load = no load, SUBCK load = no load, VDD = 3.0 V, VL = −7.5 V, VH1 = VH2 = +15.0 V, VM1 = VM2 = GND, f_{CLI} = 36 MHz, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit
LOGIC INPUTS					
High Level Input Voltage	V_{IH}	0.8 (VDD)		VDD	V
Low Level Input Voltage	V_{IL}	0	0.3 (VDD)	V	
Propagation Delays, Rise/Fall Times and Output Currents					
V1 and V3 Outputs (See Figure 43)					
Delay Times					
VL to VM1	t_{PLM1}		100		ns
VM1 to VH1	t_{PMH}		100		ns
VH1 to VM1	t_{PHM}		50		ns
VM1 to VL	t_{PML1}		50		ns
Rise Times					
VL to VM1	t_{R1}		500		ns
VM1 to VH1	t_{R2}		500		ns
Fall Times					
VH1 to VM1	t_{F1}		500		ns
VM1 to VL	t_{F2}		500		ns
Output Currents					
V1 or V3 @ VL = −7.25 V			10.0		mA
V1 or V3 @ VM1 = −0.25 V			−5.0		mA
V1 or V3 @ VM1 = +0.25 V			5.0		mA
V1 or V3 @ VH1 = +14.75 V			−7.2		mA

Parameter	Symbol	Min	Typ	Max	Unit
V2 and V4 Outputs (See Figure 43)					
Delay Times					
VL to VM2	t_{PLM2}		100		ns
VM2 to VL	t_{PML2}		50		ns
Rise Times					
VL to VM2	t_{R3}		500		ns
Fall Times					
VM2 to VL	t_{F3}		500		ns
Output Currents					
V2 or V2 @ VL =−7.25 V			10.0		mA
V2 or V4 @ VM2 = −0.25 V			−5.0		mA
SUBCK Output (See Figure 44)					
Delay Times					
VL to VH2	t_{PLH}		100		ns
VH2 to VL	t_{PHL}		50		ns
Rise Times					
VL to VH2	t_{R4}		90		ns
Fall Times					
VH2 to VL	t_{F4}		90		ns
Output Currents					
SUBCK @ VL = −7.25 V			5.4		mA
SUBCK @ VH2 = 14.75 V			−4.0		mA

TERMINOLOGY

Differential Nonlinearity (DNL)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Thus every code must have a finite width. "No missing codes guaranteed to 12-bit resolution" indicates that all 4096 codes, respectively, must be present over all operating conditions.

Peak Nonlinearity

Peak nonlinearity, a full signal-chain specification, refers to the peak deviation of the output of the AD9929 from a true straight line. The point used as zero scale occurs 1/2 LSB before the first code transition. "Positive full scale" is defined as a level 1 and 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each particular output code to the true straight line. The error is then expressed as a percentage of the 2 V ADC full-scale signal. The input signal is always appropriately gained up to fill the ADC's full-scale range.

Total Output Noise

The rms output noise is measured using histogram techniques. The standard deviation of the ADC output codes is calculated in LSBs, and represents the rms noise level of the total signal chain at the specified gain setting. The output noise can be converted to an equivalent voltage, using the relationship 1 LSB = (*ADC full scale*/2^N codes) when N is the bit resolution of the ADC. For the AD9929, 1 LSB is 0.5 mV.

Power Supply Rejection (PSR)

The PSR is measured with a step change applied to the supply pins. The PSR specification is calculated from the change in the data outputs for a given step change in the supply voltage.

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	With Respect To	Min	Max	Unit
VDD	VDVSS	VDVSS – 0.3	VDVSS + 4.0	V
VL	VDVSS	VDVSS – 10.0	VDVSS + 0.3	V
VH1, VH2	VDVSS	VL –0.3	VL + 27.0	V
VM1, VM2	VDVSS	VL – 0.3	VL + 27.0	V
AVDD	AVSS	–0.3	+3.9	V
TCVDD	TCVSS	–0.3	+3.9	V
HVDD	HVSS	–0.3	+3.9	V
RGVDD	RGVSS	–0.3	+3.9	V
DVDD	DVSS	–0.3	+3.9	V
DRVDD	DRVSS	–0.3	+3.9	V
RG Output	RGVSS	–0.3	RGVDD + 0.3	V
H1 to H2 Output	HVSS	–0.3	HVDD + 0.3	V
Digital Outputs	DVSS	–0.3	DVDD + 0.3	V
Digital Inputs	DVSS	–0.3	DVDD + 0.3	V
SCK, SL, SDATA	DVSS	–0.3	DVDD + 0.3	V
REFT, REFB	AVSS	–0.3	AVDD + 0.3	V
CCDIN	AVSS	–0.3	AVDD + 0.3	V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Resistance

θ_{JA} = 61.0 °C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulates on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTIONAL DESCRIPTIONS

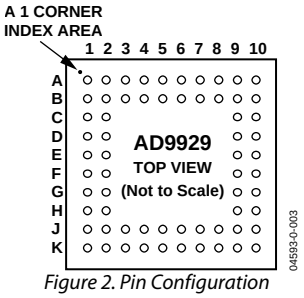


Figure 2. Pin Configuration

Table 7. Pin Function Descriptions

Pin	Mnemonic	Type[1]	Description
D1	VD	DIO	Vertical Sync Pulse (Input for Slave Mode, Output for Master Mode)
D2	HD	DIO	Horizontal Sync Pulse (Input for Slave Mode, Output for Master Mode)
B8	D0	DO	Data Output
A8	D1	DO	Data Output
A7	D2	DO	Data Output
B7	D3	DO	Data Output
A6	D4	DO	Data Output
B6	D5	DO	Data Output
B5	D6	DO	Data Output
A4	D7	DO	Data Output
B3	D8	DO	Data Output
A3	D9	DO	Data Output
B2	D10	DO	Data Output
A2	D11	DO	Data Output
A1	DCLK1	DO	Data Clock Output
B4	DRVSS	P	Data Output Driver Ground
A5	DRVDD	P	Data Output Driver Supply
G9	SUBCK	DO	CCD Substrate Clock (2 Level: VH2, VL)
D10	V1	DO	CCD Vertical Transfer Clock (3 Level: VH1, VM1, VL)
E9	V2	DO	CCD Vertical Transfer Clock (2 Level: VM2, VL)
G10	V3	DO	CCD Vertical Transfer Clock (3 Level: VH1, VM1, VL)
H9	V4	DO	CCD Vertical Transfer Clock (2 Level: VM2, VL)
H10	VH1	P	Vertical Driver High Supply (High Supply for V1 and V3)
C10	VM1	P	Vertical Driver Midsupply (Midsupply for V1 and V3)
F10	VM2	P	Vertical Driver Midsupply (Midsupply for V2 and V4)
F9	VL	P	Vertical Driver Low Supply
E10	VH2	P	Vertical Driver High Supply for SUBCK
B10	VDD	P	Vertical Driver Input Logic Supply
J9	VDVSS	P	Vertical Driver Ground
A9	VSUB	DO	CCD Substrate Bias
G1	H1	DO	CCD Horizontal Clock
F1	H2	DO	CCD Horizontal Clock
E1	HVDD	P	H1 and H2 Driver Supply
E2	HVSS	P	H1 and H2 Driver Ground
F2	HVSS	P	H1 and H2 Driver Ground
G2	HVSS	P	H1 and H2 Driver Ground
H1	RG	DO	CCD Reset Gate Clock
J1	RGVDD	P	RG Driver Supply
H2	RGVSS	P	RG Driver Ground
C9	SYNC or VGATE	DI DI	External System Sync Input VGATE Input
C1	FD or DCLK2	DO DO	Field Designator Output DCLK2 Output
K3	AVDD	P	Analog Supply for AFE
J3	AVSS	P	Analog Ground for AFE
J4	AVSS	P	Analog Ground for AFE
J5	AVSS	P	Analog Ground for AFE
J6	AVSS	P	Analog Ground for AFE
J7	AVSS	P	Analog Ground for AFE
J8	AVSS	P	Analog Ground for AFE
K4	AVSS	P	Analog Ground for AFE
K6	AVSS	P	Analog Ground for AFE
J2	CLI	DI	Reference Clock Input
K2	TCVDD	P	Analog Supply for Timing Core
K1	TCVSS	P	Analog Ground for Timing Core
K5	CCDIN	AI	CCD Input Signal
K7	REFT	AO	Voltage Reference Top Bypass
K8	REFB	AO	Voltage Reference Bottom Bypass
K9	SDATA	DI	3-Wire Serial Data Input
K10	SL	DI	3-Wire Serial Load Pulse
J10	SCK	DI	3-Wire Serial Clock
D9	OUTCONT	DI	Output Control
B1	MSHUT	DO	Mechanical Shutter Pulse
C2	STROBE	DO	Strobe Pulse
A10	DVDD	P	Digital Supply
B9	DVSS	P	Digital Ground

[1] AI = Analog Input, AO = Analog Output, DI = Digital Input, DO = Digital Output, DIO = Digital Input/Output, P = Power.

EQUIVALENT INPUT CIRCUITS

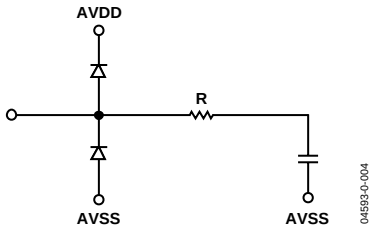


Figure 3. Circuit 1. CCDIN

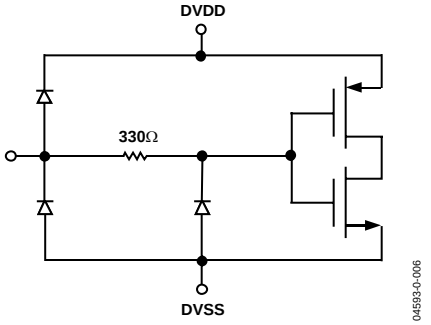


Figure 5. Circuit 3. Digital Inputs

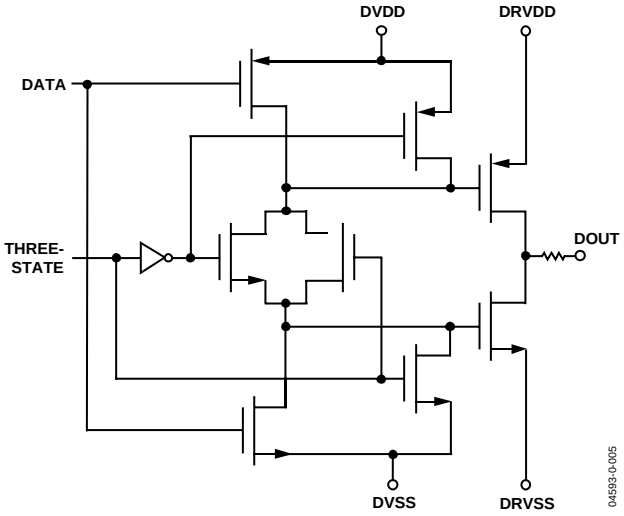


Figure 4. Circuit 2. Digital Data Output

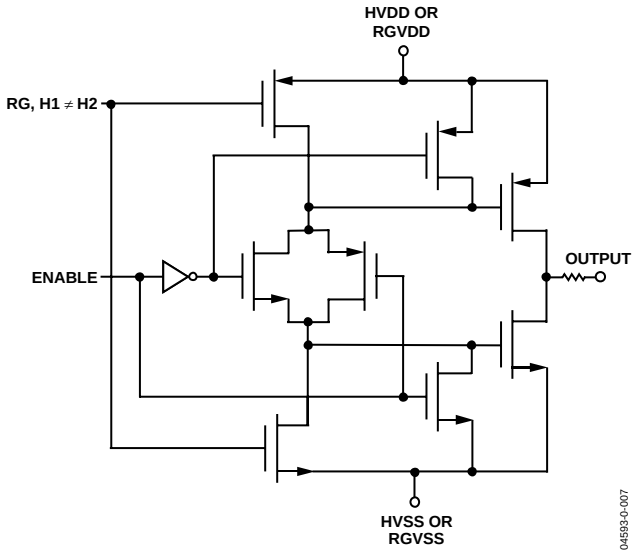


Figure 6. Circuit 4. H1 to H2, RG Drivers

Table 8. Control Register Address Map

Address	Content	Bit Width	Default Value	Register Name	Register Description
0x00	(23:0)	24	000000	SW_RESET	Software Reset = 000000 (Reset All Registers to Default)
0x01	23	1	0	Unused	
	(22:21)	2		XSUBCKSUPPRESS	Suppress XSUBCK (00 = No Suppression, 01 = Suppress First XSUBCK After Last VSG Line Pulse, 10 = Suppress All XSUBCKs, Except Final XSUBCK, 11 = No Suppression)
	(20:18)	3	0	Unused	Test Mode. Should Be Set = 0
	17	1	1	HBLKMASK	Masking Polarity for H1 During Blanking Period (0 = Low, 1 = High)
	16	1	0	SYNCPOL	External SYNC Active Polarity (0 = Active Low)
	(15:14)	2	0	Unused	
	13	1	0	XSUBCKMODE_HP	High Precision Shutter Mode Operation (0 = Single Pulse, 1 = Multiple Pulse)
	(12:10)	3	0	Unused	
	(9:8)	2	0	MSHUTPAT	Selects MSHUT Pattern. (See Figure 51) (0 = Mshutpat0,1 = Mshutpat1,2 = Mshutpat2, 3 = Mshutpat3)
	7	1	0	MSHUT/VGATE_EN	MSHUT Masking of VGATE Input (0 = MSHUT Does Not Mask VGATE, 1 = MSHUT Does Mask VGATE)
	6	1	0	Unused	
	5	1	1	CLPOB_CONT	CLPOB Control (0 = CLPOB Off, 1 = CLPOB On)
	4	1	1	CLPOB_MODE	CLPOB CCD Region Control (See Table 19)
	(3:1)	3	0	Unused	
	0	1	0	VDMODE	VD Synchronous/Asynchronous Mode Setting (0 = VD Synchronous, 1 = VD Asynchronous)
0x02	(23:22)	2	0	Unused	
	(21:16)	6	0x34	SHDLOC	SHD Sample Location
	(15:14)	2	0	Unused	
	(13:8)	6	0x18	SHPLOC	SHP Sample Location
	(7:6)	2	0	DCLKPHASE	DCLK Pulse Adjustment
	(5:0)	6	0x0B	DOUTPHASE	Data Output [11:0] Phase Adjustment
0x03	(23:17)	7	0x00	Unused	
	16	1	0	H1BLKRETIME	Retimes the H1 HBLK to Internal Clock
	(15:14)	2	0	Unused	
	(13:8)	6	0x00	H1POSLOC	H1 Positive Edge Location
	(7:6)	2	0	Unused	
	(5:0)	6	0x10	RGNEGLOC	RG Negative Edge Location
0x04	(23:16)	8	0x80	REFBLACK	Black Level Clamp
	15	1	–	Unused	
	(14:12)	3	5	H2DRV	H2 Drive Strength (0 = Off, 1 = 4.3 mA, 2 = 8.6 mA, 3 = 12.9 mA, 4 = 17.2 mA, 5 = 21.5 mA, 6 = 25.8 mA, 7 = 30.1 mA)
	11	1	0	Unused	
	(10:8)	3	5	H1DRV	H1 Drive Strength (0 = Off, 1 = 4.3 mA, 2 = 8.6 mA, 3 = 12.9 mA, 4 = 17.2 mA, 5 = 21.5 mA, 6 = 25.8 mA, 7 = 30.1 mA)
	(7:3)	5	0x00	Unused	
	(2:0)	3	2	RGDRV	RG Drive Strength (0 = Off, 1 = 2.15 mA, 2 = 4.2 mA, 3 = 6.45 mA, 4 = 8.6 mA, 5 = 10.75 mA, 6 = 12.9 mA, 7 = 15.05 mA)
0x05	(23:10)	14	0x0000	Unused	
	9	1	0	AFESTBY	AFE Standby (0 = Standby, 1 = Normal Operation)
	8	1	0	DIGSTBY	Digital Standby (0 = Standby, 1 = Normal Operation)
	(7:2)	6	00	Unused	
	1	1	0	OUTCONT_REG	Internal OUTCONT Signal Control (0 = Digital Outputs Held at Fixed DC Level, 1 = Normal Operation)
	0	1	1	OUTCONT_ENB	External OUTCONT Signal Input Pin 43 Control (0 = Pin Enabled, 1 = Pin Disabled)

Address	Content	Bit Width	Default Value	Register Name	Register Description
0x0A	23	1	0	Unused	
	22	1	0	FDPOL	FD Polarity Control (0 = Low, 1 = High)
	(21:16)	6	0x00	XVSGMASK	XVSG Masking (See Table 25)
(VD	(15:12)	4	0	SYNCCNT	External SYNC Setting
SyncReg)[1]	(11:10)	2	0	SVREP_MODE	Super Vertical Repetition Mode
	9	1	0	HBLKEXT	H Pulse Blanking Extend Control
	8	1	0	HPULSECNT	H Pulse Control During Blanking
	(7:4)	4	C	SPATLOGIC	SPAT Logic Setting (See Table 27)
	(3:2)	2	3	SVOS	Second V Output Setting (10 = Ouput Repetition 1)
	1	1	0	SPAT_EN	SPAT Control (0 = SPAT Disable, 1 = SPAT Enable)
	0	1	0	MODE	Mode Control Bit (0 = Mode_A, 1 = Mode_B)
0x0B	(23:22)	2	0	Unused	
	21	1	1	XSUBCK_EN	XSUBCK Output Enable Control (0 = Disable, 1 = Enable)
	20	1	1	XVSG_EN	XVSG Output Enable Control (0 = Disable, 1 = Enable)
(VD	(19:17)	3	0	Unused	
SyncReg)[1]	16	1	0	STROBE_EN	STROBE Output Control (0 = STROBE Output Held Low, 1 = STROBE Output Enabled)
	15	1	0	Unused	
	(14:12)	3	0	XSUBCKNUM_HP	High Precision Shutter XSUBCLK Pulse Position/Number
	11	1	0	Unused	
	(10:0)	11	0x7FF	XSUBCKNUM	Total Number of XSUBCKs Per Field
0x0C	(23:21)	3	0	Unused	
	20	1	0	MSHUTINIT	MSHUT Initialize (1 = Forces MSHUT Low)
	(19:18)	2	0	Unused	
(VD	17	1	0	Unused	
SyncReg)[1]	16	1	0	MSHUTEN	MSHUT Control (0 = MSHUT Held at Last State, 1 = MSHUT Output)
	15	1	0	Unused	
	(14:12)	3	0	MSHUTPOS_HP	MSHUT Position during High Precision Operation
	11	1	0	Unused	
	(10:0)	11	0x000	MSHUTPOS	MSHUT Position during Normal Operation
0x0D	(23:17)	7	–	Unused	
	16	1	0	VSUBPOL	VSUB Active Polarity (0 = Low, 1 = High)
(VD	(15:11)	5	–	Unused	
SyncReg)[1]	(10:0)	11	0x000	VSUBTOG	VSUB Toggle Position. Active Starting Line in any Field.
0x0E	(23:22)	2	0	Unused	
	(21:20)	2	0	TESTMODE1	This Register Should Always Be Set = 0.
	(19:18)	2	0	Unused	
(VD	17	1	0	TESTMODE2	This Register Should Always Be Set = 0.
SyncReg)[1]	16	1	0	TESTMODE3	This Register Should Always Be Set = 0.
	(15:10)	6	0x00	Unused	
	(9:0)	10	0x000	VGAGAIN	VGA Gain
0x0F	(23:8)	16	0	Unused	
	(7:0)	8	60	XVSGLEN_1	XVSGTOG_1 Pulse Width
0x17	(23:13)	11	–	Unused	
	(12:0)	13	0x1FFF	XV1SPAT_TOG1	XV1SPAT Toggle Position #1 (Mode_A Active)
0x18	(23:13)	11	–	Unused	
	(12:0)	13	0x1FFF	XV1SPAT_TOG2	XV1SPAT Toggle Position #2 (Mode_A Active)
0x19	(23:13)	11	–	Unused	
	(12:0)	13	0x1FFF	XV2SPAT_TOG1	XV2SPAT Toggle Position #1 (Mode_A Active)
0x1A	(23:13)	11	–	Unused	
	(12:0)	13	0x1FFF	XV2SPAT_TOG2	XV2SPAT Toggle Position #2 (Mode_A active)

Address	Content	Bit Width	Default Value	Register Name	Register Description
0x1B	(23:13)	11	–	Unused	
	(12:0)	13	0x1FFF	XV3SPAT_TOG1	XV3SPAT Toggle Position #1 (Mode_A active)
0x1C	(23:13))	11	–	Unused	
	(12:0	13	0x1FFF	XV3SPAT_TOG2	XV3SPAT Toggle Position #2 (Mode_A active)
0x1D	(23:13)	11	–	Unused	
	(12:0)	13	0x1FFF	XV4SPAT_TOG1	XV4SPAT Toggle Position #1 (Mode_A active)
0x1E	(23:13)	11	–	Unused	
	(12:0)	13	0x1FFF	XV4SPAT_TOG2	XV4SPAT Toggle Position #2 (Mode_A Active)
0x1F	(23:13)	11	–	Unused	
	(12:0)	13	0x1FFF	XV1SPAT_TOG1	XV1SPAT Toggle Position #1 (Mode_A Active)
0x20	(23:13)	11	–	Unused	
	(12:0)	13	0x1FFF	XV1SPAT_TOG2	XV1SPAT Toggle Position #2 (Mode_B Active)
0x21	(23:13)	11	–	Unused	
	(12:0)	13	0x1FFF	XV2SPAT_TOG1	XV2SPAT Toggle Position #1 (Mode_B Active)
0x22	(23:13)	11	–	Unused	
	(12:0)	13	0x1FFF	XV2SPAT_TOG2	XV2SPAT Toggle Position #2 (Mode_B Active)
0x23	(23:13)	11	–	Unused	
	(12:0)	13	0x1FFF	XV3SPAT_TOG1	XV3SPAT Toggle Position #1 (Mode_B Active)
0x24	(23:13)	11	–	Unused	
	(12:0)	13	0x1FFF	XV3SPAT_TOG2	XV3SPAT Toggle Position #2 (Mode_B Active)
0x25	(23:13)	11	–	Unused	
	(12:0)	13	0x1FFF	XV4SPAT_TOG1	XV4SPAT Toggle Position #1 (Mode_B Active)
0x26	(23:13)	11	–	Unused	
	(12:0)	13	0x1FFF	XV4SPAT_TOG2	XV4SPAT Toggle Position #2 (Mode_B Active)
0xD5	(23:4)	20	0x00000	Unused	
	3	1	1	DCLK2SEL	DCLK2 Selector (0 = Select Internal FD Signal To Be Output on FD/DCLK2 Pin 16, 1 = Select CLI To Be Output on FD/DCLK2 Pin 16)
	2	1	0	DCLK1SEL	DCLK1 Selector (0 = Select DLL Version for DCLK1 Output, 1 = Select CLI for DCLK1 Output)
	(1:0)	2	0	CLKDIV	Input Clock Divider (0 = No Division, 1 = 1/2, 2 = 1/3, 3 = 1/4)
0xD6	(23:1)	23	0x000000	Unused	
	0	1	1	SLAVE_MODE	Operating Mode (0 = Master Mode, 1 = Slave Mode)

[1] This register defaults to VD synchronous mode type at power-up. VD sync type registers do not get updated until the first falling edge of VD is asserted after the register has been programmed. VD sync type registers can be programmed to be asynchronous registers by setting VDMODE = 1 (Address 0x01).

Table 9. System Register Address Map (Address 0x14)

Register	Content	Bit Width	Default (Decimal)	Register Name	Register Description
Sys_Reg(0)	(31:24)	8	NA	System_Reg_addr	System Register Address is (Address 0x14)
	(23:0)	24	NA	System_Number_N	Number N Register Writes (0x000000 = Write All Registers)
Sys_Reg(1)	(31:23)	9	37	VTPLEN0	Vertical Sequence #0: Length Between Repetitions
	22	1	0	XV1STARTPOL0	Vertical Sequence #0: XV1 Start Polarity
	21	1	0	XV2STARTPOL0	Vertical Sequence #0: XV2 Start Polarity
	20	1	1	XV3STARTPOL0	Vertical Sequence #0: XV3 Start Polarity
	19	1	1	XV4STARTPOL0	Vertical Sequence #0: XV4 Start Polarity
	(18:10)	9	0	XV1TOG1POS0	Vertical Sequence #0: XV1 Toggle Position 1
	(9:1)	9	19	XV1TOG2POS0 Vertical Sequence	#0: XV1 Toggle Position 2
	0	1	0	XV2TOG1POS0 [8]	
Sys_Reg(2)	(31:24)	8	12	XV2TOG1POS0 [7:0]	Vertical Sequence #0: XV2 Toggle Position 1
	(23:15)	9	31	XV2TOG2POS0	Vertical Sequence #0: XV2 Toggle Position 2
	(14:6)	9	0	XV3TOG1POS0	Vertical Sequence #0: XV3 Toggle Position 1
	(5:0)	6		XV3TOG2POS0 [8:3]	
Sys_Reg(3)	(31:29)	3	19	XV3TOG2POS0 [2:0]	Vertical Sequence #0: XV3 Toggle Position 2
	(28:20)	9	12	XV4TOG1POS0	Vertical Sequence #0: XV4 Toggle Position 1
	(19:11)	9	31	XV4TOG2POS0	Vertical Sequence #0: XV4 Toggle Position 2
	(10:2)	9	104	VTPLEN1	Vertical Sequence #1: Length Between Repetitions
	1	1	0	XV1STARTPOL1	Vertical Sequence #1: XV1 Start Polarity
	0	1	0	XV2STARTPOL1	Vertical Sequence #1: XV2 Start Polarity
Sys_Reg(4)	31	1	1	XV3STARTPOL1	Vertical Sequence #1: XV3 Start Polarity
	30	1	1	XV4STARTPOL1	Vertical Sequence #1: XV4 Start Polarity
	(29:21)	9	18	XV1TOG1POS1	Vertical Sequence #1: XV1 Toggle Position 1
	(20:12)	9	58	XV1TOG2POS1	Vertical Sequence #1: XV1 Toggle Position 2
	(11:3)	9	47	XV2TOG1POS1	Vertical Sequence #1: XV2 Toggle Position 1
	(2:0)	3		XV2TOG2POS1 [8:6]	
Sys_Reg(5)	(31:26)	6	96	XV2TOG2POS1 [5:0]	Vertical Sequence #1: XV2Toggle Position 2
	(25:17)	9	0	XV3TOG1POS1	Vertical Sequence #1: XV3 Toggle Position 1
	(16:8)	9	76	XV3TOG2POS1	Vertical Sequence #1: XV3 Toggle Position 2
	(7:0)	8		XV4TOG1POS1 [8:1]	
Sys_Reg(6)	31	1	38	XV4TOG1POS1 [0]	Vertical Sequence #1: XV4 Toggle Position 1
	(30:22)	9	105	XV4TOG2POS1	Vertical Sequence #1: XV4 Toggle Position 2
	(21:13)	9	57	VTPLEN2	Vertical Sequence #2: Length between Repetitions
	12	1	0	XV1STARTPOL2	Vertical Sequence #2: XV1 Start Polarity
	11	1	0	XV2STARTPOL2	Vertical Sequence #2: XV2 Start Polarity
	10	1	1	XV3STARTPOL2	Vertical Sequence #2: XV3 Start Polarity
	9	1	1	XV4STARTPOL2	Vertical Sequence #2: XV4 Start Polarity
	(8:0)	9	0	XV1TOG1POS2	Vertical Sequence #2: XV1 Toggle Position 1
Sys_Reg(7)	(31:23)	9	29	XV1TOG2POS2	Vertical Sequence #2: XV1 Toggle Position 2
	(22:14)	9	19	XV2TOG1POS2	Vertical Sequence #2: XV2 Toggle Position 1
	(13:5)	9	48	XV2TOG2POS2	Vertical Sequence #2: XV2 Toggle Position 2
	(4:0)	5		XV3TOG1POS2 [8:4]	
Sys_Reg(8)	(31:28)	4	0	XV3TOG1POS2 [3:0]	Vertical Sequence #2: XV3 Toggle Position 1
	(27:19)	9	29	XV3TOG2POS2	Vertical Sequence #2: XV3 Toggle Position 2
	(18:10)	9	19	XV4TOG1POS2	Vertical Sequence #2: XV4 Toggle Position 1
	(9:1)	9	48	XV4TOG2POS2	Vertical Sequence #2: XV4 Toggle Position 2
	0	1	–	Unused	

Register	Content	Bit Width	Default (Decimal)	Register Name	Register Description
Sys_Reg(9)	(31:23)	9	89	VTPLEN3	Vertical Sequence #3: Length Between Repetitions
	22	1	0	XV1STARTPOL3	Vertical Sequence #3: XV1 Start Polarity
	21	1	0	XV2STARTPOL3	Vertical Sequence #3: XV2 Start Polarity
	20	1	1	XV3STARTPOL3	Vertical Sequence #3: XV3 Start Polarity
	19	1	1	XV4STARTPOL3	Vertical Sequence #3: XV4 Start Polarity
	(18:10)	9	0	XV1TOG1POS3	Vertical Sequence #3: XV1 Toggle Position 1
	(9:1)	9	60	XV1TOG2POS3	Vertical Sequence #3: XV1 Toggle Position 2
	0	1		XV2TOG1POS3 [8]	
Sys_Reg(10)	(31:24)	8	30	XV2TOG1POS3 [7:0]	Vertical Sequence #3: XV2 Toggle Position 1
	(23:15)	9	90	XV2TOG2POS3	Vertical Sequence #3: XV2 Toggle Position 2
	(14:6)	9	0	XV3TOG1POS3	Vertical Sequence #3: XV3 Toggle Position 1
	(5:0)	6		XV3TOG2POS3 [8:3]	
Sys_Reg(11)	(31:29)	3	60	XV3TOG2POS3 [2:0]	Vertical Sequence #3: XV3 Toggle Position 2
	(28:20)	9	30	XV4TOG1POS3	Vertical Sequence #3: XV4 Toggle Position 1
	(19:11)	9	90	XV4TOG2POS3	Vertical Sequence #3: XV4 Toggle Position 2
	(10:1)	10	0	HBLKHPOS	H1 Pulse ON Position during Blanking Period
	0	1	–	Unused	
Sys_Reg(12)	(31:20)	12	2283	HDLEN[1]	12-bit Gray Code HD Counter Value (Gray Code Number)
	(19:10)	10	130	HLEN	10-Bit HL Counter Values
	(9:1)	9	100	OLEN	9-Bit OL Counter Value
	0	1		BLLEN [8]	
Sys_Reg(13)	(31:24)	8	0	BLLEN [7:0]	9-bit BL Counter Value
	(23:16)	8	118	MSHUTLEN	MSHUT Sequence Length
	(15:5)	11	1048	XVSGTOG_0	XVSGTOG_0 Toggle Position
	(4:0)	5		XVSGTOG_1 [10:6]	
Sys_Reg(14)	(31:26)	6	1198	XVSGTOG_1 [5:0]	XVSG TOG_1 Toggle Position
	(25:18)	8	60	XVSGLEN_0	XVSGTOG_0 Pulse Width
	(17:9)	9	19	XSUBCK1TOG1	XSUBCK1 1st Toggle Position
	(8:0)	9	88	XSUBCK1TOG2	XSUBCK1 2nd Toggle Position
Sys_Reg(15)	(31:23)	9	19	XSUBCK2TOG1	XSUBCK2 1st Toggle Position
	(22:14:)	9	88	XSUBCK2TOG2	XSUBCK2 2nd Toggle Position
	(13:2)	12	2243	CLPTOG1[1]	CLPOB Toggle Position 1 (Gray Code Number)
	(1:0)	2		CLPTOG2 [11][1]	
Sys_Reg(16)	(31:22)	10	2278	CLPTOG2 [10:0] [1]	CLPOB Toggle Position 2 (Gray Code Number)
	(21:18)	4	9	VDRISE	VD Toggle Position 1
	(17:8)	10	120	HDRISE	HD Toggle Position 2
	(7:0)	8	–	Unused	

[1] Register value must be a gray code number (see Gray Code Registers section).

Table 10. Mode_A Register Map (Address 0x15)

Register	Content	Bit Width	Default (Decimal)	Register Name	Register Description
Mode_Reg(0)	(31:24)	8	NA	Mode_A_addr	Mode_A Address Is (Address 0x15)
	(23:0)	24	NA	Mode_A_Number_N	Number N Register Writes (0x000000 = Write All Registers)
Mode_Reg(1)	(31:21)	11	262	VDLEN	VD Counter Value
	(20:9)	12	1139	HDLASTLEN[1]	Number of Pixels in Last Line (Gray Code Number)
	8	1	1	XVSGSEL1	XVSG1 Sequence Selector (See Table 35)
	7	1	0	XVSGSEL2	XVSG2 Sequence Selector (See Table 35)
	(6:0)	7	0	XVSGACTLINE	XVSG Active Line
Mode_Reg(2)	31	1	0	SUBCKSEL	Select one of two SUBCK patterns
	(30:28)	3	0	VTPSEQPTR0	Vertical Transfer Sequence Region 0
	(27:25)	3	0	VTPSEQPTR1	Vertical Transfer Sequence Region 1
	(24:22)	3	0	VTPSEQPTR2	Vertical Transfer Sequence Region 2
	(21:19)	3	0	VTPSEQPTR3	Vertical Transfer Sequence Region 3
	(18:16)	3	0	VTPSEQPTR4	Vertical Transfer Sequence Region 4
	15	1	1	CLPEN0	CLPOB Output Control 1
	14	1	0	CLPEN1	CLPOB Output Control 2
	13	1	0	CLPEN2	CLPOB Output Control 3
	12	1	0	CLPEN3	CLPOB Output Control 4
	11	1	0	CLPEN4	CLPOB Output Control 5
	(10:3)	8	0	SCP1	Sequence Change Position 1
	(2:0)	3		SCP2	
Mode_Reg(3)	(31:27)	5	0	SCP2	Sequence Change Position 2
	(26:19)	8	0	SCP3	Sequence Change Position 3
	(18:11)	8	0	SCP4	Sequence Change Position 4
	(10:9)	2	0	VTPSEL0	Vertical Pattern Selection 0
	(8:7)	2	0	VTPSEL1	Vertical Pattern Selection 1
	(6:5)	2	0	VTPSEL2	Vertical Pattern Selection 2
	(4:3)	2	0	VTPSEL3	Vertical Pattern Selection 3
	(2:0)	3	3	VTPREP0	Number of Vertical Pulse Repetitions for Pattern 0
Mode_Reg(4)	(31:29)	3	0	VTPREP1	Number of Vertical Pulse Repetitions for Pattern 1
	(28:26)	3	0	VTPREP2	Number of Vertical Pulse Repetitions for Pattern 2
	(25:23)	3	0	VTPREP3	Number of Vertical Pulse Repetitions for Pattern 3
	(22:12)	11	0	SVREP0	Vertical Sweep Repetition Number for CCD Region 0
	(11:1)	11	0	SVREP3	Vertical Sweep Repetition Number for CCD Region 3
	0	1	–	Unused	
Mode_Reg(5)	(31:19)	13	988	XV1SPAT_TOG3	XV1SPAT Toggle Position 3
	(18:6)	13	1138	XV1SPAT_TOG4	XV1SPAT Toggle Position 4
	(5:0)	6		XV2SPAT_TOG3	
Mode_Reg(6)	(31:25)	7	1078	XV2SPAT_TOG3	XV2SPAT Toggle Position 3
	(24:12)	13	1168	XV2SPAT_TOG	XV2SPAT Toggle Position 4
	(11:0)	12		XV3SPAT_TOG3	
Mode_Reg(7)	31	1	958	XV3SPAT_TOG3	XV3SPAT Toggle Position 3
	(30:18)	13	1138	XV3SPAT_TOG4	XV3SPAT Toggle Position 4
	(17:5)	13	988	XV4SPAT_TOG3	XV4SPAT Toggle Position 3
	(4:0)	5		XV4SPAT_TOG4	
Mode_Reg(8)	(31:24)	8	1228	XV4SPAT_TOG4	XV4SPAT Toggle Position 4
	(23:11)	13	1392	SECONDVPOS	Second V Pattern Output Position
	(10:9)	2	3	VPATSECOND	Selected Second V-Pattern Group for VSG Active Line
	(8:0)	9	–	Unused	

[1] Register value must be a gray code number (see Gray Code Registers section).

Table 11. Mode_B Register Map (Address 0x16)

Register	Content	Bit Width	Default (Decimal)	Register Name	Register Description
Mode_Reg(0)	(31:24)	8	NA	Mode_B_addr	Mode_B Address is (Address 0x16)
	(23:0)	24	NA	Mode_B_Number_N	Number N Register Writes (0x000000 = Write All Registers)
Mode_Reg(1)	(31:21)	11	262	VDLEN	VD Counter Value
	(20:9)	12	1139	HDLASTLEN[1]	Number of Pixels in Last Line (Gray Code Number)
	8	1	1	XVSGSEL1	XVSG1 Sequence Selector (See Table 35)
	7	1	0	XVSGSEL2	XVSG2 Sequence Selector (See Table 35)
	(6:0)	7	0	XVSGACTLINE	XVSG Active Line
Mode_Reg(2)	31	1	0	SUBCKSEL	Select One of Two SUBCK Patterns
	(30:28)	3	0	VTPSEQPTR0	Vertical Transfer Sequence Region 0
	(27:25)	3	0	VTPSEQPTR1	Vertical Transfer Sequence Region 1
	(24:22)	3	0	VTPSEQPTR2	Vertical Transfer Sequence Region 2
	(21:19)	3	0	VTPSEQPTR3	Vertical Transfer Sequence Region 3
	(18:16)	3	0	VTPSEQPTR4	Vertical Transfer Sequence Region 4
	15	1	1	CLPEN0	CLPOB Output Control 1
	14	1	0	CLPEN1	CLPOB Output Control 2
	13	1	0	CLPEN2	CLPOB Output Control 3
	12	1	0	CLPEN3	CLPOB Output Control 4
	11	1	0	CLPEN4	CLPOB Output Control 5
	(10:3)	8	0	SCP1	Sequence Change Position 1
	(2:0)	3		SCP2	
Mode_Reg(3)	(31:27)	5	0	SCP2	Sequence Change Position 2
	(26:19)	8	0	SCP3	Sequence Change Position 3
	(18:11)	8	0	SCP4	Sequence Change Position 4
	(10:9)	2	0	VTPSEL0	Vertical Pattern Selection 0
	(8:7)	2	0	VTPSEL1	Vertical Pattern Selection 1
	(6:5)	2	0	VTPSEL2	Vertical Pattern Selection 2
	(4:3)	2	0	VTPSEL3	Vertical Pattern Selection 3
	(2:0)	3	3	VTPREP0	Number of VTP0 Pulse Repetitions for Pattern 0
Mode_Reg(4)	(31:29)	3	0	VTPREP1	Number of VTP1 Pulse Repetitions for Pattern 1
	(28:26)	3	0	VTPREP2	Number of VTP2 Pulse Repetitions for Pattern 2
	(25:23)	3	0	VTPREP3	Number of VTP0 Pulse Repetitions for Pattern 3
	(22:12)	11	0	SVREP0	Vertical Sweep Repetition Number for CCD Region 0
	(11:1)	11	0	SVREP3	Vertical Sweep Repetition Number for CCD Region 3
	0	1	–	Unused	
Mode_Reg(5)	(31:19)	13	988	XV1SPAT_TOG3	XV1SPAT Toggle Position 3
	(18:6)	13	1138	XV1SPAT_TOG4	XV1SPAT Toggle Position 4
	(5:0)	6		XV2SPAT_TOG3	
Mode_Reg(6)	(31:25)	7	1078	XV2SPAT_TOG3	XV2SPAT Toggle Position 3
	(24:12)	13		XV2SPAT_TOG4	XV2SPAT Toggle Position 4
	(11:0)	12		XV3SPAT_TOG3	
Mode_Reg(7)	31	1	958	XV3SPAT_TOG3	XV3SPAT Toggle Position 3
	(30:18)	13	1138	XV3SPAT_TOG4	XV3SPAT Toggle Position 4
	(17:5)	13	988	XV4SPAT_TOG3	XV4SPAT Toggle Position 3
	(4:0)	5		XV4SPAT_TOG4	
Mode_Reg(8)	(31:24)	8	1228	XV4SPAT_TOG4	XV4SPAT Toggle Position 4
	(23:11)	13	1392	SECONDVPOS	Second V Pattern Output Position
	(10:9)	2	3	VPATSECOND	Selected Second V-Pattern Group for VSG Active Line
	(8:0)	9	–	Unused	

[1] Register value must be a gray code number (See Gray Code Registers section).

SYSTEM OVERVIEW

Figure 7 shows the typical system block diagram for the AD9929. The CCD output is processed by the AD9929's AFE circuitry, which consists of a CDS, VGA, black level clamp, and an A/D converter. The digitized pixel information is sent to the digital image processor chip, which performs post-processing and compression. To operate the CCD, all CCD timing parameters are programmed into the AD9929 from the system microprocessor through the 3-wire serial interface. From the system master clock, CLI, provided by the image processor or external crystal, the AD9929 generates all of the CCDs horizontal and vertical clocks and all internal AFE clocks. External synchronization is provided by a SYNC pulse from the microprocessor, which resets internal counters and resynchronizes the VD and HD outputs.

The H-drivers for H1 to H2, and RG are included in the AD9929, allowing these clocks to be directly connected to the CCD. An H-drive voltage of up to 3.6 V is supported. The AD9929 also includes the CCD vertical driver circuits for creating the V1 to V4, and SUBCK outputs that allow direct connection to the CCD. The AD9929 also provides programmable MSHUT and STROBE outputs, which may be used to trigger mechanical shutter and strobe (flash) circuitry.

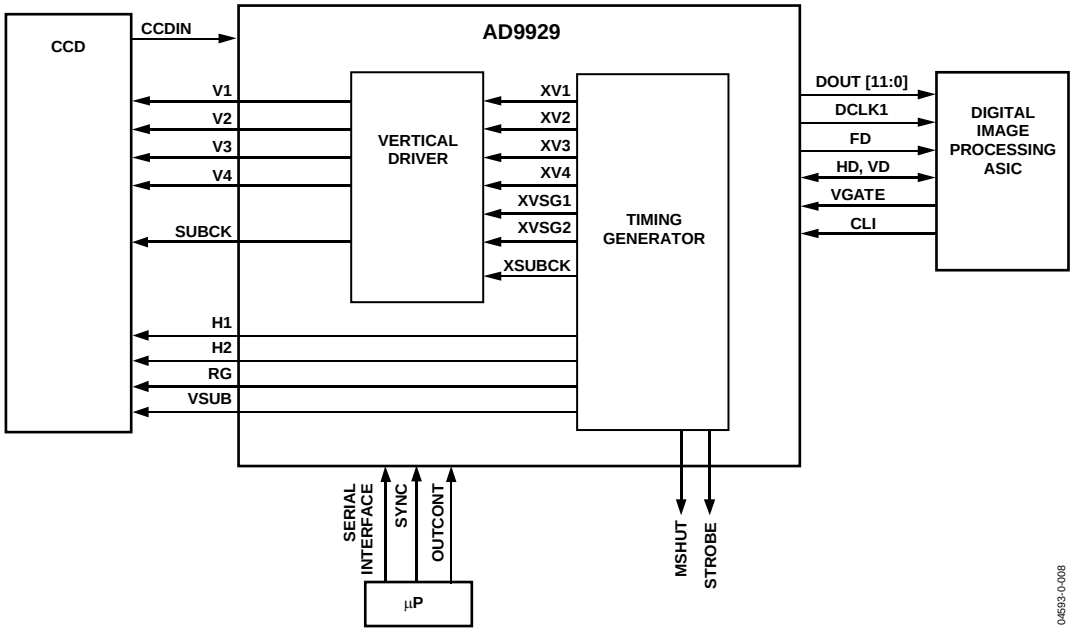


Figure 7. Typical System Block Diagram, Master Mode

THEORY OF OPERATION

MODES OF OPERATION

Slave and Master Mode Operation

The AD9929 can be operated in either slave or master mode. It defaults to slave mode operation at power-up. The SLAVE_MODE register (Address 0xD6) can be used to configure the AD9929 into master mode by setting SLAVE_MODE = 0.

Slave Mode Operation

While operating in slave mode, VD, HD, and VGATE are provided externally from the image processor. VGATE is input active high on Pin 45.

Unlike master mode operation, there is a 7 CLI clock cycle delay from the falling edge of HD to when the 12-bit gray code H counter is reset to 0 (See Figure 62).

Master Mode Operation

While operating in master mode, VD and HD are outputs and the SYNC/VGATE pin is configured for an external SYNC input. Master mode is selected by setting register SLAVE_MODE (Address 0x06) = 0.

HORIZONTAL AND VERTICAL COUNTERS

Figure 8 and Figure 9 show the horizontal and vertical counter dimensions for the AD9929. All internal horizontal and vertical clocking is programmed using these dimensions to specify line and pixel locations.

CLI INPUT CLOCK DIVIDER

The AD9929 provides the capability of dividing the CLI input clock using Register CLKDIV (Address 0xD5). The following procedure must be followed to reset the AFE and digital circuits when CLKDIV is reprogrammed back to 0 from CLKDIV = 1, 2, or 3. The DCLK1 output becomes unstable if this procedure isn't followed.

Step 1: CLKDIV = 1, 2, or 3 (CLI divided by setting value)
Step 2: CLKDIV = 0 (CLI reprogrammed for no division)
Step 3: DIGSTBY = AFESTBY = 0
Step 4: DIGSTBY = AFESTBY = 1

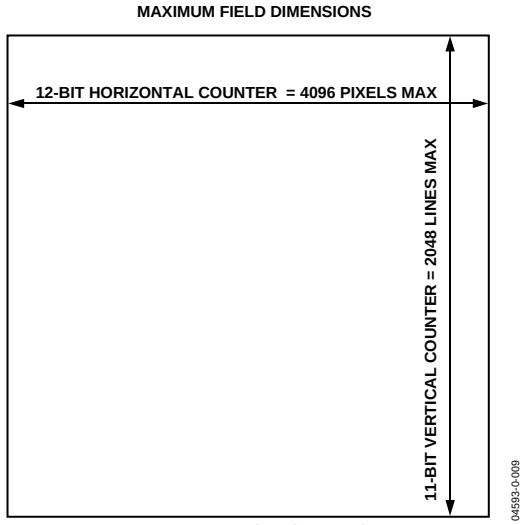


Figure 8. Horizontal and Vertical Counters

GRAY CODE REGISTERS

See Table 12 for a list of the AD9929 registers requiring gray code values. The following is an example of applying a gray code number for HDLEN using a line length of 1560 pixels:

HDLEN = (1560–4) = 1556_{10} (see Special Note about the HDLEN Register section).

Where 1556_{10} = Address 0x51E

The gray code value of Address 0x51E would be programmed in the 12-bit HDLEN register.

Table 12. AD9929 Gray Code Registers

Register Name	Register Type
HDLEN	System_Reg(12)
CLPOBTOG1	System_Reg(15)
CLPOBTOG2	System_Reg(16)
HDLASTLEN	Mode_Reg(1)

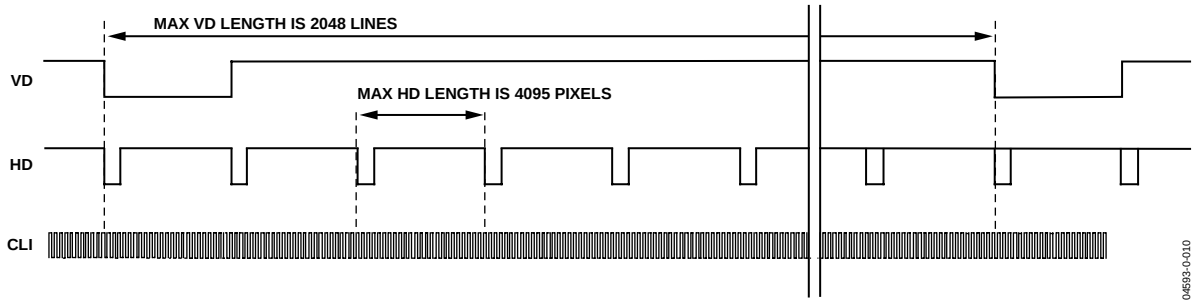


Figure 9. Maximum VD/HD Dimensions

SERIAL INTERFACE TIMING

All of the internal registers of the AD9929 are accessed through a 3-wire serial interface. The 3-wire interface consists of a clock (SCK), serial load (SL), and serial data (SDATA).

The AD9929 has three different register types that are configured by the 3-wire serial interface. As described in Table 13, the three register types are control registers, system registers, and mode registers.

Table 13. Types of Serial Interface Registers

Register	Address	Number of Registers
Control	0x00 to 0xD6	24-Bit Registers at Each Address. Not All Addresses Are Used. See Table 8.
System	0x14	Seventeen 32-Bit System Registers at Address 0x14. See Table 9.
Mode_A	0x15	Eight 32-bit Mode_A Registers at Address 0x15. See Table 10.
Mode_B	0x16	Eight 32-Bit Mode_B Registers at Address 0x16. See Table 11.

Registers

Control Register Serial Interface

The control register 3-wire interface timing requirements are shown in Figure 10. Control data must be written into the device one address at a time due to the noncontiguous address spacing for the control registers. This requires writing 8 bits of address data followed by 24 bits of configuration data between each active low period of SL for each address. The SL signal must be kept high for at least one full SCK cycle between successive writes to control registers.

System Register Serial Interface

There are seventeen 32-bit system registers that are accessed sequentially at Address 0x14, beginning with Sys_Reg [0]. When writing to the system registers, SDATA contains the 8-bit Address 0x14, followed by Number Writes N [23:0], followed by the Sys_Reg [31:0] data, as shown in Figure 5. The system register map is listed in Table 9.

The value of the Number Writes N [23:0] word determines one of two options when writing to the system registers. If Number Writes N[23:0] = 0x000000, the device enters a mode where it expects all 17 Sys_Reg [31:0] data-words to be clocked in before SL is asserted high. If the Number Writes N [23:0] is decoded as some number N other than 0x000000, then the device expects N number of registers to be programmed, where N equals the value of Number Writes N [23:0]. For example: if Number Writes N[23:0] = 0x000004, the device would expect data to be provided for Sys_Reg [3:0]. In all cases, the system registers are written beginning with Sys_Reg [0], regardless of the value of Number Writes N [23:0]. Note that SL can be brought high or low during access to system registers, as shown in Figure 11.

Mode_A and Mode_B Register Serial Interface

There are eight 32-bit Mode_A and eight 32-bit Mode_B registers that get accessed sequentially at Address 0x15 and Address 0x16, respectively. Mode_A and Mode_B registers are written to in exactly the same way as the system registers, as explained previously. The mode registers are listed in Table 10 and Table 11.

To change operation between Mode_A and Mode_B, set the 1-bit mode register (Address 0x0A). The desired Mode_A (Address 0x15) or Mode_B (Address 0x16) data must be programmed into the Mode_A or Mode_B registers before changing the mode bit.

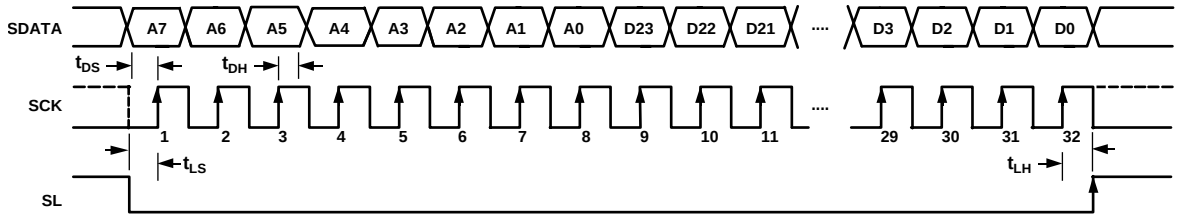


Figure 10. 3-Wire Serial Interface Timing for Control Registers

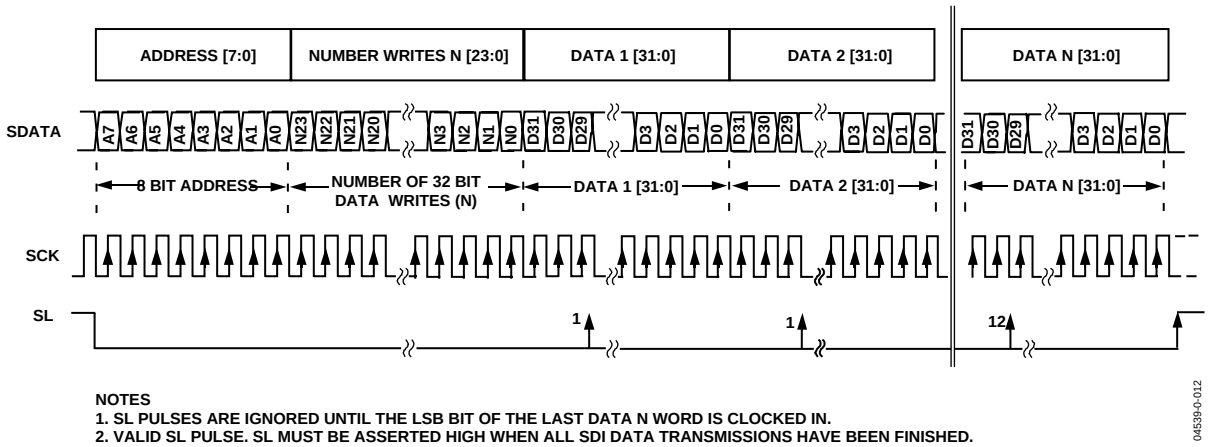


Figure 11. System and Mode Register Writes

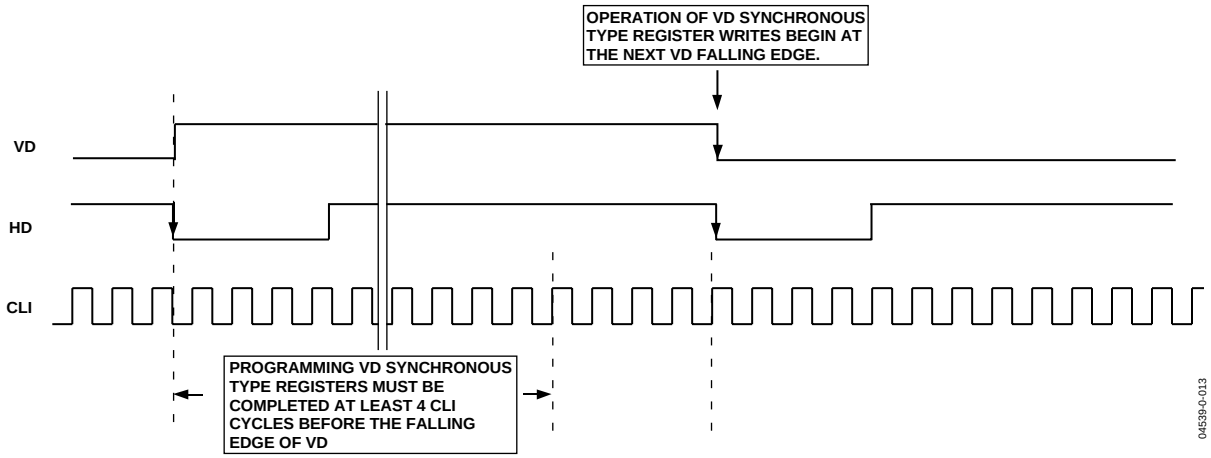


Figure 12. VD Synchronous Type Register Writes

VD Synchronous and Asynchronous Register Operation

There are two types of control registers, VD synchronous and VD asynchronous, as indicated in the address column of Table 8. Register writes to synchronous and asynchronous registers operate differently, as described in the following sections. All writes to system Mode_A and Mode_B registers occur asynchronously.

Asynchronous Register Operation

For VD asynchronous register writes, SDATA data is stored directly into the serial register at the rising edge of SL. As a result, register operation begins immediately after the rising edge of SL.

VD Synchronous Register Operation

For VD synchronous registers, SDATA data is temporarily stored in a buffer register at the rising edge of SL. This data is held in the buffer register until the next falling edge of VD is applied. Once the next falling edge of VD occurs, the buffered SDATA data is loaded into the serial register, at which time the register operation begins. See Figure 12.

All control registers at the following addresses are VD synchronous type registers: Addresses 0x0A, 0x0B, 0x0C, 0x0D, and 0x0E. Also see Table 8, the Control Register Address Map.

ANALOG FRONT END DESCRIPTION AND OPERATION

The AD9929 AFE signal processing chain is shown in Figure 13. Each processing step is essential in achieving a high quality image from the raw CCD pixel data. Registers for the AD9929 AFE section are listed in Table 14.

Table 14. AFE Registers

Register Name	Bit Width	Register Type	Description
VGAGAIN	10	Control (Address 0x0E)	VGA Gain
REFBLACK	6	Control (Address 0x04)	Black Clamp Level
AFESTBY	1	Control (Address 0x05)	AFE Standby

DC Restore

To reduce the large dc offset of the CCD output signal, a dc-restore circuit is used with an external 0.1 µF series coupling capacitor. This restores the dc level of the CCD signal to approximately 1.5 V, to be compatible with the 3 V analog supply of the AD9929.

Correlated Double Sampler

The CDS circuit samples each CCD pixel twice to extract the video information and reject low frequency noise. The timing shown in Figure 16 illustrates how the two internally generated CDS clocks, SHP and SHD, are used to sample the reference and data levels, respectively, of the CCD signal. The placement of the SHP and SHD sampling edges is determined by the setting of the SHPLOC (Address 0x02) and SHDLOC (Address 0x02) registers. Placement of these two clock edges is critical in achieving the best performance from the CCD.

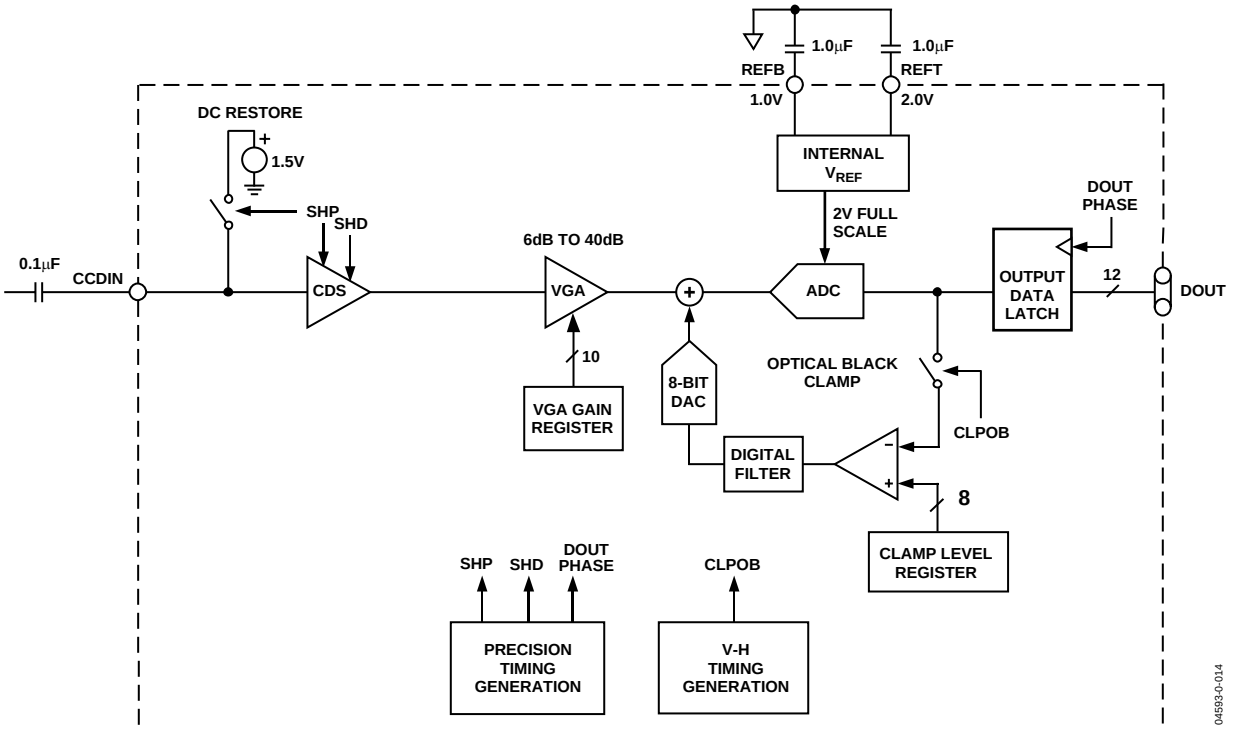


Figure 13. AFE Block Diagram

Variable Gain Amplifier

The VGA provides a gain range of 6 dB to 40 dB, programmable with 10-bit resolution through the serial digital interface. The minimum gain of 6 dB is needed to match a 1 V input signal with the ADC full-scale range of 2 V.

The VGA gain curve follows a "linear-in-dB" characteristic. The exact VGA gain can be calculated for any gain register value by using the equation

$$Gain = (0.035 \times Code) + 5.2$$

where the code range is 0 to 1023. Figure 14 shows a typical AD9929 VGA gain curve.

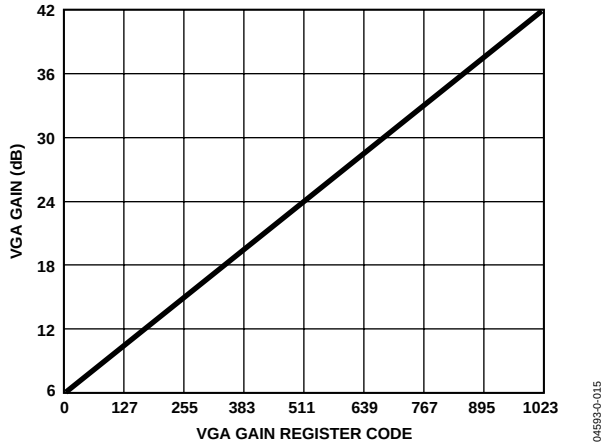


Figure 14. VGA Gain Curve

Optical Black Clamp

The optical black clamp loop is used to remove residual offsets in the signal chain and to track low frequency variations in the CCD's black level. During the optical black (shielded) pixel interval on each line, the ADC output is compared with a fixed black level reference selected by the user in the clamp level register. Any value between 0 LSB and 255 LSB may be programmed with 8-bit resolution. The resulting error signal is filtered to reduce noise, and the correction value is applied to the ADC input through a D/A converter. Normally, the optical black clamp loop is turned on once per horizontal line, but this loop can be updated more slowly to suit a particular application.

The optical black clamp is controlled by the CLPOB signal, which is fully programmable (see Horizontal Clamping and Blanking section). System timing examples are shown in the Horizontal and Vertical Synchronous Timing section. The CLPOB pulse should be placed during the CCDs optical black pixels. It is recommended that the CLPOB pulse duration be at least 20 pixels wide. Shorter pulse widths may be used, but the ability to track low frequency variations in the black level is reduced.

A/D Converter

The AD9929 uses high-performance 12-bit ADC architecture, optimized for high speed and low power. Differential Nonlinearity (DNL) performance is typically better than 0.5 LSB. The ADC uses a 2 V input range. Better noise performance results from using a larger ADC full-scale range.

PRECISION TIMING, HIGH SPEED TIMING GENERATION

The AD9929 generates flexible, high speed timing signals using the precision timing core. This core is the foundation for generating the timing used for both the CCD and the AFE: the reset gate RG, horizontal drivers H1 to H2, and the CDS sample clocks. A unique architecture makes it routine for the system designer to optimize image quality by providing precise control over the horizontal CCD readout and the AFE correlated double sampling.

Timing Resolution

The precision timing core uses the master clock input (CLI) as a reference. This clock should be the same as the CCD pixel clock frequency. Figure 15 illustrates how the internal timing core divides the master clock period into 48 steps or edge positions. Using a 36 MHz CLI frequency, the edge resolution of the precision timing core is 0.58 ns. A 72 MHz CLI frequency can be applied to the AD9929, where the AD9929 will internally divide the CLI frequency by two. Division by 1/3 and 1/4 are also provided. CLI frequency division is controlled by using CLKDIV (Address 0x05) register.

High Speed Clock Programmability

Figure 17 shows how the high speed clocks RG, H1 to H2, SHP, and SHD are generated. The RG pulse has a fixed rising edge and a programmable falling edge. The horizontal clock H1 has a programmable rising and a fixed falling edge occurring at H1POSLOC + 24 steps. The H2 clock is always the inverse of H1. Table 14 summarizes the high speed timing registers and the parameters for the high speed clocks. Each register is 6 bits wide with the 2 MSB bits used to select the quadrant region, as outlined in Table 16. Figure 17 shows the range and default locations of the high speed clock signals.

H DRIVER AND RG OUTPUTS

In addition to the programmable timing positions, the AD9929 features on-chip output drivers for the RG and H1 to H2 outputs. These drivers are powerful enough to directly drive the CCD inputs. The H-driver current can be adjusted for optimum rise/fall time into a particular load by using the H1DRV and H2DRV registers (Address 0x04). The RG drive current is adjustable using the RGDRV register (Address 0x04). The H1DRV and H2DRV register is adjustable in 4.3 mA increments. The RGDRV register is adjustable in 2.15 mA increments. All DRV registers have settings of 0 equal to OFF or three-state, and a maximum setting of 7.

As shown in Figure 17, the H2 output is the inverse of H1. The internal propagation delay resulting from the signal inversion is less than 1 ns, which is significantly less than the typical rise time driving the CCD load. This results in a H1/H2 crossover voltage at approximately 50% of the output swing. The crossover voltage is not programmable.

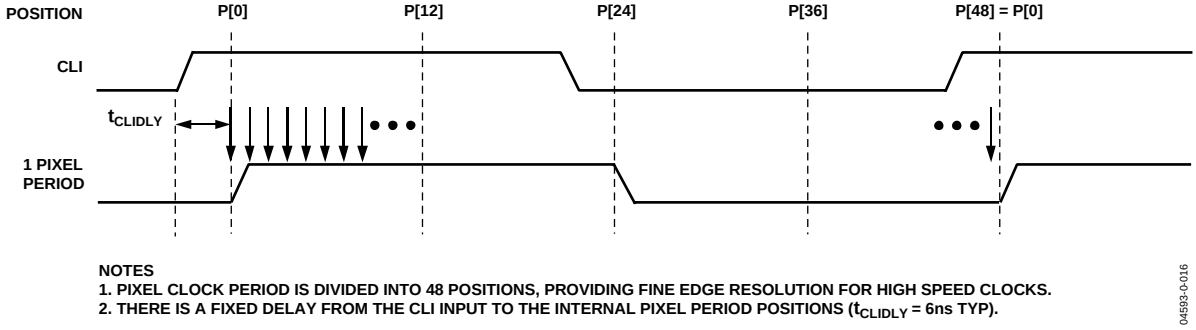


Figure 15. High Speed Clock Resolution from CLI Master Clock Input

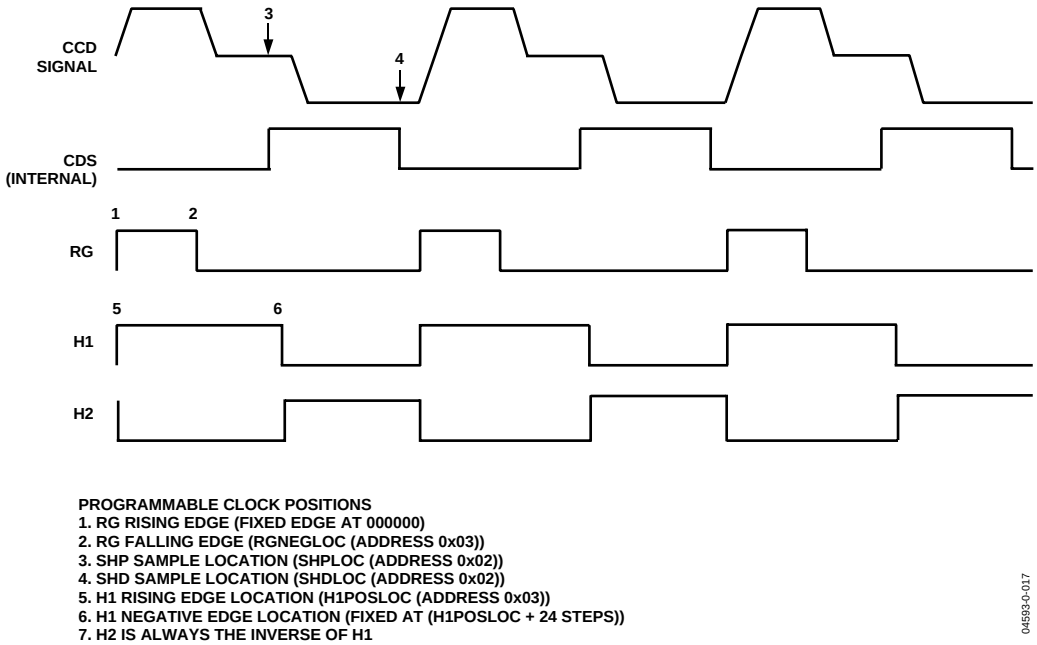


Figure 16. High Speed Clock Programmable Locations

Table 15. RG, H1, SHP, SHD, DCLK, and DOUTPHASE Timing Parameters

Register Name	Bit Width	Register Type	Range	Description
RGNEGLOC[1]	6b	Control (Address 0x03)	0 to 47 Edge Location	Falling Edge Location for RG
H1POSLOC[1]	6b	Control (Address 0x03)	0 to 47 Edge Location	Positive Edge Location for H1
SHPLOC[1]	6b	Control (Address 0x02)	0 to 47 Edge Location	Sample Location for SHP
SHDLOC[1]	6b	Control (Address 0x02)	0 to 47 Edge Location	Sample Location for SHD
DOUTPHASE[1]	6b	Control (Address 0x02)	0 to 47 Edge Location	Phase Location of Data Output [9:0]
DCLKPHASE	6b	Control (Address 0x02)	0 to 47 Edge Location	Positive Edge of DCLK 1

[1] The two MSB bits are used to select the quadrant

Table 16. Precision Timing Edge Locations for RG, H1, SHP, SHD, DCLK, and DOUTPHASE

Signal Name	Quadrant	RG Rising Edge *(Not Programmable)*	RG Falling Edge	
			RGNEGLOC	Quadrant Range
RG	I	fixed at **00**0000	**00**0000 to **00**1011	*P[0] to P[11]*
	II	fixed at **00**0000	**01**0000 to **01**1011	*P[12] to P[23]*
	III	fixed at **00**0000	**10**0000 to **10**1011	*P[24] to P[35]*
	IV	fixed at **00**0000		*P[36] to P[47]*

Signal Name	Quadrant	H1 Rising Edge		H1 Falling Edge *(Not Programmable)*
		H1POSLOC	Quadrant Range	
H1	I	**00**0000 to **00**1011	*P[0] to P[11]*	H1POSLOC + 24 Steps
	II	**01**0000 to **01**1011	*P[12] to P[23]*	H1POSLOC + 24 Steps
	III	**10**0000 to **10**1011	*P[24] to P[35]*	H1POSLOC + 24 Steps
	IV	**11**0000 to **11**1011	*P[36] to P[47]*	H1POSLOC + 24 Steps

Signal Name	Quadrant	CDS Rising Edge		CDS Falling Edge	
		SHPLOC	Quadrant Range	SHDLOC	Quadrant Range
CDS	I	**00**0000 to **00**1011	*P[0] to P[11]*	**00**0000 to **00**1011	*P[0] to P[11]*
	II	**01**0000 to **01**1011	*P[12] to P[23]*	**01**0000 to **01**1011	*P[12] to P[23]*
	III	**10**0000 to **10**1011	*P[24] to P[35]*	**10**0000 to **10**1011	*P[24] to P[35]*
	IV	**11**0000 to **11**1011	*P[36] to P[47]*	**11**0000 to **11**1011	*P[36] to P[47]*

Signal Name	Quadrant	Data Output[9:0] Rising Edge		Data Output[9:0] Falling Edge
		DOUTPHASE	Quadrant Range	*(Not Programmable)*
Data Output [9:0]	I	**00**0000 to **00**1011	*P[0] to P[11]*	DOUTPHASE + 24 Steps
	II	**01**0000 to **01**1011	*P[12] to P[23]*	DOUTPHASE + 24 Steps
	III	**10**0000 to **10**1011	*P[24] to P[35]*	DOUTPHASE + 24 Steps
	IV	**11**0000 to **11**1011	*P[36] to P[47]*	DOUTPHASE + 24 Steps

Signal Name	DCLKPHASE Value	DCLK PHASE Rising Edge	DCLKPHASE Falling Edge
DCLK1	00	P[6]	P[26]
	01	P[16]	P[36]
	10	P[26]	P[06]
	11	P[36]	P[16]

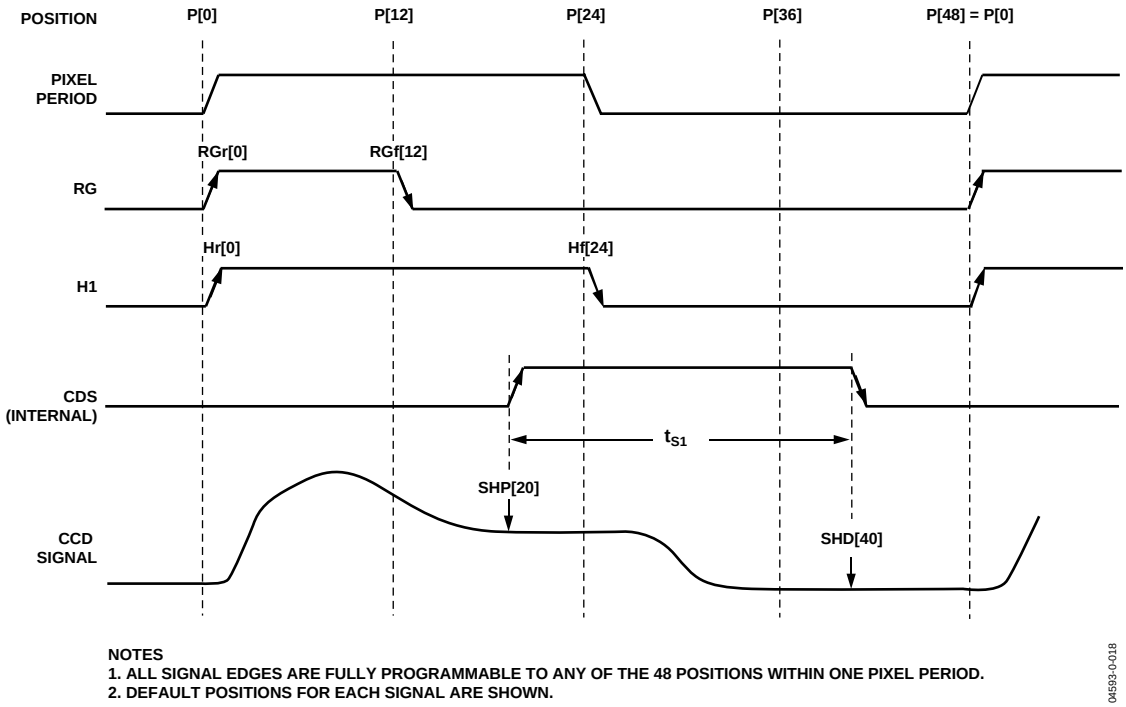


Figure 17. High Speed Clock Default and Programmable Locations

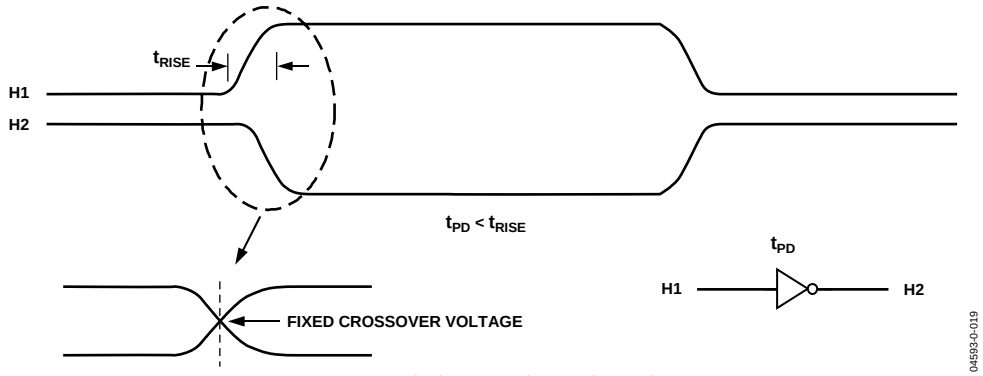


Figure 18. H-Clock Inverse Phase Relationship

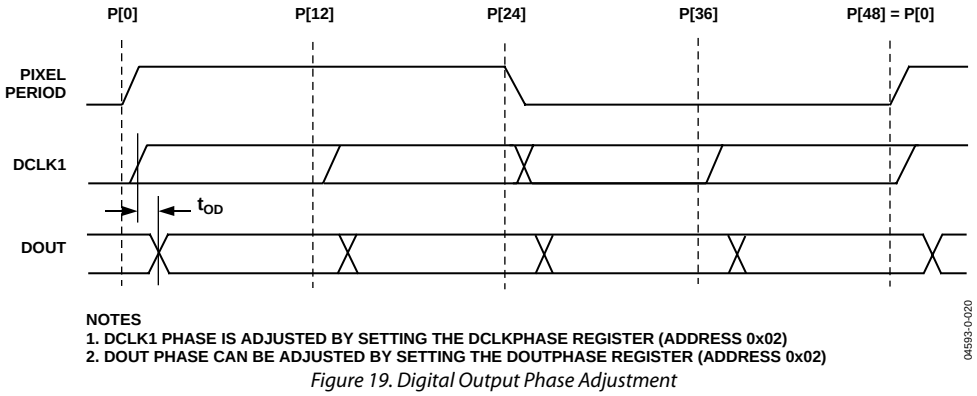


Figure 19. Digital Output Phase Adjustment

DIGITAL DATA OUTPUTS

The AD9929 DOUT[11:0] and DCLK phases are independently programmable using the DOUTPHASE register (Address 0x02) and DCLKPHASE register (Address 0x02). Refer to Figure 19.

EXTERNAL SYNCHRONIZATION (MASTER MODE)

External synchronization can be applied to synchronize the VD and HD signals by applying an external pulse on the SYNC/GATE (Pin 45) pin for master mode operation. The SYNC/GATE pin is configured as an external SYNC input for master mode operation by setting the SLAVE_MODE register (Address 0xD6) = 0 (the AD9929 defaults to slave mode at power-up).

SYNCCNT (Address 0x0A) and SYNCPOL (Address 0x01) are the only two registers used for configuring the AD9929 for external synchronization. The SYNCPOL is a 1-bit register used for configuring the SYNC input as either active low or active high. The AD9929 defaults to active low at power-up. The function of the SYNCCNT register is described in Table 17. Figure 20 and Figure 21 provide two examples of external synchronization with SYNCPOL = 0.

Table 17. External Synchronization (Master Mode)

SYNCCNT	External Synchronization Options
0	Disable External Synchronization
1	VD Sync at every SYNC Pulse
2	VD Sync after 2nd Applied SYNC Pulse
3	VD Sync after 3rd Applied SYNC Pulse
4	VD Sync after 4th Applied SYNC Pulse
5	VD Sync after 5th Applied SYNC Pulse
6	VD Sync after 6th Applied SYNC Pulse
7	VD Sync after 7th Applied SYNC Pulse
8	VD Sync after 8th Applied SYNC Pulse
9	VD Sync after 9th Applied SYNC Pulse
10	VD Sync after 10th Applied SYNC Pulse
11	VD Sync after 11th Applied SYNC Pulse
12	VD Sync after 12th Applied SYNC Pulse
13	VD Sync after 13th Applied SYNC Pulse
14	VD Sync after 14th Applied SYNC Pulse
15	VD Sync after 1st Applied SYNC Pulse Only

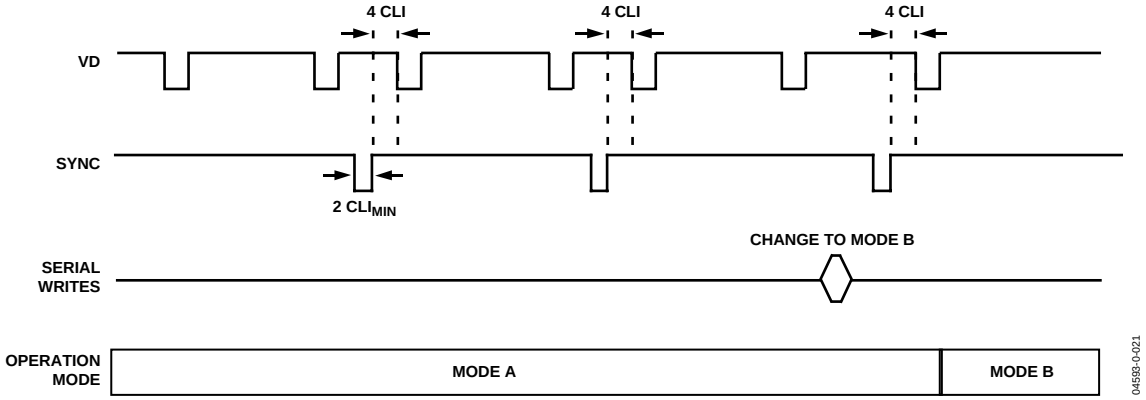


Figure 20. Example of Synchronization with SYNCPOL = 0 and SYNCCNT = 1

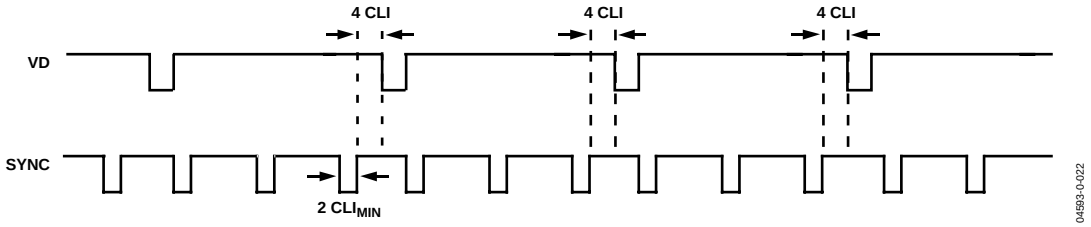


Figure 21. Example of Synchronization with SYNCPOL = 0 and CYNCCNT = 3

HORIZONTAL AND VERTICAL SYNCHRONOUS TIMING

The HD and VD output pulses are programmable using the registers listed in Table 18. The HD output is asserted low at the start of the horizontal line shift. The VD output is asserted low at the start of each line. As shown in Figure 22, the 11-bit VD counter is used to count the number of lines set by the VDLEN register. The 12-bit HD counter is used to count the number of pixels in each line set by the HDLEN register. For example, if the CCD array size is 2000 lines by 2100 pixels per line, VDLEN = 2000 and HDLEN = 0xC28. The HDLEN register sets HL as a reference for the rising edge of the HD pulse.

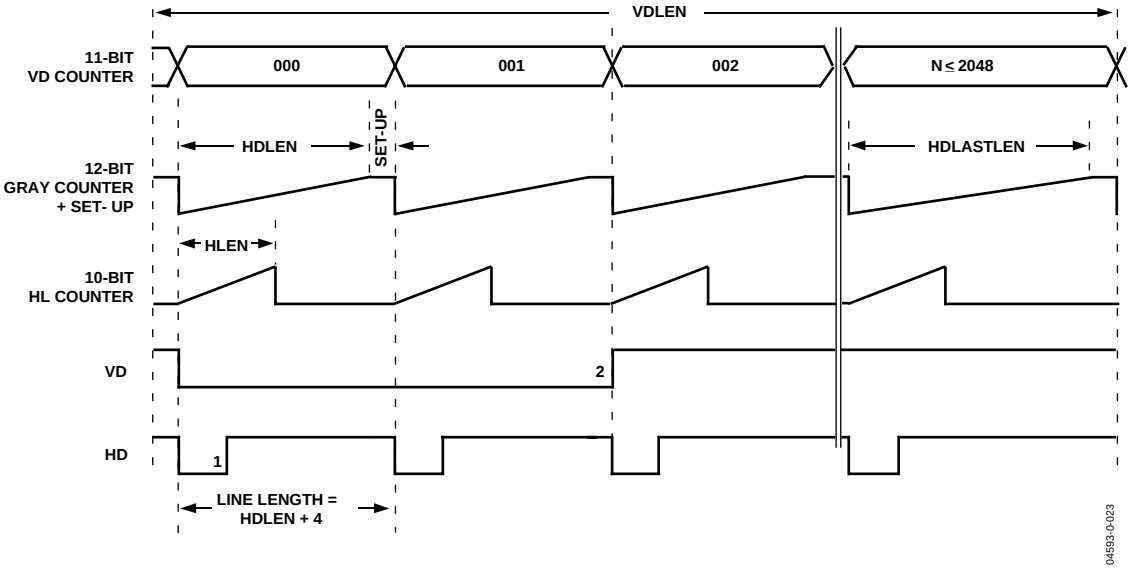
SPECIAL NOTE ABOUT THE HDLEN REGISTER

The 12-bit HD counter value must be programmed using a gray code number. There is also a 4-clock cycle, set up period that must be considered when determining the HDLEN register value, as shown in Figure 22. As a result of the 4-clock cycle, setup period, the value of HDLEN is always equal to the actual number of pixels per line minus 4. For example, if there are 2100 pixels per line, HDLEN equals (2100 – 4) = 2096. The gray code value of 2096 is 0xC28, which is what would be programmed in the HDLEN register.

Table 18. HD and VD Registers

Register Name	Bit Width	Register Type	Reference Counter	Range	Description
HDLEN[1]	12	Sys_Reg(12)	–	0–4095 Pixels	12-Bit Gray Code Counter Value
HLEN	10	Sys_Reg(12)	–	0–1023 Pixels	10-Bit HL-Counter Value
HDRISE	10	Sys_Reg(16)	HL	0–1023 Pixels	HD Rise Position
HDLASTLEN[1]	12	Mode_Reg(1)	HD	0–4095 Pixels	HD Last Line Length
VDLEN	11	Mode_Reg(1)	–	0–2047 Lines	VD Counter Value
VDRISE	4	Sys_Reg(16)	VD	0–15 Lines	VD Rise Position

[1] Register value must be a gray code number (see Gray Code Registers section).



NOTES
1. THE SET-UP DELAY IS 4 CLI CYCLES. THE ACTUAL LENGTH OF ONE LINE IS 4 MORE CYCLES THAN VALUE SET IN HDLEN AND HDLASTLEN DUE TO SET-UP DELAY.
2. VDRISE REFERENCES THE 11-BIT VD-COUNTER.
3. HDRISE REFERENCES THE 10-BIT HL-CONTER.

PROGRAMMABLE CLOCK POSITIONS
1. HDRISE (SYS_REG(16))
2. VDRISE (SYS_REG(16))

Figure 22. VD and HD Horizontal Timing

HORIZONTAL CLAMPING AND BLANKING

The AD9929's horizontal clamping and blanking pulses are programmable to suit a variety of applications. As with the vertical timing generation, individual sequences are defined for each signal, which are then organized into multiple regions during image readout. This allows the dark pixel clamping and blanking patterns to be changed at each stage of the readout, in order to accommodate different image transfer timing and high speed line shifts.

CONTROLLING CLPOB CLAMP PULSE TIMING

The AFE horizontal CLPOB pulse is generated based on the 12-bit gray code counter. Once the length of the 12-bit gray code counter is set using the HDLEN register (Sys_Reg(12)), the CLPTOG1 and CLPTOG2 registers (Sys_Reg(15 and 16)) can be used to place the CLPOB pulse location, as shown in Figure 25. Table 19 lists all CLPOB registers that are used to configure and control the placement and output of the CLPOB pulse.

The length of the last HD line is set using the HDLASTLEN register (Sys_Reg(1)). Figure 23 shows how no CLPOB pulse is asserted when the last HD length set by HDLASTLEN is shorter than the regular HD length set by HDLEN. Figure 24 shows how no CLPOB pulse is applied when the last HD length set by HDLASTLEN is longer than the regular HD length. Note that the CLPOB pulse is applied in the last line only when HDLASTLEN = HDLEN.

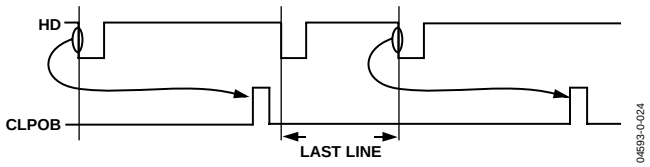


Figure 23. Last HD Shorter than Regular HD

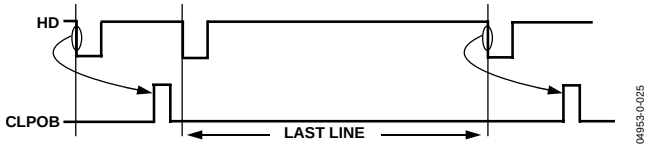


Figure 24. Last HD Longer than Regular HD

Table 19. CLPOB Registers

Register Name	Bit Width	Register Type	Counter Reference	Range	Description
CLPOB_CONT	1	Control (0x01)	–		CLPOB Control (0=CLPOB off, 1 =CLPOB On)
CLPOB_MODE	1	Control (0x01)	–		CLPOB CCD Region Control (0 = Enable CLPENx Register Settings, 1 = Disable CLPENx Register Settings)
CLPTOG1	12	Sys_Reg (15)	HD	0 to 4095 pixel locations	CLPOB Toggle Position 1 (Gray Code Number)
CLPTOG2	12	Sys_Reg (15 and 16)	HD	0 to 4095 pixel locations	CLPOB Toggle Position 2 (Gray Code Number)
CLPEN0	1	Mode_Reg (2)	–		CLPOB Control for CCD Region 0 (0 = CLPOB Disabled, 1 = CLPOB Enabled)
CLPEN1	1	Mode_Reg (2)	–		CLPOB Control for CCD Region 1 (0 = CLPOB Disabled, 1 = CLPOB Enabled)
CLPEN2	1	Mode_Reg (2)	–		CLPOB Control for CCD Region 2 (0 = CLPOB Disabled, 1 = CLPOB Enabled)
CLPEN3	1	Mode_Reg (2)	–		CLPOB Control for CCD Region 3 (0 = CLPOB Disabled, 1 = CLPOB Enabled)
CLPEN4	1	Mode_Reg (2)	–		CLPOB Control for CCD Region 4 (0 = CLPOB Disabled, 1 = CLPOB Enabled)

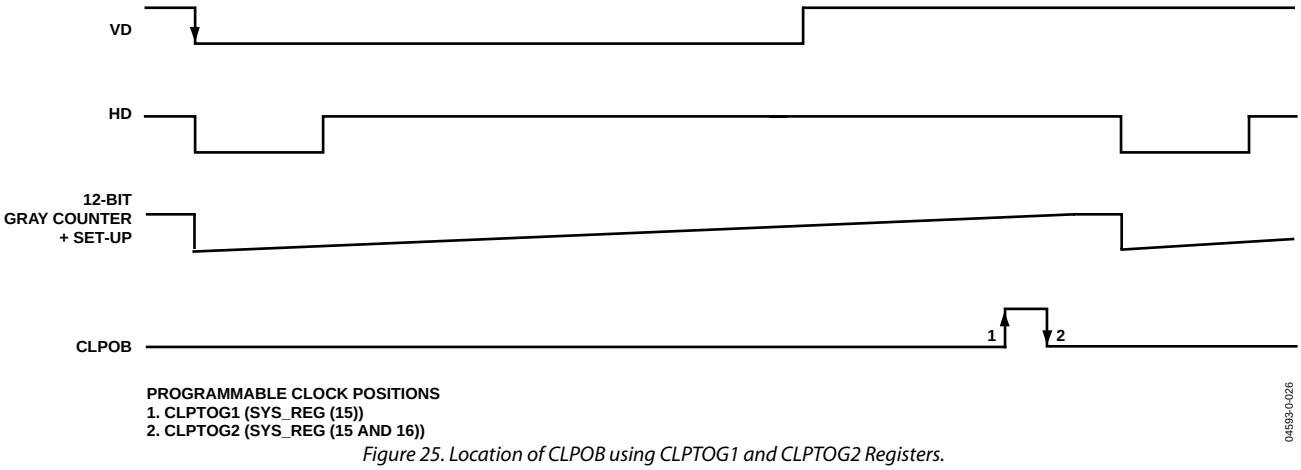


Figure 25. Location of CLPOB using CLPTOG1 and CLPTOG2 Registers.

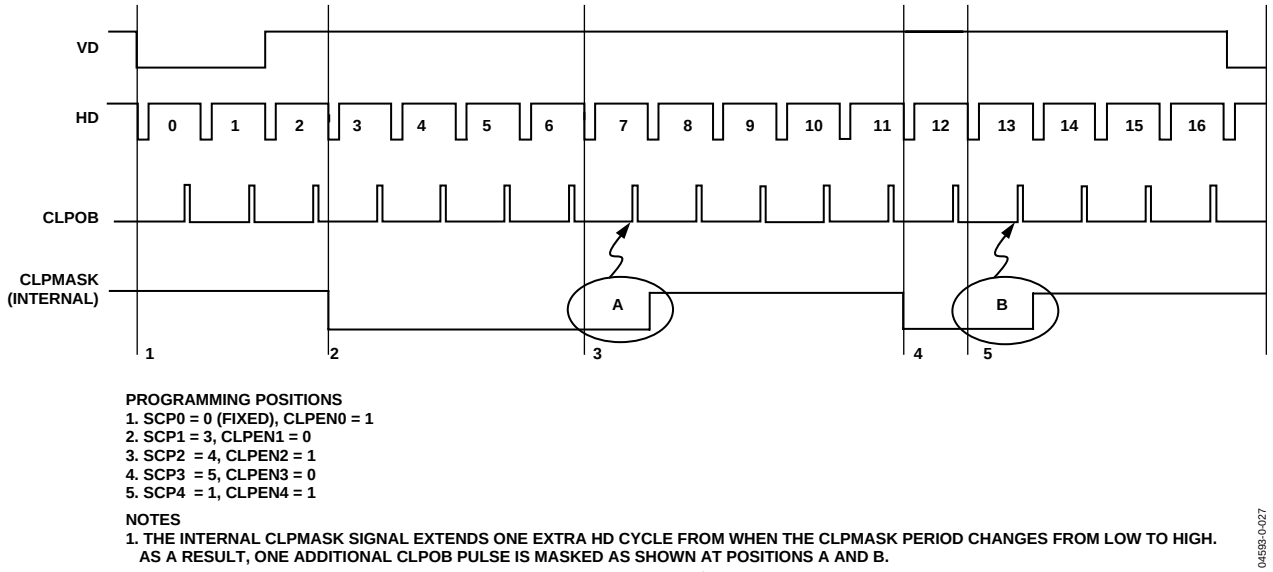


Figure 26. CLPOB Outputs with CLPMODE = 0

CONTROLLING CLPOB CLAMP PULSE OUTPUTS

The registers in Table 19 are used for programming the CLPOB pulse. The CLPOB pulse is disabled in all CCD regions by setting CLPCNT = 0. The CLPTOGx (x = 0, 1) are used to set the CLPOB toggle positions. The CLPENx (x = 0, 1, 2, 3, and 4) are used to enable or disable the CLPOB pulse separately in each CCD region when CLPMODE = 0. The CLPEN registers have no effect if CLPMODE = 1. In this case, the CLPOB pulse is asserted in all CCD regions, regardless of the value set in the CLPENx registers.

Figure 26 shows an example of the CLPOB pulse being disabled in CCD Regions 1 and 3 by setting CLPEN1 = 1 and CLPEN3 =1. Note that the CLPOB pulse remains disabled in the first line of the following CCD region.

Table 20. SCP and CLPEN

SCP[4:1][1]	CLPEN[4:0]
SCP0	CLPEN0
SCP1	CLPEN1
SCP2	CLPEN2
SCP3	CLPEN3
SCP4	CLPEN4

[1] SCP0 is not a programmable register and therefore not listed in the register map tables. SCP0 is a fixed sequence and always starts at the falling edge of VD. Although this register is not programmable, the CLPEN0 register is still used to set whether the CLPOB pulse is enabled or disabled for this SCP0 region.

H1 AND H2 BLANKING

The AD9929 provides three options for controlling the period where H1 and H2 pulses get blanked. These options are normal H blanking, selective positioning for 2 H1 and H2 outputs, and extended blanking. In all cases, HBLKMASK is used to set the polarity of H1 during the blanking period. Table 21 describes the registers used to control H blanking.

Normal H-Blanking

For normal H-blanking operation, HPULSECNT = 0 and BLKMASK = 0 or 1. The HBLKPOS register isn't used in this mode. Figure 27 shows one example where HBLKMASK = 0 and H1 and H2 are blanked while HD is low.

Selective Positioning for Two H1 and H2 Outputs

For selective positioning operation, HPULSECNT = 1 and HBLKMASK = 0 or 1. In this mode, two H1 pulses are output during the blanking period. The location of these two pulse is set using the HBLKPOS register, as shown in Figure 28.

Extended Blanking

Extended blanking is enabled by setting HBLKEXT = 1. The HBLKEXT register uses the 9-bit BL counter to suspend operation of the HD and HL counters. This delays the blanking period by the length set in the BLLEN register, as shown in Figure 29.

Table 21. H1 Blanking Registers

Register Name	Bit Width	Register Type	Description
HBLKMASK	1	Control (0x01)	Masking Polarity for H1 during Blanking Period[1] (0 = Low, 1 = High)
HPULSECNT	1	Control (0x0A)	H Pulse Control during Blanking Period
HBLKEXT	1	Control (0x0A)	(0 = No Output during Blanking,1 = Output during Blanking) H Pulse Blanking Extends Control[2] (0 = Extended Blanking Disabled, 1 = Extended Blanking Enabled)
H1BLKRETIME	1	Control (0x03)	Retimes the H1 HBLK to Internal Clock (0 = Retiming Disabled, 1 = Retiming Enabled)
HBLKHPOS	10	Sys_Reg(11)	H1 Pulse ON Position during Blanking Period

[1] H2 is always the opposite polarity of H1.
[2] The HBLKEXT extend control extends the blanking period by the number of counts set in the BLLEN register for the 9-bit BL counter.

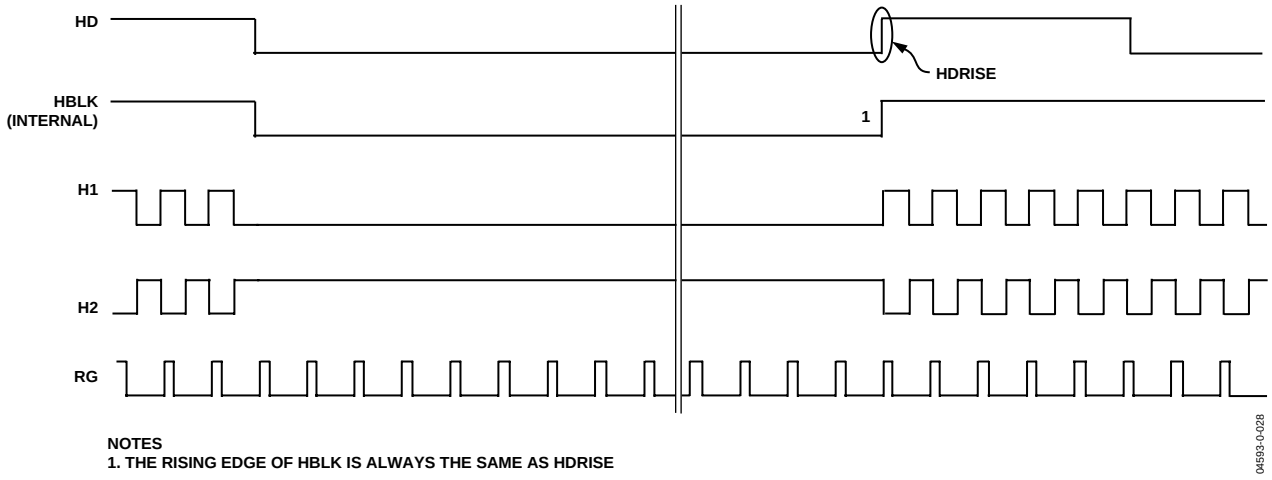


Figure 27. Normal H-Blanking Operation HBLKMASK = 0, HPULSECNT = 0, HBLKHPOS = XXX

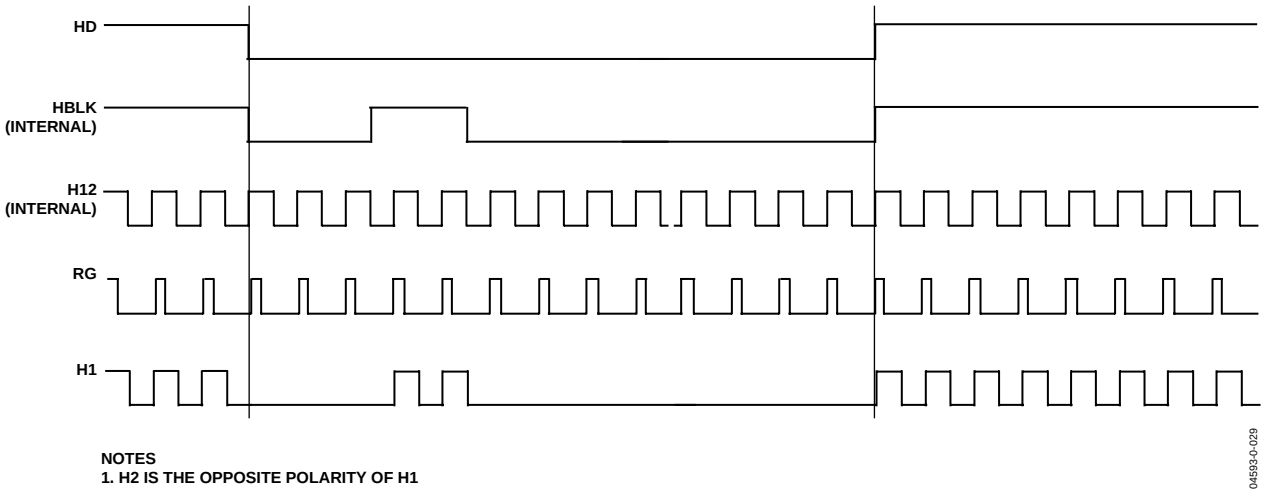


Figure 28. Selective H-Blanking Operation HBLKMASK = 0, HPULSECNT = 1, HBLKHPOS = 003.

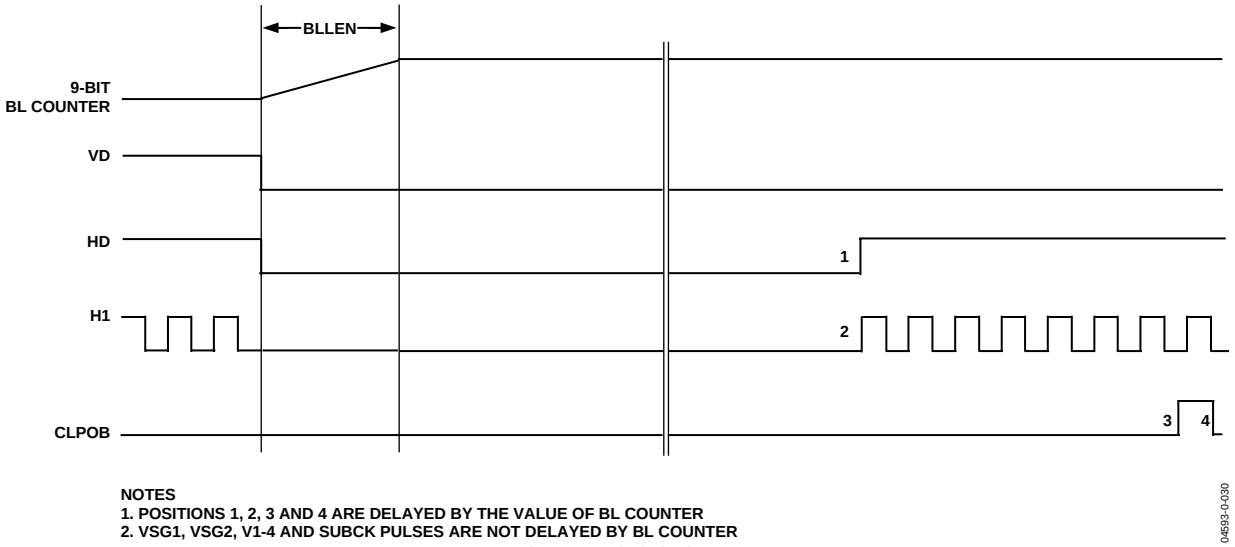


Figure 29. VD, HD, H1 and H2 Extended Blanking Operation HBLKEXT = 1.

VGATE MASKING OF XV1 TO XV4 AND CLPOB OUTPUTS

During slave mode operation, the SYNC/VGATE Pin 45 is configured as an input for an external VGATE signal. While operating in this mode, the external VGATE signal can be used to mask the XV1 to XV4 and CLPOB outputs. There are two options available for masking the XV1 to XV4 and CLPOB outputs. These options are determined by the setting of the MSHUT/VGATE_EN register located at Control Address 0x01. Examples of these two options are shown in Figure 30 and Figure 31. Figure 30 shows MSHUT/VGATE_EN = 0. In this example, the VGATE signal is internally latched on the falling edge of HD, resulting with the XV1 to XV4 and CLPOB outputs being masked when the internally latched VGATE signal is high.

Figure 31 shows MSHUT/VGATE_EN = 1. In this example, the preprogrammed MSHUT signal blocks the VGATE input from masking XV1 to XV4 and CLPOB outputs while MSHUT is low. The internally latched VGATE signal only masks XV1 to XV4 and CLPOB when MSHUT is high, while operating in this mode.

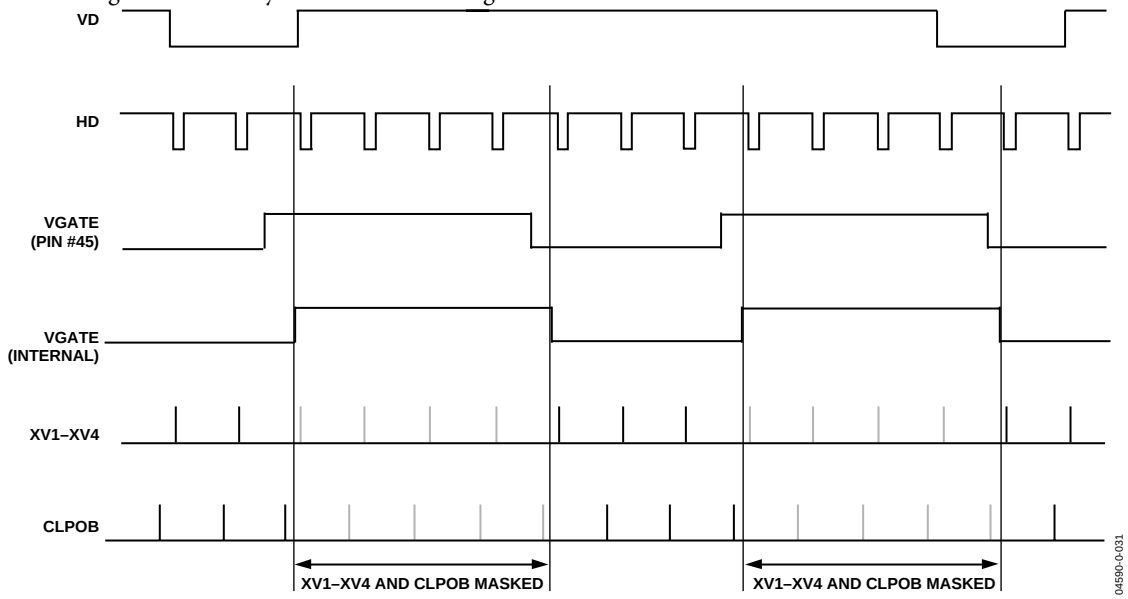


Figure 30. Example of VGATE Input Masking V1 to V4 and CLPOB Outputs with MSHUT/VGATE_EN = 0

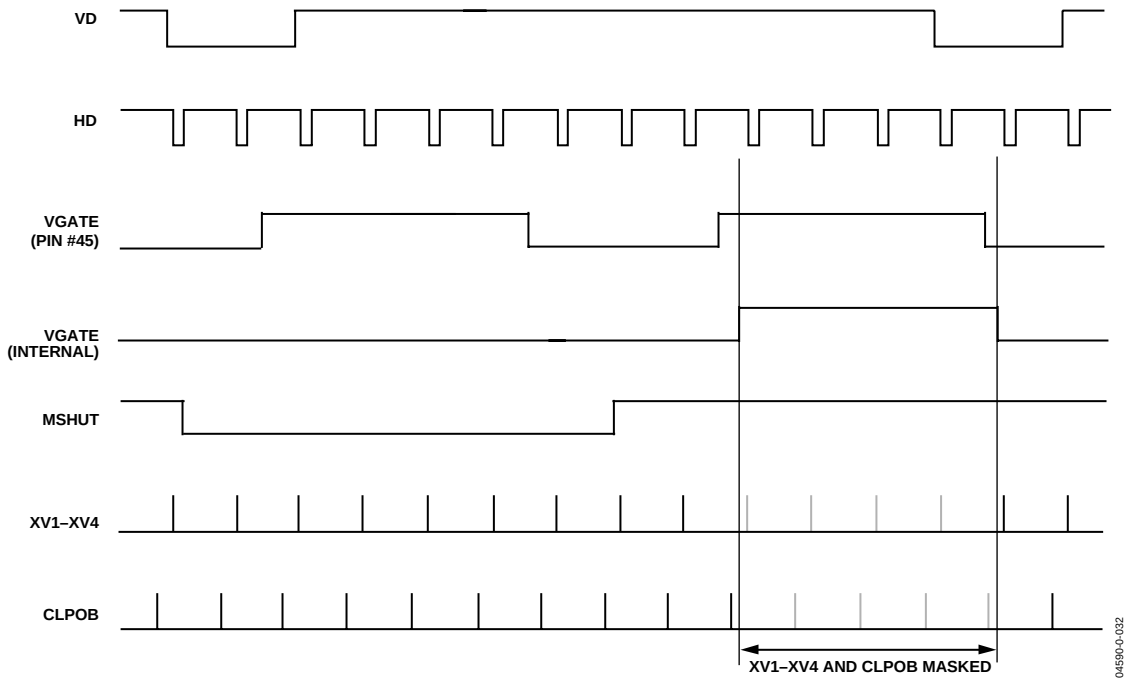


Figure 31. Example of VGATE Input Masking V1to V4 and CLPOB Outputs with MSHUT/VGATE_EN = 1

VERTICAL TIMING GENERATION

The AD9929 provides a very flexible solution for generating vertical CCD timing and can support multiple CCDs and different system architectures. The 4-phase vertical transfer clocks XV1 to XV4 are used to shift each line of pixels into the horizontal output register of the CCD. The AD9929 vertical outputs can be individually programmed into four different vertical pulse patterns identified as VTP0, VTP1, VTP2, and VTP3. Each vertical pulse pattern is a unique set of preconfigured XV1 to XV4 sequences. Once the vertical patterns have been configured using the registers shown in Table 24, pointer registers are used to select in which region of the CCD a particular vertical pattern is output. The pointer registers are described in Table 22.

Up to five unique CCD regions may be specified. Finally, the readout of the entire field is constructed by combining one or more of the individual regions sequentially. With up to five regions available, different steps of the readout such as high speed line shifts and vertical image transfer can be supported.

CREATING VERTICAL SEQUENCES

Figure 32 through Figure 34 provide an overview of how the vertical timing is generated in four basic steps.

Step 1: Create the individual pulses for patterns VTP0, VTP1, VTP2, and VTP3 (see Figure 32**).**

The registers shown in Table 22 are used to generate the individual vertical timing pulses, as shown in Figure 32.

The VTPLENx determines the number of pixels between pulse repetitions. The start polarity (XVxSTARTPOLx) sets the starting polarity of the vertical sequence and can be programmed high or low. The first toggle position (XVxTOG1POSx) and second toggle position (XVxTOG2POSx) are the pixel locations within the line where the pulse transitions.

Step 2: Create the individual vertical sequences (see Figure 33).

Create the individual vertical sequences by assigning pulse repetitions to patterns VTP0, VTP1, VTP2, and VTP3 using the VTPREPx registers as shown in Table 25. The number of repetitions (VTPREPx) determines the number of pulse repetitions desired within a single line. Programming 1 for VTPREPx gives a single pulse, and setting to 0 provides a fixed dc output based on the start polarity value. Figure 33 shows an example of a VTPx sequence of two VTPx patterns by setting VTPREPx = 2.

Step 3: Output Vertical Sequences into CCD Regions (see Figure 34**).**

The AD9929 arranges individual sequences into CCD regions through the use of sequence pointers (VTPSEQPTRx) and vertical transfer pattern select (VTPSELx) registers, as described in Table 23. The VTPSEQPTRx registers are used to point to a desired VTPSELx register whose value determines what VTPx pattern is output on the XV1 to XV4 signals. For example, if VTPSEQPTR0 = 1 and VTPSEL1 = 2, the VTP2 pulse pattern would output while operating in Region 0 of the CCD.

Step 4: Combining CCD Regions (see Figure 34**).**

Build the entire field readout by combining multiple regions by using mode registers SCP0, SCP1, SCP2, SCP3, and SCP4.

The individual CCD regions are combined into a complete field readout by using sequence change position (SCPx) pointers as described in Table 23. Figure 34 shows how each field is divided into multiple regions. This allows the user to change vertical timing during various stages of the image readout. The boundaries of each region are defined by the sequence change position (SCP). Each SCP is a 8-bit value representing the line number boundary region. A total of four SCPs allow up to five different region areas in the field to be defined. The first SCP0 is always hard-coded to line 0, and the remaining four SCPs are register programmable.

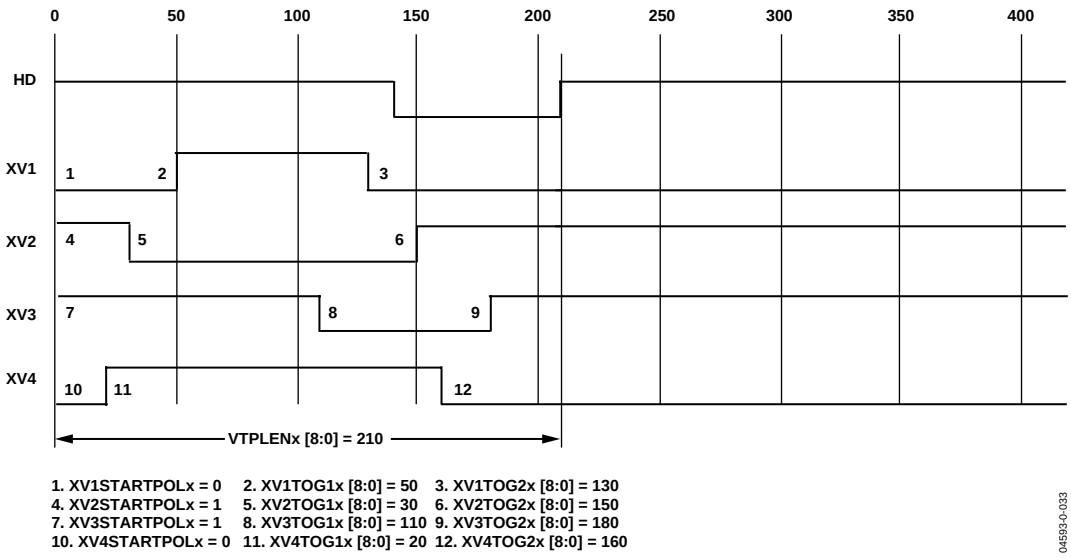


Figure 32. Step 1: Create Individual Vertical Pulses for VTP0, VTP1, VTP2, and VTP3 Patterns.

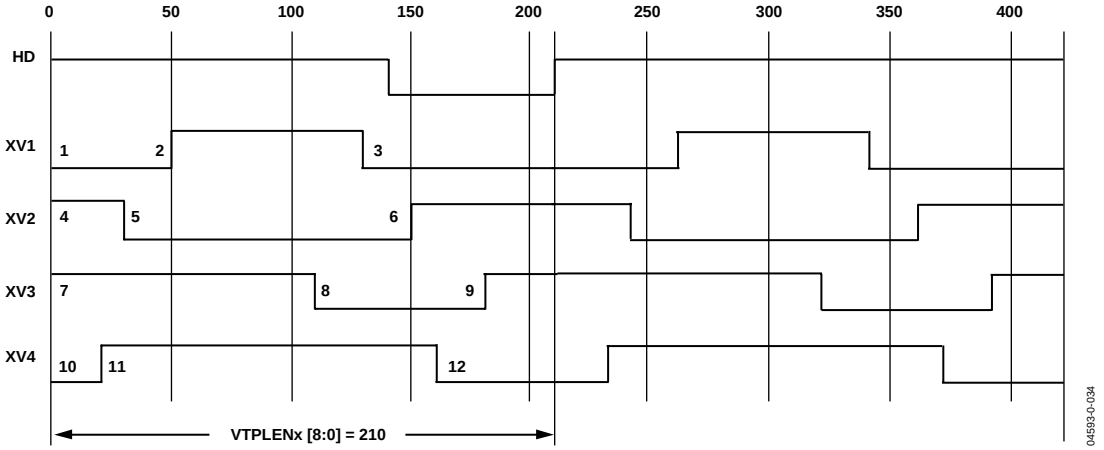
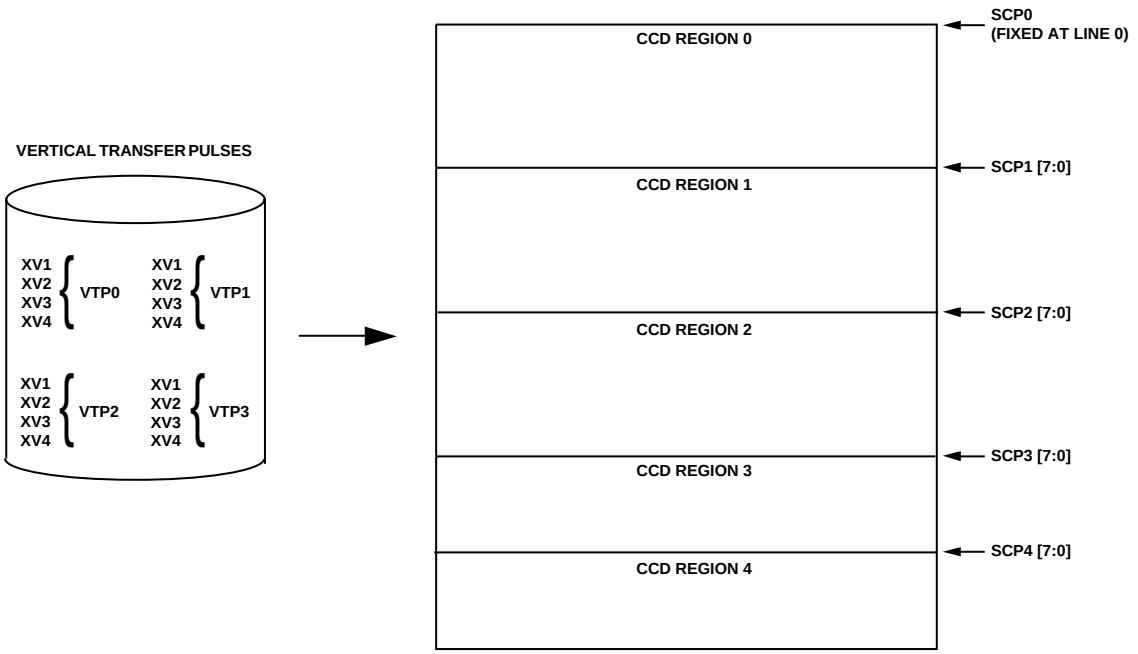


Figure 33. Step 2: Create Individual Sequences for XV1 to XV4 Outputs by Assigning Pulse Repetitions to VTP0, VTP1, VTP2 and VTP3 Patterns. This Example Shows VTPREPx = 2



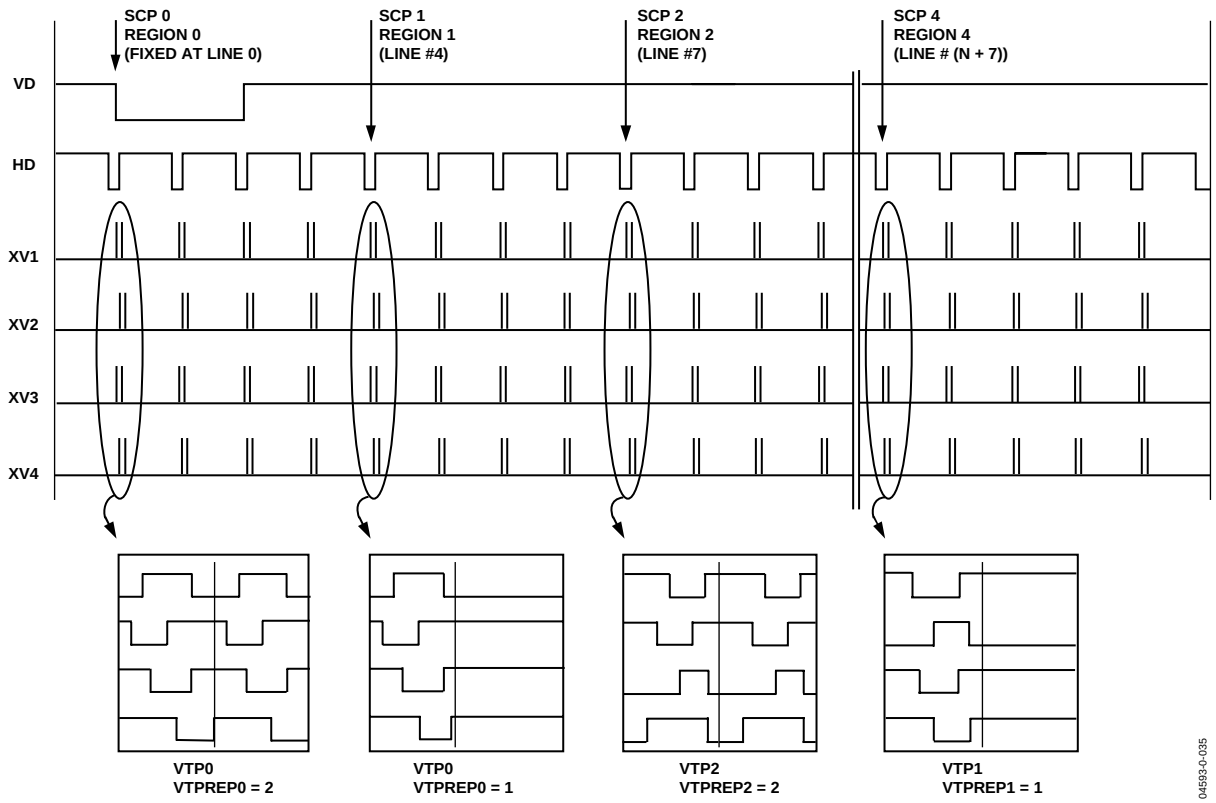


Figure 34. Steps 3 and 4: An Example of Building an Entire Field Readout by Assigning Sequences to Multiple CCD Regions

Table 22. XV1 to XV4 Registers to Configure XXV1 to XXV4 Pulses for each VTP Pattern

Register Name	Bit Width	Register Type	Reference Counter	Range	Description	VTP Pattern
VTPLEN0	9	Sys_Reg(1)	V Counter	0–511	Length between Repetitions	
XV1STARTPOL0	1	Sys_Reg(1)		High/Low	XV1 Starting Polarity for VTP0 (0 = Low, 1 = High)	
XV2STARTPOL0	1	Sys_Reg(1)		High/Low	XV2 Starting Polarity for VTP0 (0 = Low, 1 = High)	
XV3STARTPOL0	1	Sys_Reg(1)		High/Low	XV3 Starting Polarity for VTP0 (0 = Low, 1 = High)	
XV4STARTPOL0	1	Sys_Reg(1)		High/Low	XV4 Starting Polarity for VTP0 (0 = Low, 1 = High)	
XV1TOG1POS0	9	Sys_Reg(1)	V Counter	0–511	XV1 Toggle Position 1 for VTP0	VTP0
XV1TOG2POS0	9	Sys_Reg(1)	V Counter	0–511	XV1 Toggle Position 2 for VTP0	
XV2TOG1POS0	9	Sys_Reg(1 & 2)	V Counter	0–511	XV2 Toggle Position 1 for VTP0	
XV2TOG2POS0	9	Sys_Reg(2)	V Counter	0–511	XV2 Toggle Position 2 for VTP0	
XV3TOG1POS0	9	Sys_Reg(2)	V Counter	0–511	XV3 Toggle Position 1 for VTP0	
XV3TOG2POS0	9	Sys_Reg(2 & 3)	V Counter	0–511	XV3 Toggle Position 2 for VTP0	
XV4TOG1POS0	9	Sys_Reg(3)	V Counter	0–511	XV3 Toggle Position 1 for VTP0	
XV4TOG2POS0	9	Sys_Reg(3)	V Counter	0–511	XV3 Toggle Position 2 for VTP0	
VTPLEN1	9	Sys_Reg(3)	V Counter	0–512	Length between Repetitions	
XV1STARTPOL1	1	Sys_Reg(3)		High/Low	XV1 Starting Polarity for VTP1 (0 = Low, 1 = High)	
XV2STARTPOL1	1	Sys_Reg(3)		High/Low	XV2 Starting Polarity for VTP1 (0 = Low, 1 = High)	
XV3STARTPOL1	1	Sys_Reg(4)		High/Low	XV3 Starting Polarity for VTP1 (0 = Low, 1 = High)	
XV4STARTPOL1	1	Sys_Reg(4)		High/Low	XV4 Starting Polarity for VTP1 (0 = Low, 1 = High)	
XV1TOG1POS1	9	Sys_Reg(4)	V Counter	0–511	XV1 Toggle Position 1 for VTP1	VTP1
XV1TOG2POS1	9	Sys_Reg(4)	V Counter	0–511	XV1 Toggle Position 2 for VTP1	
XV2TOG1POS1	9	Sys_Reg(4	V Counter	0–511	XV2 Toggle Position 1 for VTP1	
XV2TOG2POS1	9	Sys_Reg(4 & 5)	V Counter	0–511	XV2 Toggle Position 2 for VTP1	
XV3TOG1POS1	9	Sys_Reg(5)	V Counter	0–511	XV3 Toggle Position 1 for VTP1	
XV3TOG2POS1	9	Sys_Reg(5)	V Counter	0–511	XV3 Toggle Position 2 for VTP1	
XV4TOG1POS1	9	Sys_Reg(5 & 6)	V Counter	0–511	XV3 Toggle Position 1 for VTP1	
XV4TOG2POS1	9	Sys_Reg(6)	V Counter	0–511	XV3 Toggle Position 2 for VTP1	
VTPLEN2	9	Sys_Reg(6)	V Counter	0–512	Length between Repetitions	
XV1STARTPOL2	1	Sys_Reg(6)		High/Low	XV1 Starting Polarity for VTP2 (0 = Low, 1 = High)	
XV2STARTPOL2	1	Sys_Reg(6)		High/Low	XV2 Starting Polarity for VTP2 (0 = Low, 1 = High)	
XV3STARTPOL2	1	Sys_Reg(6)		High/Low	XV3 Starting Polarity for VTP2 (0 = Low, 1 = High)	
XV4STARTPOL2	1	Sys_Reg(6)		High/Low	XV4 Starting Polarity for VTP2 (0 = Low, 1 = High)	
XV1TOG1POS2	9	Sys_Reg(6)	V Counter	0–511	XV1 Toggle Position 1 for VTP2	VTP2
XV1TOG1POS2	9	Sys_Reg(7)	V Counter	0–511	XV1 Toggle Position 1 for VTP2	
XV1TOG2POS2	9	Sys_Reg(7)	V Counter	0–511	XV1 Toggle Position 2 for VTP2	
XV2TOG1POS2	9	Sys_Reg(7)	V Counter	0–511	XV2 Toggle Position 1 for VTP2	
XV3TOG1POS2	9	Sys_Reg(7 & 8)	V Counter	0–511	XV3 Toggle Position 1 for VTP2	
XV3TOG2POS2	9	Sys_Reg(8)	V Counter	0–511	XV3 Toggle Position 2 for VTP2	
XV4TOG1POS2	9	Sys_Reg(8)	V Counter	0–511	XV3 Toggle Position 1 for VTP2	
XV4TOG2POS2	9	Sys_Reg(8)	V Counter	0–511	XV3 Toggle Position 2 for VTP2	

Register Name	Bit Width	Register Type	Reference Counter	Range	Description	VTP Pattern
VTPLEN3	9	Sys_Reg(9)	V Counter	0–512	Length between Repetitions	VTP3
XV1STARTPOL3	1	Sys_Reg(9)		High/Low	XV1 Starting Polarity for VTP3 (0 = Low, 1 = High)	
XV2STARTPOL3	1	Sys_Reg(9)		High/Low	XV1 Starting Polarity for VTP3 (0 = Low, 1 = High)	
XV3STARTPOL3	1	Sys_Reg(9)		High/Low	XV1 Starting Polarity for VTP3 (0 = Low, 1 = High)	
XV4STARTPOL3	1	Sys_Reg(9)		High/Low	XV1 Starting Polarity for VTP3 (0 = Low, 1 = High)	
XV1TOG1POS3	9	Sys_Reg(9)	V Counter	0–511	XV1 Toggle Position 1 for VTP3	
XV1TOG2POS3	9	Sys_Reg(9)	V Counter	0–511	XV1 Toggle Position 2 for VTP3	
XV2TOG1POS3	9	Sys_Reg(9 &10)	V Counter	0–511	XV2 Toggle Position 1 for VTP3	
XV2TOG2POS3	9	Sys_Reg(10)	V Counter	0–511	XV2 Toggle Position 2 for VTP3	
XV3TOG1POS3	9	Sys_Reg(10)	V Counter	0–511	XV3 Toggle Position 1 for VTP3	
XV3TOG2POS3	9	Sys_Reg(10&11)	V Counter	0–511	XV3 Toggle Position 2 for VTP3	
XV4TOG1POS3	9	Sys_Reg(11)	V Counter	0–511	XV3 Toggle Position 1 for VTP3	
XV4TOG2POS3	9	Sys_Reg(11)	V Counter	0–511	XV3 Toggle Position 2 for VTP3	

Table 23. Mode_A and Mode_B Registers for VTPx Selection

Register Name	Bit Width	Register Type	Range	Description
VTPSEQPTR0[1]	3	Mode_Reg(2)		Vertical Transfer Pulse Pointer used in CCD Region 0 (0 = VTPSEL0, 1 = VTPSEL1, 2 = VTPSEL2, 3 = VTPSEL3, 4 = VTPSEL0 for Even Line and VTPSEL1 for Odd Line, 5 = VTPSEL2 for Even Line and VTPSEL3 for Odd Line)
VTPSEQPTR1[1]	3	Mode_Reg(2)		Vertical Transfer Pulse Pointer used in CCD Region 1 (0 = VTPSEL0, 1 = VTPSEL1, 2 = VTPSEL2, 3 = VTPSEL3, 4 = VTPSEL0 for Even Line and VTPSEL1 for Odd Line, 5 = VTPSEL2 for Even Line and VTPSEL3 for Odd Line)
VTPSEQPTR2[1]	3	Mode_Reg(2)		Vertical Transfer Pulse Pointer used in CCD Region 2 (0 = VTPSEL0, 1 = VTPSEL1, 2 = VTPSEL2, 3 = VTPSEL3, 4 = VTPSEL0 for Even Line and VTPSEL1 for Odd Line, 5 = VTPSEL2 for Even Line and VTPSEL3 for Odd Line)
VTPSEQPTR3[1]	3	Mode_Reg(2)		Vertical Transfer Pulse Pointer used in CCD Region 3 (0 = VTPSEL0, 1 = VTPSEL1, 2 = VTPSEL2, 3 = VTPSEL3, 4 = VTPSEL0 for Even Line and VTPSEL1 for Odd Line, 5 = VTPSEL2 for Even Line and VTPSEL3 for Odd Line)
VTPSEQPTR4[1]	3	Mode_Reg(2)		Vertical Transfer Pulse Pointer used in CCD Region 4 (0 = VTPSEL0, 1 = VTPSEL1, 2 = VTPSEL2, 3 = VTPSEL3, 4 = VTPSEL0 for Even Line and VTPSEL1 for Odd Line, 5 = VTPSEL2 for Even Line and VTPSEL3 for Odd Line)
VTPSEL0	2	Mode_Reg(3)		0 = VTP0, 1 = VTP1, 2 = VTP2, 3 = VTP3
VTPSEL1	2	Mode_Reg(3)		0 = VTP0, 1 = VTP1, 2 = VTP2, 3 = VTP3
VTPSEL2	2	Mode_Reg(3)		0 = VTP0, 1 = VTP1, 2 = VTP2, 3 = VTP3
VTPSEL3	2	Mode_Reg(3)		0 = VTP0, 1 = VTP1, 2 = VTP2, 3 = VTP3
VTPREP0	3	Mode_Reg(3)	0–7	Number of VTP0 Pulse Repetitions within a Line
VTPREP1	3	Mode_Reg(4)	0–7	Number of VTP1 Pulse Repetitions within a Line
VTPREP2	3	Mode_Reg(4)	0–7	Number of VTP2 Pulse Repetitions within a Line
VTPREP3	3	Mode_Reg(4)	0–7	Number of VTP3 Pulse Repetitions within a Line

[1] Register settings 6 and 7 are not used.

Table 24. Mode_A and Mode_B Registers for CCD Region Selection

Register Name	Bit Width	Register Type	Range	Description
SCP1	8	Mode_Reg(2)	0–255 lines	Sequence Change Position 1
SCP2	8	Mode_Reg(2)	0–255 lines	Sequence Change Position 2
SCP3	8	Mode_Reg(2)	0–255 lines	Sequence Change Position 3
SCP4	8	Mode_Reg(2)	0–255 lines	Sequence Change Position 4

SPECIAL VERTICAL SWEEP MODE OPERATION

The AD9929 contains a special mode of vertical timing operation called sweep mode. This mode is used to generate a continuous number of repetitive vertical pulses that span multiple HD lines. One example of where this mode may be needed is at the start of the CCD readout operation. At the end of the image exposure, but before the image is transferred by the sensor gate pulses, the vertical interline CCD registers should be clean of all charge. This can be accomplished by quickly shifting out any charge with a long series of pulses on the V1 to V4 outputs. This operation spans multiple HD line lengths.

Normally the sequences are contained within one HD line length but with the sweep mode enabled, the HD boundaries will be ignored until the region is finished.

The special vertical sweep mode operation is only output in CCD Region 0 and CCD Region 3 (see Figure 34), as shown in Figure 37 and Figure 38. The SVREP_MODE register located at Control Address 0x0A is used to enable and configure the special sweep mode operation, as described in Table 25.

The maximum number of repeats in each region is 2048 while operating in this mode using the SVREP0 and SVREP3 Mode_Reg(4) registers.

Table 25. Description of SVREP_MODE Register

SVREP_MODE	Description of Sweep Mode Operation	
0	0	Normal Vertical Timing Operation in all CCD Regions
0	1	Special Vertical Sweep Mode Timing Output in CCD Region 0 Only
1	0	Special Vertical Sweep Mode Timing Output in CCD Region 3 Only
1	1	Special Vertical Sweep Mode Timing Output in CCD Region0 and CCD Region 3

Figure 35. Nonoverlapping Example while Operating in Normal Vertical Timing Operation SVREP_MODE = 0 and VTPREPx = 4

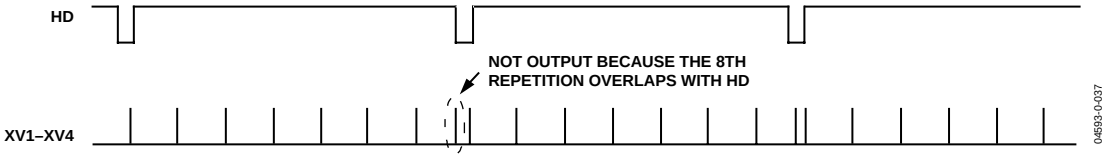


Figure 36. Overlapping Example while Operating in Normal Vertical Timing Operation SVREP_MODE = 0 and VTPREPx = 8

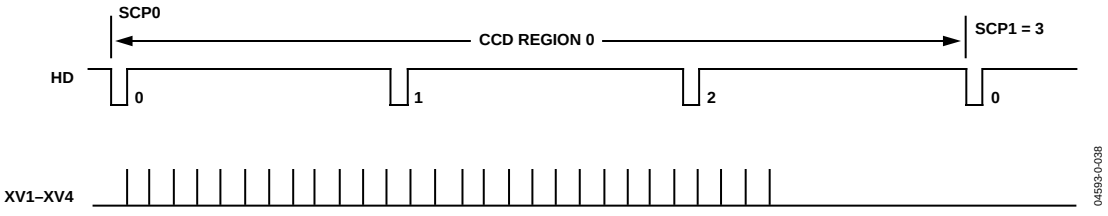


Figure 37. Sweep Mode Timing Example with SVREP_MODE = 1 and SVREP0 = 28

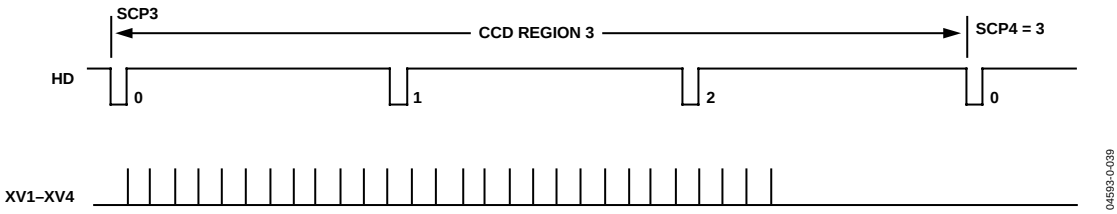


Figure 38. Sweep Mode Timing Example with SVREP_MODE = 2 and SVREP3 = 28

SPECIAL VERTICAL TIMING (SPATS)

The AD9929 provides additional special vertical timing generation (SPATs), which is applied in the same line as the VSG pulse. The SPAT timing allows for an additional vertical output pulse in the VSG line. The additional vertical output pulse can be applied to either XV1, XV2, XV3 or XV4, according to the value of the SPATLOGIC register. Table 26 lists the registers used to generate the SPATs, and Table 27 describes the SPATLOGIC settings and operation.

Figure 39 and Figure 40 show AND and OR SPAT pulse examples using four SPAT toggle positions. As shown in these figures, the internal SPAT timing for the AND case initially starts high and then goes low at the first XVxSPAT_TOG1 position. In the OR case, the internal SPAT timing initially starts low and then toggles high at the first XVxSPAT_TOG1 position. This provides the ability to output the second vertical pulse when the internal XVx pulse is in both high and low states. Note that although Figure 39 and Figure 40 show four SPAT toggle positions, two SPAT toggle positions can be applied by setting XVxSPAT_TOG3 = XVxSPAT_TOG4 = 0x1FFF.

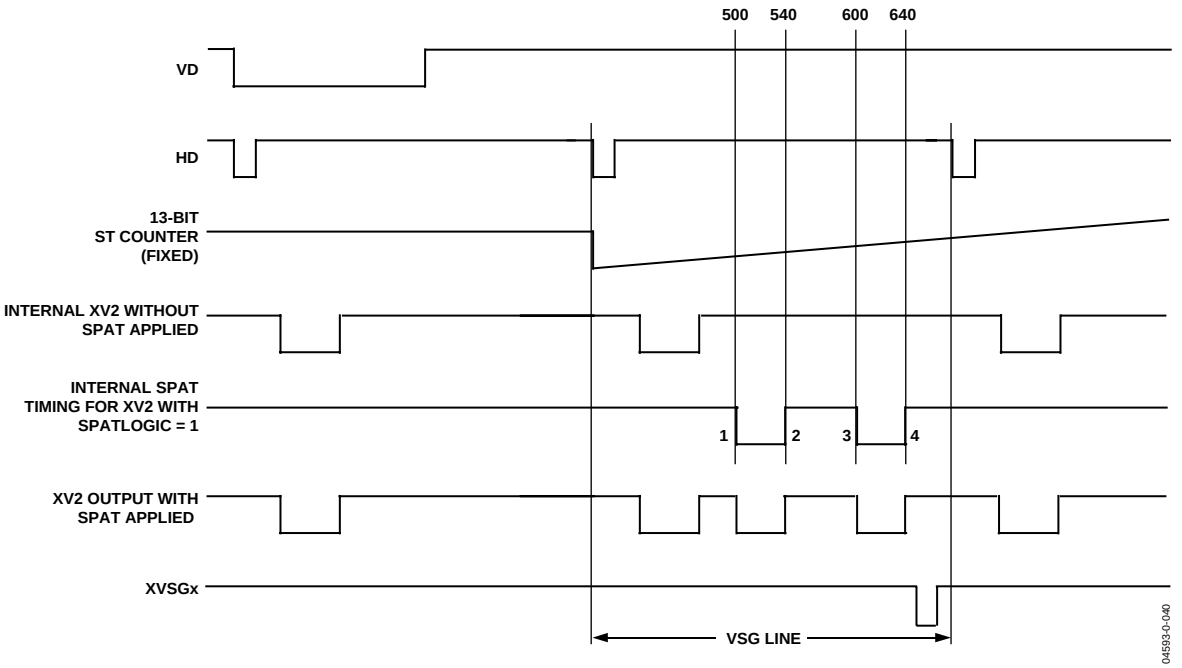
Table 26. HD and VD Registers

Register Name	Bit Width	Register Type	Reference Counter	Range (Pixels)	Description
SPAT_EN	1	Control (Address 0x01)	–		SPAT Enable Control (0 = SPAT Disabled, 1 = SPAT Enabled)
SPATLOGIC	4	Control (Address 0x0A)	–		SPAT Logic Setting
XV1SPAT_TOG1	13	Control (Address 0x17)	ST	0–8192	XV1SPAT Toggle Position #1 (Mode_A Active)
XV1SPAT_TOG2	13	Control (Address 0x18)	ST	0–8192	XV1SPAT Toggle Position #2 (Mode_A Active)
XV1SPAT_TOG3	13	Mode_A_Reg(5)	ST	0–8192	XV1SPAT Toggle Position #3 (Mode_A Active)
XV1SPAT_TOG4	13	Mode_A_Reg(5)	ST	0–8192	XV1SPAT Toggle Position #4 (Mode_A Active)
XV2SPAT_TOG1	13	Control (Address 0x19)	ST	0–8192	XV2SPAT Toggle Position #1 (Mode_A Active)
XV2SPAT_TOG2	13	Control (Address 0x1A)	ST	0–8192	XV2SPAT Toggle Position #2 (Mode_A Active)
XV2SPAT_TOG3	13	Mode_A_Reg(5)	ST	0–8192	XV2SPAT Toggle Position #3 (Mode_A Active)
XV2SPAT_TOG4	13	Mode_A_Reg(5)	ST	0–8192	XV2SPAT Toggle Position #4 (Mode_A Active)
XV3SPAT_TOG1	13	Control (Address 0x1B)	ST	0–8192	XV3SPAT Toggle Position #1 (Mode_A Active)
XV3SPAT_TOG2	13	Control (Address 0x1C)	ST	0–8192	XV3SPAT Toggle Position #2 (Mode_A Active)
XV3SPAT_TOG3	13	Mode_A_Reg(5)	ST	0–8192	XV3SPAT Toggle Position #3 (Mode_A Active)
XV3SPAT_TOG4	13	Mode_A_Reg(5)	ST	0–8192	XV3SPAT Toggle Position #4 (Mode_A Active)
XV4SPAT_TOG1	13	Control (Address 0x1D)	ST	0–8192	XV4SPAT Toggle Position #1 (Mode_A Active)
XV4SPAT_TOG2	13	Control (Address 0x1E)	ST	0–8192	XV4SPAT Toggle Position #2 (Mode_A Active)
XV4SPAT_TOG3	13	Mode_A_Reg(5)	ST	0–8192	XV4SPAT Toggle Position #3 (Mode_A Active)
XV4SPAT_TOG4	13	Mode_A_Reg(5)	ST	0–8192	XV4SPAT Toggle Position #4 (Mode_A Active)
XV1SPAT_TOG1	13	Control (Address 0x1F)	ST	0–8192	XV1SPAT Toggle Position #1 (Mode_B Active)
XV1SPAT_TOG2	13	Control (Address 0x20)	ST	0–8192	XV1SPAT Toggle Position #2 (Mode_B Active)
XV1SPAT_TOG3	13	Mode_B_Reg(5)	ST	0–8192	XV1SPAT Toggle Position #3 (Mode_B Active)
XV1SPAT_TOG4	13	Mode_B_Reg(5)	ST	0–8192	XV1SPAT Toggle Position #4 (Mode_B Active)

Register Name	Bit Width	Register Type	Reference Counter	Range (Pixels)	Description
XV2SPAT_TOG1	13	Control (Address 0x21)	ST	0–8192	XV2SPAT Toggle Position #1 (Mode_B Active)
XV2SPAT_TOG2	13	Control (Address 0x22)	ST	0–8192	XV2SPAT Toggle Position #2 (Mode_B Active)
XV2SPAT_TOG3	13	Mode_B_Reg(5)	ST	0–8192	XV2SPAT Toggle Position #3 (Mode_B Active)
XV2SPAT_TOG4	13	Mode_B_Reg(5)	ST	0–8192	XV2SPAT Toggle Position #4 (Mode_B Active)
XV3SPAT_TOG1	13	Control (Address 0x23)	ST	0–8192	XV3SPAT Toggle Position #1 (Mode_B Active)
XV3SPAT_TOG2	13	Control (Address 0x24)	ST	0–8192	XV3SPAT Toggle Position #2 (Mode_B Active)
XV3SPAT_TOG3	13	Mode_B_Reg(5)	ST	0–8192	XV3SPAT Toggle Position #3 (Mode_B Active)
XV3SPAT_TOG4	13	Mode_B_Reg(5)	ST	0–8192	XV3SPAT Toggle Position #4 (Mode_B Active)
XV4SPAT_TOG1	13	Control (Address 0x25)	ST	0–8192	XV4SPAT Toggle Position #1 (Mode_B Active)
XV4SPAT_TOG2	13	Control (Address 0x26)	ST	0–8192	XV4SPAT Toggle Position #2 (Mode_B Active)
XV4SPAT_TOG3	13	Mode_B_Reg(5)	ST	0–8192	XV4SPAT Toggle Position #3 (Mode_B Active)
XV4SPAT_TOG4	13	Mode_B_Reg(5)	ST	0–8192	XV4SPAT Toggle Position #4 (Mode_B Active)

Table 27. SPATLOCIC Register (Address 0x0A)

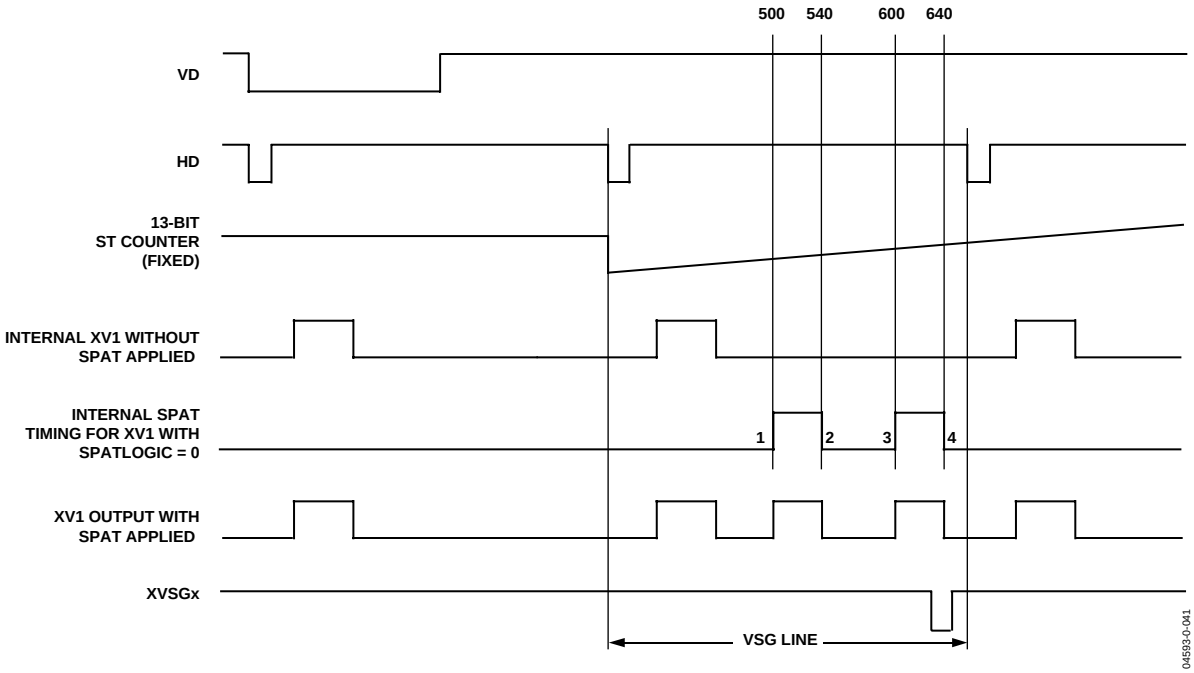
SPATLOGIC[3:0]				SPAT Description
3	2	1	0	
XV4	XV3	XV2	XV1	0 = OR, 1 = AND



NOTES
1. THE XVxSPAT_TOG1 AND XVxSPAT_TOG2 REGISTERS REFERENCE THE 13-BIT ST COUNTER.
2. THE INTERNAL SPAT TIMING IS APPLIED IN THE SAME LINE AS THE XVSGx PULSE.

PROGRAMMABLE CLOCK POSITIONS
1. XVXSPAT_TOG1 (PROGRAMMABLE AT CONTROL REGS) 2. XVXSPAT_TOG2 (PROGRAMMABLE AT CONTROL REGS)
3. XVXSPAT_TOG3 (PROGRAMMABLE AT MODE_REGS) 4. XVXSPAT_TOG4 (PROGRAMMABLE AT MODE_REGS)

Figure 39. SPAT Example for XV2 with XV2SPAT_TOG1 = 500, XV2SPAT_TOG2 = 540, XV2SPAT_TOG3 = 600, XV2SPAT_TOG4 = 640, and SPATLOGIC = XX1X



NOTES
1. THE XVxSPAT_TOG1 AND XVxSPAT_TOG2 REGISTERS REFERENCE THE 13-BIT ST COUNTER.
2. THE INTERNAL SPAT TIMING IS APPLIED IN THE SAME LINE AS THE XVSGx PULSE.

PROGRAMMABLE CLOCK POSITIONS
1. XVXSPAT_TOG1 (PROGRAMMABLE AT CONTROL REGS) 2. XVXSPAT_TOG2 (PROGRAMMABLE AT CONTROL REGS)
3. XVXSPAT_TOG3 (PROGRAMMABLE AT MODE_REGS) 4. XVXSPAT_TOG4 (PROGRAMMABLE AT MODE_REGS)

Figure 40. SPAT (OR) Example for XV1 with XV1SPAT_TOG1 = 500, XV1SPAT_TOG2 = 540, XV1SPAT_TOG3 = 600, XV1SPAT_TOG4 = 640, and SPATLOGIC = XXX0

V1 TO V4 AND SUBCK OUTPUT POLARITIES

As shown in Figure 41, the XV1 to XV4 and XSUBCK are output signals from the AD9929 timing generator, whereas the V1 to V1 and SUBCK are output signals from the AD9929 vertical driver. The V1 to V4 and SUBCK polarities are not the same as the internal XV1 to XV4 and XSUBCK polarities configured by the AD9929 registers. Table 28 through Table 32 describe the output polarities for these signals versus their input levels. These tables must be referred to when determining the register settings for the desired output levels. Figure 46 shows an example of the V3 output.

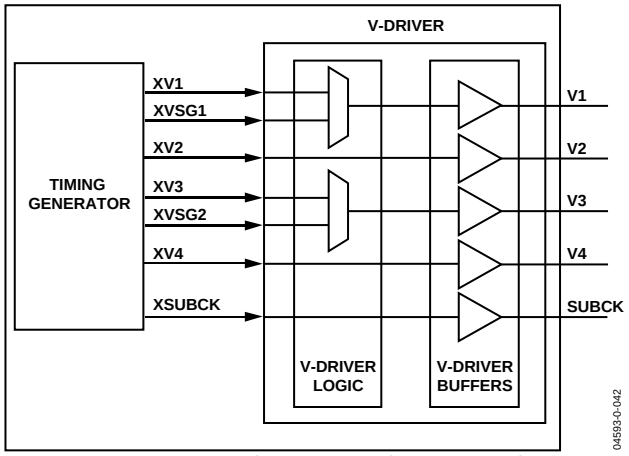


Figure 41. Internal XV1 to XV4 and XSUBCK Signals

Table 28. V1 Output Polarity

V-Driver Input		V1 Output
XV1	**XVSG1**	
L	L	VH1
L	H	VM1
H	L	VL
H	H	VL

Table 29. V2 Output Polarity

V-Driver Input	V2 Output
XV2	
L	VM2
H	VL

Table 30. SUBCK Output Polarity

V-Driver Input	SUBCK Output
XSUBCK	
L	VH2
H	VL

Table 31. V3 Output Polarity

V-Driver Input		V3 Output
XV3	**XVSG2**	
L	L	VH1
L	H	VM1
H	L	VL
H	H	VL

Table 32. V4 Output Polarity

V-Driver Input	V4 Output
XV4	
L	VM2
H	VL

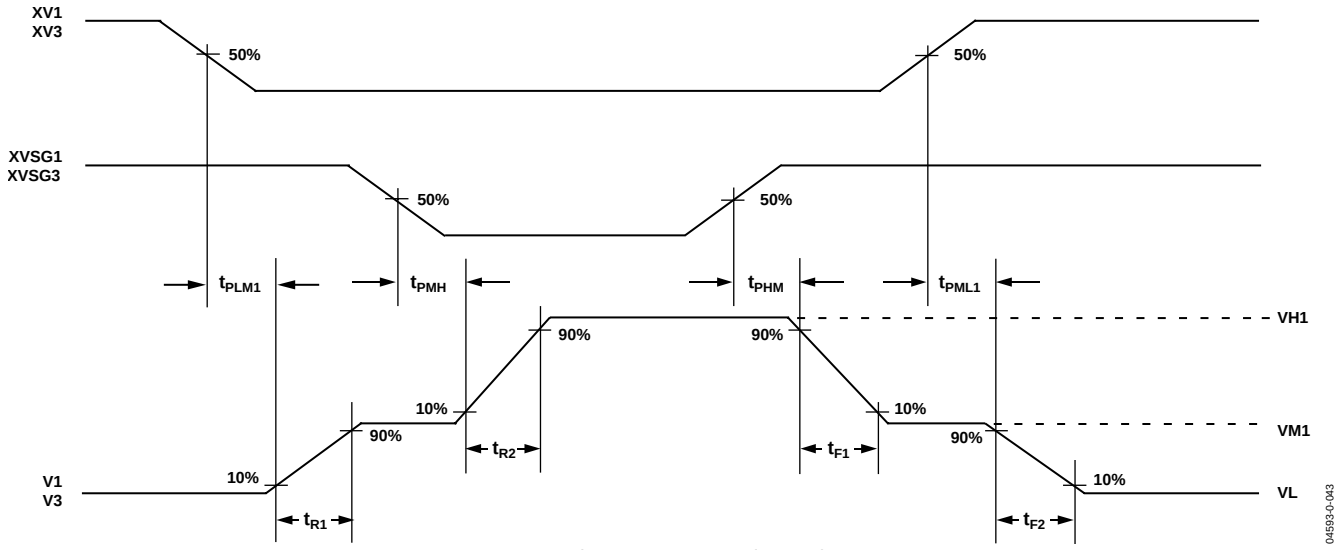


Figure 42. V1 and V3 Transmission Delays and Rise Times

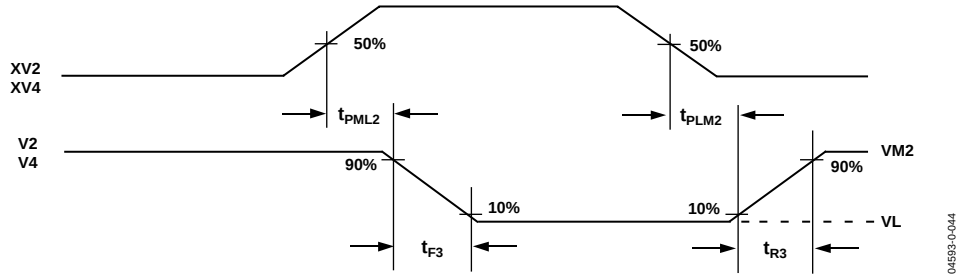


Figure 43. V2 and V4 Transmission Delays and Rise Times

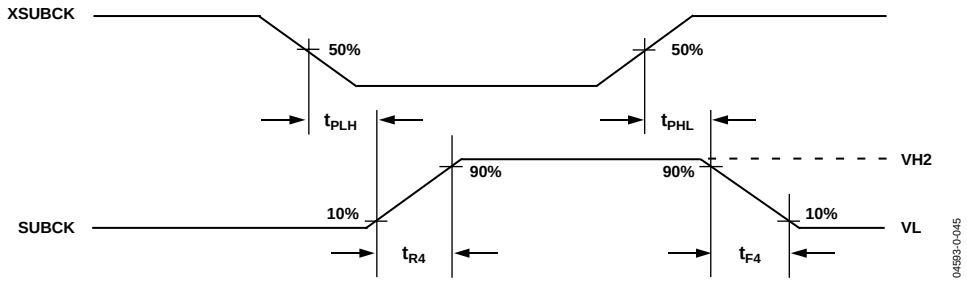


Figure 44. SUBCK Transmission Delays and Rise Times

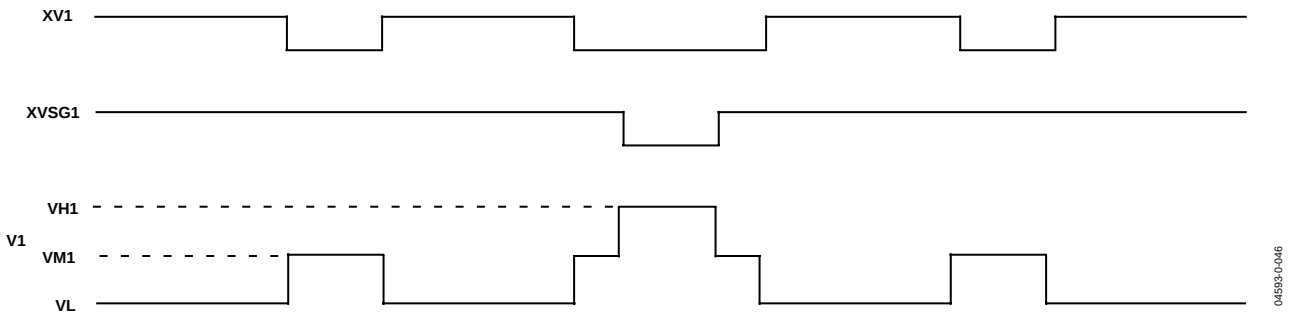


Figure 45. Example Showing V1 Output versus XV1 and XVSG1 Signals

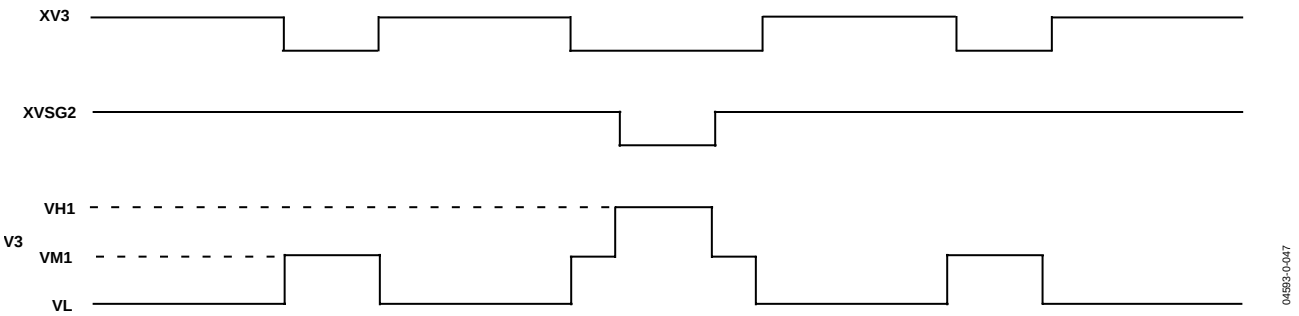


Figure 46. Example Showing V3 Output versus XV3 and XVSG2 Signals

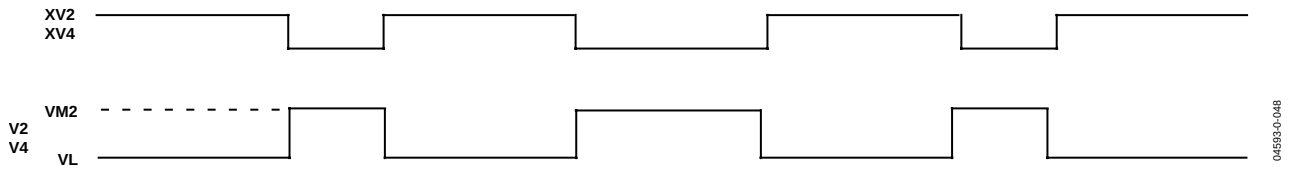


Figure 47. Example Showing V2 and V4 Outputs versus XV2 and XV4 Signals

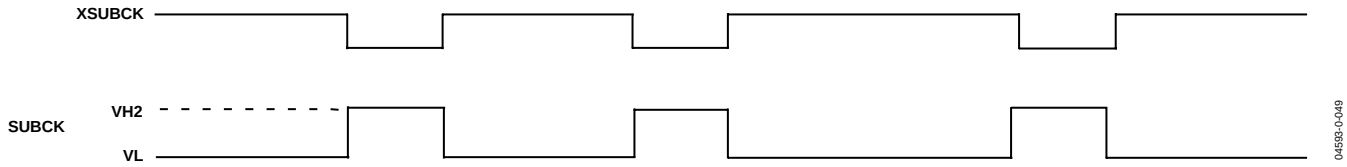


Figure 48. Example Showing SUBCK Output versus XSUBCK Signal

TIMING CONTROL

ELECTRONIC SHUTTER TIMING CONTROL

CCD image exposure time is controlled through the use of the CCD substrate clock signal (XSUBCK), which pulses the CCD substrate to clear out accumulated charges prior to the exposure period. The AD9929 supports three types of electronic shuttering: normal shutter mode, suppression shutter mode, and high speed shutter mode. Table 34 contains the registers required for programming of XSUBCK pulses for each mode.

Normal Shutter Mode

Figure 49 shows the VD and XSUBCK output for normal shutter mode. The XSUBCK pulses once per line. The number of XSUBCK pulses per field can be programmed by setting register XSUBCKNUM (Address 0x0B). As shown in Figure 49, the XSUBCK pulses always begin on the line after the sensor gate, as specified by XVSGACTLINE (Mode_Reg(1)).

SUBCK Suppression Mode

Normally, the XSUBCKs begin to pulse on the line following the last sensor gate line (VSG). With some CCDs, the first XSUBCK following the VSG line needs to be suppressed. The XSUBCKSUPPRESS register allows for this suppression. The first XSUBCK following the last VSG pulse is suppressed when XSUBCKSUPPRESS = 1, as shown in Figure 50.

High Precision Shutter Mode

The high speed shutter mode can be operated in two different modes, known as single pulse mode and multiple pulse mode. These modes are set up by programming the XSUBCKNUM_HP register and XSUBCKMODE_HP register, as described in Table 28, Table 33, and shown in Figure 52 and Figure 54.

Single Pulse Mode

In addition to the normal operating XSUBCK pulse, one additional XSUBCK pulse can be applied within the HD line while operating in this mode. As shown in Figure 49, the location of the additional XSUBCK pulse is adjustable by setting the XSUBCK_HPNUM register as described in Table 33. Finer resolution of the exposure time is possible using this mode by adding an additional XSUBCK pulse in the line, as shown in Figure 54.

Multiple Pulse Mode

In addition to the normal operating XSUBCK pulse, up to seven sequential XSUBCK pulses can be applied within the same line while operating in this mode. As shown in Figure 54, the number of additional XSUBCK pulses is selectable by setting XSUBCKMODE_HP = 1, and the XSUBCK_HPNUM registers as described in Table 33.

Table 33. Single and Multiple Pulse Mode

XSUBCKNUM_HP	XSUBCKMODE_HP	
	0	1
	Single Pulse Mode	Multiple Pulse Mode
0	Normal Shutter Mode Operation	Normal Shutter Mode Operation
1	Position #1	1 additional pulse
2	Position #2	2 additional pulses
3	Position #3	3 additional pulses
4	Position #4	4 additional pulses
5	Position #5	5 additional pulses
6	Position #6	6 additional pulses
7	Position #7	7 additional pulses

Table 34. XSUBCK Registers

Register Name	Bit Width	Register Type	Reference Counter	Range	Description
XSUBCKNUM	11	Control (Address 0x0B)	–	0–2047 Number of Pulses	Number of XSUBCK Pulses per Field.
XSUBCKSUPPRESS	1	Control (Address 0x01)	–	0–1 Number of Pulses	Suppress First XSUBCK after Last XVSG Line Pulse
XSUBCK_EN	1	Control (Address 0x0B)	–	–	XSUBCK Output Enable Control (0 = Disable, 1 = Enable)
XSUBCKMODE_HP	1	Control (Address 0x01)	–	–	High Speed Shutter Mode Operation
XSUBCKNUM_HP	3	Control (Address 0x0B)	–	0–7 Number of Pulses	High Speed Shutter XSUBCLK Position/Number
XSUBCK1TOG1	9	System_Reg(14)	OL Counter	0–511 Pixel Location	XSUBCLK1 1st Toggle Position
XSUBCK1TOG2	9	System_Reg(14)	OL Counter	0–511 Pixel Location	XSUBCLK1 2nd Toggle Position
XSUBCK2TOG1	9	System_Reg(15)	OL Counter	0–511 Pixel Location	XSUBCLK2 1st Toggle Position
XSUBCK2TOG2	9	System_Reg(15)	OL Counter	0–511 Pixel Location	XSUBCLK2 2nd Toggle Position
XSUBCKSEL	1	Mode_Reg(2)	–	–	(0 = XSUBCK1, 1 = XSUBCK2)

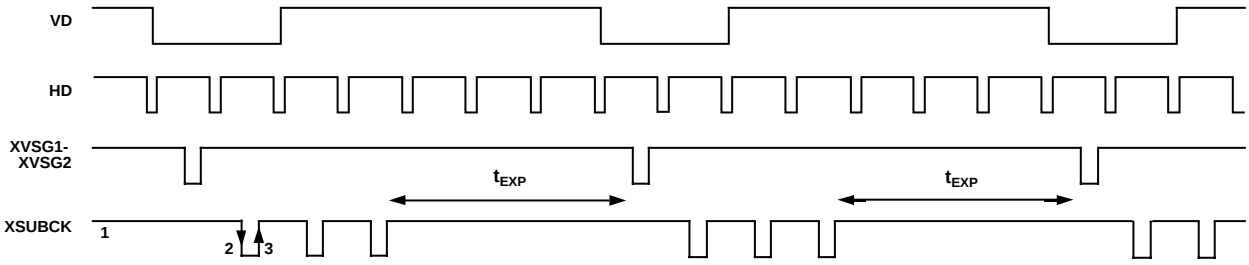


Figure 49. Normal Shutter Mode

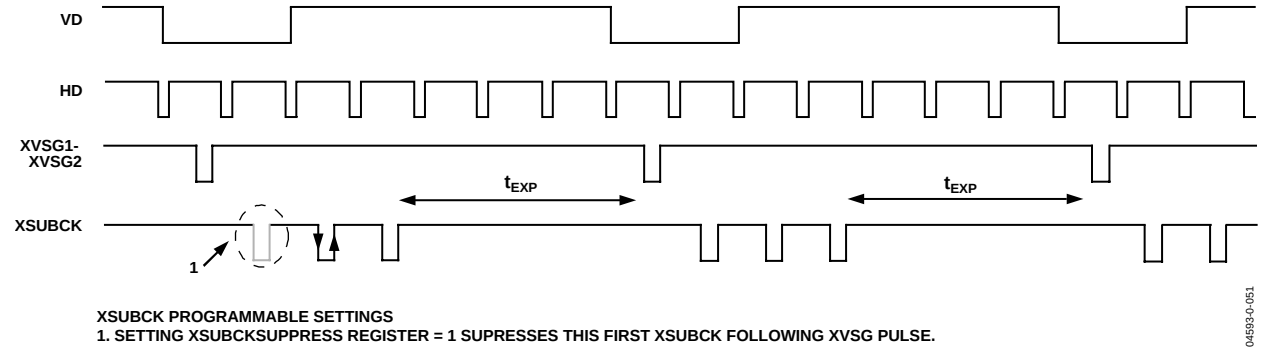


Figure 50. XSUBCK Suppression Mode

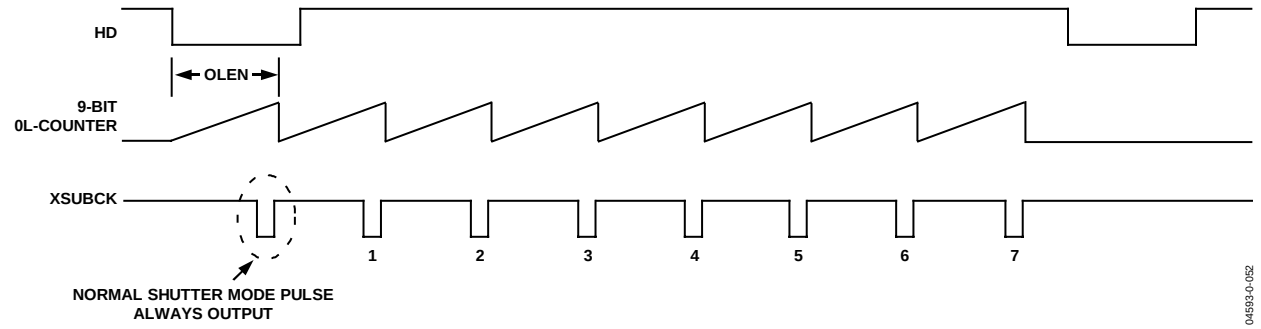


Figure 51. Electronic Shutter Timing

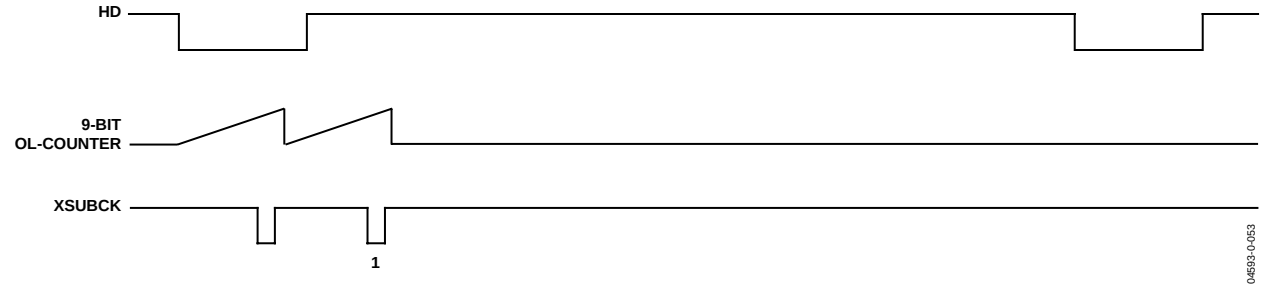


Figure 52. Electronic Shutter Timing Example with XSUBCKMODE_HP = 0 and XSUBCKNUM_HP = 1

VSG TIMING

The VSG Timing is controlled using the registers in Table 35. Two unique preprogrammed VSG pulses can be configured using the XVSGTOG_x (x = 0, 1) registers. As shown in Figure 55, the period of the VSG pulse is set by programming the XVSGLEN_x registers. The XVSGSELx (x = 1, 2) can then be used to select the XVSGTOG_0 or XVSGTOG_1 pulse. Figure 55 also shows an example of the XVSG pulse being output in the fourth line by setting the XVSGACTLINE = 3. The XVSG pulses references the 13-bit fixed ST counter, which starts counting from the line set in the XVSGACTLINE register. The 13-bit counter allows for overlapping of the XVSG pulse into the next line if needed.

Figure 53 describes the XVSG1 and XVSG2 MUX operation using the XVSGSELx registers.

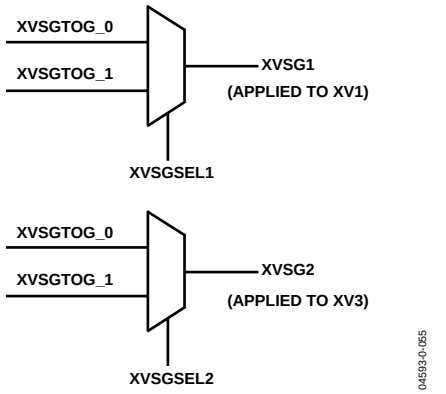


Figure 53. XVSGSELx Registers

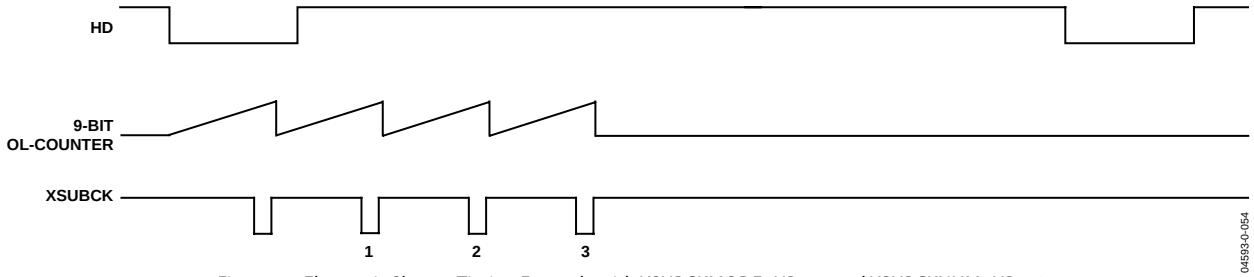
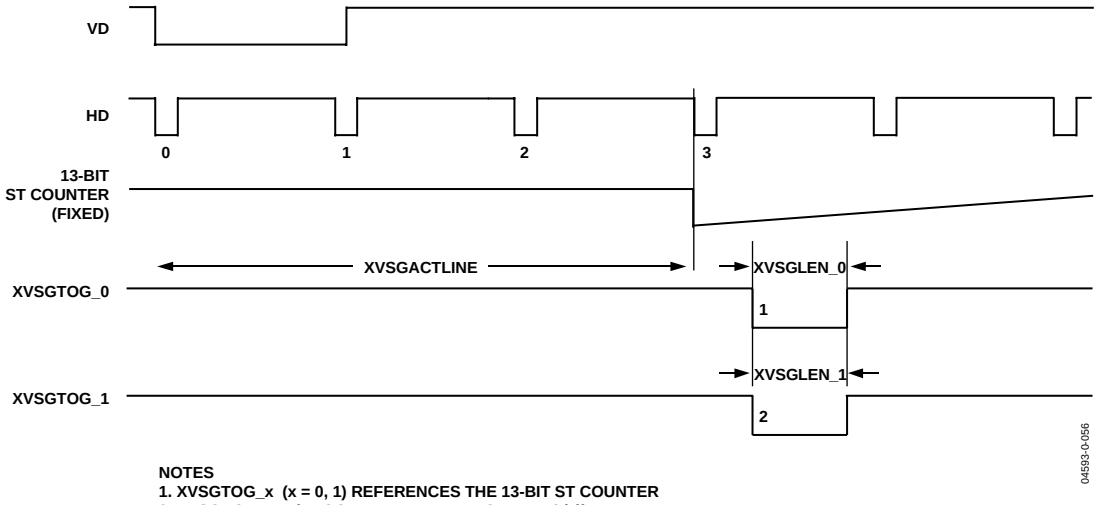


Figure 54. Electronic Shutter Timing Example with XSUBCKMODE_HP = 1 and XSUBCKNUM_HP = 3.

Table 35. VSG Registers

Register Name	Bit Width	Register Type	Reference Counter	Range	Description
XVSGMASK	6	Control (Address 0x0A)	–	–	VSG Mask Control (00 = XVSG1 Masked, XVSG2 Masked) (02 = XVSG1 Not Masked, XVSG2 Masked) (08 = XVSG1 Masked, XVSG2 Not Masked) (0A= XVSG1 Not Masked, XVSG2 Not Masked)
XVSG_EN	1	Control (Address 0x0B)	–	High/Low	XVSG Output Enable Control (0 = Disable XVSG Outputs, 1 = Enable XVSG Outputs)
XVSGTOG_0	11	Sys_Reg(13)	ST	0–8191 Pixels	XVSGTOG_0 Toggle Position
XVSGTOG_1	11	Sys_Reg(13)	ST	0–8191 Pixels	XVSG TOG_1 Toggle Position
XVSGLEN_0	8	Sys_Reg(14)	ST	0–255 Pixels	XVSGTOG_0 Pulse Width
XVSGLEN_1	8	Control (Address 0x0F)	ST	0–255 Pixels	XVSGTOG_1 Pulse Width
XVSGSEL1	1	Mode_Reg(1)	–	High/Low	XVSG1 Selector (0 = XVSGTOG_0 Applied on XVSG1, 1 = XVSGTOG_1 Applied on XVSG1)
XVSGSEL2	1	Mode_Reg(1)	–	High/Low	XVSG2 Selector (0 = XVSGTOG_0 Applied on XVSG2, 1 = XVSGTOG_1 Applied on XVSG2)
XVSGACTLINE	7	Mode_Reg(1)		0–128 Lines	VSG Active Line



NOTES
1. XVSGTOG_x (x = 0, 1) REFERENCES THE 13-BIT ST COUNTER
2. XVSGACTLINE (PROGRAMMABLE AT MODE_REG(1))
3. XVSGLEN (PROGRAMMABLE AT SYS_REG(14))

PROGRAMMABLE CLOCK POSITIONS
1. XVSGTOG_0 (PROGRAMMABLE AT SYS_REG(13))
2. XVSGTOG_1 (PROGRAMMABLE AT SYS_REG(13))

Figure 55. Example of VSG Pulse

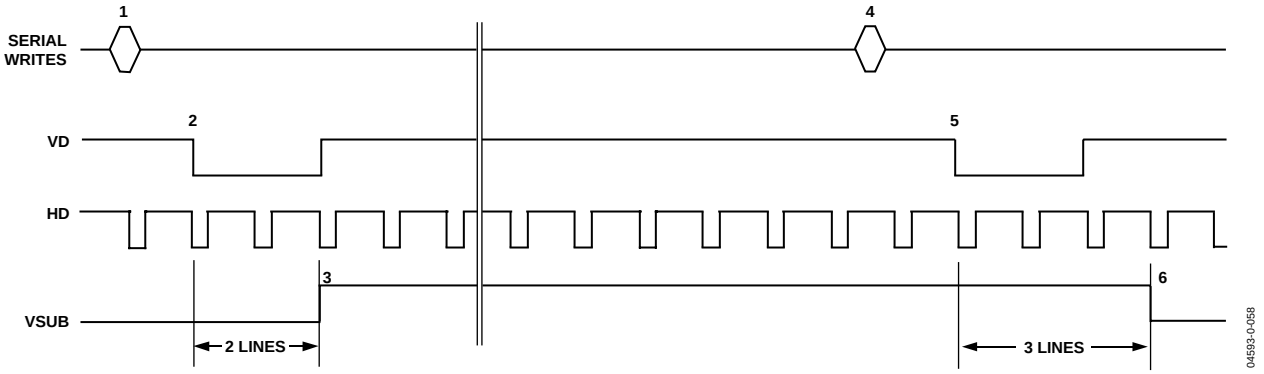


Figure 56. VSUB Timing Example

VSUB TIMING

The CCD readout bias (VSUB) can be programmed to accommodate different CCDs. VSUB on and off toggle positions and polarity are controlled using VSUBTOG (Address 0x0D) and VSUBPOL (Address 0x0D) registers, respectively, as described in Table 36. Since the VSUBTOG is an 11-bit register, the VSUB on position is programmable within any line. Figure 56 shows an example of controlling VSUB using these registers.

Table 36. VSUB Registers

Register Name	Bit Width	Register Type	Range (Lines)	Description
VSUBPOL	1	Control	–	(0 = Low, 1 = High)
VSUBTOG	11	Control	0–2048	VSUB toggle position

VSUB Placement and Polarity

Figure 56 shows the sequence of events for programming the VSUB on and off toggle positions and polarity.

1. Program VSUBTOG = 2 and VSUBPOL = 1.
2. Since the VSUBTOG and VSUBPOL are VD synchronous type registers, the falling edge of VD updates the serial writes from Step 1.
3. VSUB is asserted high after two HD cycles.
4. Program VSUBTOG = 3 and VSUBPOL = 0.
5. Since the VSUBTOG and VSUBPOL are VD synchronous type registers, the falling edge of VD updates the serial writes from Step 4.
6. VSUB is asserted low after three HD cycles.

MSHUT TIMING

MSHUT Basic Operation

The AD9929 provides an MSHUT output pulse that can be configured to control the mechanical shutter of the camera. The registers used to control the MSHUT pulse are listed in Table 37.

The MSHUT pulse can be placed at the start of any line by using the 11-bit MSHUTPOS register. The MSHUT pulse width is controlled by using the MSHUTLEN register. The AD9929 offers four preprogrammed MSHUT patterns that are selectable using the MSHUTPAT register.

The preprogrammed length is the same for all patterns set by the MSHUTLEN register, but the active on period of the MSHUT pulse is different for each pattern, as shown in Figure 57. Figure 58 shows an example of selecting MSHUTPAT0 positioned to start 3 lines after the falling edge of VD, with MSHUTLEN = 5.

Table 37. MSHUT and STROBE Registers

Register Name	Bit Width	Register Type	Description
MSHUTPAT	2	Control (Address 0x01)	Selects MSHUT Pattern. (0 = MSHUTPAT0, 1 = MSHUTPAT1, 2 = MSHUTPAT2, 3 = MSHUTPAT3)
MSHUTINIT	1	Control (Address 0x0C)	MSHUT Initialize (1 = MSHUT Output Held Low, 0 = Normal Operation Resumes)
MSHUTEN	1	Control (Address 0x0C)	MSHUT Control (0 = MSHUT Held at Last State, 1 = MSHUT Output Enabled for Normal Operation)
MSHUTPOS	11	Control (Address 0x0C)	MSHUT Position during Normal Operation
MSHUTPOS_HP	3	Control (Address 0x0C)	MSHUT Position during High Precision Operation
MSHUTLEN	8	Sys_Reg(13)	MSHUT Pattern Length.
STROBE_EN	1	Control (Address 0x0B)	STROBE Output Enable Control (0 = STROBE Output Held Low, 1 = Enable STROBE Output)

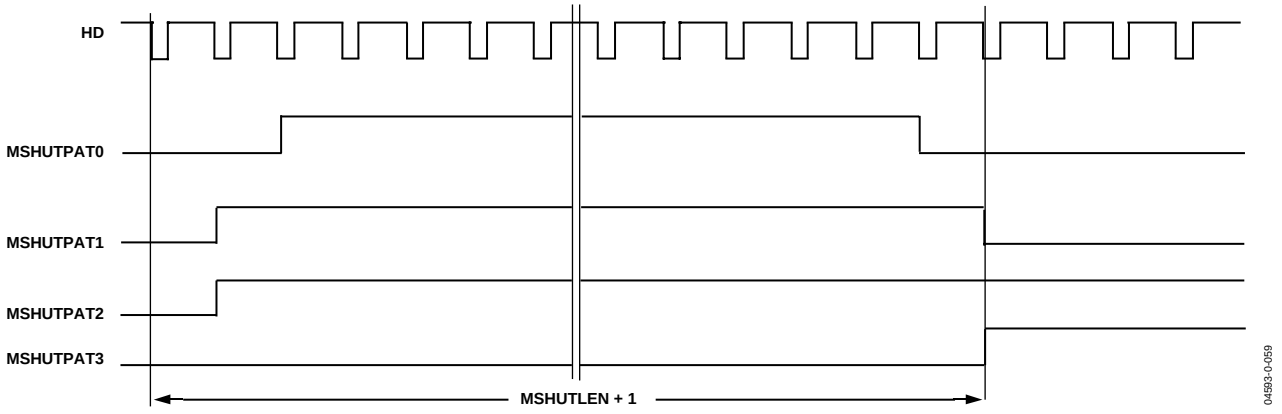


Figure 57. MSHUT Patterns Available by Setting MSHUTPAT Register

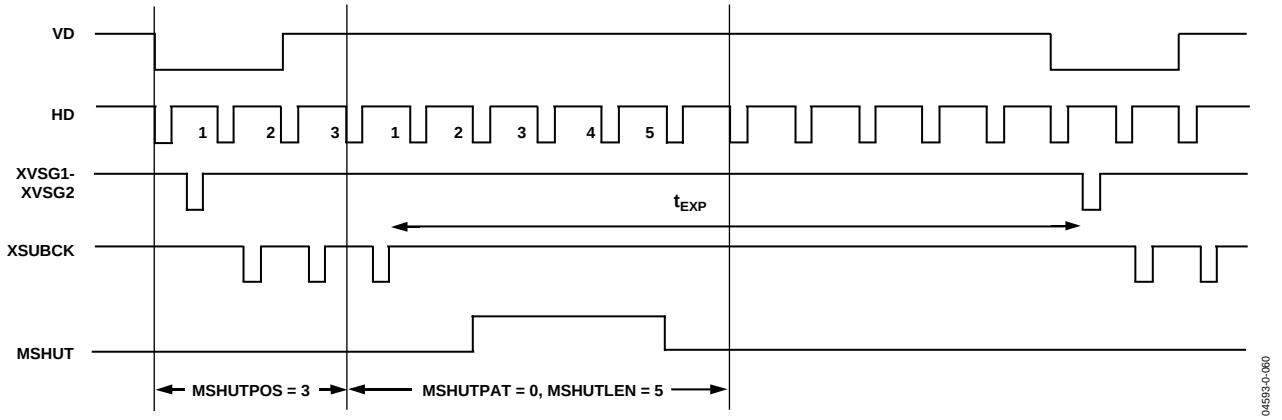


Figure 58. Example of MSHUT Timing with MSHUTEN = 1 and MSHUTPOS_HP = 0

MSHUT High Precision Operation

The MSHUTPOS_HP register allows fine precision control of the MSHUT position within a line. Under normal MSHUT operation when MSHUTPOS_HP = 0, the MSHUT polarity changes from high to low on the negative edge of the HD pulse, as shown in Figure 53. By using the MSHUTPOS_HP register, the rising and falling edges of MSHUT can be delayed by multiples of the OL counter length that has been set in the OLEN register. For example, if MSHUTPOS_HP = 3, the MSHUT rising and falling edges are delayed by three OL counter cycles after the falling edge of HD, as shown in Figure 56.

Figure 56 provides an example of high precision MSHUT and SUBCK timing. In this example, the length of the OL counter is shorter. This provides finer precision control of the placement of the MSHUT pulse within a line.

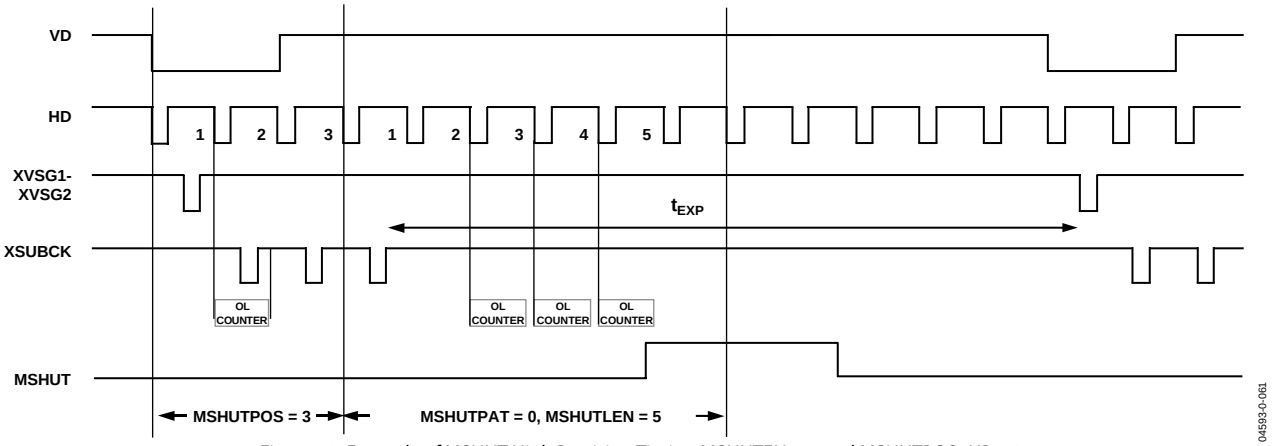


Figure 59. Example of MSHUT High Precision Timing MSHUTEN = 1 and MSHUTPOS_HP = 3

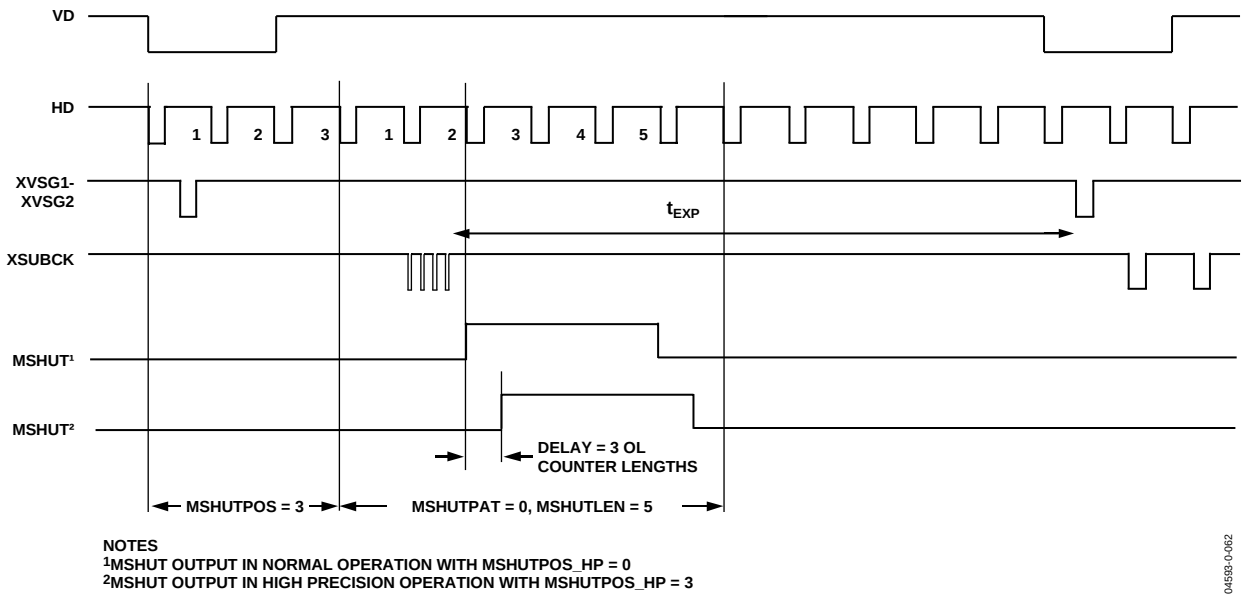


Figure 60. Example of MSHUT High Precision Timing MSHUTEN = 1, MSHUTPOS_HP = 3, with XSUBCKMODE_HP = 1, XSUBCKNUM_HP = 3

STROBE TIMING

The AD9929 provides a STROBE output pulse that can be used to trigger the camera flash circuit. STROBE operation is set by only one register, as described in Table 32. The STROBE output is held low when STROBE_EN (Address 0x0B) is set to 0 and enabled when set to 1. Providing STROBE_EN = 1, the STROBE output pulse is asserted high on the rising edge of the last XSUBCK pulse in the field, as shown in Figure 61. Also shown in Figure 61, the STROBE pulse is asserted low again on the rising edge of VSG.

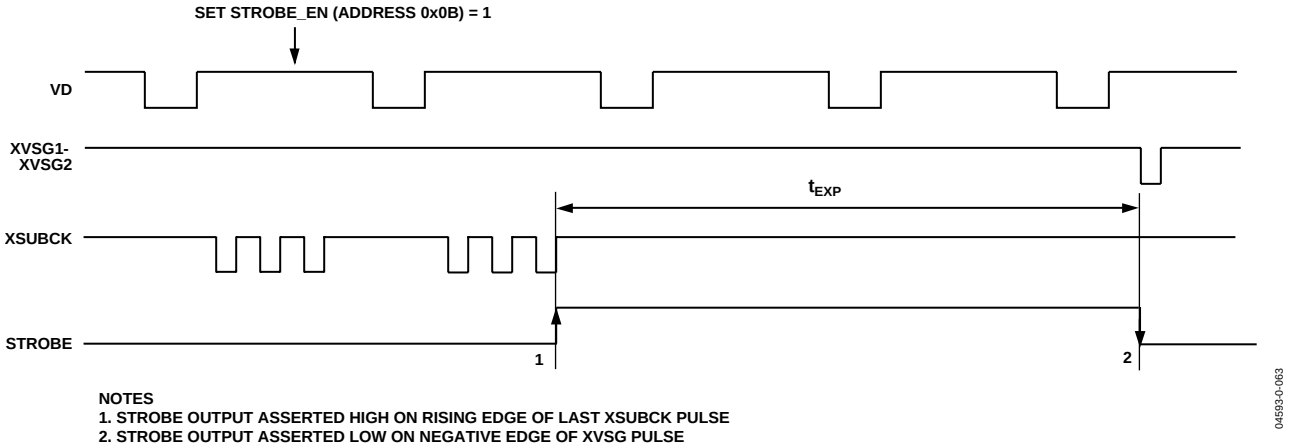


Figure 61. STROBE Output Timing

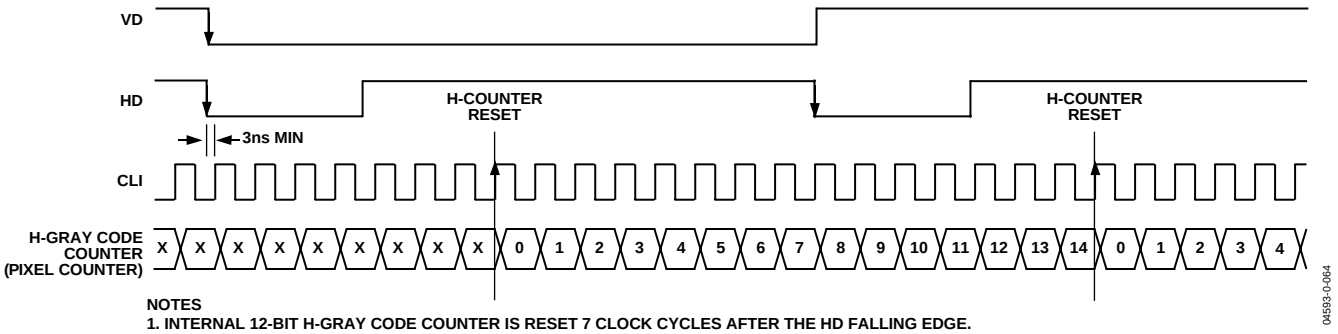


Figure 62. External VD/HD and Internal 12-Bit H-Gray Code Counter Synchronization, Slave Mode

DIGITAL I/O STATES FOR DIFFERENT OPERATING CONDITIONS

Table 38 describes the state of the digital I/Os for different operating conditions.

Table 38. I/O Levels

I/O	OCONT_REG[1] = 0	DIGSTBY
DCLK1	ACTIVE	H
DCLK2	ACTIVE	ACTIVE
VD[2]	H	H
HD[2]	H	H
RG	L	L
H1	H	H
H2	L	L
V1	VL	VL
V2	VL	VL
V3	VL	VL
V4	VL	VL
SUBCK	SUBVDD	VL
STROBE	L	L
MSHUT	L	L
FD	H	L

[1] OUTCONT_REG is a register setting located at Address 0x05. It defaults to 0 at power-up.
[2] VD and HD operate in master mode.

POWER SUPPLY SEQUENCING

The recommended power-up and power-down sequences are shown in Figure 64 and Figure 65, respectively. As shown, the VM1 and VM2 voltage level should never exceed the VH1 and VH2 voltage level during power-up or power-down. Excessive current results if this requirement is not met due to a PN junction diode turning on between the VM1/2 and VH supply pins.

Figure 63 describes the AD9929 AFETG and V-driver supplies associated with vertical driver outputs.

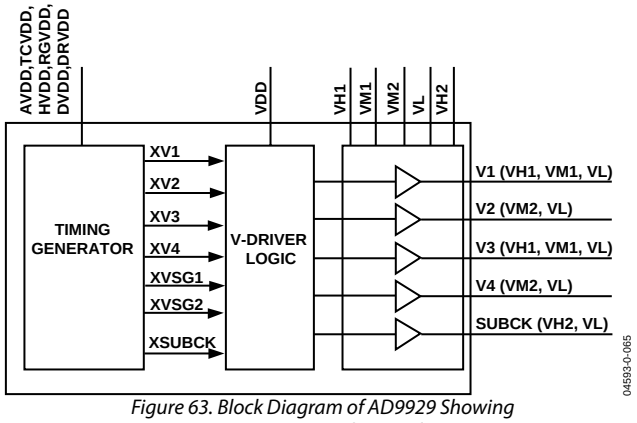


Figure 63. Block Diagram of AD9929 Showing Timing Generator and Vertical Driver

RECOMMENDED POWER-UP SUPPLY SEQUENCING

When the AD9929 is powered up, the following power supply sequence is recommended. Refer to Figure 64.

1. Turn ON: VDD, DVDD, DRVDD, HVDD, RGVDD, TCVDD, and AVDD.
2. Turn ON: VH1 VH2, VM1,VM2, and VL.

Caution:
There is a PN junction diode from VM1 and VM2 to VH. Excessive current occurs if the VM1 and VM2 supply level is greater than VH1 and VH2 supplies.

RECOMMENDED POWER-DOWN SUPPLY SEQUENCING

When the AD9929 is powered down, the following power supply sequence is recommended. Refer to Figure 65.

1. Turn OFF: VH1, VH2, VM1, VM2, and VL.
2. Turn OFF: VDD, DVDD, DRVDD, HVDD, RGVDD, TCVDD, and AVDD.

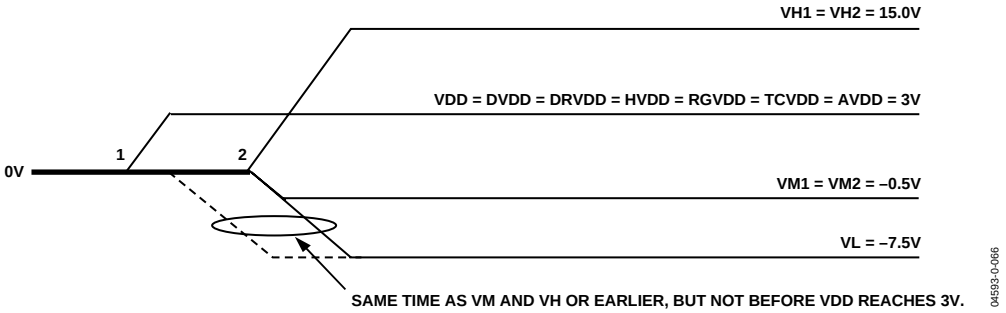


Figure 64. Power-Up Supply Sequencing

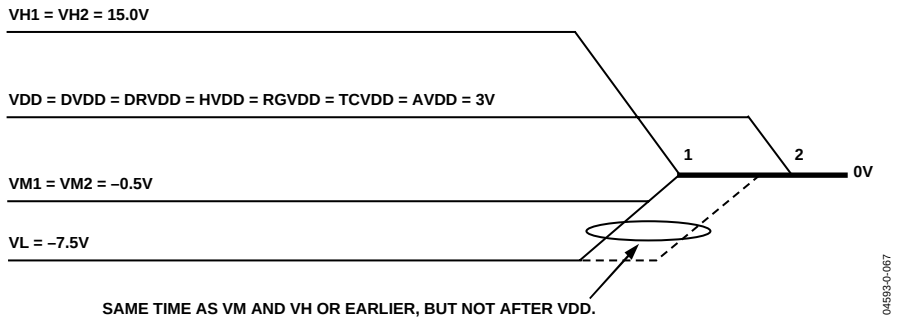


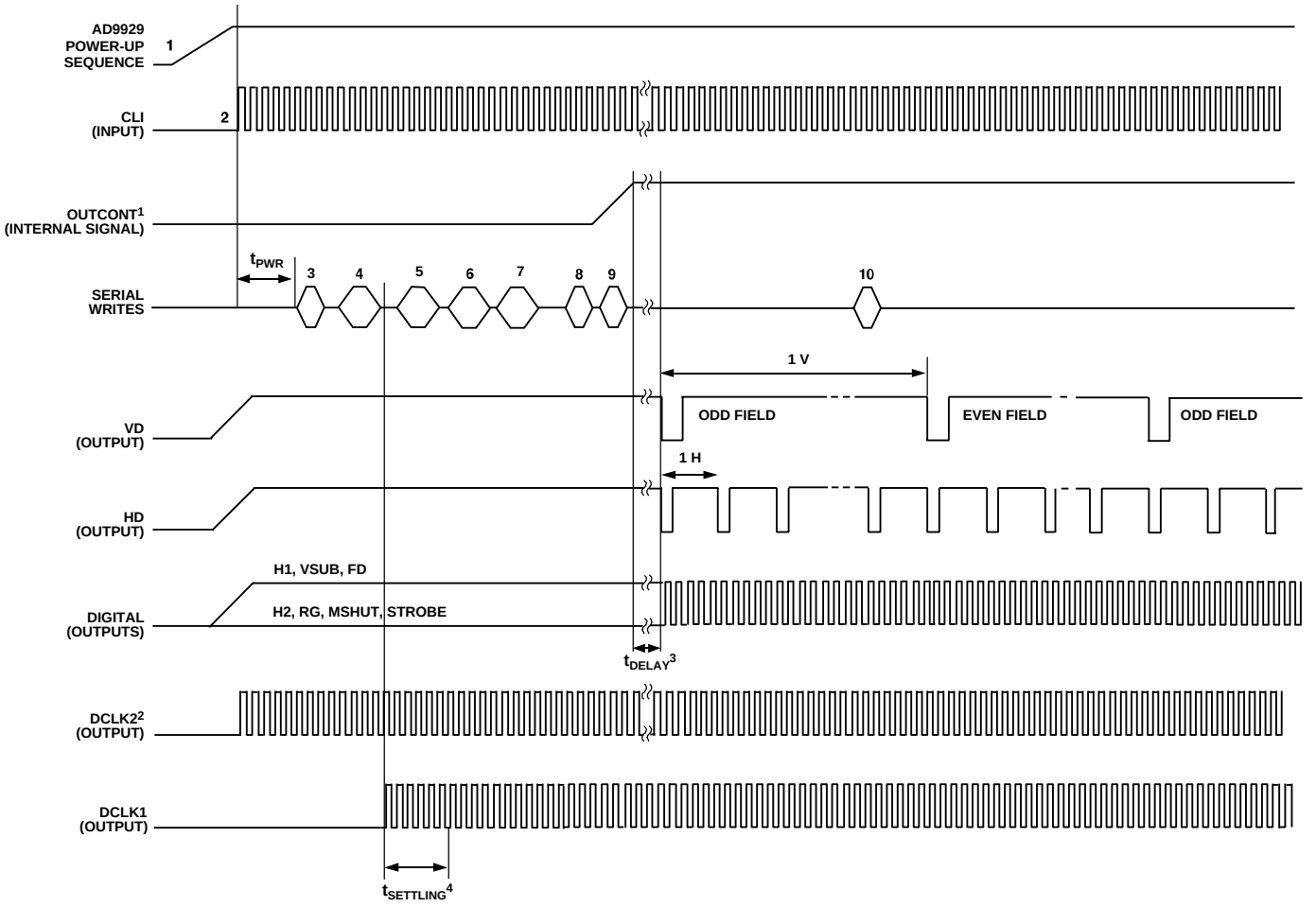
Figure 65. Power-Down Supply Sequencing

INITIAL START-UP SEQUENCE

Recommended Start-Up Sequence for Master Mode

When the AD9929 is powered up, the following sequence is recommended (refer to Figure 66 for each step).

1. Turn on power supplies as described in the Power Supply Sequencing section.
2. Apply the CLI master clock input.
   CLI is output on DCLK2 Pin 16 at this time.
3. Reset the internal AD9929 registers. Write a 0x000000 to the SW_RESET register (Address 0x00). This sets all internal register values to their default values. (This step is optional because there is an internal power-on reset circuit that is applied at power-up.)
4. Program DIGSTBY and AFESTBY registers (Address 0x05) = 1 and all other necessary control registers.
5. Program system registers (Address 0x20).
6. Program Mode_A registers (Address 0x21).
7. Program Mode_B registers (Address 0x22).
8. Program OUTCONT_REG register (Address 0x05) = 1. (The internal OUTCONT signal is asserted high at this time. This enables the digital outputs.)
9. Program control register MODE (Address 0x0A) = 0. This selects Mode_A operation. (This step is optional because the AD9929 defaults to Mode_A at power-up.)
10. Program control register MODE (Address 0x0A) = 1. This selects Mode_B operation. Note: Complete this write at least 4 CLI cycles before the start of the next field.



NOTES
[1]OUTCONT IS AN INTERNAL SIGNAL THAT IS CONTROLLED USING REGISTER OUTCONT_REG (ADDRESS 0x05).
[2]DCLK2 WILL BE OUTPUT ON THE FD/DCLK2 PIN 16 PROVIDING REGISTER DCLK2SEL (ADDRESS 0xD5) = 1. THE DCLK2SEL REGISTER DEFAULTS TO 1 AT POWER-UP.
[3]IT TAKES 11 CLI CLOCKS FROM WHEN OCONT GOES HIGH UNTIL VD, HD, AND DIGITAL OUTPUT DATA IS VALID.
[4]THERE IS A 500µS SETTLING TIME FROM WHEN THE DIGSTBY REGISTER IS SET TO WHEN THE DCLK1 IS STABLE.

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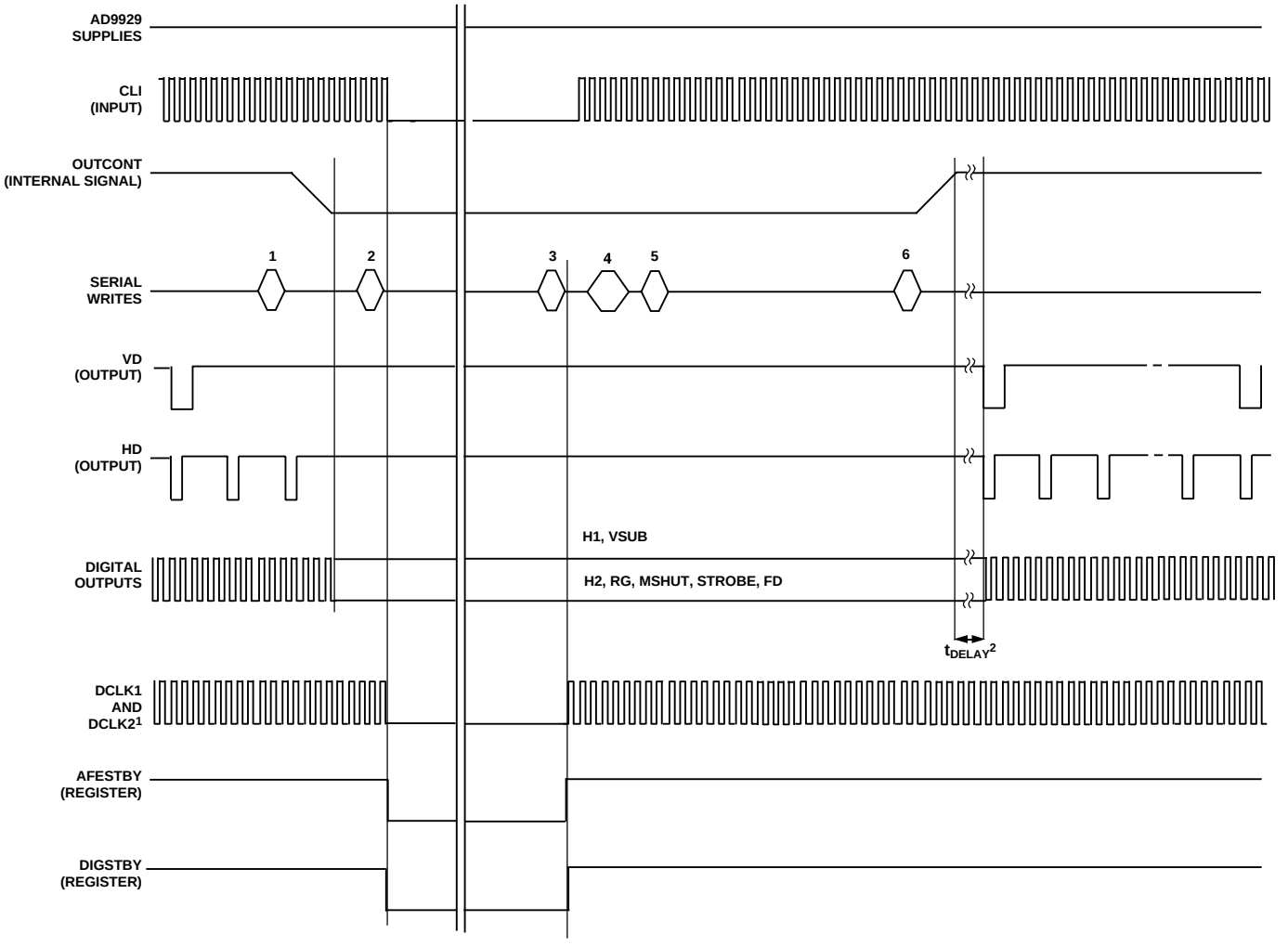
Figure 66. Recommended Start-Up Sequence and Synchronization, Master Mode

STANDBY MODE OPERATION

Recommended Standby Mode Sequence

When the AD9929 is going into standby operation, the following sequence is recommended (refer to Figure 67 for each step).

1. Program OUTCONT_REG (Address 0x05) = 0. This asserts the internal OUTCONT signal low, causing all digital outputs to become disabled.
2. Program registers AFESTBY (Address 0x05) = 0 and DIGSTBY (Address 0x05) = 0. The AD9929 is now in standby operation.
3. When ready to come out of standby operation, program register DIGSTBY (Address 0x05) = 1 and register AFESTBY (Address 0x05) = 1.
4. Program necessary control registers.
5. Program control register MODE (Address 0x0A) = 0. This selects Mode_A operation.
6. Program register OUTCONT_REG (Address 0x05) = 1. This asserts the internal OUTCONT signal high, causing all digital outputs to become active.



NOTES
[1]DCLK2 WILL BE OUTPUT ON THE FD/DCLK2 PIN 16 PROVIDING REGISTER DCLK2SEL (ADDRESS 0xD5) = 1.
[2]IT TAKES 11 CLI CLOCKS FROM WHEN OCONT GOES HIGH UNTIL VD, HD, AND DIGITAL OUTPUT DATA IS VALID.

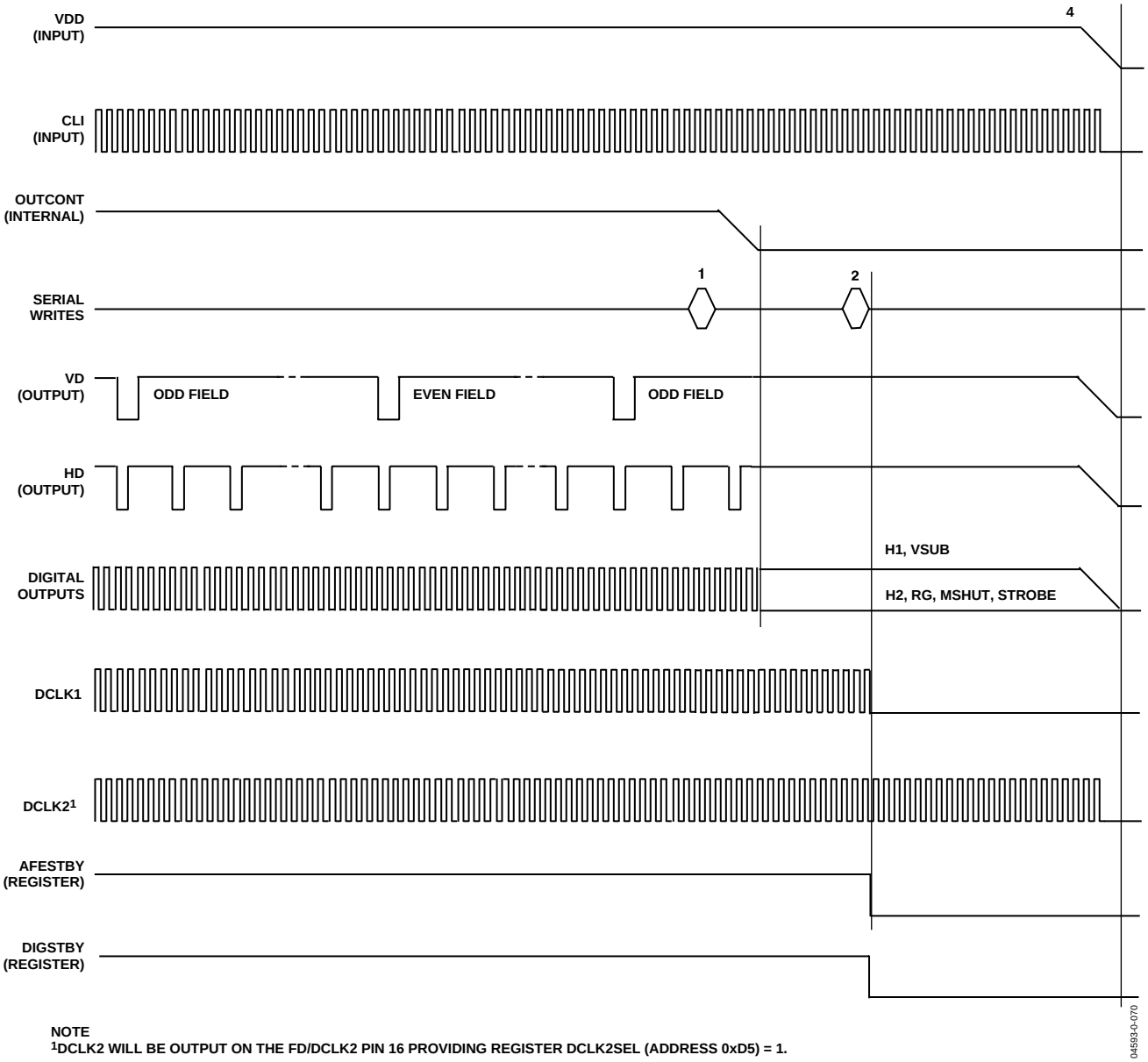
Figure 67. Recommended Standby Sequence

SHUT-DOWN MODE OPERATION

Recommended Power-Down Sequence

When the AD9929 is going to be powered down, the following sequence is recommended (refer to Figure 68 for each step).

1. Program OUTCONT_REG (Address 0x05) = 0.
2. Program registers AFESTBY (Address 0x05) = 0 and DIGSTBY (Address 0x05) = 0.
3. Remove power from AD9929.

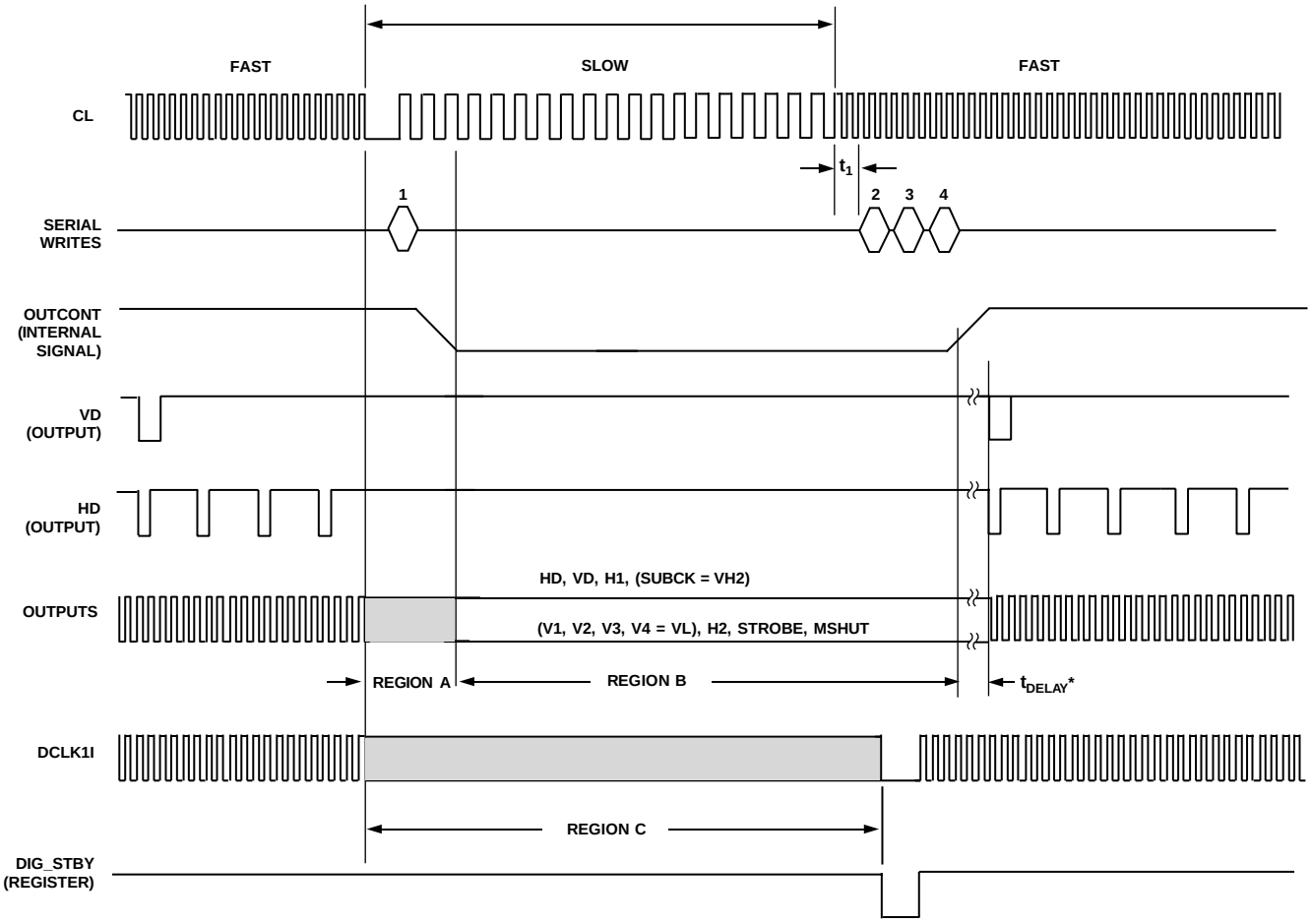


NOTE
[1]DCLK2 WILL BE OUTPUT ON THE FD/DCLK2 PIN 16 PROVIDING REGISTER DCLK2SEL (ADDRESS 0xD5) = 1.

Figure 68. Recommended Shut-Down Sequence

APPLICATIONS WHERE THE CLI CLOCK FREQUENCY CHANGES DURING OPERATION

The AD9929 must be reset, as described in Figure 69, if the CLI clock frequency is changed during operation. The DCLK1 output can become unstable if this reset sequence is not applied after any changes in the CLI clock frequency.



SERIAL PROGRAMMING STEPS MUST BE FOLLOWED WHEN THE CLI CLOCK FREQUENCY CHANGES
1. OUTCONT_REG = 0
2. DIG_STBY = 0
3. DIG_STBY = 1
4. OUTCONT_REG = 1

NOTES ABOUT REGIONS A, B, AND C
[1]DIGITAL OUTPUTS MAY BECOME INVALID IN REGION A
[2]DIGITAL OUTPUTS ARE OUTPUT AS SHOWN IN REGION B
[3]DCLK1 OUTPUT MAY BECOME INVALID IN REGION C
[4]APPLICATIONS SHOULD NOT USE OUTPUT SIGNALS IN REGION C

t_1 = MINIMUM OF 2 CLI CLOCK CYCLES

*IT TAKES 4 CLI CLOCK CYCLES FROM WHEN OUTCONT GOES HIGH UNTIL VD, HD AND DIGITAL OUTPUT DATA IS VALID.

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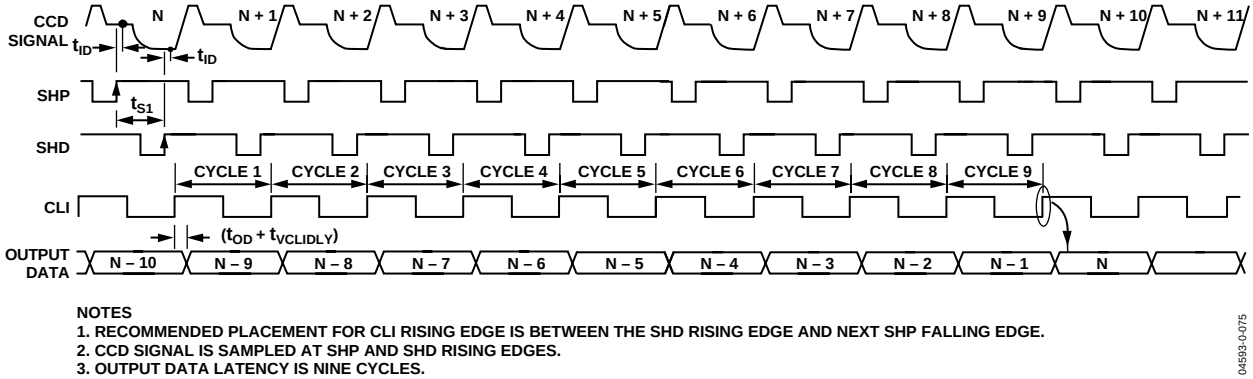
Figure 69. Reset Sequence That Must Be Applied when Changing the CLI Clock Frequency During Operation



NOTES
1. RECOMMENDED PLACEMENT FOR CLI RISING EDGE IS BETWEEN THE SHD RISING EDGE AND NEXT SHP FALLING EDGE.
2. CCD SIGNAL IS SAMPLED AT SHP AND SHD RISING EDGES.
3. OUTPUT DATA LATENCY IS NINE CYCLES.

Figure 70. Output Data Pipeline Delay

CIRCUIT LAYOUT INFORMATION

The AD9929 typical circuit connection is shown in Figure 71. The PCB layout is critical in achieving good image quality from the AD9929 product. All of the supply pins must be decoupled to ground with good quality, high frequency chip capacitors. The 0.1 µF decoupling capacitors should be located as close as possible to the supply pins, and should have a very low inductance path to a continuous ground plane. There should also be a 4.7 µF or larger capacitor for each main supply, although it is not necessary for each individual pin.

In most applications it is easier and recommended to share the same supply for AVDD, DVDD, TCVDD, RGVDD, and HVDD, as long as the individual supply pins are separately bypassed at each supply pin. A separate 3 V supply should be used for DRVDD with this supply pin decoupled to the same ground plane as the rest of the chip. A separate ground for DRVSS is not recommended.

The vertical driver VM supply pins can be connected to individual supplies or to the same supply, depending on the application requirement for the mid-level voltage on the vertical outputs. These pins may also be directly connected to the common ground plane, as shown in Figure 71.

The analog bypass pins, REFB, REFT, should also be carefully decoupled to ground as close as possible to their respective pins. The analog input, CCDIN, capacitor should also be located close to the pin.

The H1, H2, and RG printed circuit board traces should be designed to have low inductance to avoid excessive distortion of the signals. Heavier traces are recommended because of the large transient current demand by the CCD on H1 and H2. If possible, physically locate the AD9929 close to the CCD to reduce the inductance on these lines. As always, the routing path should be as direct as possible from the AD9929 to the CCD. Careful trace impedance considerations must also be made with applications using a flex printed circuit (FPC) connecting the CCD to the AD9929. FPC trace impedances can be controlled by applying a solid uniform ground plane under the H1, H2, and RG traces. This helps minimize the amount of overshoot and ringing on these signals at the CCD inputs.

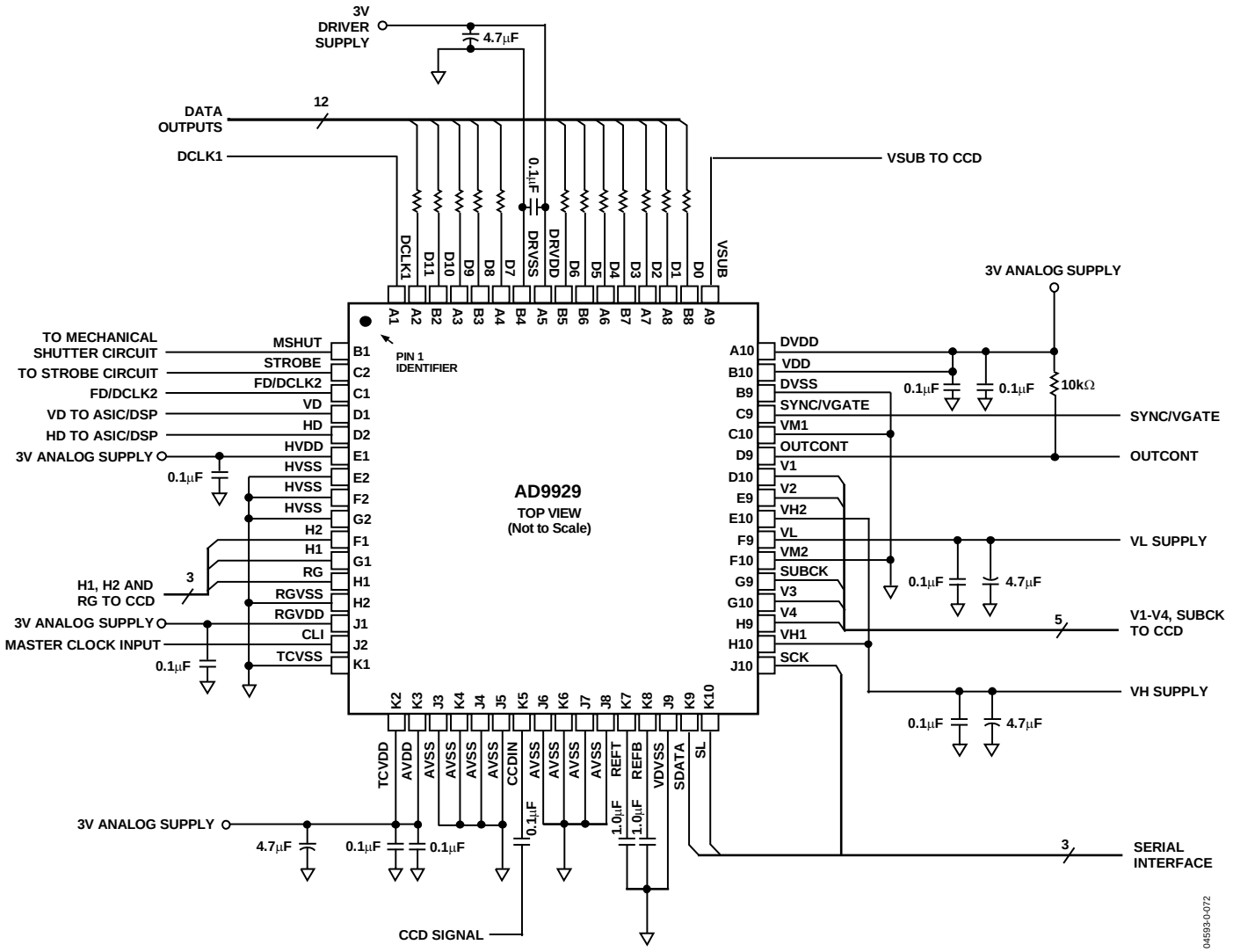


Figure 71. AD9929 Typical Circuit Configuration

OUTLINE DIMENSIONS

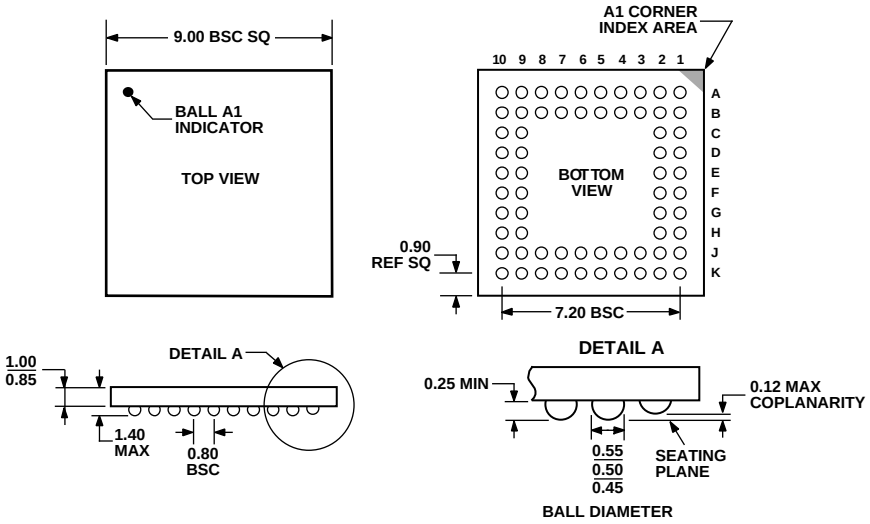


Figure 72. 64-Lead Chip Scale Ball Grid Array [CSPBGA]
(BC-64)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9929BBCZ[1]	−25°C to +85°C	64-Lead Plastic Ball Grid Array	BC-64

[1] Z = Pb-free part.

NOTES

NOTES

D04593-0-1/04(A)