Thermoelectric Cooler (TEC) Controller

Preliminary Technical Data

ADN8831

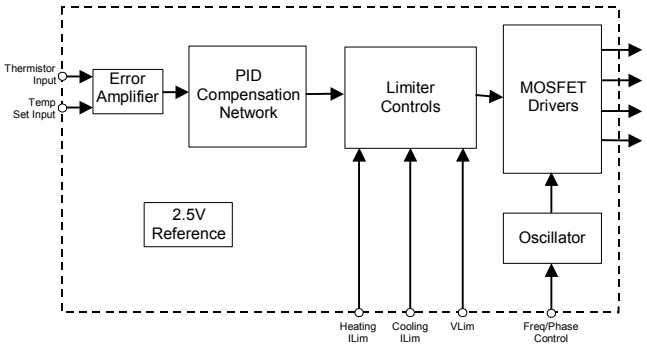
FEATURES

True current sensing and over current protection
Separate heating and cooling current limits
High efficiency: >90%
Long-term temperature stability: 0.1°C
Temperature lock indication
Temperature monitoring output
Oscillator synchronization with an external signal
Clock phase adjustment for multiple controllers
Programmable switching frequency up to 1MHz
Programmable maximum TEC voltage
Low noise: <0.05% TEC current ripple
TEC current monitoring
Compact 5mm x 5mm LFCSP

APPLICATIONS

Thermoelectric Cooler (TEC) temperature control
Resistive heating element control
Temperature-Stabilization Substrate (TSS) control

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADN8831 is a monolithic controller that drives a Thermoelectric Cooler (TEC) to stabilize the temperature of a laser diode or a passive component used in telecommunications equipment.

This device relies on a Negative Temperature Coefficient (NTC) thermistor or a positive temperature coefficient RTD device to sense the temperature of the object attached to the TEC. The target temperature is set with an analog input voltage either from a DAC or with an external resistor divider.

The loop is stabilized by a PID compensation amplifier with high stability and low noise. The compensation network can be adjusted by the user to optimize temperature settling time. The component values for this network can be calculated based on the thermal transfer function of the laser diode or obtained from the look-up table given in the applications notes.

Voltage outputs are provided to monitor both the temperature of the object and the voltage across the TEC. A 2.5V voltage reference is provided for the thermistor temperature sensing bridge.

An external sense resistor provides true current sensing. Current limits for both heating and cooling can be set independently.

Rev. PrC

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REVISION HISTORY

Revision PrC
7/03—Data Sheet Changed from REV PrB to REV PrC.

SPECIFICATIONS

Table 1. ADN8831—Electrical Characteristics (V_+ = 3.0 V to 5.5 V, T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
TEMPERATURE STABILITY						
Long Term Stability		10 kΩ thermistor with α = -4.4% at 25C			0.01	°C
PWM OUTPUT DRIVERS						
Output Transition Time	t_R, t_F	C_L = 3,300 pF		20		ns
Nonoverlapping Clock Delay			50	65		ns
Output Resistance	$R_{O(N1,P1)}$	I_L = 10 mA		6		Ω
Output Voltage Swing	SFB	V_{LIM} = 0 V	0		V_{DD}	V
Output Voltage Ripple	ΔSFB	f_{CLK} = 1 MHz		0.2		%
Output Current Ripple	ΔI_{TEC}	f_{CLK} = 1 MHz		0.2		%
LINEAR OUTPUT AMPLIFIER						
Output Resistance	$R_{O, LNGATE}$ $R_{O, LPGATE}$	I_{OUT} = 2 mA I_{OUT} = 2 mA		85 178		Ω Ω
Output Voltage Swing	LFB		0		V_{DD}	V
POWER SUPPLY						
Power Supply Voltage	V_{DD}		3.0		5.5	V
Supply Current	I_{SY}	PWM not switching -40C ≤ TA ≤ +85		8	12 15	mA mA
Shutdown Current	I_{SD}	SYNCIN/$\overline{SD}$ = 0 V		5		µA
Soft-Start Charging Current	I_{SS}			2		µA
Undervoltage Lockout	UVLO	Low to high threshold		2.5	2.7	V
Standby Current	I_{SB}	SINCIN/$\overline{SD}$ = V_{DD}, SS/SB = 0 V		1		mA
Standby Threshold	V_{SB}	SYNCIN/$\overline{SD}$ = V_{DD}		200	300	mV
ERROR AMPLIFIERS						
Input Offset Voltage	V_{OS1} V_{OS2}	V_{CM1} = 1.5 V, V_{IN1P} – V_{IN1M} V_{CM2} = 1.5 V, V_{IN2P} – V_{IN2M}		10 10	100 100	µV µV
Input Voltage Range	$V_{CM1,2}$		0		V_{DD}	V
Common-Mode Rejection Ratio	$CMRR_{1,2}$			120		dB
Output Voltage Range	$V_{OUT1,2}$		0		V_{DD}	V
Power Supply Rejection Ratio	$PSRR_{1,2}$	3.0 V ≤ V_{DD} ≤ 5.0 V		120		dB
Output Current	$I_{OUT1,2}$		-5		+5	mA
Gain Bandwidth Product	$GBW_{1,2}$			2		MHz
OSCILLATOR						
Sync Range	f_{CLK}	SYNCIN/$\overline{SD}$ connected to external clock	200		1,000	KHz
Oscillator Frequency	f_{CLK}	COMPOSC = V_{DD}, RFREQ = 150kΩ, SYNCIN/$\overline{SD}$ = V_{DD}	800	1,000	1,250	kHz
Free-Run Oscillation Frequency	f_{CLK}	COMPOSC = V_{DD}, SYNCIN/$\overline{SD}$ = V_{DD}	100		1000	KHz
Phase Adjustment Range	Φ_{CLK}	0.1 V ≤ V_{PHASE} ≤ 2.4 V	25		335	°
Phase Adjustment Default	Φ_{CLK}	PHASE = open		180		°
REFERENCE VOLTAGE						
Reference voltage	V_{REF}	I_{REF} < 2mA	2.37	2.47	2.57	V
LOGIC OUTPUTS						
Logic Low Output Level		TEMPGD, SYNCOUT			0.2	V
Logic High Outut Threshold			V_{DD} - 0.2V			V

Table 2. ADN8831—Electrical Characteristics (V_+ = 3.0 V to 5.5 V, T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
TEC CURRENT MEASUREMENT						
ITEC Gain	$A_{V,ITEC}$	$V_{ITEC}/(V_{LFB}-V_{CS})$	98	100	102	V/V
ITEC Output Range	V_{ITEC}		0		V_{DD}	V
ITEC Input Range	$V_{CS, VLFB}$		0		V_{DD}	V
ITEC Bias Voltage	$V_{ITEC, B}$	$V_{LFB} = V_{CS} = 0$	1.2	1.25	1.3	V
ITEC Output Current	$I_{OUT,TEC}$			1		mA
TEC VOLTAGE MEASUREMENT						
VTEC Gain	$A_{V,VTEC}$	$V_{VTEC}/(V_{LFB}-V_{SFB})$	0.23	0.25	0.27	V/V
VTEC Output Range	V_{VTEC}		0		2.5	V
VTEC Bias Voltage	$V_{VTEC,B}$	$V_{LFB} = V_{SFB} = 2.5V$	1.2	1.25	1.3	V
VTEC Output Current	I_{VTEC}			1		mA
VOLTAGE LIMIT						
VLIM Gain	$A_{V,LIM}$	V_{SFB}/V_{VLIM}		5		V/V
VLIM Input Range	V_{VLIM}		0		V_{DD}	V
VLIM Input Current, cooling	$I_{VLIM,COOL}$	$V_{OUT2} < 1.25V$			100	nA
VLIM Input Current, heating	$I_{VLIM,HEAT}$	$V_{OUT2} > 1.25V$		I_{FREQ}		mA
VLIM Input Current Accuracy, heating	$I_{VLIM,HEAT}$	I_{VLIM}/I_{FREQ}	0.9	1.0	1.1	A/A
CURRENT LIMIT						
ILIMC Input Voltage Range	V_{ILIMC}		1.25		V_{DD}	V
ILIMH Input Voltage Range	V_{ILIMH}		0		1.25	V
ILIMC Limit Threshold	$V_{TH,ILIMC}$	$V_{ITEC} = 2.0V$	1.98	2.0	2.02	V
ILIMH Limit Threshold	$V_{TH,ILIMH}$	$V_{ITEC} = 0.5V$	0.48	0.5	0.52	V
TEMPERATURE GOOD						
High Threshold	$V_{OUT1,TH1}$	IN2M tied to OUT2, $V_{IN2P} = 1.5V$		1.525	1.530	V
Low Threshold	$V_{OUT1,TH2}$	IN2M tied to OUT2, $V_{IN2P} = 1.5V$	1.470	1.475		V

ABSOLUTE MAXIMUM RATINGS

Table 3. Absolute Maximum Ratings (at 25°C, unless otherwise noted)

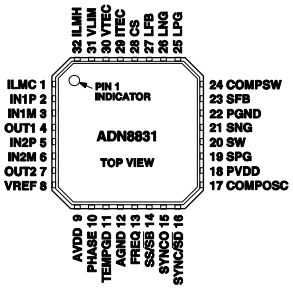
Parameter	Rating
Supply Voltage	6 V
Input Voltage	GND to Vs + 0.3V
Storage Temperature Range	–65°C to +150°C
Operating Temperature Range	–40°C to +85°C
Operating Junction Temperature	125°C
Lead Temperature Range (Soldering, 60 Sec)	300°C

Table 2. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}	Unit
32-lead LFCSP (ACP)	35	10	°C/W

[1] θ_{JA} is specified for the worst-case conditions, i.e., θ_{JA} is specified for device soldered in circuit board for surface mount packages.

Pin Configuration



Pin Descriptions

Pin No.	Mneumonic	Type	Description
1	ILIMC	Analog Input	Analog input sets TEC cooling current protection limit.
2	IN1P	Analog Input	Non-inverting input to error amplifier.
3	IN1M	Analog Input	Inverting input to error amplifier.
4	OUT1	Analog Output	Output of error amplifer.
5	IN2P	Analog Input	Non-inverting input to compensation amplifier.
6	IN2M	Analog Input	Inverting input to compensation amplifier.
7	OUT2	Analog Output	Output of compensation amplifier.
8	VREF	Analog Output	2.5V Voltage Reference output.
9	AVDD	Power	Power for non-driver sections. 3.0 V min; 5.5V max.
10	PHASE	Analog Input	Sets SYNCOUT clock phase relative to SYNCIN clock.
11	TMPGD	Digital Output	Indicates when thermistor temperature is within ±0.01°C if target temperature as set by TEMPSET voltage.
12	AGND	Ground	Analog ground. Connect to low noise ground.
13	FREQ	Analog Input	Sets switching frequency with an external resistor.
14	SS/$\overline{SB}$	Analog Input	Sets soft-start time for output voltage. Pull low to put ADN8831 into standby mode (VTEC = 0V).
15	SYNCO	Digital Output	Phase adjustment clock output. Phase set from PHASE pin. Used to drive SYNCIN of other ADN8831 devices.
16	SYNCI/$\overline{SD}$	Digital Input	Optional clock input. If not connected, clock frequency is set by FREQ pin. Pull low to put ADN8831 into shutdown mode.
17	COMPOSC	Analog Output	Comensation for oscillator; connect capacitor to ground.
18	PVDD	Power	Power for output driver sections. 3.0V min; 5.5V max.
19	SPGATE	Analog Output	Drives PWM output external PMOS gate.
20	SWITCH	Analog Input	Connects to PWM FET drains.
21	SNGATE	Analog Output	Drives PWM output external NMOS gate.
22	PGND	Ground	Power ground. External NMOS devices connect to PGND. Connect to digital ground.
23	SFB	Analog Input	PWM feedback. Typically connects to TEC- pin of TEC.
24	COMPSW	Analog Input	Comensation for switching amplifier.
25	LPGATE	Analog Ouput	Drives linear output external PMOS gate.
26	LNGATE	Analog Output	Drives linear output external NMOS gate.
27	LFB	Analog Input	Linear feedback. Will typically connect to TEC+ pin of TEC.
28	CS	Analog Input	Connect to output current sense resistor.
29	ITEC	Analog Ouput	Indicates TEC current.
30	VTEC	Analog Ouput	Indicates TEC voltage.
31	VLIM	Analog Input	Sets maximum TEC voltage.
32	ILIMH	Analog Input	Sets TEC heating current protection limit.

DETAILED BLOCK DIAGRAM

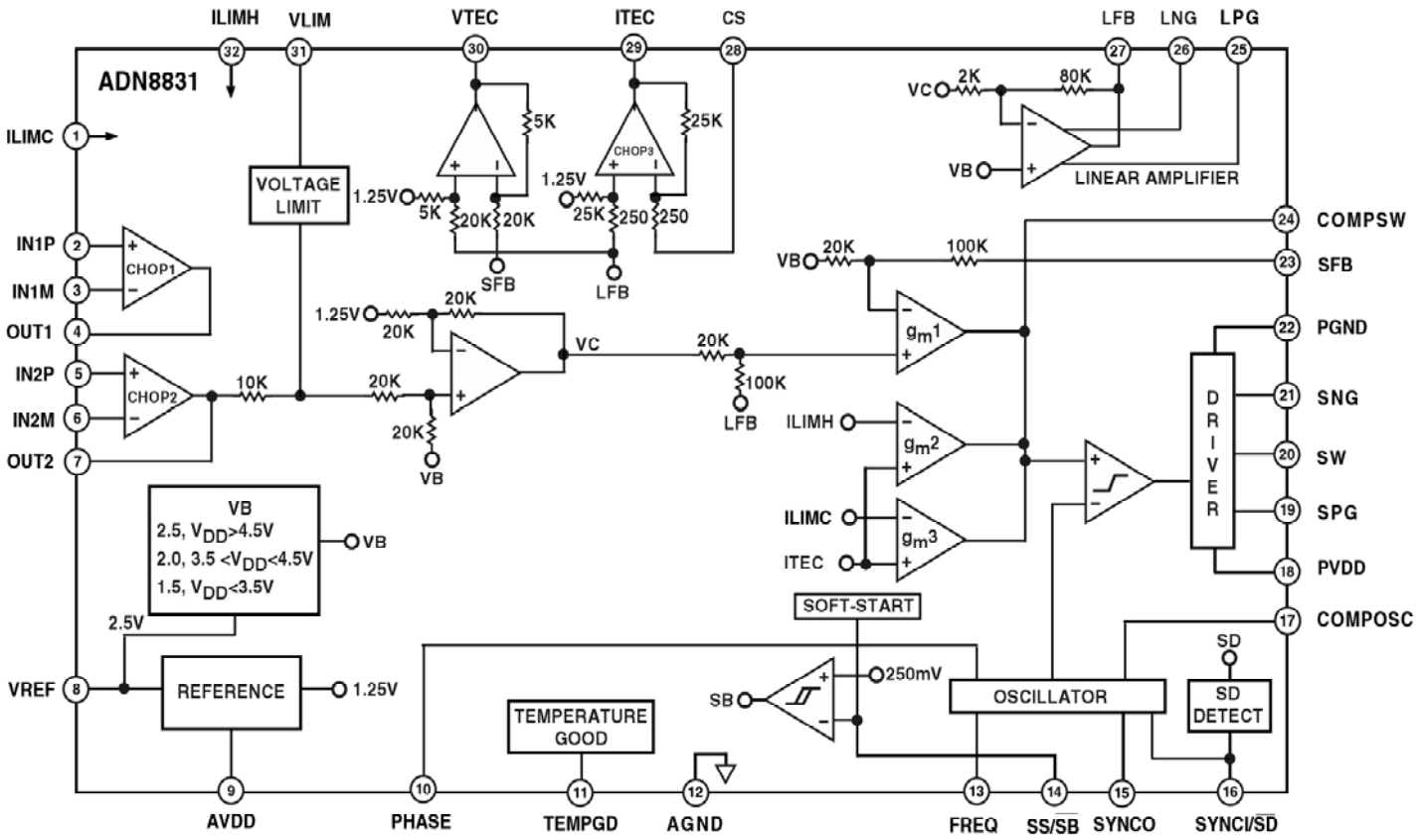


Figure 2. Detailed Block Diagram

TYPICAL APPLICATION CIRCUIT

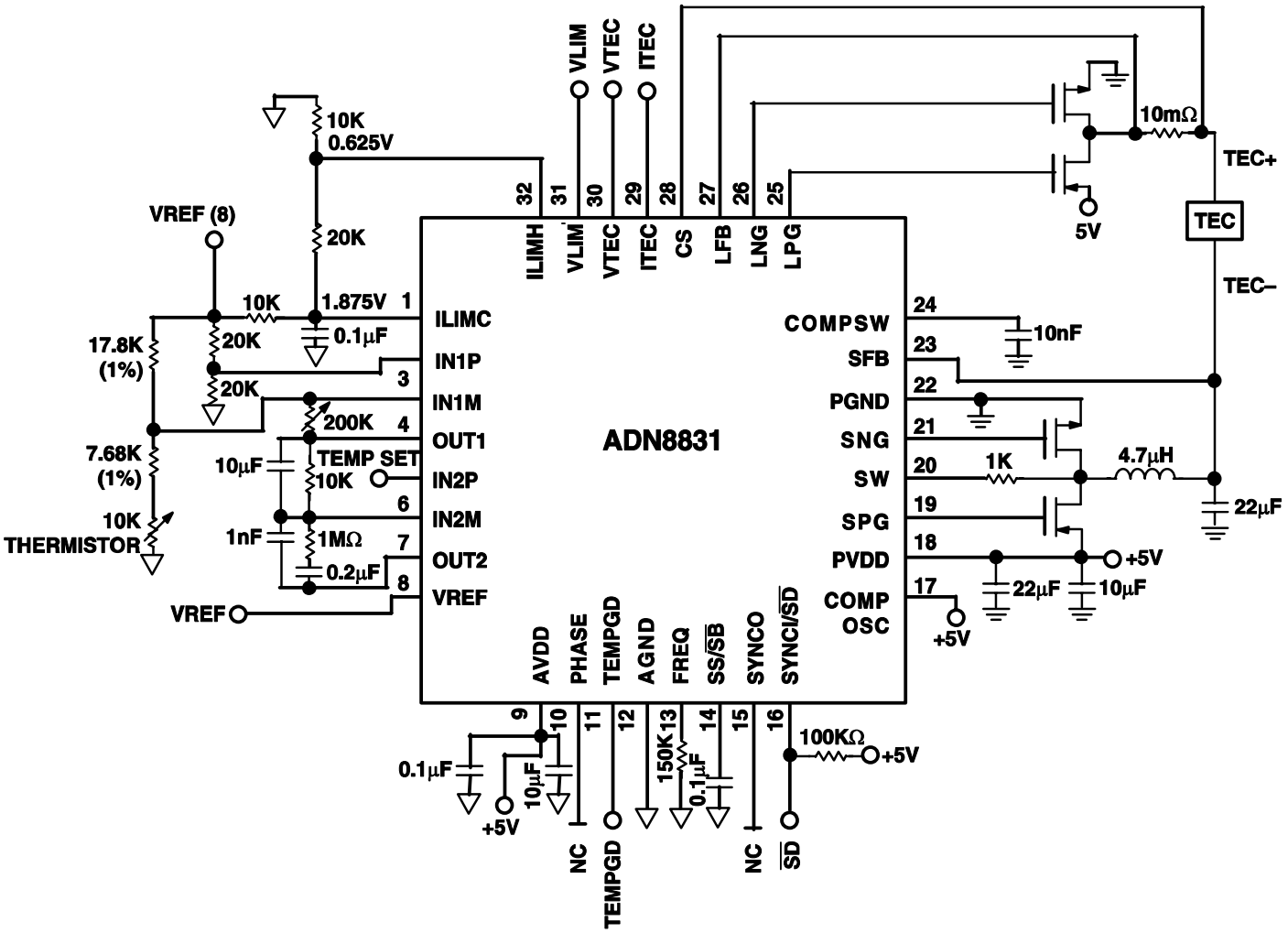


Figure 3. Typical Application Circuit I

THEORY OF OPERATION

Introduction

The ADN831 is a thermoelectric cooler (TEC) controller used to set and stabilize the temperature of the TEC. A voltage applied to the input of the ADN8831 corresponds to a target temperature set-point. Using a thermistor to monitor the current temperature of the target object, the ADN8831 applies the appropriate current to the TEC to pump heat either towards or away from the target object until the set-point temperature is reached.

Self correcting auto-zero amplifiers (chop1 and chop2) are used in the input and compesation stages of the aDN8831 to provide a maximum offset voltage of 100uV over time and temperature. This results in a final temperature accuracy of 0.01C in typical applications, eliminating the ADN8831 as an error source in the temperature control loop.

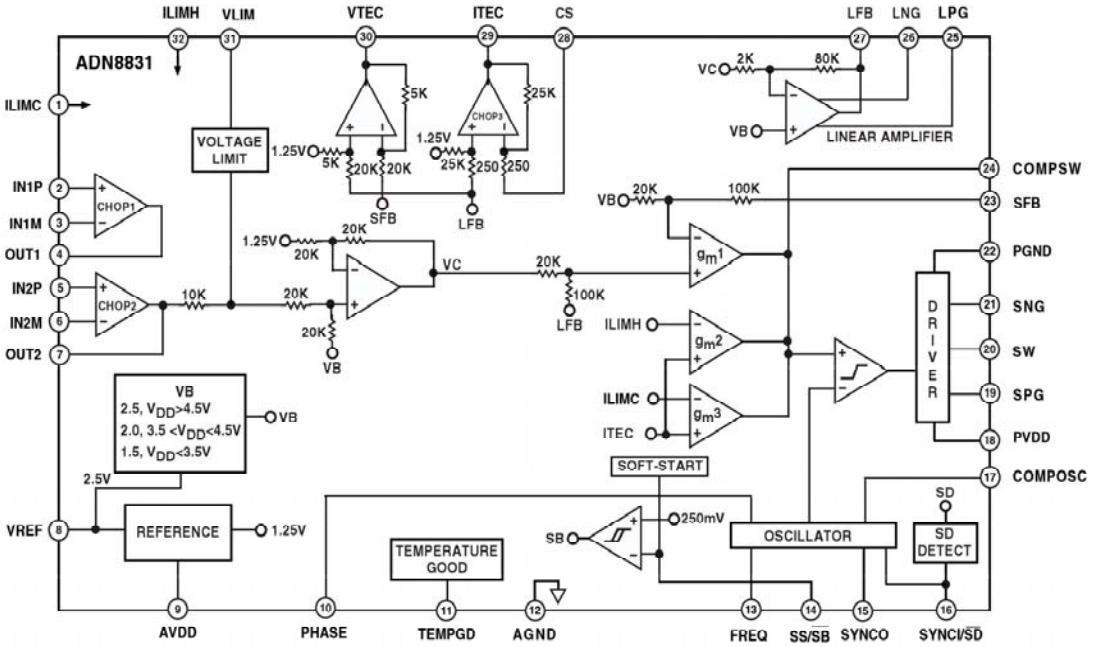
The TEC is driven differentially using an H-bridge configuration. The ADN8831 drives external transistors that are used to provide the current to the TEC. The maximum voltage across the TEC and current flowing through the TEC can be set using the VLIM and ILIM pins. Additional details are provided in the Setting Voltage and Current Limits section.

One side of the H-bridge uses a switched output, while the other is linear. This proprietary configuration allows the ADN8831 to provide efficiency of >90%, while minimizing external filtering component count. The ADN8831 requires only one inductor and one capacitor to filter the switching frequency of the switched output. For most applications, a 4.7uH inductor, a 22uF capacitor and a switching frequency of 1MHz maintains less than 0.5% worst-case output voltage ripple across the TEC.

The switched output is controlled by the ADN8831's oscillator. A single resistor on the FREQ pin (pin #13) sets the switching frequency from 100kHz to 1MHz. The clock output is available at the SYNCO pin (pin #15). Connecting SYNCO to the SYNI pin of another ADN8831 allows multiple ADN8831s to be driven using a single clock.

The clock phase can be changed using a simple resistor divider at the PHASE pin)pin #10). Phase adjustment allows two or more ADN8831 devices to operate from the same clock frequency and not have all outputs switch simultaneously, which could create excessive power supply ripple. Details of how to adjust the clock frequency and phase are provided in the Setting the Frequency section.

The logic output of the TEMPGD pin (pin #11) indicates when the target temperature is reached. Shutdown, standby, and true current-sensing are also provided by the ADN8831 to protect from catastrophic system failures that could damage the TEC.



OUTLINE DIMENSIONS

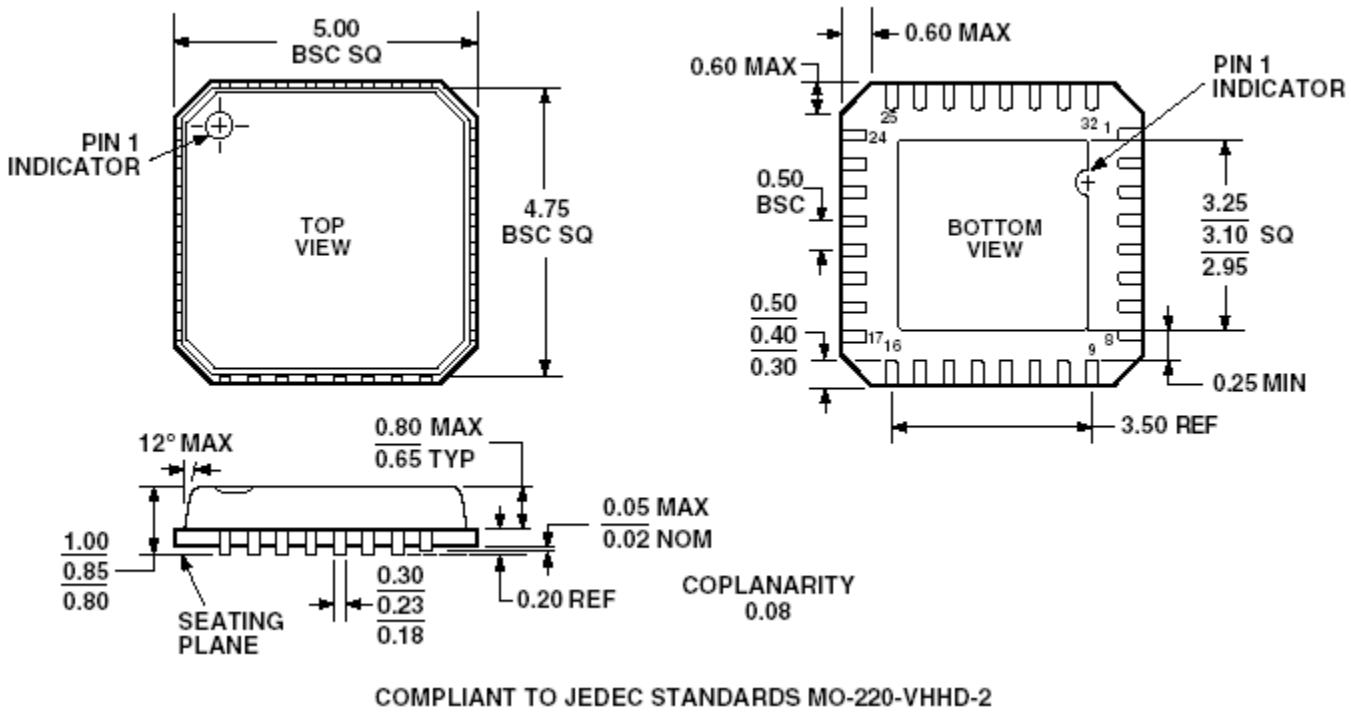


Figure 1. 32-Lead Lead Frame Chip Scale Package [LFCSP]
(CP-32)
Dimensions Shown in Millimeters

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although these products feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ORDERING GUIDE

Table 3.

Model	Temperature Range	Package Description	Package Option
ADN8831ACP	-40°C to +85°C	32-Lead Lead Frame Chip Scale Package	CP-32
ADN8831-EVAL	-40°C to +85°C	Evaluation Board	

PR04663-0-2/04(PrC)