12-Bit 400 MSPS A/D Converter

AD12400

FEATURES

400 MSPS sample rate
SNR of 63 dBFS @128 MHz
SFDR of 70 dBFS @128 MHz
VSWR of 1:1.5
Wideband ac-coupled input signal conditioning
Enhanced spurious-free dynamic range
Single-ended or differential encode signal
LVDS output levels
Twos complement output data

APPLICATIONS

Communications test equipment
Radar and satellite subsystems
Phased array antennas—digital beam forming
Multichannel, multimode receivers
Secure communications
Wireless and wired broadband communications
Wideband carrier frequency systems

GENERAL DESCRIPTION

The AD12400 is a 12-bit analog-to-digital converter with a transformer-coupled analog input and digital post processing for enhanced SFDR. The product operates at a 400 MSPS conversion rate with outstanding dynamic performance in wideband carrier systems.

The AD12400 requires 3.8 V analog, 3.3 V digital, and 1.5 V digital supplies and provides a flexible encode signal that can be differential or single-ended. No external reference is required.

The AD12400 package style is an enclosed 2.9" × 2.6" × 0.6" module. Performance is rated over a 0°C to 60°C case temperature range.

FUNCTIONAL BLOCK DIAGRAM

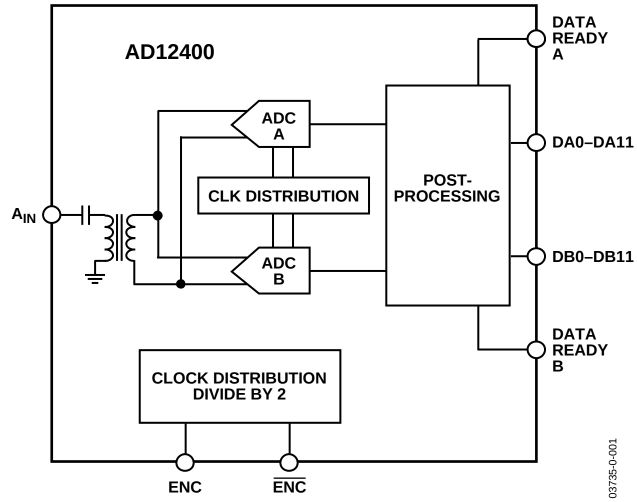

Figure 1.

PRODUCT HIGHLIGHTS

1. Guaranteed sample rate of 400 MSPS.
2. Input signal conditioning with optimized dynamic performance to 180 MHz.
3. Additional performance options available—contact factory.
4. Proprietary Advanced Filter Bank™ digital post processing from VCorp® Technologies, Inc.

Rev. 0

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REVISION HISTORY

Revision 0: Initial Version

SPECIFICATIONS

DC SPECIFICATIONS

Table 1. VA = 3.8 V, VC = 3.3 V, VD = 1.5 V, Encode = 400 MSPS, 0°C ≤ T_{CASE} ≤ 60°C, unless otherwise noted.

			AD12400JWS			AD12400KWS			
Parameter	**Case Temp**	**Test Level**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION				12			12		Bits
ACCURACY									
No Missing Codes	Full	IV		Guaranteed			Guaranteed		
Offset Error	Full	I	−12		+12	−12		+12	LSB
Gain Error @ 10 MHz	Full	I	−10		+10	−10		+10	%FS
Differential Nonlinearity (DNL)	60°C	V		0.3			0.3		LSB
Integral Nonlinearity (INL)	60°C	V		0.5			0.5		LSB
TEMPERATURE DRIFT									
Gain Error	60°C	V		0.02			0.02		%/°C
ANALOG INPUT (AIN)									
Full-Scale Input Voltage Range	60°C	V		3.2			3.2		V p-p
Frequency Range	Full	IV	10		180	10		180	MHz
Flatness (10 MHz-180 MHz)	Full	IV		0.5	1		0.5	1	dB
Input VSWR (50 Ω)	60°C	V		1.5			1.5		
(10 MHz–180 MHz)									
Analog Input Bandwidth	60°C	V		450			450		MHz
POWER SUPPLY[1]									
Supply Voltage									
VA	Full	IV	3.6		3.8	3.6		3.8	V
VC	Full	IV	3.2		3.4	3.2		3.4	V
VD	Full	IV	1.475		1.575	1.475		1.575	V
Supply Current									
I_{VA} (VA = 3.8 V)	Full	I		0.95	1.11		0.95	1.11	A
I_{VC} (VC = 3.3 V)	Full	I		400	500		400	500	mA
I_{VD} (VD = 1.5 V)	Full	I		1.4	1.8		1.4	1.8	A
Total Power Dissipation	Full	I		7.0	8.5		7.0	8.5	W
ENCODE INPUTS[2]									
Differential Inputs (ENC, $\overline{ENC}$)									
Input Voltage Range	Full	IV	0.4			0.4			V
Input Resistance	60°C	V		100			100		Ω
Input Capacitance	60°C	V		4			4		pF
Common-Mode Voltage	60°C	V		±3			±3		V
Single-Ended Inputs (ENC)									
Input Voltage	Full	IV	0.4	2	2.5	0.4	2	2.5	V p-p
Input Resistance	60°C	V		50			50		Ω
LOGIC INPUTS ($\overline{RESET}$)[3]									
Logic 1 Voltage	Full	IV	2.0			2.0			V
Logic 0 Voltage	Full	IV			0.8			0.8	V
Source I_{IH}	60°C	V		10			10		µA
Source I_{IL}	60°C	V		1			1		mA
LOGIC OUTPUTS									
(DRA, DRB, Output Bits)[4]									
Differential Output Voltage	Full	IV	247		454	247		454	mV

			AD12400JWS			AD12400KWS			
LOGIC OUTPUTS									
Output Drive Current	Full	IV	−4		+4	−4		+4	mA
Output Common-Mode Voltage	Full	IV	1.125		1.375	1.125		1.375	V
Start-Up Time	Full	IV		600			600		ms

[1] Tested using input frequency of 70 MHz. See Figure 17 for I(VD) variation vs. input frequency.
[2] All ac specifications tested by driving ENC single-ended.
[3] Refer to Table 5 for logic convention on all logic inputs.
[4] Digital Output Logic Levels: DR V = 3.3 V, C_{LOAD} = 8 pF. 3.3 V LVDS R1 = 100 Ω.
Specifications subject to change without notice.

AC SPECIFICATIONS[1]

Table 2. VA = 3.8 V, VC = 3.3 V, VD = 1.5 V, Encode = 400 MSPS, 0°C ≤ T_{CASE} ≤ 60°C, unless otherwise noted.

			AD12400JWS			AD12400KWS			
Parameter	**Case Temp**	**Test Level**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
DYNAMIC PERFORMANCE[2]									
SNR									
Analog Input @ −1.0 dBFS 10 MHz	Full	I	62	64.4		62	64.4		dBFS
70 MHz	Full	I	61.5	64		61.5	64		dBFS
128 MHz	Full	I	60	63.5		60	63.5		dBFS
180 MHz	Full	I	60	62.5		60	62.5		dBFS
SINAD[3]									
Analog Input @ −1.0 dBFS 10 MHz	Full	I	61	64		61	64		dBFS
70 MHz	Full	I	60.5	64		60.5	64		dBFS
128 MHz	Full	I	59	62.5		59	62.5		dBFS
180 MHz	Full	I	57	61		57	61		dBFS
Spurious-Free Dynamic Range[3]									
Analog Input @ −1.0 dBFS 10 MHz	Full	I	69	80		69	80		dBFS
70 MHz	Full	I	69	84		69	84		dBFS
128 MHz	Full	I	67	76		67	76		dBFS
180 MHz	Full	I	62	71		62	71		dBFS
Image Spur[4]									
Analog Input @ −1.0 dBFS 10 MHz	Full	I	60	75		62	75		dBFS
70 MHz	Full	I	60	72		62	72		dBFS
128 MHz	Full	I	56	70		62	70		dBFS
180 MHz	Full	I	54	70		62	70		dBFS
Offset Spur[4]	60°C	V		65			65		dBFS
Analog Input @ −1.0 dBFS									
Two-Tone IMD[5]									
F1, F2 @ −6 dBFS	60°C	V		−75			−75		dBc
SWITCHING SPECIFICATIONS									
Conversion Rate[6]	Full	IV	396	400	404	396	400	404	MSPS
Encode Pulsewidth High (t_{EH})[1]	60°C	V		1.25			1.25		ns
Encode Pulsewidth Low (t_{EL})[1]	60°C	V		1.25			1.25		ns
DIGITAL OUTPUT PARAMETERS									
Valid Time (t_V)	Full	IV	1.9	2.4	3.1	1.9	2.4	3.1	ns
Propagation Delay (t_{PD})	60°C	V		1.20			1.20		ns
Rise Time (t_R) (20% to 80%)	60°C	V		1			1		ns
Fall Time (t_F) (20% to 80%)	60°C	V		1			1		ns

Parameter	Case Temp	Test Level	AD12400JWS Min	AD12400JWS Typ	AD12400JWS Max	AD12400KWS Min	AD12400KWS Typ	AD12400KWS Max	Unit
DR Propagation Delay (t_{EDR})	60°C	V		3.88			3.88		ns
Data to DR Skew ($t_{EDR} - t_{PD}$)	60°C	V		2.68			2.68		ns
Pipeline Latency[7]	Full	IV		40			40		Cycles
Aperture Delay (t_A)	60°C	V		1.6			1.6		ns
Aperture Uncertainty (Jitter, t_J)	60°C	V		0.4			0.4		ps rms

[1] All ac specifications tested with a single-ended 2.0 V p-p ENCODE.
[2] Dynamic performance guaranteed for analog input frequencies of 10 MHz to 180 MHz.
[3] Not including image spur.
[4] Image spur will be at fs/2–A_{IN} and the offset spur will be at fs/2.
[5] F1 = 70 MHz, F2 = 73 MHz.
[6] Parts are tested with 400 MSPS encode. Device can be clocked at lower encode rates, but specifications are not guaranteed. Specifications will be guaranteed by design for encode 400 MSPS ± 1%.
[7] Pipeline latency will be exactly 40 cycles.

EXPLANATION OF TEST LEVELS

- I 100% production tested.
- II 100% production tested at 25°C and sample tested at specified temperatures.
- III Sample tested only.
- IV Parameter is guaranteed by design and characterization testing.
- V Parameter is a typical value only.
- VI 100% production tested at 25°C; guaranteed by design and characterization testing for industrial temperature range; 100% production tested at temperature extremes for military devices.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Value
VA to AGND	5 V
VC to DGND	4 V
VD to DGND	1.65 V
Analog Input Voltage	6 V (DC)
Analog Input Power	18 dBm (AC)
Encode Input Voltage	6 V (DC)
Encode Input Power	12 dBm (AC)
Logic Inputs and Outputs to DGND	5 V
Storage Temperature Range, Ambient	−65°C to +150°C
Operating Temperature	0°C to 60°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Table 4. Output Coding (Twos Complement)

Code	AIN (V)	Digital Output
4095	+1.6	0111 1111 1111
.	.	.
.	.	.
.	.	.
2048	0	0000 0000 0000
2047	−0.000781	1111 1111 1111
.	.	.
.	.	.
0	−1.6	1000 0000 0000

Table 5. Option Pin List With Necessary Associated Circuitry

Pin Name	Active High or Low	Logic Level Type	Default Level	Associated Circuitry Within Part
$\overline{\text{RESET}}$	Low	LVTTL	High	3.74 kΩ Pull-Up
LEAD/LAG	Low	LVTTL	Low	10 kΩ – 60 kΩ Pull-Down

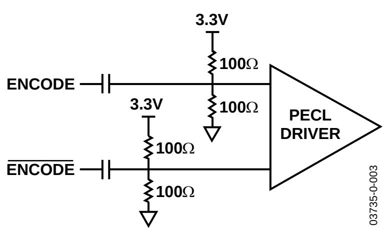

Figure 2. Encode Equivalent Circuit

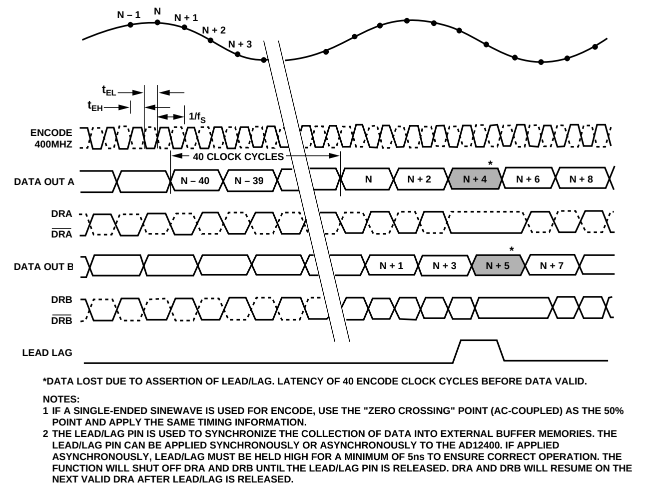

Figure 3. Timing Diagram

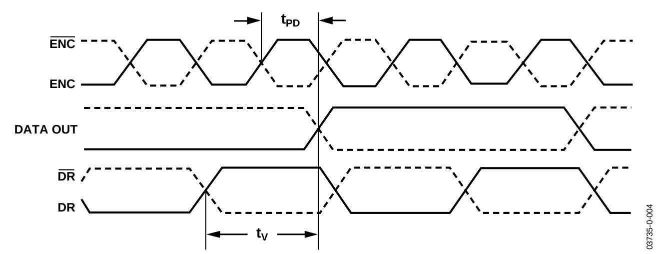

Figure 4. Highlighted Timing Diagram

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

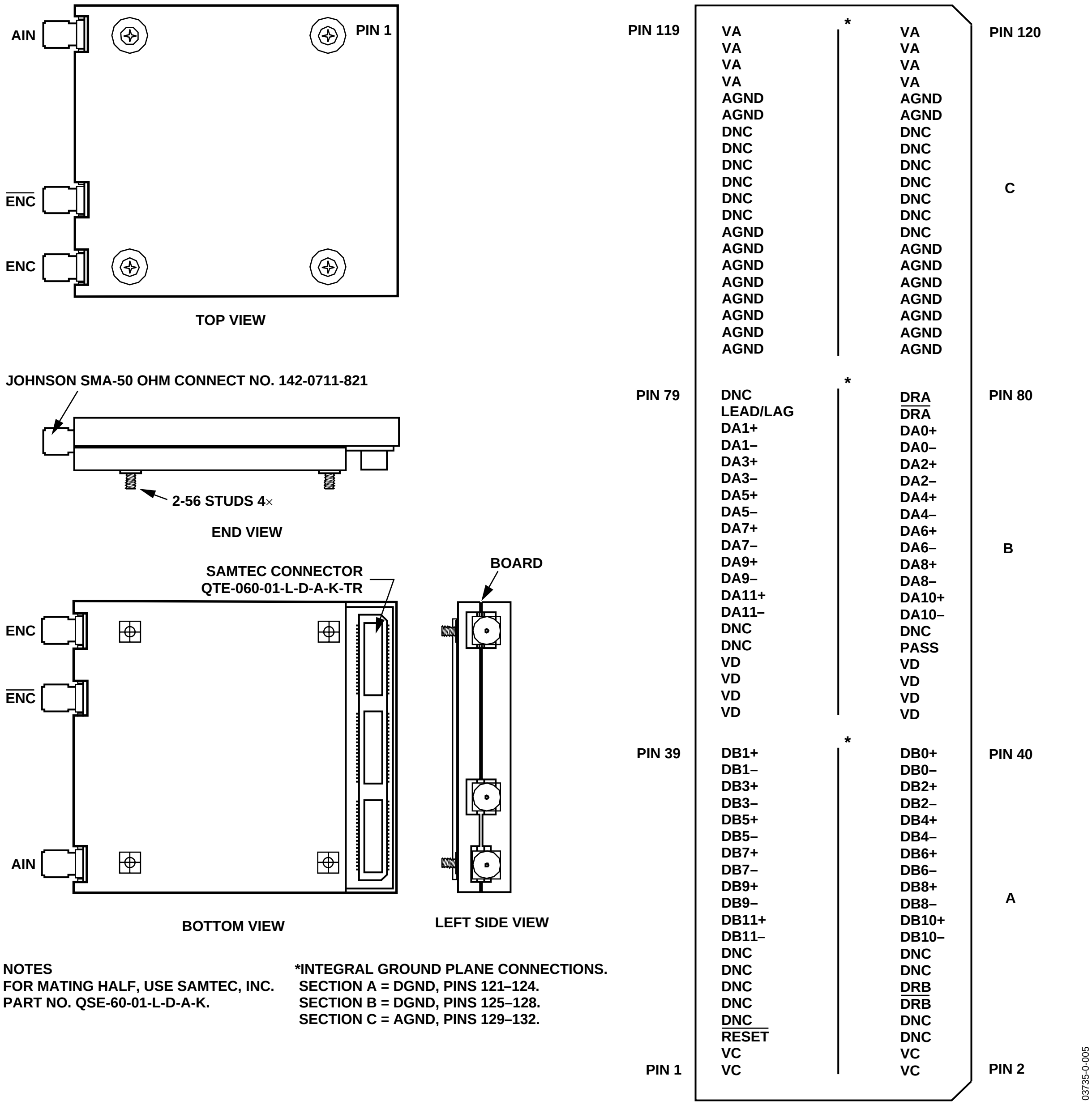

Figure 5. Pin Configuration

Table 6. Pin Function Descriptions

Pin Number	Mnemonic	Function
1, 2, 3, 4	VC	Digital Supply, +3.3 V.
5	$\overline{\text{RESET}}$	LVTTL. 0 = Device Reset. Minimum Width = 200 ns. Device resumes operation after 600 ms maximum.
6–9, 11, 13–16,	DNC	Do Not Connect.
49, 51–52, 79,		
96–108		
10	$\overline{\text{DRB}}$	Channel B Data Ready. Complement output.
12	DRB	Channel B Data Ready. True output.
17	DB11−	Channel B Data Bit 11. Complement output bit.
18	DB10−	Channel B Data Bit 10. Complement output bit.
19	DB11+	Channel B Data Bit 11. True output bit.
20	DB10+	Channel B Data Bit 10. True output bit.
21	DB9−	Channel B Data Bit 9. Complement output bit.
22	DB8−	Channel B Data Bit 8. Complement output bit.
23	DB9+	Channel B Data Bit 9. True output bit.
24	DB8+	Channel B Data Bit 8. True output bit.
25	DB7−	Channel B Data Bit 7. Complement output bit.
26	DB6−	Channel B Data Bit 6. Complement output bit.
27	DB7+	Channel B Data Bit 7. True output bit.
28	DB6+	Channel B Data Bit 6. True output bit.
29	DB5−	Channel B Data Bit 5. Complement output bit.
30	DB4−	Channel B Data Bit 4. Complement output bit.
31	DB5+	Channel B Data Bit 5. True output bit.
32	DB4+	Channel B Data Bit 4. True output bit.
33	DB3−	Channel B Data Bit 3. Complement output bit.
34	DB2−	Channel B Data Bit 2. Complement output bit.
35	DB3+	Channel B Data Bit 3. True output bit.
36	DB2+	Channel B Data Bit 2. True output bit.
37	DB1−	Channel B Data Bit 1. Complement output bit.
38	DB0−	Channel B Data Bit 0. Complement output bit. DB0 is LSB.
39	DB1+	Channel B Data Bit 1. True output bit.
40	DB0+	Channel B Data Bit 0. True output bit. DB0 is LSB.
41–48	VD	Digital Supply, +1.5 V.
50	PASS	LVTTL. Factory use only. (DNC)
53	DA11−	Channel A Data Bit 11. Complement output bit.
54	DA10−	Channel A Data Bit 10. Complement output bit.
55	DA11+	Channel A Data Bit 11. True output bit.
56	DA10+	Channel A Data Bit 10. True output bit.
57	DA9−	Channel A Data Bit 9. Complement output bit.
58	DA8−	Channel A Data Bit 8. Complement output bit.
59	DA9+	Channel A Data Bit 9. True output bit.
60	DA8+	Channel A Data Bit 8. True output bit.
61	DA7−	Channel A Data Bit 7. Complement output bit.
62	DA6−	Channel A Data Bit 6. Complement output bit.
63	DA7+	Channel A Data Bit 7. True output bit.
64	DA6+	Channel A Data Bit 6. True output bit.
65	DA5−	Channel A Data Bit 5. Complement output bit.
66	DA4−	Channel A Data Bit 4. Complement output bit.
67	DA5+	Channel A Data Bit 5. True output bit.

Pin Number	Mnemonic	Function
68	DA4+	Channel A Data Bit 4. True output bit.
69	DA3−	Channel A Data Bit 3. Complement output bit.
70	DA2−	Channel A Data Bit 2. Complement output bit.
71	DA3+	Channel A Data Bit 3. True output bit.
72	DA2+	Channel A Data Bit 2. True output bit.
73	DA1−	Channel A Data Bit 1. Complement output bit.
74	DA0−	Channel A Data Bit 0. Complement output bit. DA0 is LSB.
75	DA1+	Channel A Data Bit 1. True output bit.
76	DA0+	Channel A Data Bit 0. True output bit. DA0 is LSB.
77	LEAD/LAG	Typically DNC. See LEAD/LAG note on Page 17.
78	$\overline{\text{DRA}}$	Channel A Data Ready. Complement output.
80	DRA	Channel A Data Ready. True output.
81−95, 109−112,		
129−132*	AGND	Analog Ground.
113−120	VA	Analog Supply, 3.8 V
121−128*	DGND	Digital Ground.

*Internal Ground Plane Connections: Section A = DGND, Pins 121−124, Section B = DGND, Pins 125−128, Section C = AGND, Pins 129−132.

DEFINITIONS OF SPECIFICATIONS

Analog Bandwidth

The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Aperture Delay

The delay between the 50% point on the rising edge of the ENCODE command and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)

The sample-to-sample variation in aperture delay.

Full-Scale Input Voltage Range

This is the maximum peak-to-peak input signal magnitude that will result in a full-scale response, 0 dBFS on a single-tone input signal case. Any magnitude increase from this value will result in an over-range condition.

Analog Input VSWR (50 Ω)

The Voltage Standing Wave Ratio is a ratio of the transmitted and reflected signals. The VSWR can be related to input impedance using the following equations:

$$\Gamma = \frac{Z_L - Z_S}{Z_L + Z_S}$$

$$VSWR = \frac{1-|\Gamma|}{1+|\Gamma|}$$

Z_L = Actual Load Impedance

Z_S = Reference Impedance

Differential Nonlinearity

The deviation of any code width from an ideal 1 LSB step.

Effective Number of Bits (ENOB)

Calculated from the measured SNR based on the equation

$$ENOB = \frac{SNR_{MEASURED} - 1.76\ dB}{6.02}$$

Encode Pulsewidth/Duty Cycle

Pulsewidth high is the minimum amount of time the ENCODE pulse should be left in Logic 1 state to achieve rated performance; pulsewidth low is the minimum time the ENCODE pulse should be left in low state. See timing implications of changing t_{ENCH} in the Application Notes, Encode Input section. At a specified clock rate of 400 MSPS, these specifications define an acceptable ENCODE duty cycle.

Full-Scale Input Power

Expressed in dBm. Computed using the following equation:

$$POWER_{FULL-SCALE} = 10\log\left(\frac{V^2_{FULL-SCALErms}}{|Z_{INPUT}|(0.001)}\right)$$

Gain Error

The difference between the measured and ideal full-scale input voltage range of the ADC.

Harmonic Distortion, Second

The ratio of the RMS signal amplitude to the RMS value of the second harmonic component, reported in dBFS.

Harmonic Distortion, Third

The ratio of the RMS signal amplitude to the RMS value of the third harmonic component, reported in dBFS.

Distortion, Image Spur

The ratio of the RMS signal amplitude to the RMS signal amplitude of the image spur, reported in dBFS. The image spur, a result of gain and phase errors between two time-interleaved conversion channels, is located at fs/2 – f_{AIN}.

Distortion, Offset Spur

The ratio of the RMS signal amplitude to the RMS signal amplitude of the offset spur, reported in dBFS. The offset spur, a result of offset errors between two time-interleaved conversion channels, is located at fs/2.

Integral Nonlinearity

The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a "best straight line" determined by a least square curve fit.

Minimum Conversion Rate

The minimum ENCODE rate at which the image spur calibration will degrade no more than 1 dB (when image spur is 70 dB).

Maximum Conversion Rate

The maximum ENCODE rate at which the image spur calibration will degrade no more than 1 dB (when image spur is 70 dB).

Output Propagation Delay

The delay between a differential crossing of ENCODE and $\overline{\text{ENCODE}}$ (or zero crossing of a single-ended ENCODE).

Total Noise

Calculated as follows:

$$V_{NOISE} = \sqrt{Z \times 0.001 \times 10^{\left(\frac{FS_{dBm} - SNR_{dBc} - SIGNAL_{dBFS}}{10}\right)}}$$

where *Z* is the input impedance, FS is the full scale of the device for the frequency in question, SNR is the value of the particular input level, and *SIGNAL* is the signal level within the ADC reported in dB below full scale. This value includes both thermal and quantization noise.

Offset Error

The DC offset imposed on the input signal by the ADC, reported in LSB (codes).

Pipeline Latency

The number of clock cycles that the output data will lag the corresponding clock cycle.

Power Supply Rejection Ratio

The ratio of power supply voltage change to the resulting ADC output voltage change.

Signal-to-Noise-and-Distortion (SINAD)

The ratio of the RMS signal amplitude (set 1 dB below full scale) to the RMS value of the sum of all other spectral components, including harmonics but excluding DC and image spur.

Signal-to-Noise Ratio (SNR)

The ratio of the RMS signal amplitude (set at 1 dB below full scale) to the RMS value of the sum of all other spectral components, excluding the first five harmonics and DC.

Spurious-Free Dynamic Range (SFDR)

The ratio of the RMS signal amplitude to the RMS value of the peak spurious spectral component, except the image spur. The peak spurious component may or may not be a harmonic. May be reported in dBc (i.e., degrades as signal level is lowered) or dBFS (always related back to converter full-scale).

Two-Tone Intermodulation Distortion Rejection

The ratio of the RMS value of either input tone to the RMS value of the worst third-order intermodulation product; reported in dBc.

Two-Tone SFDR

The ratio of the RMS value of either input tone to the RMS value of the peak spurious component. The peak spurious component may or may not be an IMD product. May be reported in dBc (i.e., degrades as signal level is lowered) or in dBFS (always related back to converter full-scale).

TYPICAL PERFORMANCE CHARACTERISTICS

NOTE
X = Image spur
N = Interleaved offset spur

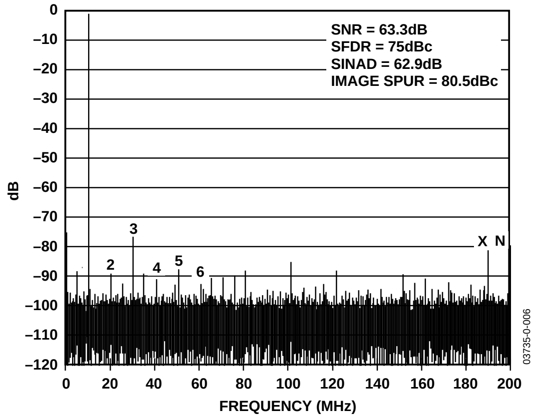

Figure 6. FFT: f_S = 400 MSPS, A_{IN} = 10.123 MHz @ –1.0 dBFS

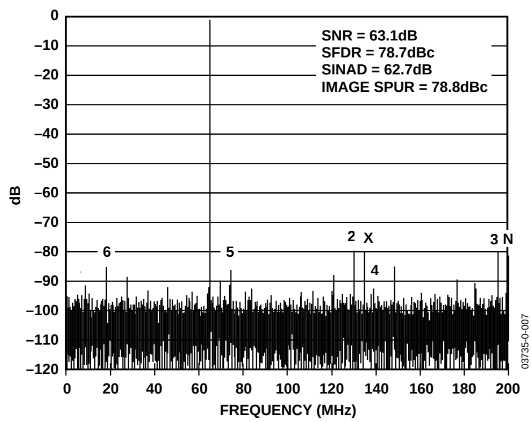

Figure 7. FFT: f_S = 400 MSPS, A_{IN} = 65.123 MHz @ –1.0 dBFS

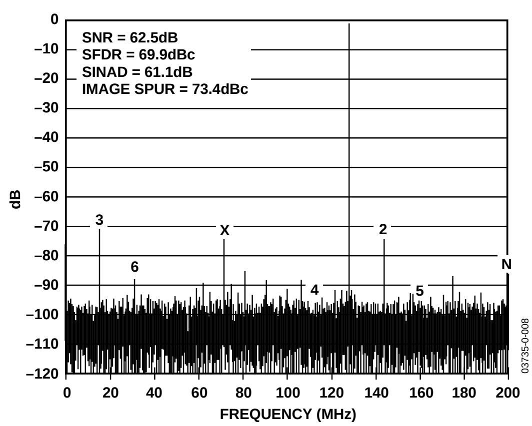

Figure 8. FFT: f_S = 400 MSPS, A_{IN} = 128.123 MHz @ –1.0 dBFS

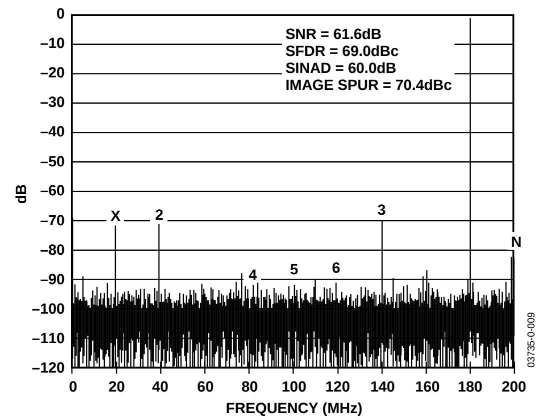

Figure 9. FFT: f_S = 400 MSPS, A_{IN} = 180.123 MHz @ –1.0 dBFS

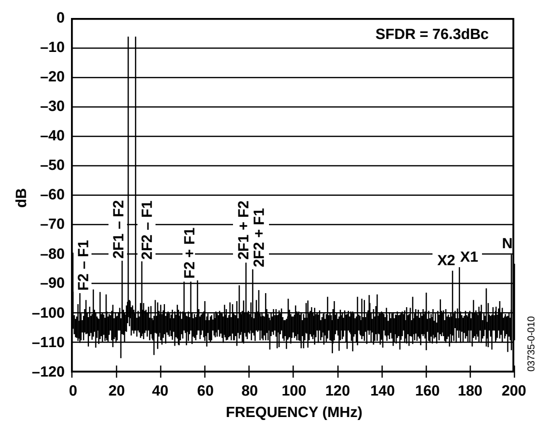

Figure 10. Two-Tone Intermodulation Distortion (25.1 MHz and 28.1 MHz; f_S = 400 MSPS)

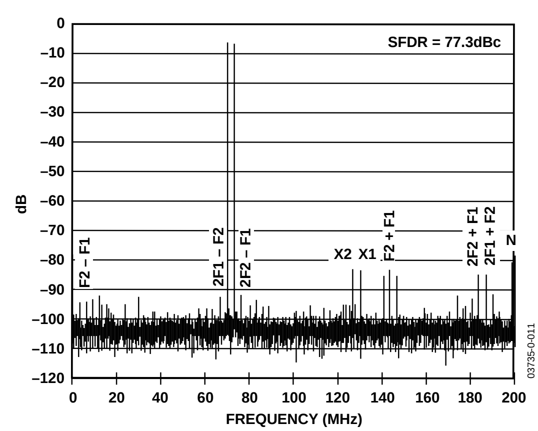

Figure 11. Two-Tone Intermodulation Distortion (70.1 MHz and 73.1 MHz; f_S = 400 MSPS)

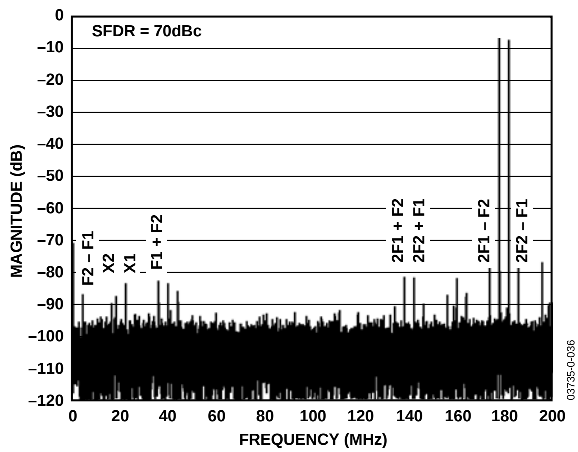

Figure 12. Two-Tone Intermodulation Distortion (178.1 MHz and 182.1 MHz; fs = 400 MSPS) SFDR = 70 dBc

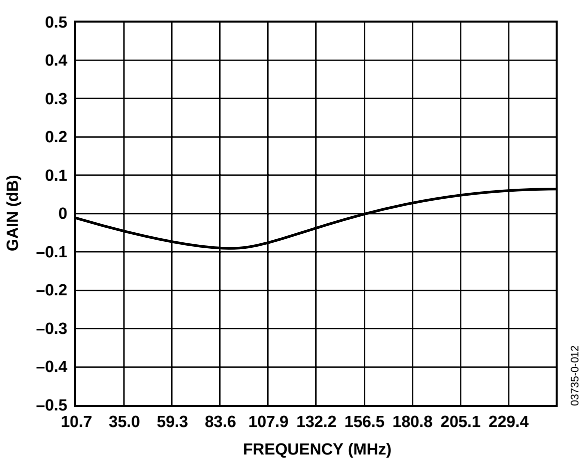

Figure 13. Interleaved Gain Flatness

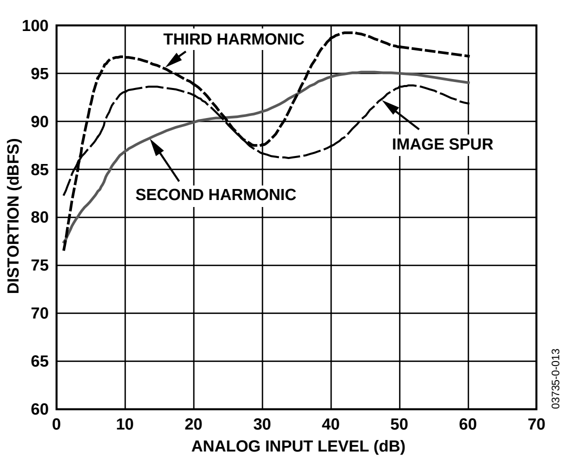

Figure 14. 2nd/3rd Harmonics and Image Spur vs. Analog Input Level— f_S = 400 MSPS, A_{IN} = 70 MHz

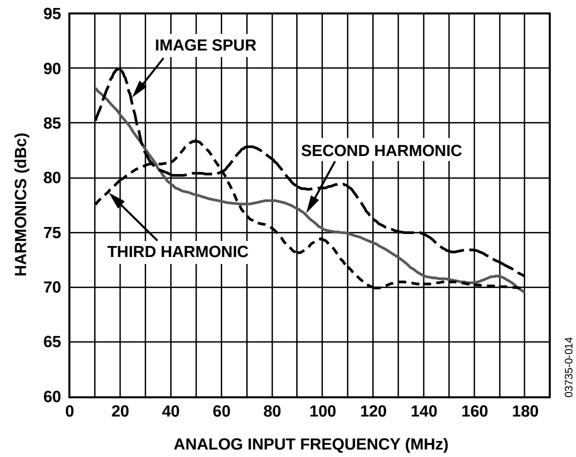

Figure 15. Harmonics vs. Analog Input Frequency

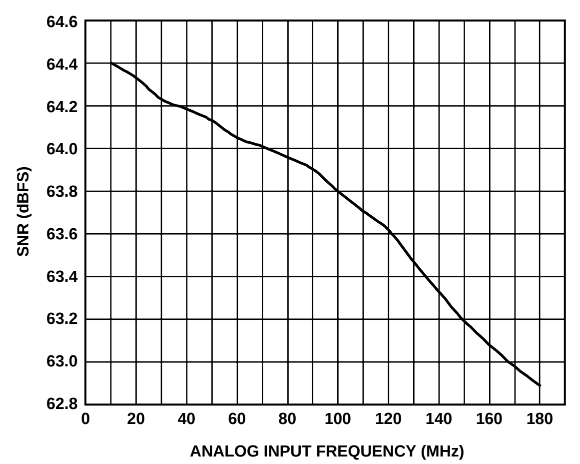

Figure 16. SNR vs. Analog Input Frequency

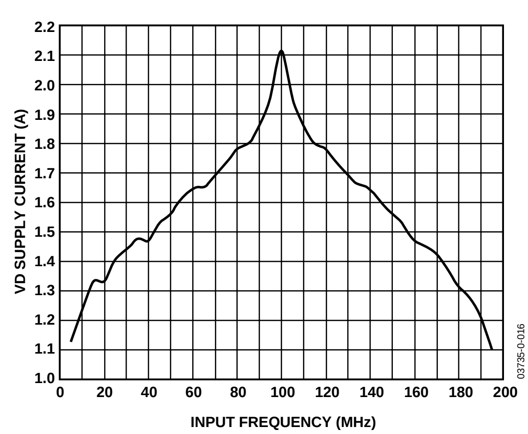

Figure 17. +VD Current vs. A_{IN} Frequency

THEORY OF OPERATION

The AD12400 uses two high-speed, 12-bit analog-to-digital converters (ADCs) in a time-interleaved configuration to double the sample rate, while maintaining a high level of dynamic range performance. The digital output of each ADC channel is calibrated using a proprietary digital post processing technique, Advanced Filter Bank (AFB™), from VCorp Technologies. AFB is implemented using a state-of-the-art Field Programmable Gate Array (FPGA) and provides a wide bandwidth, wide temperature match for any gain, phase, and clock timing errors between each ADC channel.

TIME-INTERLEAVING ADCS

When two ADCs are time-interleaved, gain and/or phase mismatches between each channel will produce an *Image Spur* at fs/2 – f_{AIN} and an *Offset Spur* as shown in Figure 18. These mismatches can be the result of any combination of device tolerance, temperature, and frequency deviations.

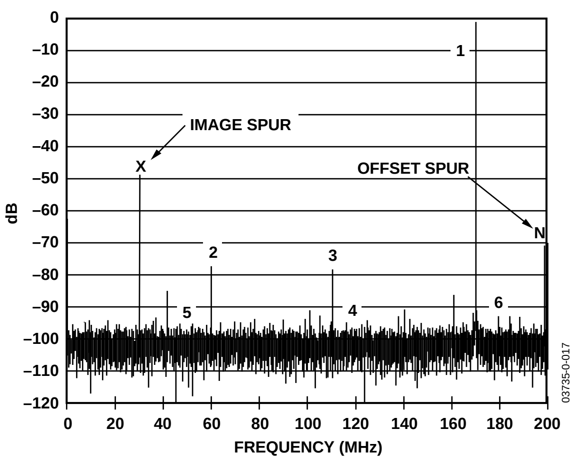

Figure 18. Image Spur Due to Mismatches between Two Interleaved ADCs ***(No AFB Digital Post Processing)***

Figure 19 displays the performance of a similar converter with on-board, AFB post processing implemented. The –44 dBFS image spur has been reduced to –77 dBFS and as a result, the dynamic range of this time-interleaved ADC is no longer limited by the channel matching.

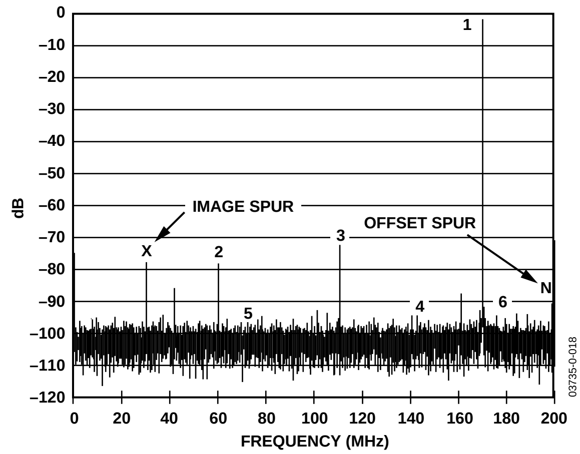

Figure 19. AD12400 with AFB Digital Post Processing

The relationship between image spur and channel mismatches is captured in Table 7 for specific conditions.

Table 7. Image Spur vs. Channel Mismatch

Gain Error (%)	Aperture Delay Error (ps)	Image Spur (dBc)
1	15	–40
0.25	2.7	–54
0.2	1.1	–62
0.025	0.5	–70

For a more detailed description of time-interleaving in ADCs and a design example using the AD12400, refer to “Advanced Digital Post-Processing Techniques Enhance Performance in Time Interleaved ADC Systems,” published in the August, 2003 edition of Analog Dialogue. This article can be found at http://www.analog.com/analogDialogue.

ANALOG INPUT

The AD12400 analog input is ac-coupled using a proprietary, transformer front end circuit that provides 1 dB of gain flatness over the first Nyquist zone and a –3 dB bandwidth of 450 MHz. This front end circuit provides a VSWR of 1.5 (50 Ω) over the first Nyquist zone, and the typical full-scale input is 3.2 V p-p The MiniCircuits HELA-10 amplifier module can be used to drive the input at these power levels.

CLOCK INPUT

The AD12400 requires a 400 MSPS encode that is divided by 2 and distributed to each ADC channel, 180° out of phase from each other. Internal ac-coupling and bias networks provide the framework for flexible clock input requirements that include single-ended sine-wave, single-ended PECL, and differential PECL. While the AD12400 is tested and calibrated using a single-ended sine-wave, properly designed PECL circuits that provide fast slew rates (>1V/ns) and minimize ringing will result in comparable dynamic range performance.

There are two major factors to consider when designing the input clock circuit for the AD12400: aperture jitter and harmonic content. The relationship between aperture jitter and SNR can be characterized using the following equation. The equation assumes a single-tone full-scale input signal.

$$SNR = -20\log\left[\sqrt{\left(2\pi \times f_A \times 0t_{JRMS}\right)^2 + \frac{1}{1.5}\times\left(\frac{1+\varepsilon}{2^N}\right)^2 + \left(\frac{2\sqrt{2}\times V_{NOISErms}}{2^N}\right)^2}\right]$$

f_A = Input frequency
t_{JRMS} = Aperture jitter
N = ADC resolution (bits)
ε = ADC DNL (LSB)
V_{NOISE} = ADC input noise (LSB*rms*)

Figure 20 displays the application of this relationship to full-scale, single-tone input signal on the AD12400, where the DNL was assumed to be 0.4 LSB, and the input noise was assumed to be 0.8 LSBrms. The vertical marker at 0.4 ps displays the SNR at the jitter level present in the AD12400 evaluation system, including the jitter associated with the AD12400 itself.

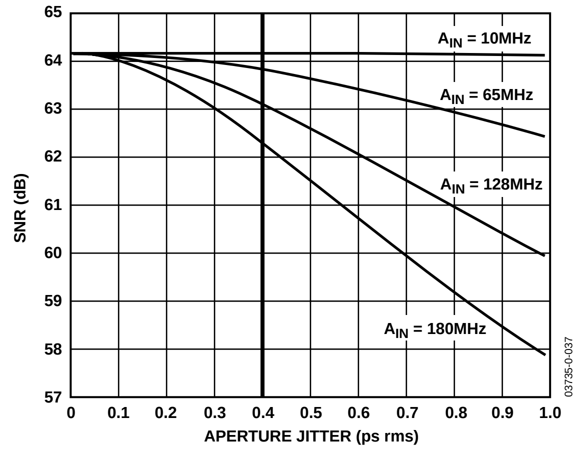

Figure 20. SNR vs. Aperture Jitter

In addition to jitter, the harmonic content of single-ended sine wave clock sources must be controlled as well. The clock source used in the test and calibration process has a harmonic performance that is better than 60 dBc. Also, when using PECL or other square-wave clock sources, unstable behavior such as overshoot and ringing can affect phase matching and degrade the image spur performance

DIGITAL OUTPUTS

The AD12400's digital post processing circuit provides two parallel, 12-bit 200 MSPS data output buses. By providing two output busses that operate at one half the conversion rate, the AD12400 eliminates the need for large, expensive, high power demultiplexing circuits. The output data format is twos complement, maintaining the standard set by other high speed A/D converters such as the AD9430 and AD6645. Data-ready signals are provided for facilitating proper timing in the data capture circuit. Finally, the digital post processing circuit can be configured to provide alternate data output formats. Contact the factory for more details.

POWER SUPPLIES

The AD12400 requires three different supply voltages: a 1.5 V supply for the digital post processing circuit, a 3.3 V supply to facilitate digital I/O through the system, and a 3.8 V supply for the analog conversion and clock distribution circuits. The AD12400 incorporates two key features that result in solid power supply rejection ratio (PSRR) performance. First, on-board linear regulators are used to provide an extra level of power supply rejection for the analog circuits. The linear regulator used to supply the A/D converters provides an additional 60 dB of rejection at 100 kHz. Second, in order to address higher frequency noise (where the linear regulators' rejection degrades), the AD12400 incorporates high quality ceramic decoupling capacitors.

While this product has been designed to provide good PSRR performance, systems designers need to be aware of the risks associated with switching power supplies and consider using linear regulators in their high speed ADC systems. Switching power supplies typically produce both conducted and radiated energy that result in common-/differential-mode EMI currents. Any system that requires 12-bit performance has very little room for errors associated with power supply EMI. For example, a system goal of 74 dB dynamic range performance on the AD12400 will require noise currents that are less than 4.5 μA and noise voltages of less than 225 μV in the analog input path.

START-UP AND $\overline{\text{RESET}}$

The AD12400's FPGA configuration is stored in the on-board EPROM and loaded into the FPGA when power is applied to the device. The $\overline{\text{RESET}}$ pin (active low) allows the user to reload the FPGA in case of a low digital supply voltage condition or a power supply glitch. Pulling the $\overline{\text{RESET}}$ pin low will pull the data ready and output bits high until the FPGA has been reloaded. The $\overline{\text{RESET}}$ pin should remain low for a minimum of 200 ns. On the rising edge of the reset pulse, the AD12400 will start loading the configuration into the FPGA. The reload process requires a maximum of 600 ms to complete. Valid signals on the data ready pins indicate that the reset process is complete. Also, system designers need be aware of the thermal conditions of the AD12400 at start-up. If large thermal imbalances are present, the AD12400 may require additional time to stabilize before providing specified image spur performance.

LEAD/LAG

The LEAD/LAG pin is used to synchronize the collection of data into external buffer memories. The LEAD/LAG pin can be applied synchronously or asynchronously to the AD12400. If applied asynchronously, LEAD/LAG must be held high for a minimum of 5 ns to ensure correct operation. The function will shut off DRA and DRB until the LEAD/LAG pin is released. DRA and DRB will resume on the next valid DRA after LEAD/LAG is released. If this feature is not required, tie this pin to DGND.

THERMAL CONSIDERATIONS

The module is rated to operate over a case temperature of 0°C to 60°C. In order to maintain the tight channel matching and reliability of the AD12400, care must be taken to assure that proper thermal and mechanical considerations have been made and addressed to assure case temperature is kept within this range. Each application will require evaluation of the thermal management as applicable to the system design. The following provides information that should be used in the evaluation of AD12400 thermal management for each specific use.

In addition to the radiation of heat into its environment, the AD12400 module enables flow of heat through the mounting studs and standoffs as they contact the motherboard. As described in the Package Integrity/Mounting Guidelines section, the module should be secured to the motherboard using 2-56 nuts (washer use is optional). The torque on the nuts should not exceed 32 inch ounces. Use of a thermal grease at the standoffs will result in better thermal coupling between the board and module. Depending on the ambient conditions, air flow may be necessary to ensure the components in the module do not exceed their maximum operating temperature. In terms of reliability, the most sensitive component has a maximum junction temperature rating of 125°C.

Figures 21 and 22 provide a basic guideline for two key thermal management decisions: the use of thermal interface material between the module bottom cover/mother board and airflow. Figure 21 characterizes the typical thermal profile of an AD12400 that is not using thermal interface material. Figure 22 provides the same information for a configuration that uses gap-filling thermal interface material (in this case Thermagon T-Flex 600 series, 0.040" thickness was used). One can see from these profiles that the maximum die temperature is reduced by approximately 2°C when thermal interface material is used. Figures 21 and 22 also provide a guideline for determining the airflow requirements for given ambient conditions. For example, a goal of 120°C die temperature in a 40°C ambient environment without the use of thermal interface material would require an air flow of 100 LFM. See the AD12400 Thermal Management and Measurement Application Note for further details.

From a channel matching perspective, the most important consideration will be external thermal influences. It is possible for thermal imbalances in the end application to adversely affect the dynamic performance. Due to the temperature dependence of the image spur, substantial deviation from the factory calibration conditions can have a detrimental effect. Unbalanced thermal influences can cause gradients across the module, and performance degradation may result. Examples of unbalanced thermal influences may include large heat dissipating elements near one side of the AD12400 or obstructed air flow that does not flow uniformly across the module. The thermal sensitivity of the module can be affected by a change in thermal gradient across the module of 2°C.

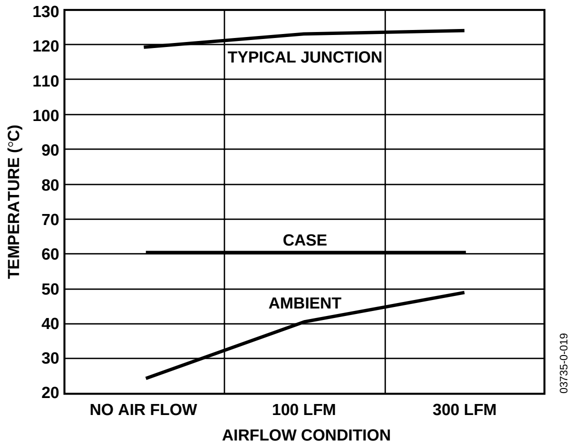

Figure 21. Typical Temperature vs. Air Flow with No Module/Board Interface Material (Normalized to 60°C Module Case Temperature)

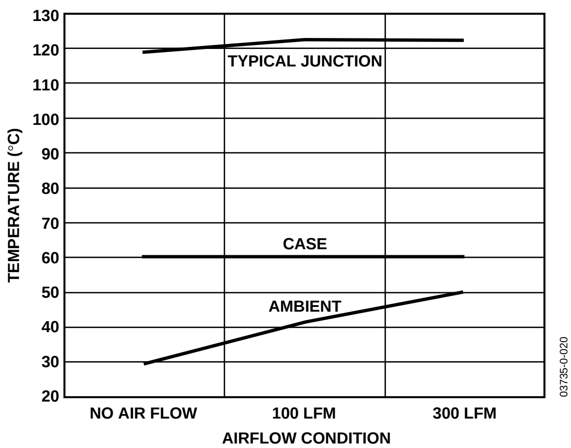

Figure 22. Typical Temperature vs. Air Flow with T-FLEX Module/Board Interface Material (Normalized to 60°C Module Case Temperature Ambient)

PACKAGE INTEGRITY/MOUNTING GUIDELINES

The AD12400 is a printed circuit board (PCB) based module designed to provide mechanical stability and support the intricate channel-to-channel matching necessary to achieve high dynamic range performance. The module should be secured to the motherboard using 2-56 nuts (washer use is optional). The torque on the nuts should not exceed 32 inch ounces.

The SMA edge connectors (AIN, ENC/ENC) are surface mounted to the board in order to achieve minimum height of the module. When attaching and routing the cables, one must ensure they are stress-relieved and do not apply stress to the SMA connector/board. The presence of stress on the cables may degrade electrical performance and mechanical integrity of the module. In addition to the routing precautions, the smallest torque necessary to achieve consistent performance should be used to secure the system cable to the AD12400's SMA connectors. In no case should the torque exceed 5 inch pounds.

Any disturbances to the AD12400 structure, including removing the covers or mounting screws, will invalidate the calibration and result in degraded performance. Refer to the Outline Dimensions section for mounting stud dimensions. Refer also to Figure 37 for PCB interface locations. Mounting stud length will typically accommodate a PCB thickness of 0.093". Consult the factory if board thickness requirements exceed this dimension.

AD12400 EVALUATION KIT

The AD12400/KIT offers an easy way to evaluate the AD12400. The AD12400/KIT includes the AD12400KWS mounted on an adapter card, the AD12400 evaluation board, the power supply cables, a 225 MHz Buffer Memory FIFO board, and the Dual Analyzer software. The user must supply a clock source, an analog input source, a 1.5 V power supply, a 3.3 V power supply, a 5 V power supply, and a 3.8 V power supply. The clock source and analog input source connect directly to the AD12400KWS. The power supply cables (included) and a parallel port cable (not included) connect to the evaluation board.

Power Connector

Power is supplied to the board via a detachable 12-lead power strip (three 4 pin blocks).

Table 8. Power Connector

VA 3.8 V	Analog supply for the ADC (950 mA typical)
VC 3.3 V	Digital supply for the ADC outputs (200 mA typical)
VD 1.5 V*	Digital supply for the FPGA (2.5 A max, 1.4 A typical)
VB 5.0 V	Digital supply for the Buffer memory board (400 mA typical)

*The power supply cable has approximately 100 mV drop. The VD supply current is dependent upon the analog input frequency. Refer to Figure 17.

Analog Input

The analog input source connects directly to an SMA on the AD12400KWS.

Encode

The single-ended or differential encode signal connects directly to SMA connector(s) on the AD12400KWS. A single-ended sine wave at 10 dBm connected to the Encode SMA is recommended. A low jitter clock source is recommended (<0.5 ps) to properly evaluate the AD12400.

Data Outputs

The AD12400KWS digital outputs are available at the 80-pin connector, P2, on the evaluation board. The AD12400/KIT comes with a Buffer Memory FIFO board connected to P2 that provides the interface to the parallel port of a PC. The Dual Analyzer software is compatible with Windows® 95, Windows® 98, Windows® 2000, and Windows NT®.

The Buffer Memory FIFO board can be removed and an external logic analyzer, or other data acquisition module, can be connected to this connector if required.

Adapter Card

The AD12400KWS is attached to an adapter card that interfaces to the evaluation board through a 120-pin connector, P1, which is on the top side of the evaluation board.

Digital Post Processing Control

The AD12400 has a two-pin jumper labeled AFB that allows the user to enable/disable the digital post processing. The digital post processing is active when the AFB jumper is applied. When the jumper is removed, the FPGA is set to a pass through mode, which will demonstrate to the user the performance of the AD12400 without the digital post processing.

$\overline{\text{RESET}}$

The AD12400KWS's FPGA configuration is stored in an EEPROM and loaded into the FPGA when power is applied to the AD12400. The $\overline{\text{RESET}}$ switch, SW1 (active low), allows the user to reload the FPGA in case of a low voltage condition or a power supply glitch. Depressing the $\overline{\text{RESET}}$ switch will pull the data ready and output bits high. The $\overline{\text{RESET}}$ switch should remain low for a minimum of 200 ns. On the rising edge of the $\overline{\text{RESET}}$ pulse, the AD12400 will start loading the configuration into the on-module FPGA. The reload process requires a maximum of 600 ms to complete. Valid signals on the data-ready pins indicate that the reset process is complete.

The AD12400 is not compatible with the HSC-ADC-EVAL-DC/SC hardware or software.

Table 9. Evaluation Board Bill of Materials

Item No.	Quantity	REF-DES	Device	Package	Value
1	2	C3, C5	Capacitor	603	0.1 μF 25 V
2	2	C4, C6	Capacitor	805	10 μF 6.3 V
3	1	R9	Resistor	603	4.02 kΩ 1%
4	1	AFB	2 Pin Header/Jumper	Pin Strip	Molex/GC/Weldon
5	1	P2	80 Pin Dual Connector Assemble	Surface Mount	Post Header AMP
6	1	SW1	Switch Push Button SPST	6 MM	Panasonic
7	3	J2, J3, J4	4 Pin Header Power Connecter	Pin Strip	Wieland
8	1	P1	60 Pin Dual-Socket Assembly	Surface Mount	SAMTEC
9	1	PCB	AD12400 Interface Bd GS08054	PCB	

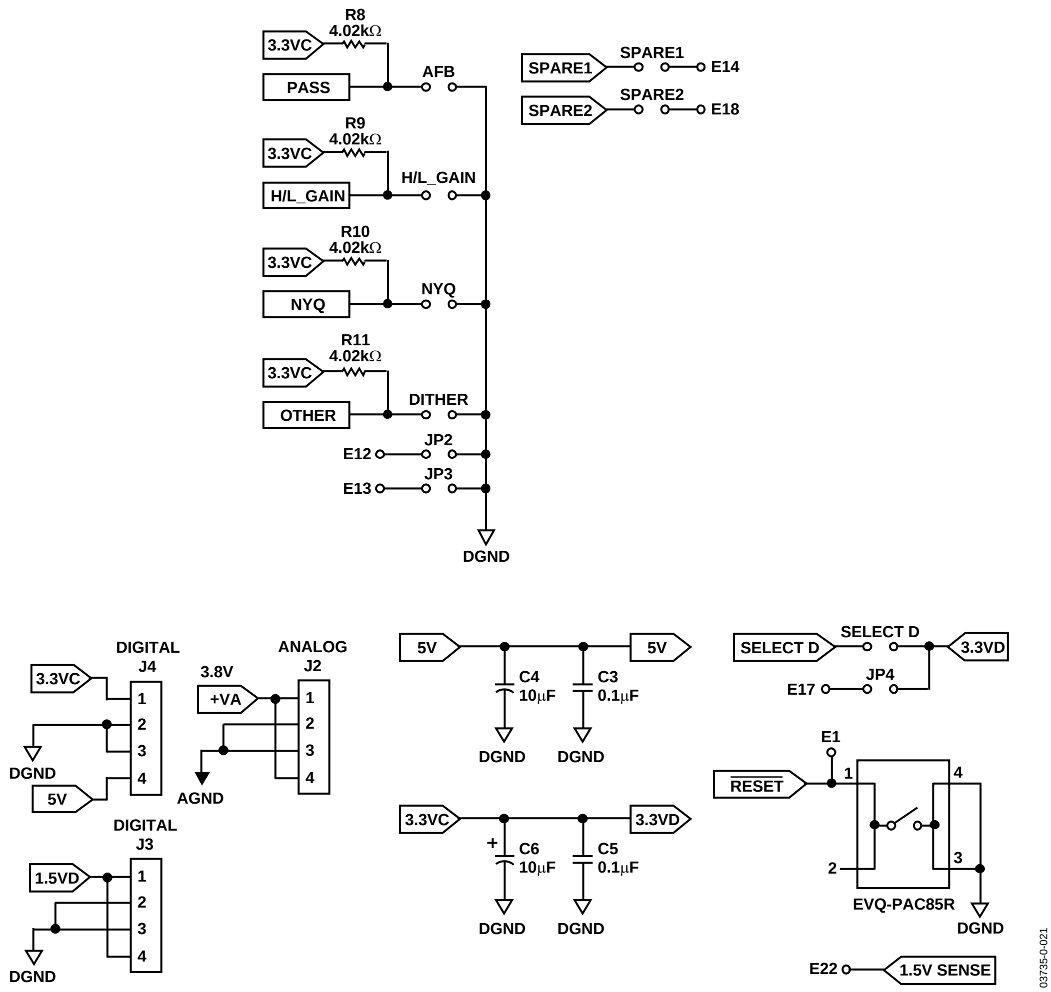

Figure 23. Evaluation Board

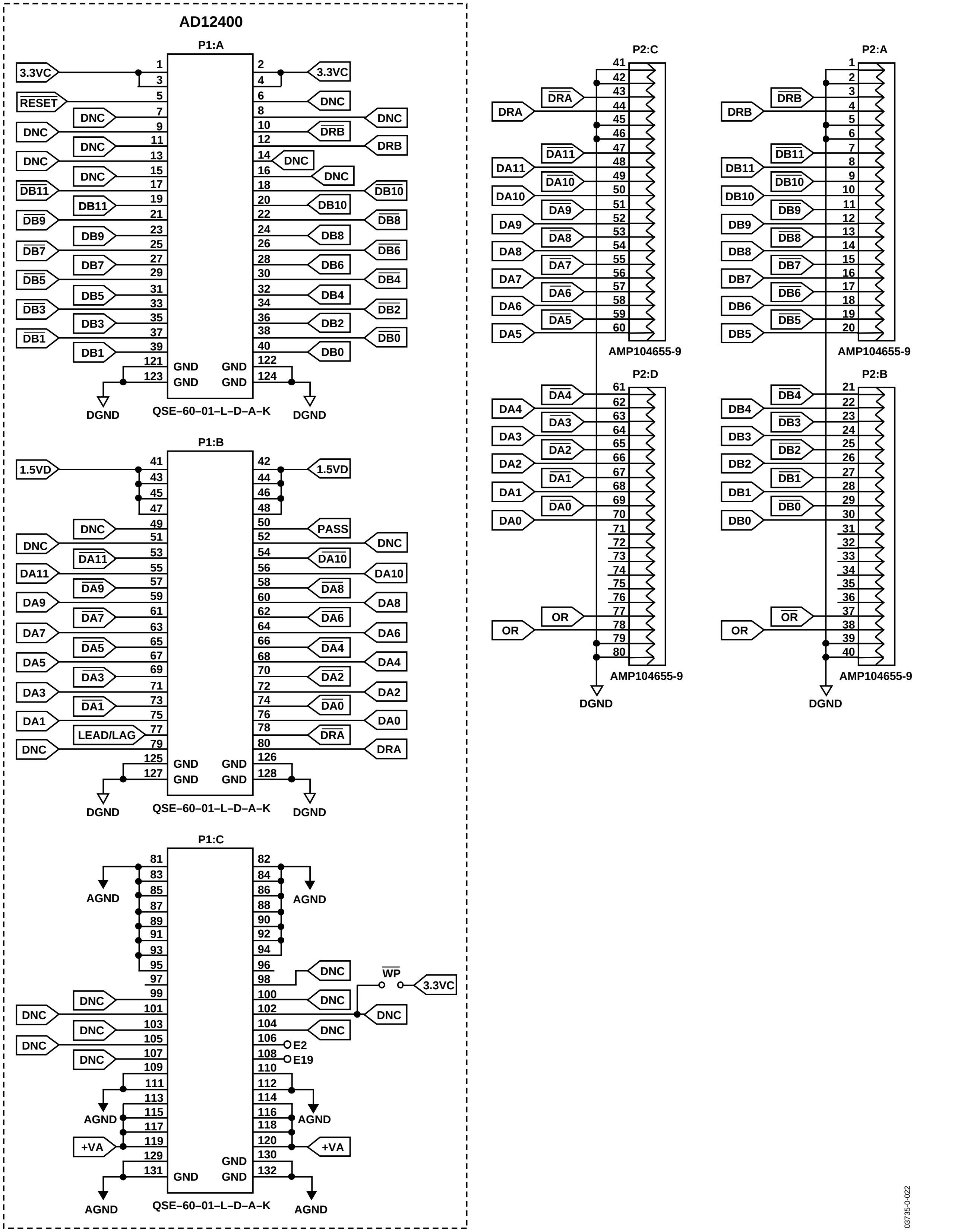

Figure 24. Evaluation Board

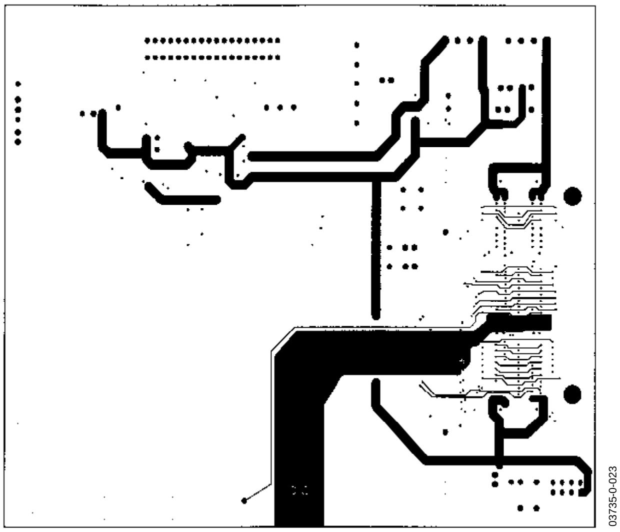

Figure 25. Power Plane 1

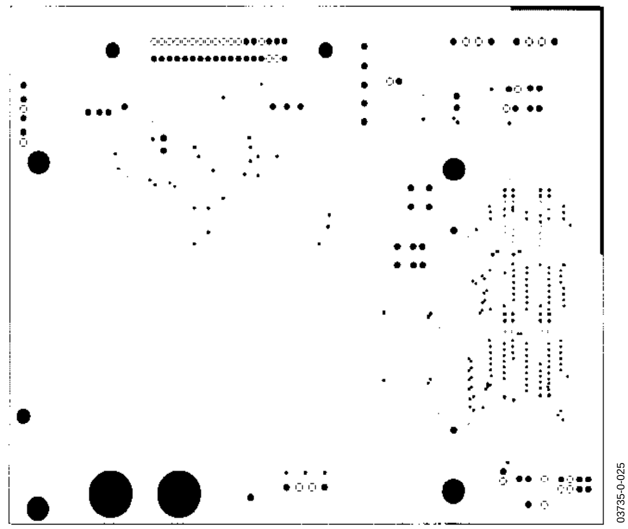

Figure 27. First Ground Plane

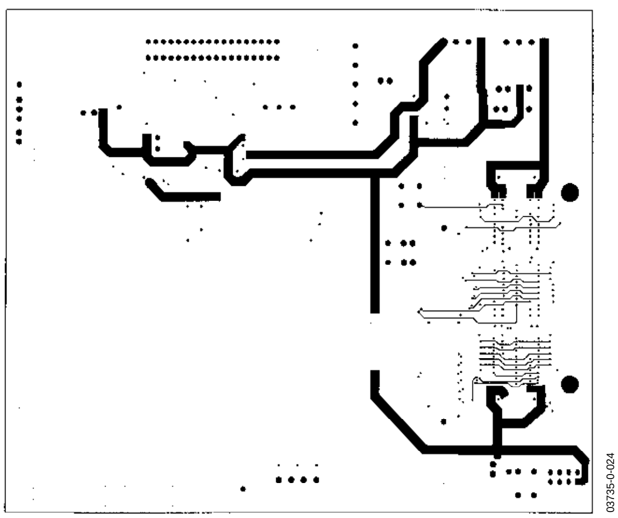

Figure 26. Power Plane 2

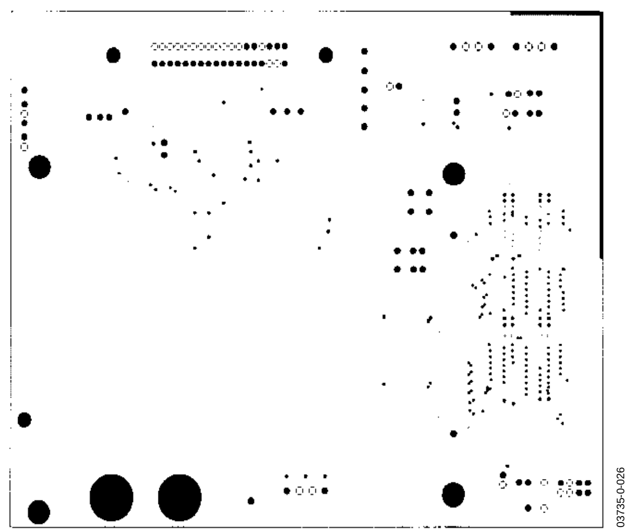

Figure 28. Second Ground Plane

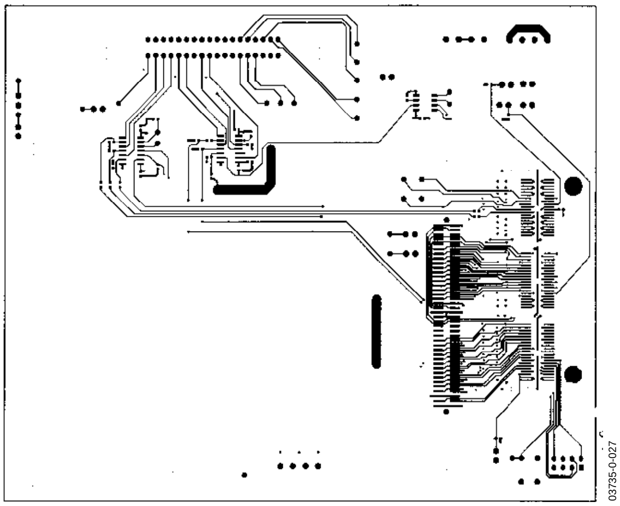

Figure 29. Top Side Copper

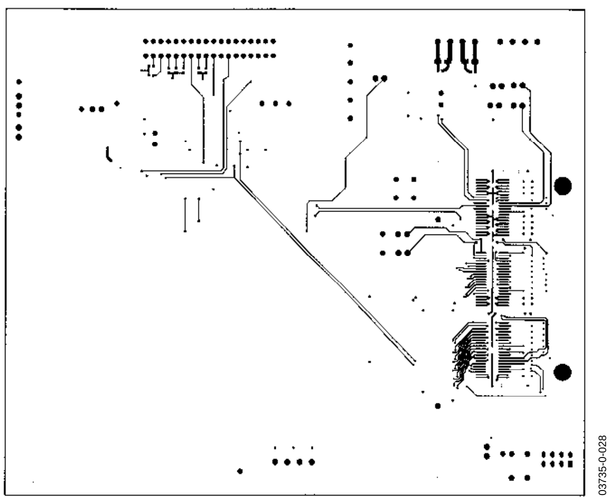

Figure 30. Bottom Side Copper

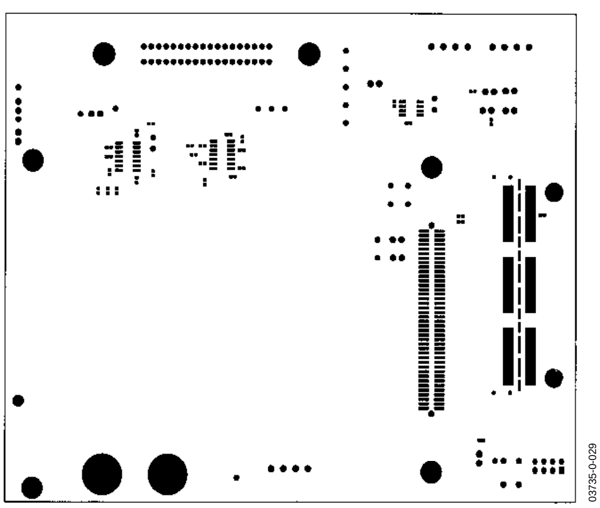

Figure 31. Top Mask

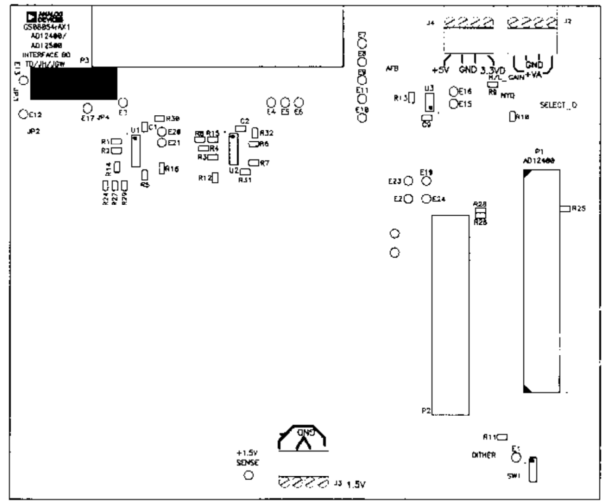

Figure 32. Top Silkscreen

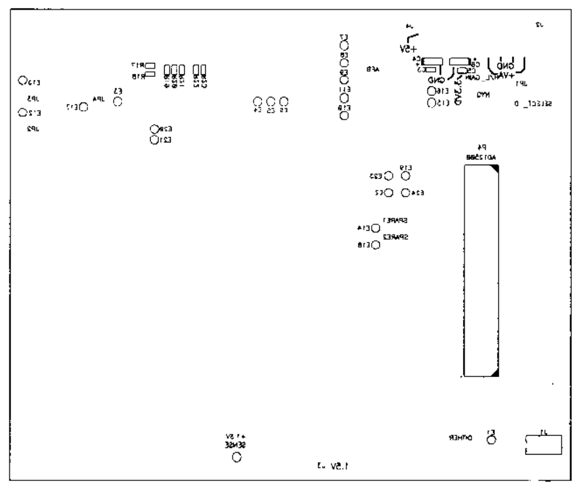

Figure 33. Bottom Silkscreen

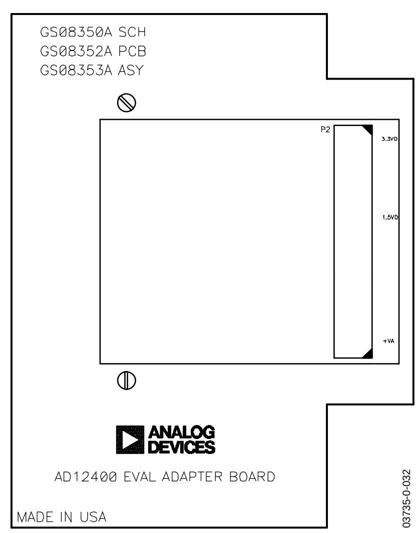

Figure 34. Evaluation Adapter Board—Top Silkscreen

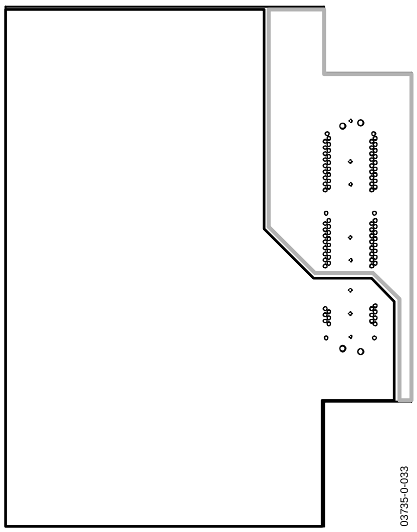

Figure 35. Evaluation Adapter Board—Analog and Digital Layers

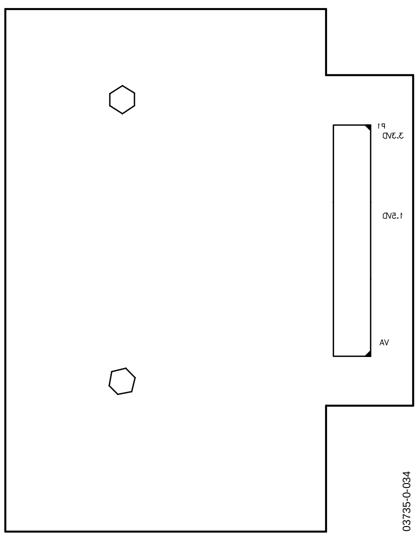

Figure 36. Evaluation Adapter Board—Bottom Silkscreen

LAYOUT GUIDELINES

The AD12400 requires a different approach to traditional high speed analog-to-digital converter system layouts. While the AD12400's internal PCB isolates digital and analog grounds, these planes are tied together through the product's aluminum case structure. Therefore, the decision of isolating the analog and digital grounds on the system PCB has additional factors to consider. For example, if the AD12400 will be attached with conductive thermal interface material to the system PCB, there will be essentially no benefit to keeping the analog and digital ground planes separate. If either no thermal interface material or nonconductive interface material is used, system architects will have to consider the ground loop that will be created if analog and digital planes are tied together directly under the AD12400. This EMI based decision will have to be considered on a case-by-case basis and will be largely dependent on the other sources of EMI in the system. One critical consideration is that a 12-bit performance requirement (–74 dBc) will require keeping conducted EMI currents (referenced to the input of the AD12400) below 4.5 µA. All of the characterization and testing of the AD12400 was performed using a system that isolated these ground planes.

If thermal interface material is used in the final system design, the following layout factors will need to be considered: open solder mask on the area that contacts the interface material and the thickness of the ground plane. While this should be analyzed in each specific system design, the use of solder mask may negate any advantage achieved by using the thermal interface material, and its use should be carefully considered. The ground plane thickness will not have a major impact on the thermal performance, but if design margin is slight, additional thickness can yield incremental improvements.

PCB INTERFACE

Figure 37 provides the mounting hole footprint for assembling the AD12400 to the second-level assembly. The diagram is referenced to the center of the mating QTE connector. Refer to the QTE/QSE series connector documentation at www.samtec.com for the SMT footprint of the mating connector.

The top view of the second-level assembly footprint provides a diagram of the second-level assembly locating tab locations for mating the SAMTEC QTE-060-01-L-A-K-TR terminal strip on the AD12400BWS to a QSE-060-01-L-A-K-TR socket on the second-level assembly. The diagram is referenced to the center of the QTE terminal strip on the AD12400BWS and the mounting holds for the screws, which will hold the AD12400BWS to the second-level assembly board. The relationship of these locating tabs is based on information provided by SAMTEC (connector supplier) and should be verified with SAMTEC by the customer.

Mating and unmating forces—the knifing or peeling action of applying force to one end or one side—must be avoided to prevent damage to the connector and guidepost.

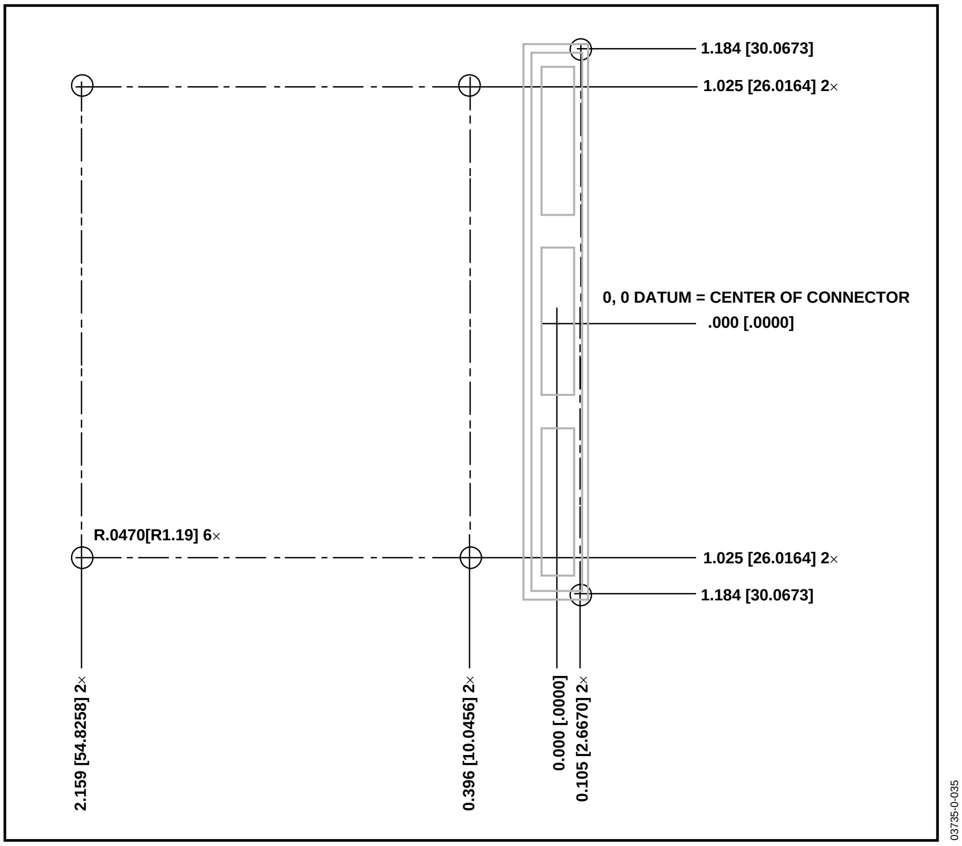

Figure 37. Top View of Interface PCB Assembly

OUTLINE DIMENSIONS

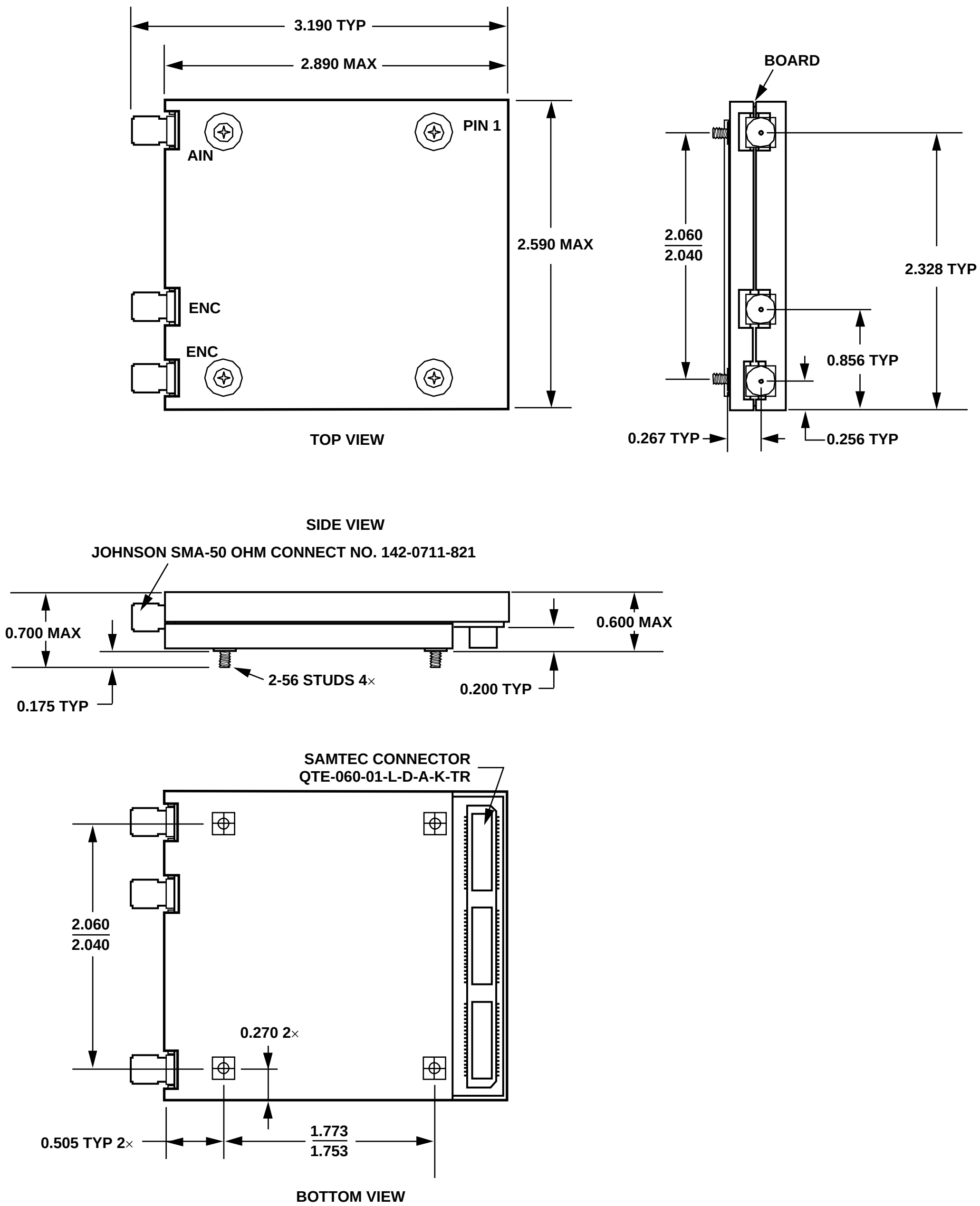

Figure 38. Outline Dimensions
Dimensions shown in inches
Tolerances:
0.xx = ±10 mils
0.xxx = ±5 mils

ORDERING GUIDE

Model	Temperature Range	Package Description
AD12400KWS	0°C to 60°C (Case)	2.9" × 2.6" × 0.6"
AD12400JWS	0°C to 60°C (Case)	2.9" × 2.6" × 0.6"
AD12400/KIT	25°C	Evaluation Kit

C03735-0-11/03(0)