ANALOG DEVICES

Dual 8-,10-,12-Bit High Bandwidth Multiplying DACs with Serial Interface

AD5429/AD5439/AD5449

FEATURES

10 MHz multiplying bandwidth
50 MHz serial interface
2.5 V to 5.5 V supply operation
±10 V reference input
Pin compatible 8-, 10-, and 12-bit DACs
Extended temperature range: −40°C to +125°C
16-lead TSSOP package
Guaranteed monotonic
Power-on reset
Daisy-chain mode
Readback function
0.5 μA typical current consumption

APPLICATIONS

Portable battery-powered applications
Waveform generators
Analog processing
Instrumentation applications
Programmable amplifiers and attenuators
Digitally controlled calibration
Programmable filters and oscillators
Composite video
Ultrasound
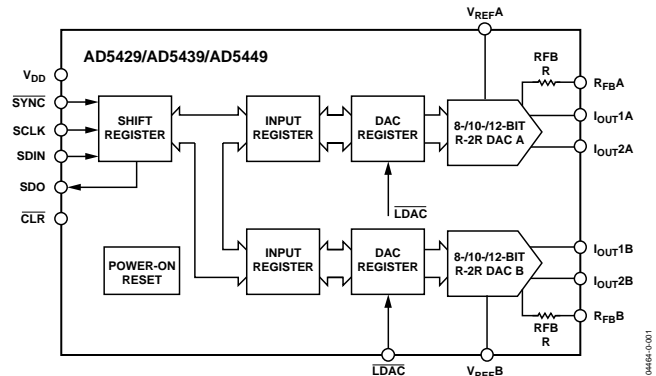**Gain, offset, and voltage trimming**

FUNCTIONAL BLOCK DIAGRAM

Figure 1.

GENERAL DESCRIPTION

The AD5429/AD5439/AD5449[1] are CMOS 8-, 10-, and 12-bit dual-channel current output digital-to-analog converters, respectively. These devices operate from a 2.5 V to 5.5 V power supply, making them suited to battery-powered and other applications.

The applied external reference input voltage (V_{REF}) determines the full-scale output current. An integrated feedback resistor (R_{FB}) provides temperature tracking and full-scale voltage output when combined with an external current-to-voltage precision amplifier.

These DACs utilize a double-buffered, 3-wire serial interface that is compatible with SPI®, QSPI™, MICROWIRE™, and most DSP interface standards. In addition, a serial data out pin (SDO) allows daisy-chaining when multiple packages are used. Data readback allows the user to read the contents of the DAC register via the SDO pin. On power-up, the internal shift register and latches are filled with zeros and the DAC outputs are at zero scale.

As a result of manufacture on a CMOS submicron process, these parts offer excellent 4-quadrant multiplication character-istics, with large signal multiplying bandwidths of 10 MHz.

The AD5429/AD5439/AD5449 DAC are available in 16-lead TSSOP packages.

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[1] US Patent Number 5,689,257.

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REVISION HISTORY

7/04—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 2.5 V to 5.5 V, V_{REF} = 10 V, $I_{OUT}2A$, $I_{OUT}2B$ = 0 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted. DC performance measured with OP1177, ac performance with AD9631, unless otherwise noted. Temperature range for Y version is −40°C to +125°C.

Table 1.

Parameter	Min	Typ	Max	Unit	Conditions
STATIC PERFORMANCE					
AD5429					
Resolution			8	Bits	
Relative Accuracy			±0.5	LSB	
Differential Nonlinearity			±1	LSB	Guaranteed monotonic
AD5439					
Resolution			10	Bits	
Relative Accuracy			±0.5	LSB	
Differential Nonlinearity			±1	LSB	Guaranteed monotonic
AD5449					
Resolution			12	Bits	
Relative Accuracy			±1	LSB	
Differential Nonlinearity			−1/+2	LSB	Guaranteed monotonic
Gain Error			±10	mV	
Gain Error Temp Coefficient[1]		±5		ppm FSR/°C	
Output Leakage Current			±5	nA	Data = 0000$_H$, T_A = 25°C, $I_{OUT}1$
			±10	nA	Data = 0000$_H$, $I_{OUT}1$
REFERENCE INPUT[1]					Typical resistor TC = −50 ppm/°C
Reference Input Range		±10		V	
$V_{REF}A$,$V_{REF}B$ Input Resistance	8	10	12	kΩ	DAC input resistance
$V_{REF}A/B$ Input Resistance Mismatch		1.6	2.5	%	Typ = 25°C, max = 125°C
DIGITAL INPUTS/OUTPUT[1]					
Input High Voltage, V_{IH}	1.7			V	V_{DD} = 2.5 V to 5.5 V
Input Low Voltage, V_{IL}		0.8		V	V_{DD} = 2.7 V to 5.5 V
		0.7		V	V_{DD} = 2.5 V to 2.7 V
Input Leakage Current, I_{IL}		1		μA	
Input Capacitance		10		pF	
V_{DD} = 4.5 V to 5.5 V					
Output Low Voltage, V_{OL}		0.4		V	I_{SINK} = 200 μA
Output High Voltage, V_{OH}	V_{DD} − 1			V	I_{SOURCE} = 200 μA
V_{DD} = 2.5 V to 3.6 V					
Output Low Voltage, V_{OL}		0.4		V	I_{SINK} = 200 μA
Output High Voltage, V_{OH}	V_{DD} − 0.5			V	I_{SOURCE} = 200 μA
DYNAMIC PERFORMANCE[1]					
Reference Multiplying BW			10	MHz	V_{REF} = 5 V p-p, DAC loaded all 1s
Output Voltage Settling Time					Measured to ±4 mV of FS, R_{LOAD} = 100 Ω, C_{LOAD} = 0s
AD5429		50	100	ns	
AD5439		55	110	ns	DAC latch alternately loaded with 0s and 1s
AD5449		90	160	ns	R_{LOAD} = 100 Ω, C_{LOAD} = 15 pF
Digital Delay		20	40	ns	
Digital-to-Analog Glitch Impulse		3		nV-s	1 LSB change around major carry, V_{REF} = 0 V
Multiplying Feedthrough Error			−75	dB	DAC latch loaded with all 0s, reference = 10 kHz

Parameter	Min	Typ	Max	Unit	Conditions
Output Capacitance			2	pF	DAC latches loaded with all 0s
			4	pF	DAC latches loaded with all 1s
Digital Feedthrough		5		nV-s	Feedthrough to DAC output with CS high and alternate loading of all 0s and all 1s
Total Harmonic Distortion		−75		dB	V_{REF} = 5 V p-p, all 1s loaded, f = 1 kHz
		−75		dB	V_{REF} = 5 V, sine wave generated from digital code
Output Noise Spectral Density		25		nV/√Hz	@ 1 kHz
SFDR PERFORMANCE (Wideband)					AD5449, 65 k codes, V_{REF} = 3.5 V
Clock = 10 MHz					
500 kHz fout		55		dB	
100 kHz fout		63		dB	
50 kHz fout		65		dB	
Clock = 25 MHz					
500 kHz fout		50		dB	
100 kHz fout		60		dB	
50 kHz fout		62		dB	
SFDR PERFORMANCE (Narrow Band)					AD5449, 65 k codes, V_{REF} = 3.5 V
Clock = 10 MHz					
500 kHz fout		73		dB	
100 kHz fout		80		dB	
50 kHz fout		87		dB	
Clock = 25 MHz					
500 kHz fout		70		dB	
100 kHz fout		75		dB	
50 kHz fout		80		dB	
INTERMODULATION DISTORTION					AD5449, 65 k codes, V_{REF} = 3.5 V
Clock = 10 MHz					
f_1 = 400 kHz, f_2 = 500 kHz		65		dB	
f_1 = 40 kHz, f_2 = 50 kHz		72		dB	
Clock = 25 MHz					
f_1 = 400 kHz, f_2 = 500 kHz		51		dB	
f_1 = 40 kHz, f_2 = 50 kHz		65		dB	
POWER REQUIREMENTS					
Power Supply Range	2.5		5.5	V	
I_{DD}			10	µA	Logic inputs = 0 V or V_{DD}
Power Supply Sensitivity[1]			0.001	%/%	ΔV_{DD} = ±5%

[1] Guaranteed by design and characterization, not subject to production test.

TIMING CHARACTERISTICS

V_{DD} = 2.5 V to 5.5 V, V_{REF} = 5 V, $I_{OUT}2$ = 0 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

See Figure 2 and Figure 3. Temperature range for Y version is −40°C to +125°C. Guaranteed by design and characterization, not subject to production test. All input signals are specified with tr = tf = ns (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2.

Table 2.

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Conditions/Comments[1]
f_{SCLK}	50	MHz max	Max clock frequency
t_1	20	ns min	SCLK cycle time
t_2	8	ns min	SCLK high time
t_3	8	ns min	SCLK low time
t_4	13	ns min	$\overline{SYNC}$ falling edge to SCLK falling edge setup time
t_5	5	ns min	Data setup time
t_6	4	ns min	Data hold time
t_7	5	ns min	$\overline{SYNC}$ rising edge to SCLK falling edge
t_8	30	ns min	Minimum $\overline{SYNC}$ high time
t_9	0	ns min	SCLK falling edge to $\overline{LDAC}$ falling edge
t_{10}	12	ns min	$\overline{LDAC}$ pulse width
t_{11}	10	ns min	SCLK falling edge to $\overline{LDAC}$ rising edge
t_{12}[2]	25	ns min	SCLK active edge to SDO valid, strong SDO driver
	60	ns min	SCLK active edge to SDO valid, weak SDO driver

[1] Falling or rising edge as determined by the control bits of the serial word. Strong or weak SDO driver selected via the control register.
[2] Daisy-chain and readback modes cannot operate at maximum clock frequency. SDO timing specifications are measured with a load circuit, as shown in Figure 4.
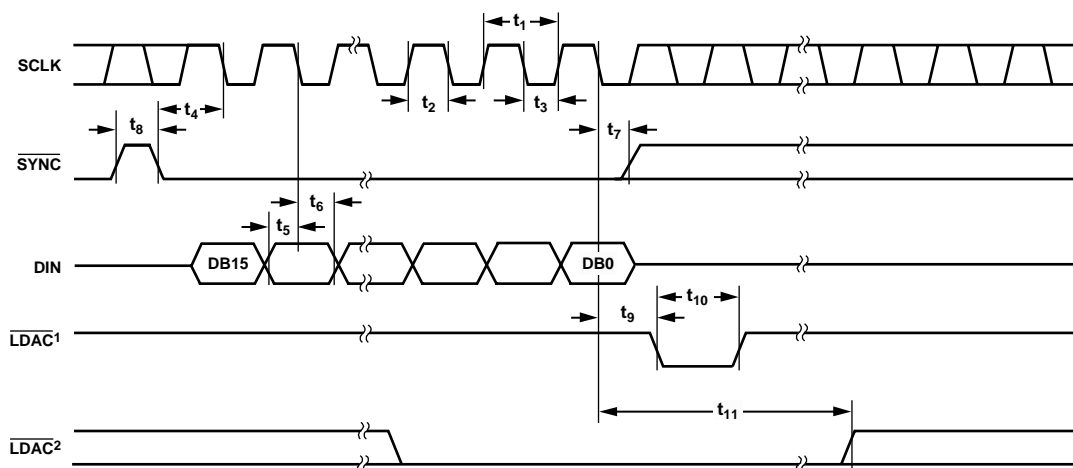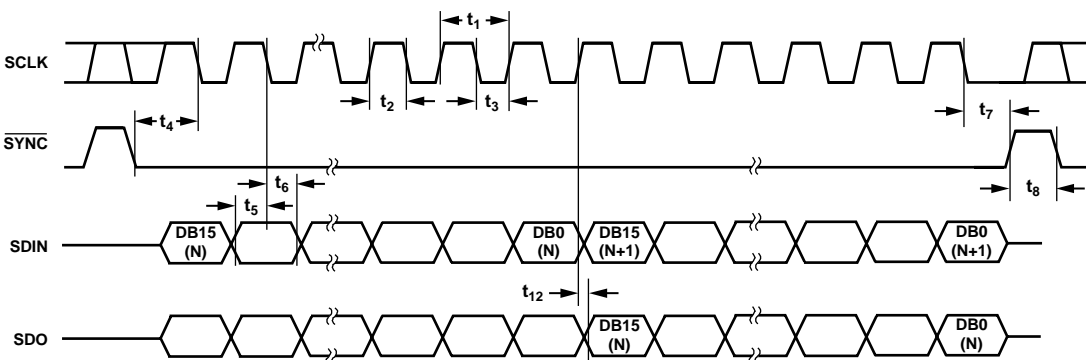
NOTES
[1] ASYNCHRONOUS $\overline{LDAC}$ UPDATE MODE
[2] SYNCHRONOUS $\overline{LDAC}$ UPDATE MODE

ALTERNATIVELY, DATA CAN BE CLOCKED INTO INPUT SHIFT REGISTER ON RISING EDGE OF SCLK AS DETERMINED BY CONTROL BITS. TIMING AS ABOVE, WITH SCLK INVERTED.

Figure 2. Standalone Mode Timing Diagram

ALTERNATIVELY, DATA CAN BE CLOCKED INTO INPUT SHIFT REGISTER ON RISING EDGE OF SCLK AS DETERMINED BY CONTROL BITS. IN THIS CASE, DATA WOULD BE CLOCKED OUT OF SDO ON FALLING EDGE OF SCLK. TIMING AS ABOVE, WITH SCLK INVERTED.

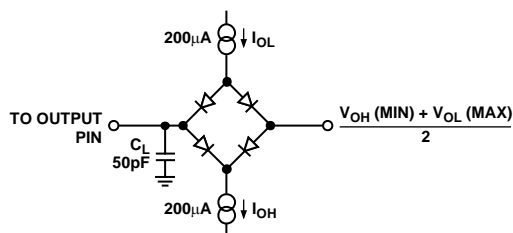Figure 3. Daisy-Chain and Readback Modes Timing Diagram

Figure 4. Load Circuit for SDO Timing Specifications

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
V_{REF}, R_{FB} to GND	−12 V to +12 V
$I_{OUT}1$, $I_{OUT}2$ to GND	−0.3 V to +7 V
Input Current to Any Pin except Supplies	±10 mA
Logic Inputs and Output[1]	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Extended (Y Version)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
16-Lead TSSOP θ_{JA} Thermal Impedance	150°C/W
Lead Temperature, Soldering (10 s)	300°C
IR Reflow, Peak Temperature (< 20 s)	235°C

[1] Overvoltages at SCLK, $\overline{SYNC}$, and DIN are clamped by internal diodes.
Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

Transient currents of up to 100 mA do not cause SCR latch-up.

T_A = 25°C unless otherwise noted.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.
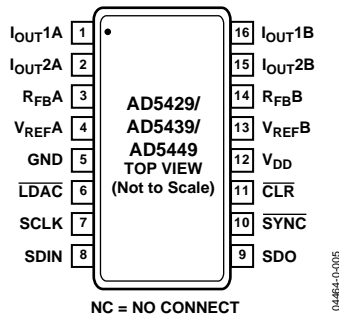

WARNING!
ESD SENSITIVE DEVICE

AD5429/AD5439/AD5449

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Figure 5. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Function
1	$I_{OUT}1A$	DAC A Current Output.
2	$I_{OUT}2A$	DAC A Analog Ground. This pin should typically be tied to the analog ground of the system, but can be biased to achieve single-supply operation.
3	$R_{FB}A$	DAC Feedback Resistor Pin. Establish voltage output for the DAC by connecting to an external amplifier output.
4	$V_{REF}A$	DAC A Reference Voltage Input Pin.
5	GND	Ground Pin.
6	$\overline{LDAC}$	Load DAC Input. Allows asynchronous or synchronous updates to the DAC output. The DAC is asynchronously updated when this signal goes low. Alternatively, if this line is held permanently low, an automatic or synchronous update mode is selected whereby the DAC is updated on the 16th clock falling edge when the device is in standalone mode, or on the rising edge of $\overline{SYNC}$ when in daisy-chain mode.
7	SCLK	Serial Clock Input. By default, data is clocked into the input shift register on the falling edge of the serial clock input. Alternatively, by means of the serial control bits, the device can be configured such that data is clocked into the shift register on the rising edge of SCLK.
8	SDIN	Serial Data Input. Data is clocked into the 16-bit input register on the active edge of the serial clock input. By default, on power-up, data is clocked into the shift register on the falling edge of SCLK. The control bits allow the user to change the active edge to rising edge.
9	SDO	Serial Data Output. This allows a number of parts to be daisy-chained. By default, data is clocked into the shift register on the falling edge and out via SDO on the rising edge of SCLK. Data is always clocked out on the alternate edge to loading data to the shift register. Writing the readback control word to the shift register makes the DAC register contents available for readback on the SDO pin, clocked out on the next 16 opposite clock edges to the active clock edge.
10	$\overline{SYNC}$	Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes low, it powers on the SCLK and DIN buffers, and the input shift register is enabled. Data is loaded to the shift register on the active edge of the following clocks. In standalone mode, the serial interface counts clocks, and data is latched to the shift register on the16th active clock edge.
11	$\overline{CLR}$	Active Low Control Input. This pin clears the DAC output, input, and DAC registers. Configuration mode allows the user to enable the hardware $\overline{CLR}$ pin as a clear to zero scale or midscale as required.
12	V_{DD}	Positive Power Supply Input. These parts can be operated from a supply of 2.5 V to 5.5 V.
13	$V_{REF}B$	DAC B Reference Voltage Input Pin.
14	$R_{FB}B$	DAC B Feedback Resistor Pin. Establish voltage output for the DAC by connecting to an external amplifier output.
15	$I_{OUT}2B$	DAC B Analog Ground. This pin typically should be tied to the analog ground of the system, but can be biased to achieve single-supply operation.
16	$I_{OUT}1B$	DAC B Current Output.

TERMINOLOGY

Relative Accuracy
Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale and is typically expressed in LSBs or as a percentage of full-scale reading.

Differential Nonlinearity
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum over the operating temperature range ensures monotonicity.

Gain Error
Gain error or full-scale error is a measure of the output error between an ideal DAC and the actual device output. For these DACs, ideal maximum output is V_{REF} − 1 LSB. Gain error of the DACs is adjustable to zero with external resistance.

Output Leakage Current
Output leakage current is current that flows in the DAC ladder switches when these are turned off. For the $I_{OUT}1$ terminal, it can be measured by loading all 0s to the DAC and measuring the $I_{OUT}1$ current. Minimum current flows in the $I_{OUT}2$ line when the DAC is loaded with all 1s.

Output Capacitance
Capacitance from $I_{OUT}1$ or $I_{OUT}2$ to AGND.

Output Current Settling Time
The amount of time needed for the output to settle to a specified level for a full-scale input change. For these devices, it is specified with a 100 Ω resistor to ground.

Digital-to-Analog Glitch lmpulse
The amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA-s or nV-s, depending upon whether the glitch is measured as a current or voltage signal.

Digital Feedthrough
When the device is not selected, high frequency logic activity on the device digital inputs is capacitively coupled through the device to show up as noise on the I_{OUT} pins and subsequently into the following circuitry. This noise is digital feedthrough.

Multiplying Feedthrough Error
The error due to capacitive feedthrough from the DAC reference input to the DAC $I_{OUT}1$ terminal, when all 0s are loaded to the DAC.

Digital Crosstalk
The glitch impulse transferred to the outputs of one DAC in response to a full-scale code change (all 0s to all 1s and vice versa) in the input register of the other DAC. It is expressed in nV-s.

Analog Crosstalk
The glitch impulse transferred to the output of one DAC due to a change in the output of another DAC. It is measured by loading one of the input registers with a full-scale code change (all 0s to all 1s and vice versa), while keeping $\overline{LDAC}$ high. Then pulse $\overline{LDAC}$ low and monitor the output of the DAC whose digital code was not changed. The area of the glitch is expressed in nV-s.

Channel-to-Channel Isolation
The proportion of input signal from the reference input of one DAC that appears at the output of the other DAC. It is expressed in dB.

Total Harmonic Distortion (THD)
The DAC is driven by an ac reference. The ratio of the rms sum of the harmonics of the DAC output to the fundamental value is the THD. Usually only the lower-order harmonics are included, such as second to fifth.

$$THD = 20 \log \sqrt{\frac{\left(V_2^2 + V_3^2 + V_4^2 + V_5^2\right)}{V_1}}$$

Intermodulation Distortion
The DAC is driven by two combined sine wave references of frequencies fa and fb. Distortion products are produced at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3… Intermodulation terms are those for which m or n is not equal to zero. The second-order terms include (fa + fb) and (fa − fb) and the third-order terms are (2fa + fb), (2fa − fb), (f + 2fa + 2fb) and (fa − 2fb). IMD is defined as

$$IMD = 20 \log \frac{\left(rms\ sum\ of\ the\ sum\ and\ diff\ distortion\ products\right)}{rms\ amplitude\ of\ the\ fundamental}$$

Compliance Voltage Range
The maximum range of (output) terminal voltage for which the device provides the specified characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS
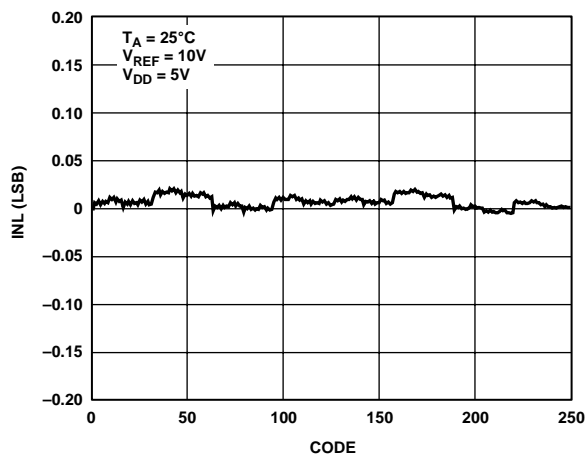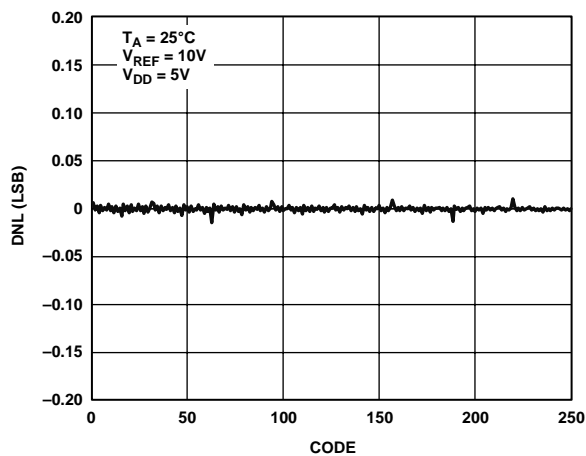

Figure 6. INL vs. Code (8-Bit DAC)
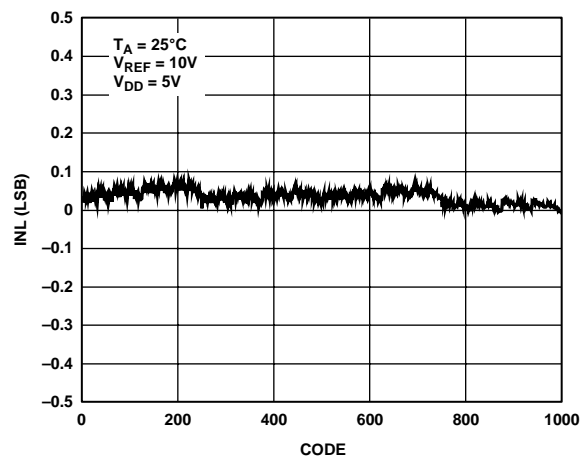

Figure 9. DNL vs. Code (8-Bit DAC)

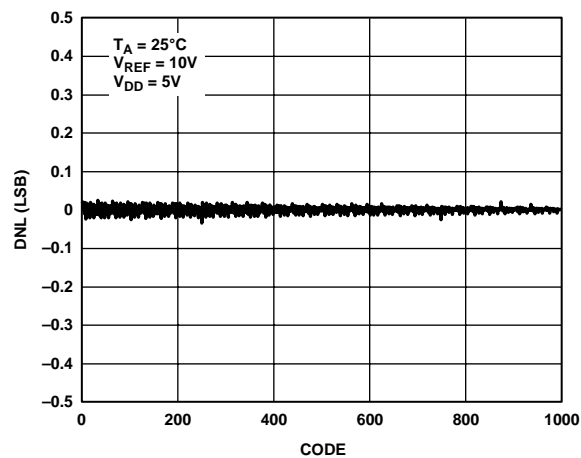Figure 7. INL vs. Code (10-Bit DAC)

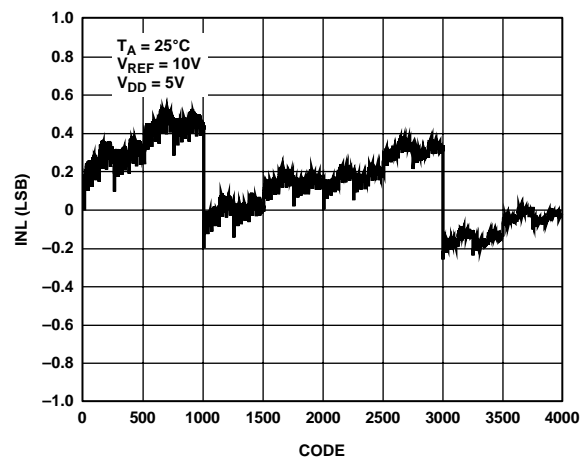Figure 10. DNL vs. Code (10-Bit DAC)
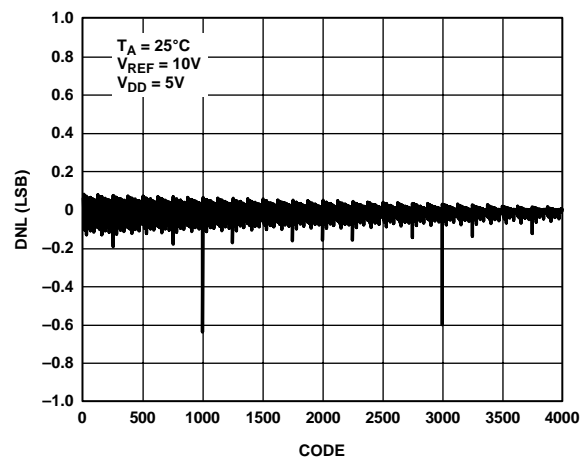

Figure 8. INL vs. Code (12-Bit DAC)

Figure 11. DNL vs. Code (12-Bit DAC)
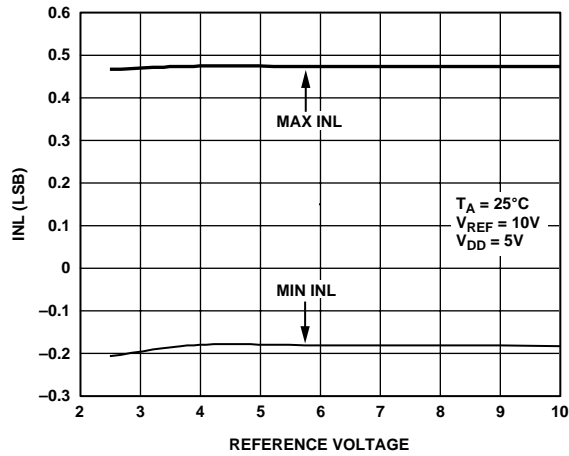
Figure 12. INL vs. Reference Voltage

Figure 13. DNL vs. Reference Voltage
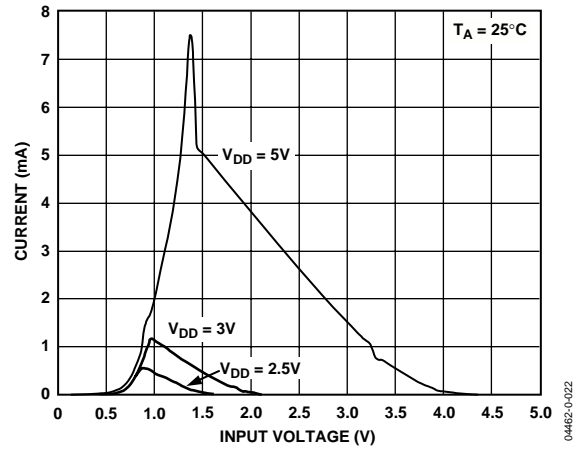

Figure 14. Gain Error vs. Temperature

Figure 15. Supply Current vs. Logic Input Voltage

Figure 16. $I_{OUT}1$ Leakage Current vs. Temperature
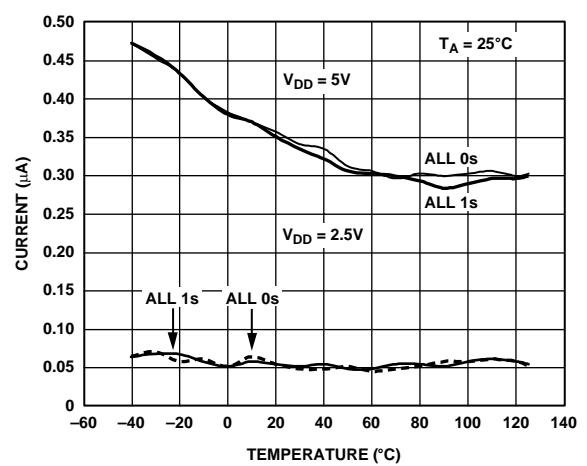

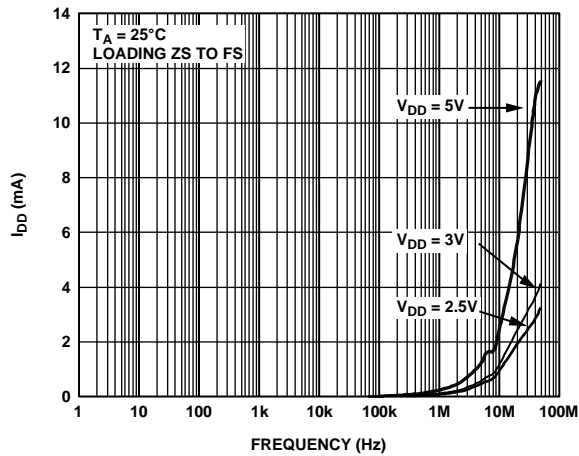Figure 17. Supply Current vs. Temperature
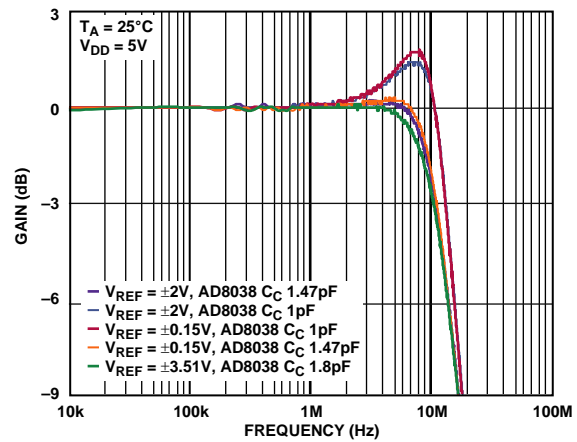
Figure 18. Supply Current vs. Update Rate

Figure 21. Reference Multiplying Bandwidth vs. Frequency and Compensation Capacitor
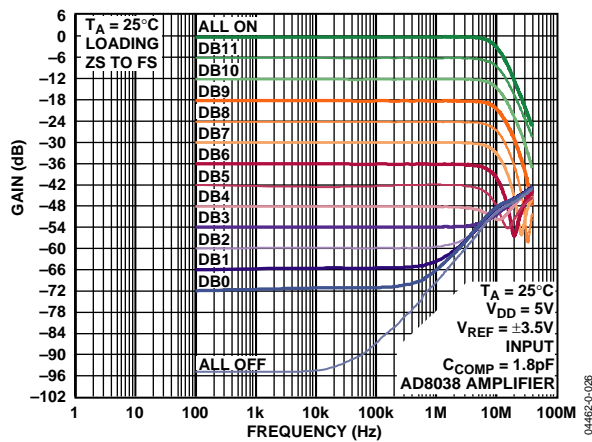
Figure 19. Reference Multiplying Bandwidth vs. Frequency and Code
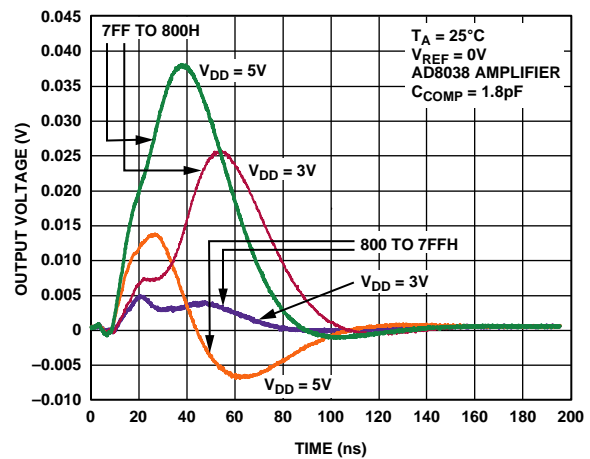
Figure 22. Midscale Transition, V_{REF} = 0 V
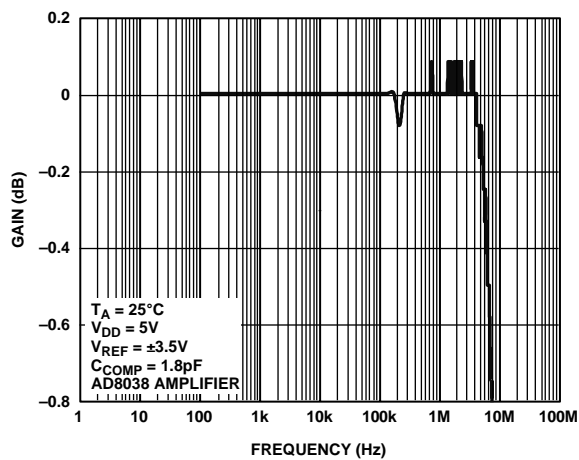
Figure 20. Reference Multiplying Bandwidth–All 1s Loaded
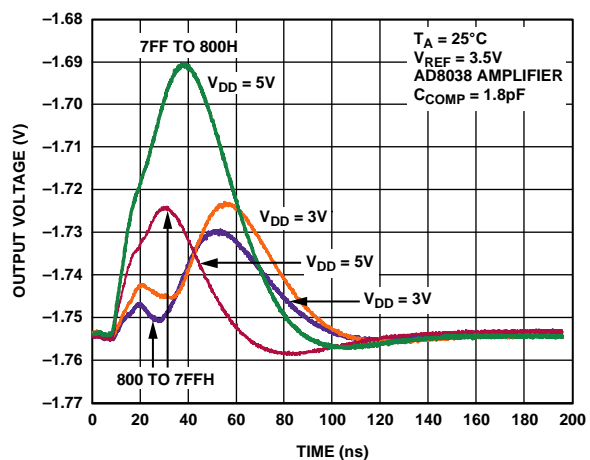
Figure 23. Midscale Transition, V_{REF} = 3.5 V
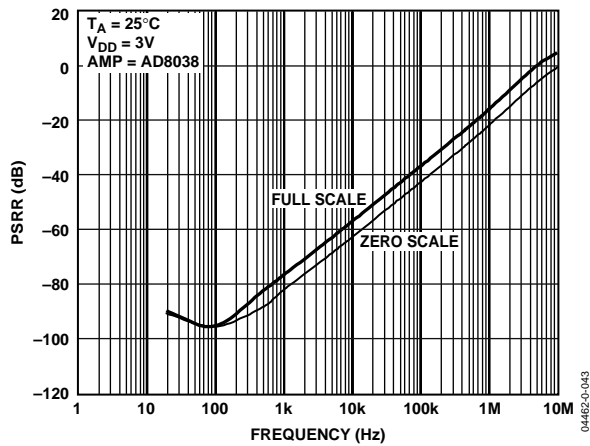
Figure 24. Power Supply Rejection vs. Frequency

Figure 25. THD + Noise vs. Frequency

Figure 26. Wideband SFDR vs. f_{OUT} Frequency

Figure 27. Wideband SFDR vs. f_{OUT} Frequency

Figure 28. Wideband SFDR, f_{OUT} = 100 kHz, Clock = 25 MHz
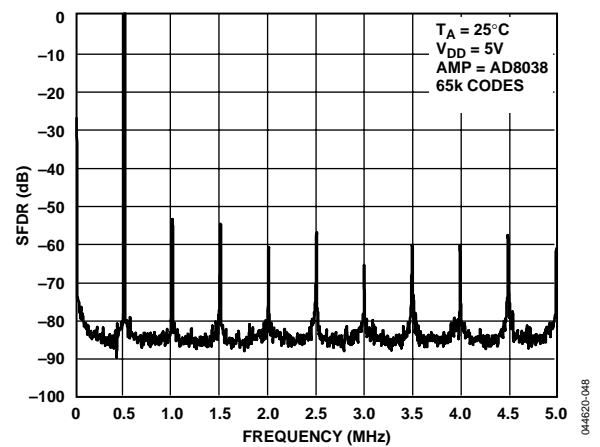
Figure 29. Wideband SFDR, f_{OUT} = 500 kHz, Clock = 10 MHz
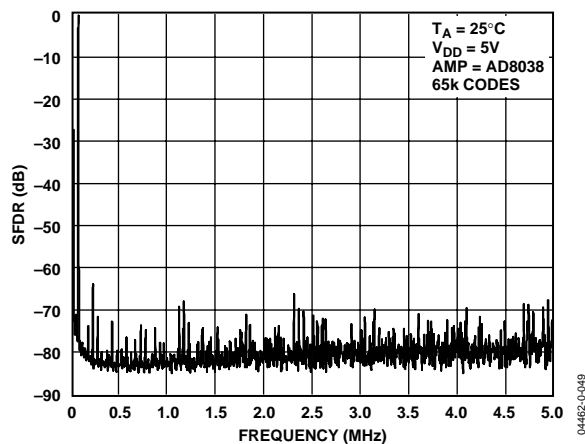
Figure 30. Wideband SFDR, f_OUT = 50 kHz, Clock = 10 MHz

Figure 31. Narrow-Band Spectral Response, f_OUT = 500 kHz, Clock = 25 MHz

Figure 32. Narrow-Band SFDR, f_OUT = 100 kHz, Clock = 25 MHz

Figure 33. Narrow-Band IMD, f_OUT = 90 kHz, 100 kHz, Clock = 10 MHz

Figure 34. Wideband IMD, f_OUT = 90 kHz, 100 kHz, Clock = 25 MHz
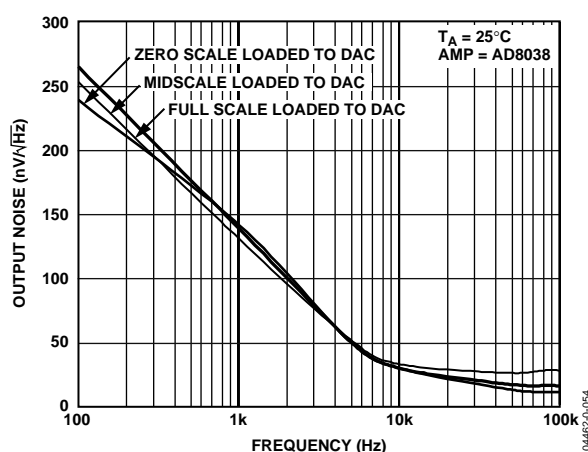
Figure 35. Output Noise Spectral Density

GENERAL DESCRIPTION

The AD5429/AD5439/AD5449 are 8-, 10-, and 12-bit dual-channel current output DACs consisting of a standard inverting R–2R ladder configuration. A simplified diagram of one DAC channel for the AD5449 is shown in Figure 36. The feedback resistor R_{FB} has a value of R. The value of R is typically 10 kΩ (minimum 8 kΩ and maximum 12 kΩ). If $I_{OUT}1$ and $I_{OUT}2$ are kept at the same potential, a constant current flows in each ladder leg, regardless of digital input code. Therefore, the input resistance presented at V_{REF} is always constant.
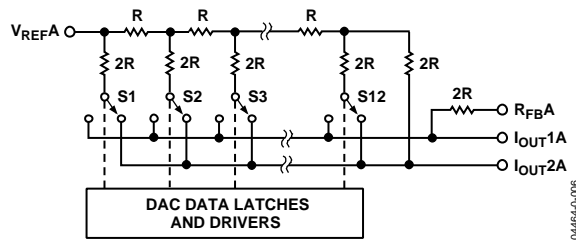
Figure 36. Simplified Ladder

Access is provided to the V_{REF}, R_{FB}, $I_{OUT}1$, and $I_{OUT}2$ terminals of the DACs, making the devices extremely versatile and allowing them to be configured in several operating modes, such as unipolar mode, bipolar output mode, or single-supply mode.

UNIPOLAR MODE

Using a single op amp, these devices can easily be configured to provide 2-quadrant multiplying operation or a unipolar output voltage swing, as shown in Figure 37.

When an output amplifier is connected in unipolar mode, the output voltage is given by

$$V_{OUT} = -V_{REF} \times D/2^n$$

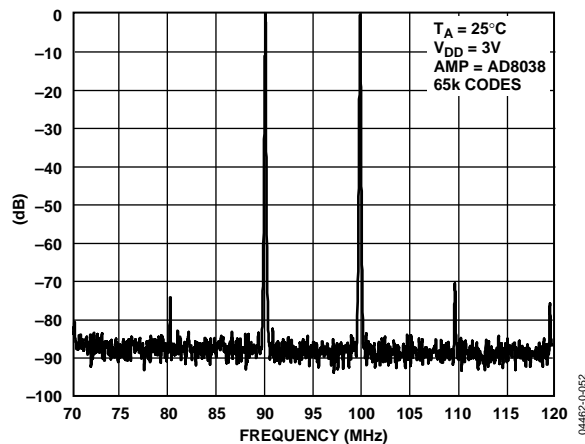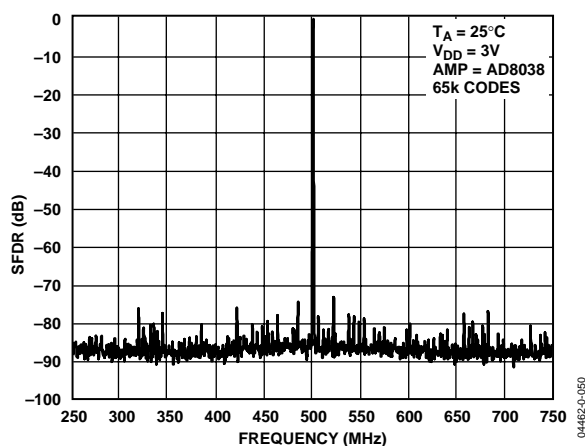where D is the fractional representation of the digital word loaded to the DAC, and n is the number of bits.

D = 0 to 255 (AD5429)
= 0 to 1023 (AD5439)
= 0 to 4095 (AD5449)

With a fixed 10 V reference, the circuit shown in Figure 37 gives a unipolar 0 V to −10 V output voltage swing. When V_{IN} is an ac signal, the circuit performs 2-quadrant multiplication.

Table 5 shows the relationship between digital code and the expected output voltage for unipolar operation for the AD5429.

Table 5. Unipolar Code Table

Digital Input	Analog Output (V)
1111 1111	$-V_{REF}$ (4095/4096)
1000 0000	$-V_{REF}$ (2048/4096) = $-V_{REF}$/2
0000 0001	$-V_{REF}$ (1/4096)
0000 0000	$-V_{REF}$ (0/4096) = 0
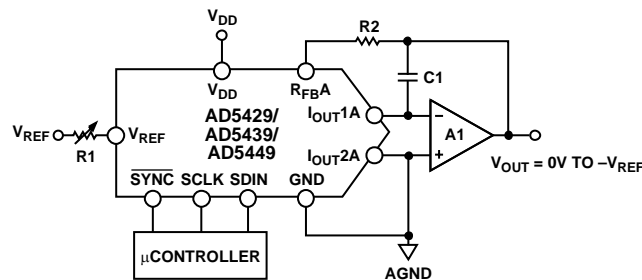
NOTES:
1. R1 AND R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
2. C1 PHASE COMPENSATION (1pF TO 2pF) MAY BE REQUIRED
   IF A1 IS A HIGH SPEED AMPLIFIER.
3. DAC B OMITTED FOR CLARITY.

Figure 37. Unipolar Operation

BIPOLAR OPERATION

In some applications, it might be necessary to generate full 4-quadrant multiplying operation or a bipolar output swing. This can be easily accomplished by using another external amplifier and three external resistors, as shown in Figure 38.

When V_{IN} is an ac signal, the circuit performs 4-quadrant multiplication. When connected in bipolar mode, the output voltage is

$$V_{OUT} = \left(V_{REF} \times D/2^{n-1}\right) - V_{REF}$$

where D is the fractional representation of the digital word loaded to the DAC, and n is the number of bits.

D = 0 to 255 (AD5429)
= 0 to 1023 (AD5439)
= 0 to 4095 (AD5449)

Table 6 shows the relationship between digital code and the expected output voltage for bipolar operation with the AD5429.

Table 6. Bipolar Code Table

Digital Input	Analog Output (V)
1111 1111	$+V_{REF}$ (2047/2048)
1000 0000	0
0000 0001	$-V_{REF}$ (2047/2048)
0000 0000	$-V_{REF}$ (2048/2048)

STABILITY

In the I-to-V configuration, the I_{OUT} of the DAC and the inverting node of the op amp must be connected as closely as possible, and proper PCB layout techniques must be employed. Because every code change corresponds to a step function, gain peaking can occur, if the op amp has limited GBP and there is excessive parasitic capacitance at the inverting node. This parasitic capacitance introduces a pole into the open loop response, which can cause ringing or instability in the closed-loop applications circuit.

As shown in Figure 37 and Figure 38, an optional compensation capacitor, C1, can be added in parallel with R_{FB} for stability. Too small a value of C1 can produce ringing at the output, while too large a value can adversely affect the settling time. C1 should be found empirically, but 1 pF to 2 pF is generally adequate for the compensation.
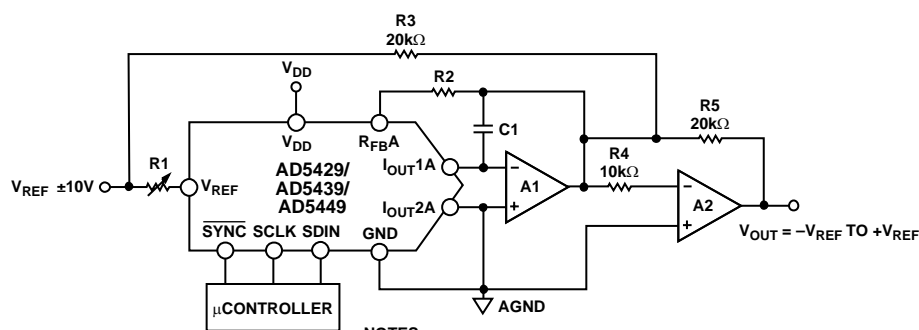
NOTES:
1. R1 AND R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
   ADJUST R1 FOR V_{OUT} = 0V WITH CODE 10000000 LOADED TO DAC.
2. MATCHING AND TRACKING IS ESSENTIAL FOR RESISTOR PAIRS
   R3 AND R4.
3. C1 PHASE COMPENSATION (1pF TO 2pF) MAY BE REQUIRED,
   IF A1/A2 IS A HIGH SPEED AMPLIFIER.
4. DAC B AND ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 38. Bipolar Operation

SINGLE-SUPPLY APPLICATIONS
Voltage-Switching Mode

Figure 39 shows the DACs operating in voltage-switching mode. The reference voltage, V_{IN}, is applied to the $I_{OUT}1$ pin, $I_{OUT}2$ is connected to AGND, and the output voltage is available at the V_{REF} terminal. In this configuration, a positive reference voltage results in a positive output voltage, making single-supply operation possible. The output from the DAC is voltage at a constant impedance (the DAC ladder resistance). Therefore, an op amp is necessary to buffer the output voltage. The reference input no longer sees a constant input impedance, but one that varies with code. So, the voltage input should be driven from a low impedance source.

Note that V_{IN} is limited to low voltages, because the switches in the DAC ladder no longer have the same source-drain drive voltage. As a result, their on resistance differs and this degrades the integral linearity of the DAC. Also, V_{IN} must not go negative by more than 0.3 V or an internal diode turns on, exceeding the maximum ratings of the device. In this type of application, the DAC's full range of multiplying capability is lost.

POSITIVE OUTPUT VOLTAGE

The output voltage polarity is opposite to the V_{REF} polarity for dc reference voltages. To achieve a positive voltage output, an applied negative reference to the input of the DAC is preferred over the output inversion through an inverting amplifier because of the resistor's tolerance errors. To generate a negative reference, the reference can be level-shifted by an op amp such that the V_{OUT} and GND pins of the reference become the virtual ground and −2.5 V, respectively, as shown in Figure 40.
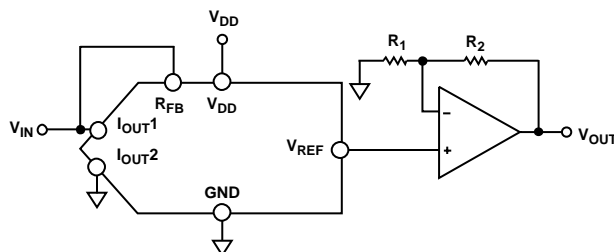
NOTES:
1. ADDITIONAL PINS OMITTED FOR CLARITY.
2. C1 PHASE COMPENSATION (1pF–2pF) MAY BE REQUIRED IF A1 IS A HIGH SPEED AMPLIFIER.

Figure 39. Single-Supply Voltage-Switching Mode
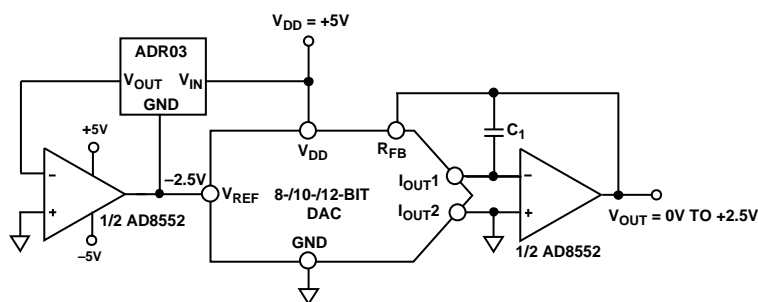
NOTES
1. ADDITIONAL PINS OMITTED FOR CLARITY.
2. C1 PHASE COMPENSATION (1pF–2pF) MAY BE REQUIRED IF A1 IS A HIGH SPEED AMPLIFIER.

Figure 40. Positive Voltage Output with Minimum Components

ADDING GAIN

In applications in which the output voltage is required to be greater than V_{IN}, gain can be added with an additional external amplifier, or it can be achieved in a single stage. Be sure to take into consideration the effect of temperature coefficients of the thin film resistors of the DAC. Simply placing a resistor in series with the R_{FB} resistor causes mismatches in the temperature coefficients, resulting in larger gain temperature coefficient errors. Instead, the circuit of Figure 41 is a recommended method of increasing the gain of the circuit. R_1, R_2, and R_3 should all have similar temperature coefficients, but they need not match the temperature coefficients of the DAC. This approach is recommended in circuits in which gains of > 1 are required.

DIVIDER OR PROGRAMMABLE GAIN ELEMENT

Current-steering DACs are very flexible and lend themselves to many different applications. If this type of DAC is connected as the feedback element of an op amp, and R_{FB} is used as the input resistor, as shown in Figure 42, then the output voltage is inversely proportional to the digital input fraction D. For $D = 1 - 2^n$ the output voltage is

$$V_{OUT} = -V_{IN} / D = -V_{IN} / \left(1 - 2^{-n}\right)$$

As D is reduced, the output voltage increases. For small values of the digital fraction D, it is important to ensure that the amplifier does not saturate and also that the required accuracy is met. For example, an 8-bit DAC driven with the binary code 0×10 (00010000)—that is, 16 decimal—in the circuit of Figure 42 should cause the output voltage to be $16 \times V_{IN}$.

However, if the DAC has a linearity specification of ±0.5 LSB, then D can, in fact, have a weight in the range 15.5/256 to 16.5/256, so that the possible output voltage is in the range 15.5 V_{IN} to 16.5 V_{IN} with an error of +3%, even though the DAC itself has a maximum error of 0.2%.

DAC leakage current is also a potential error source in divider circuits. The leakage current must be counterbalanced by an opposite current supplied from the op amp through the DAC. Because only a fraction D of the current into the V_{REF} terminal is routed to the $I_{OUT}1$ terminal, the output voltage has to change as follows:

Output Error Voltage Due to DAC Leakage = (Leakage × R)/D

where R is the DAC resistance at the V_{REF} terminal. For a DAC leakage current of 10 nA, R = 10 kΩ and a gain (that is, 1/D) of 16, the error voltage is 1.6 mV.
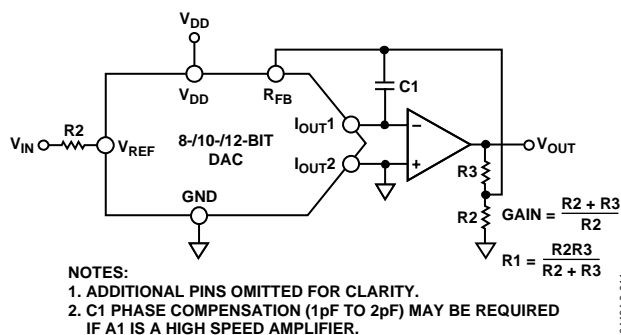

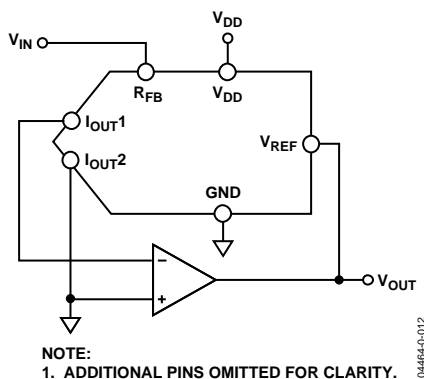*Figure 41. Increasing Gain of Current Output DAC*

Figure 42. Current-Steering DAC Used as a Divider or Programmable Gain Element

REFERENCE SELECTION

When selecting a reference for use with the AD5429/AD5439/AD5449 family of current output DACs, pay attention to the reference's output voltage temperature coefficient specification. This parameter affects not only the full-scale error, but also the linearity (INL and DNL) performance. The reference temperature coefficient should be consistent with the system accuracy specifications. For example, an 8-bit system required to hold its overall specification to within 1 LSB over the temperature range 0°C to 50°C dictates that the maximum system drift with temperature should be less than 78 ppm/°C. A 12-bit system with the same temperature range to overall specification within 2 LSBs requires a maximum drift of 10 ppm/°C. By choosing a precision reference with low output temperature coefficient, this error source can be minimized. Table 7 lists some of the references available from Analog Devices that are suitable for use with this range of current output DACs.

AMPLIFIER SELECTION

The primary requirement for the current-steering mode is an amplifier with low input bias currents and low input offset voltage. The input offset voltage of an op amp is multiplied by the variable gain (due to the code-dependent output resistance of the DAC) of the circuit. A change in this noise gain between two adjacent digital fractions produces a step change in the output voltage due to the amplifier's input offset voltage. This output voltage change is superimposed upon the desired change in output between the two codes and gives rise to a differential linearity error, which, if large enough, could cause the DAC to be nonmonotonic. The input bias current of an op amp also generates an offset at the voltage output as a result of the bias current flowing in the feedback resistor R_{FB}. Most op amps have input bias currents low enough to prevent any significant errors in 12-bit applications.

Common-mode rejection of the op amp is important in voltage-switching circuits, because it produces a code-dependent error at the voltage output of the circuit. Most op amps have adequate common-mode rejection for use at 8-, 10-, and 12-bit resolution.

Provided that the DAC switches are driven from true wideband low impedance sources (V_{IN} and AGND), they settle quickly. Consequently, the slew rate and settling time of a voltage-switching DAC circuit is determined largely by the output op amp. To obtain minimum settling time in this configuration, it is important to minimize capacitance at the V_{REF} node (voltage output node in this application) of the DAC. This is done by using low input capacitance buffer amplifiers and careful board design.

Most single-supply circuits include ground as part of the analog signal range, which in turns requires an amplifier that can handle rail-to-rail signals. Analog Devices supplies a large range of single-supply amplifiers.

Table 7. Suitable ADI Precision References Recommended for Use with AD5429/AD5439/AD5449 DACs

Reference	Output Voltage	Initial Tolerance	Temperature Drift	0.1 Hz to 10 Hz Noise	Package
ADR01	10 V	0.1%	3 ppm/°C	20 µV p-p	SC70, TSOT, SOIC
ADR02	5 V	0.1%	3 ppm/°C	10 µV p-p	SC70, TSOT, SOIC
ADR03	2.5 V	0.2%	3 ppm/°C	10 µV p-p	SC70, TSOT, SOIC
ADR425	5 V	0.04%	3 ppm/°C	3.4 µV p-p	MSOP, SOIC

Table 8. Precision ADI Op Amps Suitable for Use with AD5429/AD5439/AD5449 DACs

Part No.	Max Supply Voltage (V)	V_{OS} (max) µV	I_B (max) nA	GBP MHz	Slew Rate V/µs
OP97	±20	25	0.1	0.9	0.2
OP1177	±18	60	2	1.3	0.7
AD8551	±6	5	0.05	1.5	0.4

Table 9. High Speed ADI Op Amps Suitable for Use with AD5429/AD5439/AD5449 DACs

Part No.	Max Supply Voltage (V)	BW @ A_{CL} (MHz)	Slew Rate (V/µs)	V_{OS} (max) µV	I_B max (nA)
AD8065	±12	145	180	1500	0.01
AD8021	±12	200	100	1000	1000
AD8038	±5	350	425	3000	0.75

SERIAL INTERFACE

The AD5429/AD5439/AD5449 have an easy to use, 3-wire interface that is compatible with SPI, QSPI, MICROWIRE, and DSP interface standards. Data is written to the device in 16-bit words. This 16-bit word consists of 4 control bits and either 8, 10, or 12 data bits, as shown in Figure 43, Figure 44, and Figure 45.

Low Power Serial Interface

To minimize the power consumption of the device, the interface powers up fully only when the device is being written to, that is, on the falling edge of $\overline{SYNC}$. The SCLK and DIN input buffers are powered down on the rising edge of $\overline{SYNC}$.

DAC Control Bits C3–C0

Control bits C3 to C0 allow control of various functions of the DAC, as shown in Table 11. Default setting of the DAC at power-on are as follows.

Data is clocked into the shift register on falling clock edges; daisy-chain mode is enabled. The device powers on with zero-scale load to the DAC register and I_{OUT} lines. The DAC control bits allow the user to adjust certain features at power-on; for example, daisy-chaining can be disabled if not in use, active clock edge can be changed to rising edge, and DAC output can be cleared to either zero scale or midscale. The user can also initiate a readback of the DAC register contents for verification.

Control Register (Control Bits = 1101)

While maintaining software compatibility with the single-channel current output DACs (AD5426/AD5432/AD5443), these DACs also feature some additional interface functionality. Set the control bits to 1101 to enter control register mode. Figure 46 shows the contents of the control register. The following sections describe the functions of the control register.

SDO Control (SDO1 and SDO2)

The SDO bits enable the user to control the SDO output driver strength, disable the SDO output, or configure it as an open-drain driver. The strength of the SDO driver affects the timing of t_{12}, and, when stronger, allows a faster clock cycle.

Table 10. SDO Control Bits

SDO2	SDO1	Function Implemented
0	0	Full SDO driver
0	1	SDO configured as open-drain
1	0	Weak SDO driver
1	1	Disable SDO output

Daisy-Chain Control (DSY)

DSY allows the enabling or disabling of daisy-chain mode. A 1 enables daisy-chain mode, and 0 disables daisy-chain mode. When disabled, a readback request is accepted, SDO is automatically enabled, the DAC register contents of the relevant DAC are clocked out on SDO, and, when complete, SDO is disabled again.

Hardware $\overline{CLR}$ Bit (HCLR)

The default setting for the hardware $\overline{CLR}$ bit is to clear the registers and DAC output to zero code. A 1 in the HCLR bit allows the $\overline{CLR}$ pin to clear the DAC outputs to midscale and a 0 clears to zero scale.

Active Clock Edge (SCLK)

The default active clock edge is falling edge. Write a 1 to this bit to clock data in on the rising edge, or a 0 for falling edge.

DB15 (MSB) **DB0 (LSB)**

C3	C2	C1	C0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	0	0	0	0

|← CONTROL BITS →|←——————————————— DATA BITS ———————————————→|
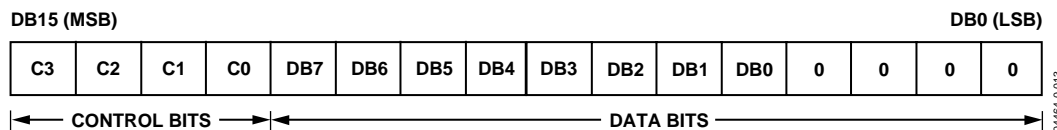
Figure 43. AD5429 8-Bit Input Shift Register Contents

DB15 (MSB) **DB0 (LSB)**

C3	C2	C1	C0	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	0	0

|← CONTROL BITS →|←——————————————— DATA BITS ———————————————→|
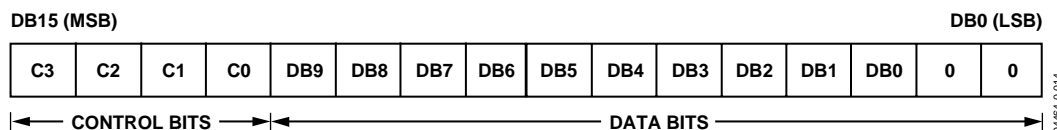
Figure 44. AD5439 10-Bit Input Shift Register Contents

DB15 (MSB) **DB0 (LSB)**

C3	C2	C1	C0	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

|← CONTROL BITS →|←——————————————— DATA BITS ———————————————→|

Figure 45. AD5449 12-Bit Input Shift Register Contents

SYNC Function

$\overline{SYNC}$ is an edge-triggered input that acts as a frame synchron-ization signal and chip enable. Data can be transferred into the device only while $\overline{SYNC}$ is low. To start the serial data transfer, $\overline{SYNC}$ should be taken low, observing the minimum $\overline{SYNC}$ falling to SCLK falling edge setup time, t_4.

Daisy-Chain Mode

Daisy-chain mode is the default power-on mode. To disable the daisy-chain function, write 1001 to the control word. In daisy-chain mode, the internal gating on SCLK is disabled. The SCLK is continuously applied to the input shift register when $\overline{SYNC}$ is low. If more than 16 clock pulses are applied, the data ripples out of the shift register and appears on the SDO line. This data is clocked out on the rising edge of SCLK (this is the default, use the control word to change the active edge) and is valid for the next device on the falling edge (default). By connecting this line to the SDIN input on the next device in the chain, a multidevice interface is con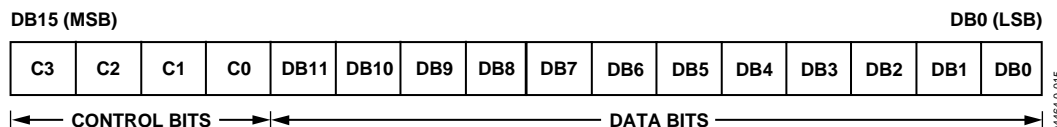structed. For each device in the system, 16 clock pulses are required. Therefore, the total number of clock cycles must equal 16, where N is the total number of devices in the chain. See Figure 3.

When the serial transfer to all devices is complete, $\overline{SYNC}$ should be taken high. This prevents additional data from being clocked into the input shift register. A burst clock containing the exact number of clock cycles can be used and $\overline{SYNC}$ taken high some time later. After the rising edge of $\overline{SYNC}$, data is automatically transferred from each device's input shift register to the addressed DAC. When control bits = 0000, the device is in no operation mode. This might be useful in daisy-chain applica-tions, in which the user does not wish to change the settings of a particular DAC in the chain. Write 0000 to the control bits for that DAC, and the following data bits are ignored.

Standalone Mode

After power-on, write 1001 to the control word to disable daisy-chain mode. The first falling edge of $\overline{SYNC}$ resets a counter that counts the number of serial clocks to ensure that the correct number of bits are shifted in and out of the serial shift registers. A $\overline{SYNC}$ edge during the 16-bit write cycle causes the device to abort the current write cycle.

After the falling edge of the 16th SCLK pulse, data is automat-ically transferred from the input shift register to the DAC. In order for another serial transfer to take place, the counter must be reset by the falling edge of $\overline{SYNC}$.

LDAC Function

The $\overline{LDAC}$ function allows asynchronous or synchronous updates to the DAC output. The DAC is asynchronously updated when this signal goes low. Alternatively, if this line is held permanently low, an automatic or synchronous update mode is selected, whereby the DAC is updated on the 16th clock falling edge when the device is in standalone mode, or on the rising edge of $\overline{SYNC}$ when in daisy-chain mode.

Table 11. DAC Control Bits

C3	C2	C1	C0	DAC	Function Implemented
0	0	0	0	A and B	No operation (power-on default)
0	0	0	1	A	Load and update
0	0	1	0	A	Initiate readback
0	0	1	1	A	Load input register
0	1	0	0	B	Load and update
0	1	0	1	B	Initiate readback
0	1	1	0	B	Load input register
0	1	1	1	A and B	Update DAC outputs
1	0	0	0	A and B	Load input registers
1	0	0	1	-	Daisy chain disable
1	0	1	0	-	Clock data to shift register on rising edge
1	0	1	1	-	Clear DAC output to zero scale
1	1	0	0	-	Clear DAC output to midscale
1	1	0	1	-	Control word
1	1	1	0	-	Reserved
1	1	1	1	-	No operation

DB15 (MSB)															DB0 (LSB)
1	1	0	1	SDO2	SDO1	DSY	HCLR	SCLK	X	X	X	X	X	X	X

|← CONTROL BITS →|
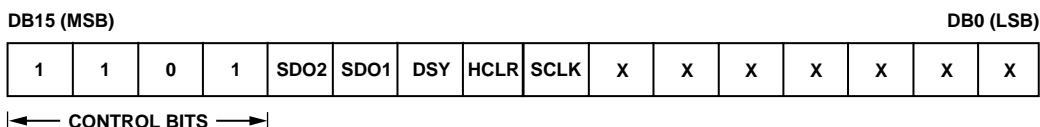
Figure 46. Control Register Loading Sequence

Software LDAC Function

Load and update mode can also function as a software update function, irrespective of the voltage level on the LDAC pin.

MICROPROCESSOR INTERFACING

Microprocessor interfacing to this family of DACs is via a serial bus that uses standard protocol compatible with microcontrollers and DSP processors. The communications channel is a 3-wire interface consisting of a clock signal, a data signal, and a synchronization signal. The AD5429/AD5439/AD5449 require a 16-bit word with the default being data valid on the falling edge of SCLK, but this is changeable via the control bits in the data-word.

ADSP-21xx to AD5429/AD5439/AD5449 Interface

The ADSP-21xx family of DSPs is easily interfaced to this family of DACs without the need for extra glue logic. Figure 47 is an example of an SPI interface between the DAC and the ADSP-2191M. SCK of the DSP drives the serial data line, DIN. SYNC is driven from one of the port lines, in this case SPIxSEL.
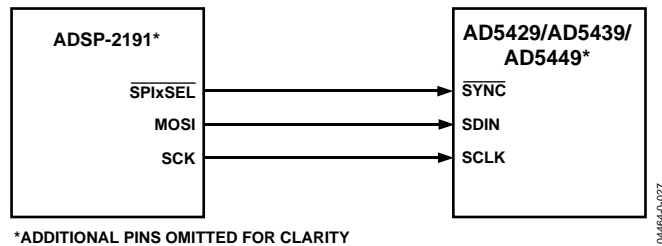

*ADDITIONAL PINS OMITTED FOR CLARITY

Figure 47. ADSP-2191 SPI to AD5429/AD5439/AD5449 Interface

A serial interface between the DAC and DSP SPORT is shown in Figure 48. In this interface example, SPORT0 is used to transfer data to the DAC shift register. Transmission is initiated by writing a word to the Tx register after the SPORT has been enabled. In a write sequence, data is clocked out on each rising edge of the DSP's serial clock and clocked into the DAC input shift register on the falling edge of its SCLK. The update of the DAC output takes place on the rising edge of the SYNC signal.
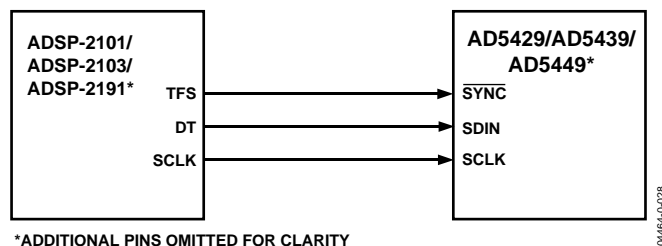

*ADDITIONAL PINS OMITTED FOR CLARITY

Figure 48. ADSP-2101/ADSP-2103/ADSP-2191 SPORT to AD5429/AD5439/AD5449 Interface

Communication between two devices at a given clock speed is possible when the following specifications are compatible: frame sync delay and frame sync setup-and-hold, data delay and data setup-and-hold, and SCLK width. The DAC interface expects a t_4 SYNC falling edge to SCLK falling edge setup time) of 13 ns minimum. See the *ADSP-21xx User Manual* for details on clock and frame sync frequencies for the SPORT register.

Table 12 shows how the SPORT control register must be set up.

Table 12.

Name	Setting	Description
TFSW	1	Alternate framing
INVTFS	1	Active low frame signal
DTYPE	00	Right-justify data
ISCLK	1	Internal serial clock
TFSR	1	Frame every word
ITFS	1	Internal framing signal
SLEN	1111	16-bit data-word

80C51/80L51 to AD5429/AD5439/AD5449 Interface

A serial interface between the DAC and the 80C51/80L51 is shown in Figure 49. TxD of the 80C51/80L51drives SCLK of the DAC serial interface, while RxD drives the serial data line, DIN. P1.1 is a bit-programmable pin on the serial port and is used to drive SYNC. When data is to be transmitted to the switch, P1.1 is taken low. The 80C51/80L51 transmit data only in 8-bit bytes; thus, only eight falling clock edges occur in the transmit cycle. To load data correctly to the DAC, P1.1 is left low after the first eight bits are transmitted, and a second write cycle is initiated to transmit the second byte of data. Data on RXD is clocked out of the microcontroller on the rising edge of TXD and is valid on the falling edge. As a result, no glue logic is required between the DAC and microcontroller interface. P1.1 is taken high following the completion of this cycle. The 80C51/80L51 provide the LSB of the SBUF register as the first bit in the data stream. The DAC input register requires its data with the MSB as the first bit received. The transmit routine should take this into account.
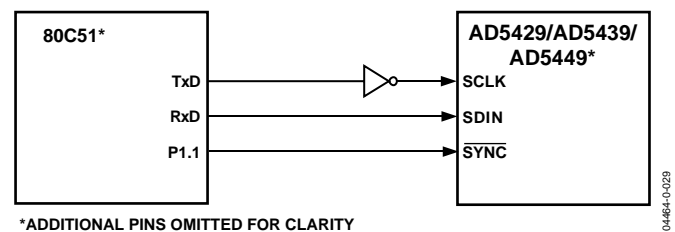

*ADDITIONAL PINS OMITTED FOR CLARITY

Figure 49. 80C51/80L51 to AD5429/AD5439/AD5449 Interface

MC68HC11 to AD5429/AD5439/AD5449 Interface

Figure 50 is an example of a serial interface between the DAC and the MC68HC11 microcontroller. The serial peripheral interface (SPI) on the MC68HC11 is configured for master mode (MSTR) = 1, clock polarity bit (CPOL) = 0, and the clock phase bit (CPHA) = 1. The SPI is configured by writing to the SPI control register (SPCR)—see the *68HC11 User Manual.* The SCK of the 68HC11 drives the SCLK of the DAC interface; the MOSI output drives the serial data line (D_{IN}) of the AD5429/AD5439/AD5449.

The $\overline{SYNC}$ signal is derived from a port line (PC7). When data is being transmitted to the AD5429/AD5439/AD5449, the $\overline{SYNC}$ line is taken low (PC7). Data appearing on the MOSI output is valid on the falling edge of SCK. Serial data from the 68HC11 is transmitted in 8-bit bytes with only 8 falling clock edges occurring in the transmit cycle. Data is transmitted MSB first. To load data to the DAC, PC7 is left low after the first eight bits are transferred, and a second serial write operation is performed to the DAC. PC7 is taken high at the end of this procedure.
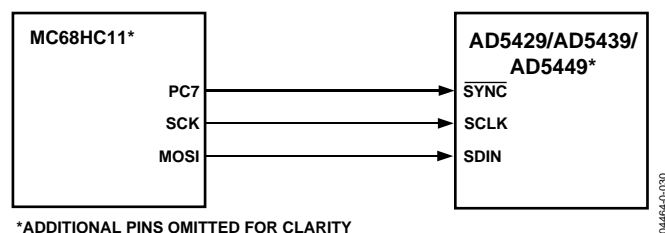

*ADDITIONAL PINS OMITTED FOR CLARITY

Figure 50. MCH68HC11/68L11 to AD5429/AD5439/AD5449 Interface

If the user wants to verify the data previously written to the input shift register, the SDO line can be connected to MISO of the MC68HC11, and, with $\overline{SYNC}$ low, the shift register clocks data out on the rising edges of SCLK.

MICROWIRE to AD5429/AD5439/AD5449 Interface

Figure 51 shows an interface between the DAC and any MICROWIRE compatible device. Serial data is shifted out on the falling edge of the serial clock, SK, and is clocked into the DAC input shift register on the rising edge of SK, which corresponds to the falling edge of the DAC's SCLK.
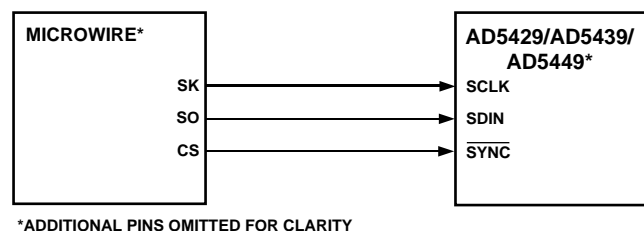

*ADDITIONAL PINS OMITTED FOR CLARITY

Figure 51. MICROWIRE to AD5429/AD5439/AD5449 Interface

PIC16C6x/7x to AD5429/AD5439/AD5449

The PIC16C6x/7x synchronous serial port (SSP) is configured as an SPI master with the clock polarity bit (CKP) = 0. This is done by writing to the synchronous serial port control register (SSPCON). See the *PIC16/17 Microcontroller User Manual.* In this example, the I/O port RA1 is used to provide a $\overline{SYNC}$ signal and enable the serial port of the DAC. This micro-controller transfers only eight bits of data during each serial transfer operation; therefore, two consecutive write operations are required. Figure 52 shows the connection diagram.
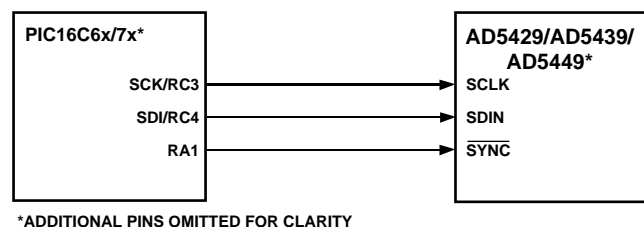

*ADDITIONAL PINS OMITTED FOR CLARITY

Figure 52. PIC16C6x/7x to AD5429/AD5439/AD5449 Interface

PCB LAYOUT AND POWER SUPPLY DECOUPLING

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the DAC is mounted should be designed so that the analog and digital sections are separated and confined to certain areas of the board. If the DAC is in a system in which multiple devices require an AGND to DGND connection, the connection should be made at one point only. The star ground point should be established as close as possible to the device.

These DACs should have ample supply bypassing of 10 μF in parallel with 0.1 μF on the supply located as close to the package as possible, ideally right up against the device. The 0.1 μF capacitor should have low effective series resistance (ESR) and effective series inductance (ESI), like the common ceramic types that provide a low impedance path to ground at high frequencies, to handle transient currents due to internal logic switching. Low ESR 1 μF to 10 μF tantalum or electrolytic capacitors should also be applied at the supplies to minimize transient disturbance and filter out low frequency ripple.

Fast switching signals such as clocks should be shielded with digital ground to avoid radiating noise to other parts of the board, and should never be run near the reference inputs.

Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough on the board. A microstrip technique is by far the best, but not always possible with a double-sided board. In this technique, the component side of the board is dedicated to the ground plane, while signal traces are placed on the soldered side.

It is good practice to employ compact, minimum lead-length PCB layout design. Leads to the input should be as short as possible to minimize IR drops and stray inductance.

The PCB metal traces between V_{REF} and R_{FB} should also be matched to minimize gain error. To maximize high frequency performance, the I-to-V amplifier should be located as close to the device as possible.

## POWER SUPPLIES FOR THE EVALUATION BOARD

The board requires ±12 V and +5 V supplies. The 12 V V_{DD} and V_{SS} are used to power the output amplifier, while the 5 V is used to power the DAC (V_{DD1}) and transceivers (V_{CC}).

Both supplies are decoupled to their respective ground plane with 10 μF tantalum and 0.1 μF ceramic capacitors.

EVALUATION BOARD FOR THE DACS

The evaluation board includes a DAC from the AD5429/ AD5439/AD5449 family and a current-to-voltage amplifier, AD8065. On the evaluation board is a 10 V reference, ADR01. An external reference can also be applied via an SMB input.

The evaluation kit consists of a CD-ROM with self-installing PC software to control the DAC. The software allows the user to write a code to the device.
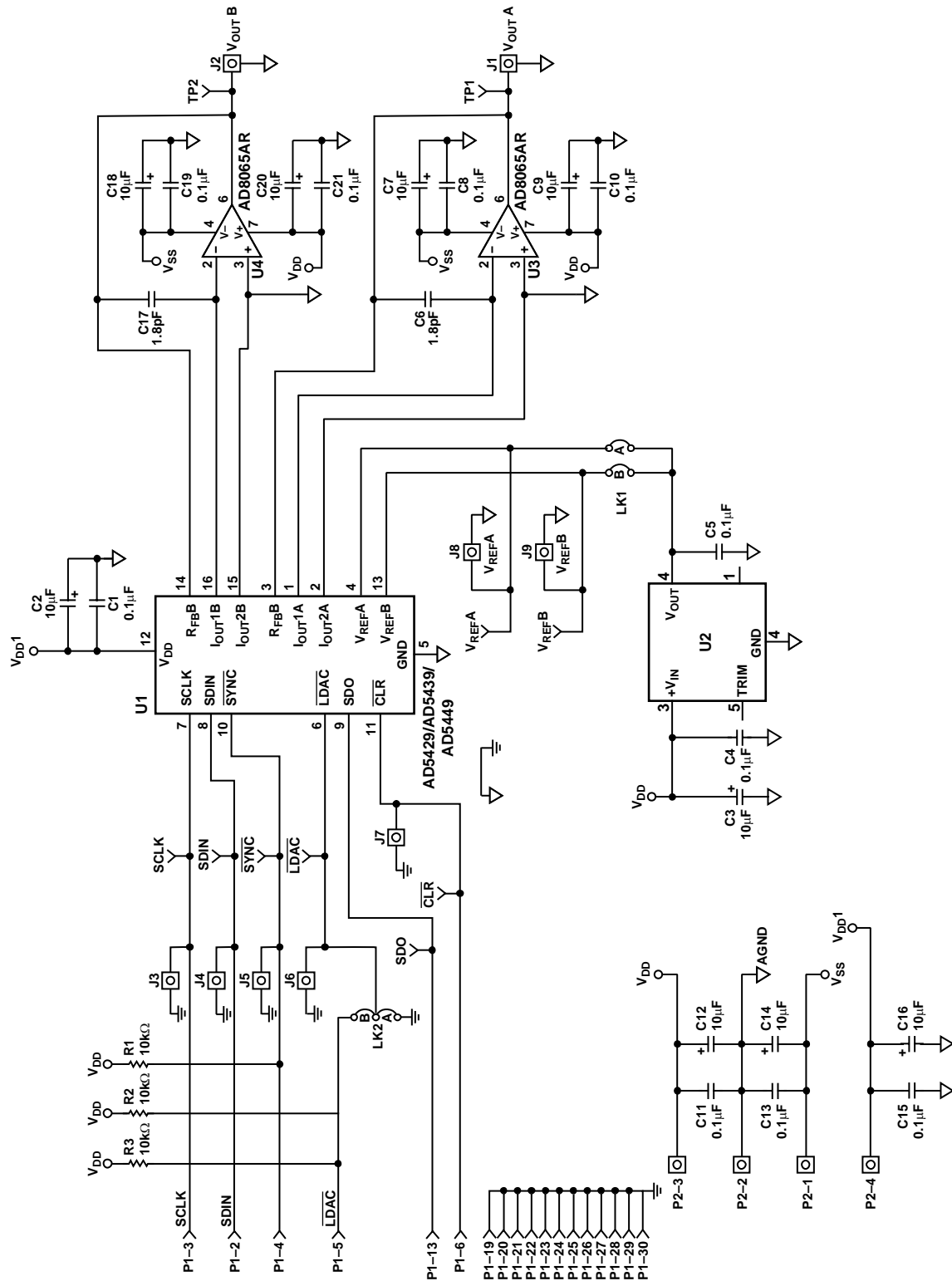
Figure 53. Schematic of the Evaluation Board

04464-0-023

Figure 54. Component-Side Artwork
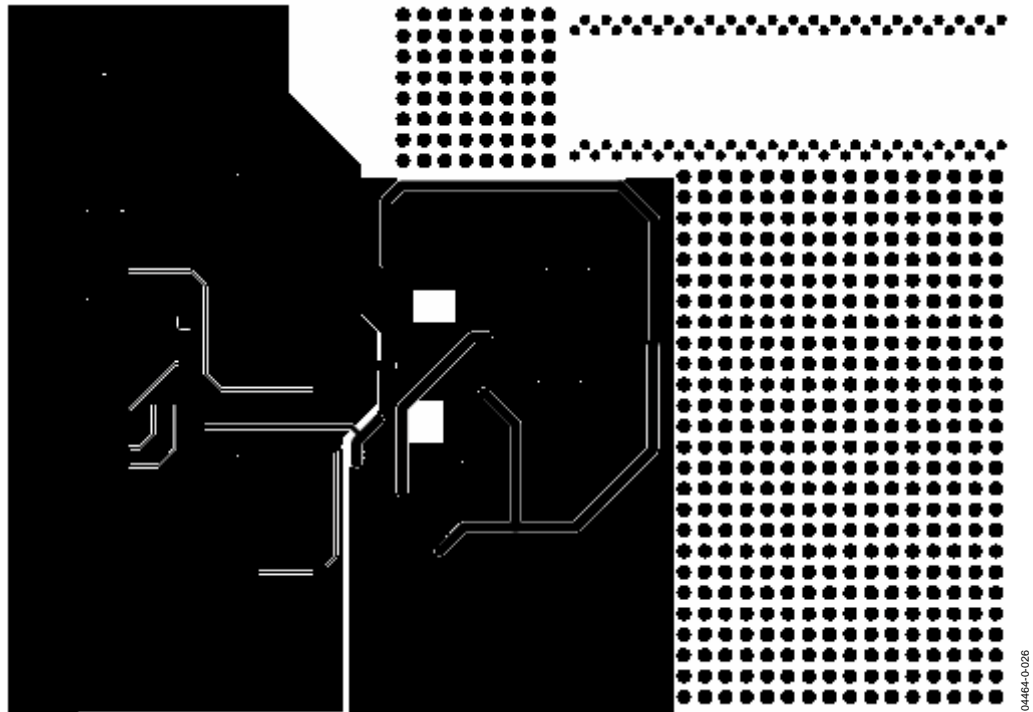

Figure 55. Silkscreen—Component-Side View (Top)

Figure 56. Solder-Side Artwork

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OVERVIEW OF AD54xx DEVICES

Table 13.

Part No.	Resolution	No. DACs	INL (LSB)	Interface	Package	Features
AD5424	8	1	±0.25	Parallel	RU-16, CP-20	10 MHz BW, 17 ns $\overline{CS}$ Pulse Width
AD5426	8	1	±0.25	Serial	RM-10	10 MHz BW, 50 MHz Serial
AD5428	8	2	±0.25	Parallel	RU-20	10 MHz BW, 17 ns $\overline{CS}$ Pulse Width
AD5429	8	2	±0.25	Serial	RU-10	10 MHz BW, 50 MHz Serial
AD5450	8	1	±0.25	Serial	RJ-8	10 MHz BW, 50 MHz Serial
AD5432	10	1	±0.5	Serial	RM-10	10 MHz BW, 50 MHz Serial
AD5433	10	1	±0.5	Parallel	RU-20, CP-20	10 MHz BW, 17 ns $\overline{CS}$ Pulse Width
AD5439	10	2	±0.5	Serial	RU-16	10 MHz BW, 50 MHz Serial
AD5440	10	2	±0.5	Parallel	RU-24	10 MHz BW, 17 ns $\overline{CS}$ Pulse Width
AD5451	10	1	±0.25	Serial	RJ-8	10 MHz BW, 50 MHz Serial
AD5443	12	1	±1	Serial	RM-10	10 MHz BW, 50 MHz Serial
AD5444	12	1	±0.5	Serial	RM-8	10 MHz BW, 50 MHz Serial
AD5415	12	2	±1	Serial	RU-24	10 MHz BW, 58 MHz Serial
AD5445	12	2	±1	Parallel	RU-20, CP-20	10 MHz BW, 17 ns $\overline{CS}$ Pulse Width
AD5447	12	2	±1	Parallel	RU-24	10 MHz BW, 17 ns $\overline{CS}$ Pulse Width
AD5449	12	2	±1	Serial	RU-16	10 MHz BW, 50 MHz Serial
AD5452	12	1	±0.5	Serial	RJ-8, RM-8	10 MHz BW, 50 MHz Serial
AD5446	14	1	±1	Serial	RM-8	10 MHz BW, 50 MHz Serial
AD5453	14	1	±2	Serial	UJ-8, RM-8	10 MHz BW, 50 MHz Serial
AD5553	14	1	±1	Serial	RM-8	4 MHz BW, 50 MHz Serial Clock
AD5556	14	1	±1	Parallel	RU-28	4 MHz BW, 20 ns $\overline{WR}$ Pulse Width
AD5555	14	2	±1	Serial	RM-8	4 MHz BW, 50 MHz Serial Clock
AD5557	14	2	±1	Parallel	RU-38	4 MHz BW, 20 ns $\overline{WR}$ Pulse Width
AD5543	16	1	±2	Serial	RM-8	4 MHz BW, 50 MHz Serial Clock
AD5546	16	1	±2	Parallel	RU-28	4 MHz BW, 20 ns $\overline{WR}$ Pulse Width
AD5545	16	2	±2	Serial	RU-16	4 MHz BW, 50 MHz Serial Clock
AD5547	16	2	±2	Parallel	RU-38	4 MHz BW, 20 ns $\overline{WR}$ Pulse Width

OUTLINE DIMENSIONS
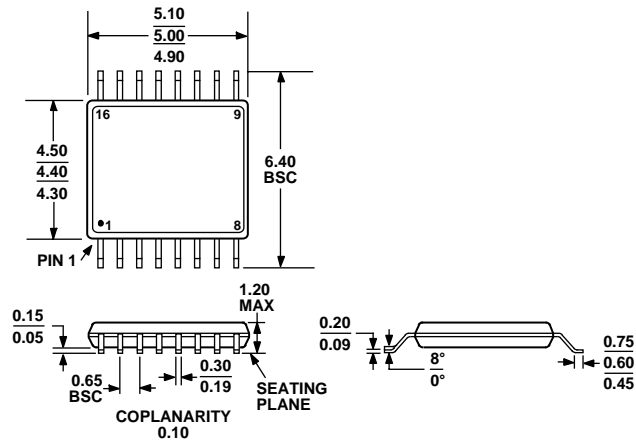
COMPLIANT TO JEDEC STANDARDS MO-153AB

Figure 57. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Resolution	INL (LSBs)	Temperature Range	Package Description	Package Option
AD5429YRU	8	±0.5	−40°C to +125°C	TSSOP	RU-16
AD5429YRU-REEL	8	±0.5	−40°C to +125°C	TSSOP	RU-16
AD5429YRU-REEL7	8	±0.5	−40°C to +125°C	TSSOP	RU-16
AD5439YRU	10	±0.5	−40°C to +125°C	TSSOP	RU-16
AD5439YRU-REEL	10	±0.5	−40°C to +125°C	TSSOP	RU-16
AD5439YRU-REEL7	10	±0.5	−40°C to +125°C	TSSOP	RU-16
AD5449YRU	12	±1	−40°C to +125°C	TSSOP	RU-16
AD5449YRU-REEL	12	±1	−40°C to +125°C	TSSOP	RU-16
AD5449YRU-REEL7	12	±1	−40°C to +125°C	TSSOP	RU-16
EVAL-AD5429EB				Evaluation Board	
EVAL-AD5439EB				Evaluation Board	
EVAL-AD5449EB				Evaluation Board	

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