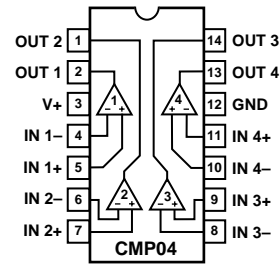


FEATURES

- High Gain: 200 V/mV typ
- Single or Dual Supply Operation
- Input Voltage Range Includes Ground
- Low Power Consumption (1.5 mW/Comparator)
- Low Input Bias Current: 100 nA max
- Low Input Offset Current: 10 nA max
- Low Offset Voltage: 1 mV max
- Low Output Saturation Voltage: 250 mV @ 4 mA
- Logic Output Compatible with TTL, DTL, ECL, MOS and CMOS
- Directly Replaces LM139/239/339 Comparators
- Available in Die Form

PIN CONNECTIONS

- 14-Lead Cerdip
- 14-Lead Plastic DIP
- 14-Lead SOIC



GENERAL DESCRIPTION

Four precision independent comparators comprise the CMP04. Performance highlights include a very low offset voltage, low output saturation voltage and high gain in a single supply design. The input voltage range includes ground for single supply operation and V^- for split supplies. A low power supply current of 2 mA, which is independent of supply voltage, makes this the preferred comparator for precision applications requiring minimal power consumption. Maximum logic interface flexibility is offered by the open-collector TTL output.

TYPICAL INTERFACE

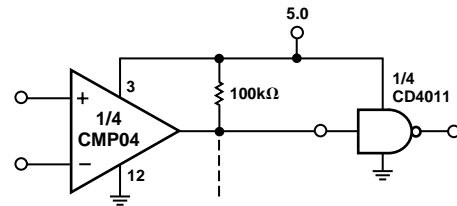


Figure 2a. Driving CMOS

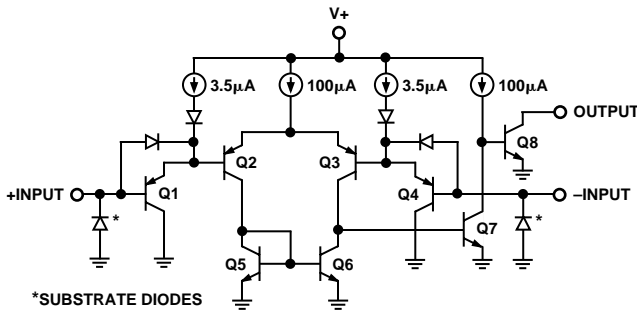


Figure 1. Simplified Schematic (1/4 CMP04)

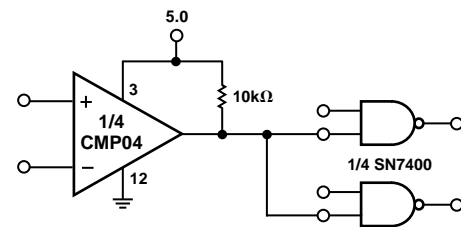


Figure 2b. Driving TTL

REV. C

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CMP04—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ $V_+ = +5\text{ V}$, $T_A = +25^\circ\text{C}$, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Offset Voltage	V_{OS}	$R_S = 0\ \Omega$, $R_L = 5.1\ \text{k}\Omega$, $V_O = 1.4\ \text{V}^1$		0.4	1	mV
Input Offset Current	I_{OS}	$I_{IN(+)} - I_{IN(-)}$, $R_L = 5.1\ \text{k}\Omega$, $V_O = 1.4\ \text{V}$		2	10	nA
Input Bias Current	I_B	$I_{IN(+)}$ or $I_{IN(-)}$		25	100	nA
Voltage Gain	A_V	$R_L \geq 15\ \text{k}\Omega$, $V_+ = 15\ \text{V}^2$	80	200		V/mV
Large-Signal Response Time	t_r	$V_{IN} = \text{TTL Logic Swing}$, $V_{REF} = 1.4\ \text{V}^3$ $V_{RL} = 5\ \text{V}$, $R_L = 5.1\ \text{k}\Omega$		300		ns
Small-Signal Response Time	t_r	$V_{IN} = 100\ \text{mV Step}^3$, $5\ \text{mV Overdrive}$ $V_{RL} = 5\ \text{V}$, $R_L = 5.1\ \text{k}\Omega$		1.3		μs
Input Voltage Range	CMVR	(Note 4)	0		$V_+ - 1.5$	V
Common-Mode Rejection Ratio	CMRR	(Notes 2, 5)	80	100		dB
Power Supply Rejection Ratio	PSRR	$V_+ = +5\ \text{V}$ to $+18\ \text{V}^2$	80	100		dB
Saturation Voltage	V_{OL}	$V_{IN(-)} \geq 1\ \text{V}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4\ \text{mA}$		250	400	mV
Output Sink Current	I_{SINK}	$V_{IN(-)} \geq 1\ \text{V}$, $V_{IN(+)} = 0$, $V_O \leq 1.5\ \text{V}$	6	16		mA
Output Leakage Current	I_{LEAK}	$V_{IN(+)} \geq 1\ \text{V}$, $V_{IN(-)} = 0$, $V_O = 30\ \text{V}$		0.1	100	nA
Supply Current	I_+	$R_L = \infty$, All Comps $V_+ = 30\ \text{V}$		0.8	2.0	mA

NOTES

¹At output switch point, $V_O = 1.4\ \text{V}$, $R_S = 0\ \Omega$ with V_+ from $5\ \text{V}$; and over the full input common-mode range ($0\ \text{V}$ to $V_+ - 1.5\ \text{V}$).

²Guaranteed by design.

³Sample tested.

⁴The input common-mode voltage or input signal voltage should not be allowed to go negative by more than $0.3\ \text{V}$. The upper end of the common-mode voltage range is $V_+ - 1.5\ \text{V}$, but either or both inputs can go to $+30\ \text{V}$ without damage.

⁵ $R_L \geq 15\ \text{k}\Omega$, $V_+ = 15\ \text{V}$, $V_{CM} = 1.5\ \text{V}$ to $13.5\ \text{V}$.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS¹

Supply Voltage	36 V or $\pm 18\ \text{V}$
Differential Input Voltage	36 V dc
Input Voltage	$-0.3\ \text{V}$ to $+36\ \text{V}$
Operating Temperature Range	
CMP04BY	-55°C to $+125^\circ\text{C}$
CMP04FP, FS	-40°C to $+85^\circ\text{C}$
Junction Temperature (T_J)	-65°C to $+150^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
(P Suffix)	-65°C to $+125^\circ\text{C}$
Input Current ($V_{IN} < -3.0\ \text{V}$)	50 mA
Output Short-Circuit to GND	Continuous
Lead Temperature (Soldering, 60 sec)	$+300^\circ\text{C}$

Package Type	θ_{JA}^2	θ_{JC}	Units
14-Lead Hermetic DIP (Y)	94	10	$^\circ\text{C}/\text{W}$
14-Lead Plastic DIP (P)	83	39	$^\circ\text{C}/\text{W}$
14-Lead SOIC	120	36	$^\circ\text{C}/\text{W}$

NOTES

¹Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

² θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for cerdip and plastic DIP packages; θ_{JA} is specified for device soldered to printed circuit board for SO package.

ORDERING GUIDE

Model	$T_A = +25^\circ\text{C}$ V_{OS}	Temperature Ranges	Package Descriptions	Package Options
CMP04BY/883C	1 mV	-55°C to $+125^\circ\text{C}$	14-Lead Cerdip	Q-14
CMP04FP	1 mV	-40°C to $+85^\circ\text{C}$	14-Lead Plastic DIP	N-14
CMP04FS	1 mV	-40°C to $+85^\circ\text{C}$	14-Lead SOIC	R-14/SO-14

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as $4000\ \text{V}$ readily accumulate on the human body and test equipment and can discharge without detection. Although the CMP04 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



ELECTRICAL CHARACTERISTICS (@ $V_+ = +5\text{ V}$, $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ for CMP04BY, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ for CMP04FP/FS, unless otherwise noted)

Parameter	Symbol	Conditions	CMP04B/F ¹			Units
			Min	Typ	Max	
Input Offset Voltage	V_{OS}	$R_S = 0\ \Omega$, $R_L = 5.1\ \text{k}\Omega$ $V_O = 1.4\ \text{V}^2$		1	2	mV
				1	2	mV
Input Offset Current	I_{OS}	$I_{IN(+)} - I_{IN(-)}$ $R_L = 5.1\ \text{k}\Omega$ $V_O = 1.4\ \text{V}$		4	20	nA
				4	20	nA
				4	20	nA
Input Bias Current	I_B	$I_{IN(+)}$ or $I_{IN(-)}$		40	200	nA
Voltage Gain	A_V	$R_L \geq 15\ \text{k}\Omega$, $V_+ = 15\ \text{V}^3$	70	125		V/mV
Large-Signal Response Time	t_r	$V_{IN} = \text{TTL Logic Swing}$ $V_{REF} = 1.4\ \text{V}^4$ $V_{RL} = 5\ \text{V}$, $R_L = 5.1\ \text{k}\Omega$		300		ns
				300		ns
				300		ns
Small-Signal Response Time	t_r	$V_{IN} = 100\ \text{mV Step}^4$ 5 mV Overdrive $V_{RL} = 5\ \text{V}$, $R_L = 5.1\ \text{k}\Omega$		1.3		μs
				1.3		μs
				1.3		μs
Input Voltage Range	CMVR	(Note 5)	0		$V_+ - 1.5$	V
Common-Mode Rejection Ratio	CMRR	(Notes 1, 3)	60	100		dB
Power Supply Rejection Ratio	PSRR	$V_+ = +5\ \text{V}$ to $+18\ \text{V}$	80	100		dB
Saturation Voltage	V_{OL}	$V_{IN(-)} \geq 1\ \text{V}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4\ \text{mA}$		250	700	mV
				250	700	mV
Output Sink Current	I_{SINK}	$V_{IN(-)} \geq 1\ \text{V}$, $V_{IN(+)} = 0$, $V_O \leq 1.5\ \text{V}$	5	16		mA
			5	16		mA
Output Leakage Current	I_{LEAK}	$V_{IN(+)} \geq 1\ \text{V}$, $V_{IN(-)} = 0$, $V_O = 30\ \text{V}$		0.1	200	nA
				0.1	200	nA
Supply Current	I_+	$R_L = \infty$, All Comps $V_+ = 30\ \text{V}$		1.2	3.0	mA
				1.2	3.0	mA

NOTES

¹ $R_L \geq 15\ \text{k}\Omega$, $V_+ = 15\ \text{V}$, $V_{CM} = 1.5\ \text{V}$ to $13.5\ \text{V}$.

²At output switch point, $V_O = 1.4\ \text{V}$, $R_S = 0\ \Omega$ with V_+ from $5\ \text{V}$; and over the full input common-mode range ($0\ \text{V}$ to $V_+ - 1.5\ \text{V}$).

³Guaranteed by design.

⁴Sample tested.

⁵The input common-mode voltage or input signal voltage should not be allowed to go negative by more than $0.3\ \text{V}$. The upper end of the common-mode voltage range is $V_+ - 1.5\ \text{V}$, but either or both inputs can go to $+30\ \text{V}$ without damage.

Specifications subject to change without notice.

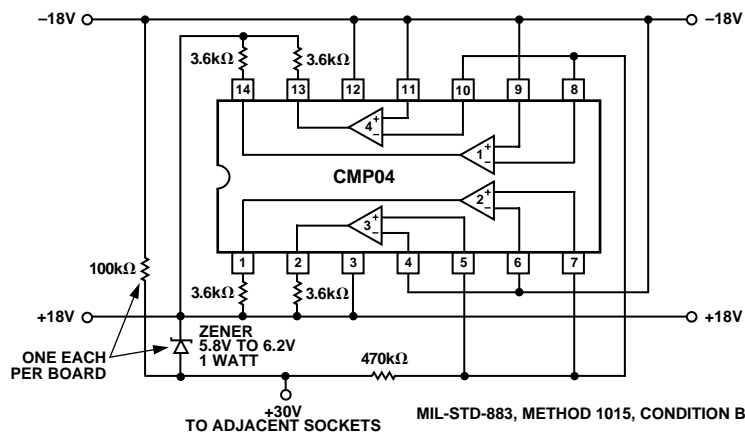
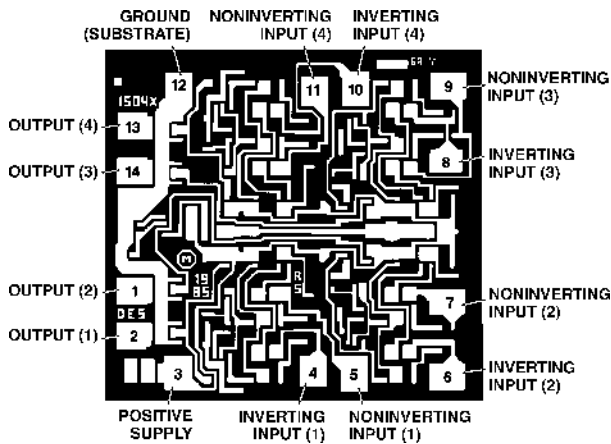


Figure 3. Burn-In Circuit

CMP04

DICE CHARACTERISTICS



DIE SIZE 0.058 × 0.055 inch, 3190 sq. mils
(1.47 × 1.40 mm, 2.058 sq. mm)

WAFER TEST LIMITS (@ V₊ = +5 V, T_A = +25°C, unless otherwise noted)

Parameter	Symbol	Conditions	CMP04N Limit	CMP04G Limit	Units
Input Offset Voltage	V _{OS}	R _S = 0 Ω, R _L = 5.1 kΩ V _O = 1.4 V ¹	1	2	mV max
Input Offset Current	I _{OS}	I _{IN(+)} - I _{IN(-)} R _L = 5.1 kΩ V _O = 1.4 V	10	25	nA max
Input Bias Current	I _B	I _{IN(+)} or I _{IN(-)} ¹	100	100	nA max
Voltage Gain	A _V	R _L ≥ 15 kΩ, V ₊ = 15 V ³	80	50	V/mV min
Input Voltage Range	CMVR	(Notes 2, 3)	V ₊ -1.5	V ₊ -1.5	V max
Common-Mode Rejection Ratio	CMRR	(Note 4)	80	80	dB min
Power Supply Rejection Ratio	PSRR	V ₊ = +5 V to +18 V	80	80	dB min
Saturation Voltage	V _{OL}	V _{IN(-)} ≥ 1 V, V _{IN(+)} = 0, I _{SINK} ≤ 4 mA	400	400	mV max
Output Sink Current	I _{SINK}	V _{IN(-)} ≥ 1 V, V _{IN(+)} = 0, V _O ≤ 1.5 V	6	6	mA min
Output Leakage Current	I _{LEAK}	V _{IN(+)} ≥ 1 V, V _{IN(-)} = 0, V _O = 30 V	100	100	nA max
Supply Current	I ₊	R _L = ∞, All Comps V ₊ = 30 V	2	2	mA max

NOTES

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS (@ V₊ = +5 V, unless otherwise noted)

Parameter	Symbol	Conditions	CMP04N Typical	CMP04G Typical	Units
Large-Signal Response Time	t _r	V _{IN} = TTL Logic Swing V _{REF} = 1.4 V ⁵ V _{RL} = 5 V, R _L = 5.1 kΩ	600	600	ns
Small-Signal Response Time	t _r	V _{IN} = 100 mV Step ⁵ 5 mV Overdrive V _{RL} = 5 V, R _L = 5.1 kΩ	1.3	1.3	μs

NOTES

¹At output switch point, V_O = 1.4 V, R_S = 0 Ω with V₊ from 5 V; and over the full input common-mode range (0 V to V₊ -1.5 V).

²The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V₊ -1.5 V, but either or both inputs can go to +30 V without damage.

³Guaranteed by design.

⁴R_L ≥ 15 kΩ. V_{CM} = 1.5 V to 13.5 V.

⁵Sample tested.

Specifications subject to change without notice.

Typical Performance Characteristics

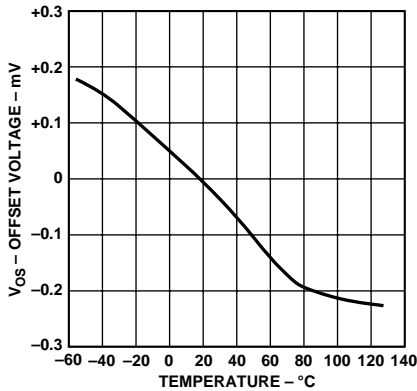


Figure 4. Offset Voltage vs. Temperature

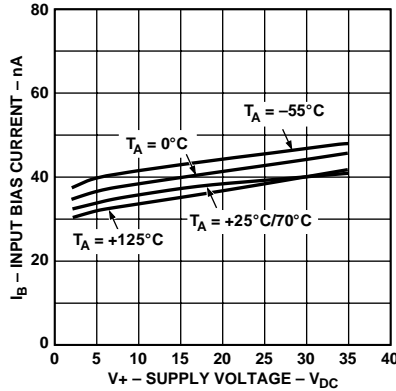


Figure 5. Input Bias Current vs. V_+ and Temperature

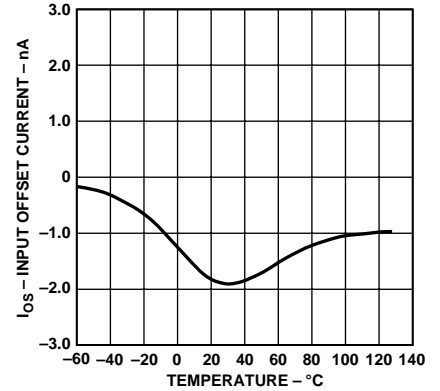


Figure 6. Input Offset Current vs. Temperature

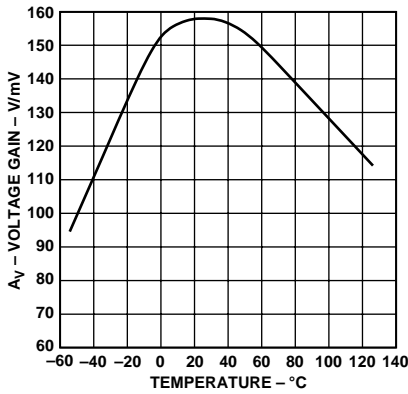


Figure 7. Voltage Gain vs. Temperature

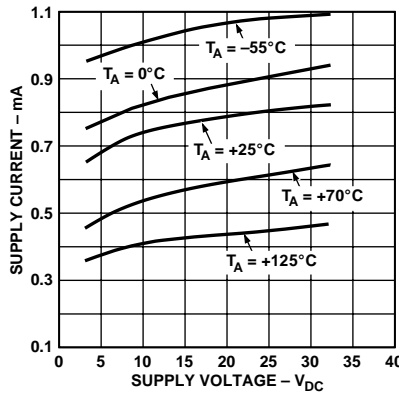


Figure 8. Supply Current vs. Supply Voltage

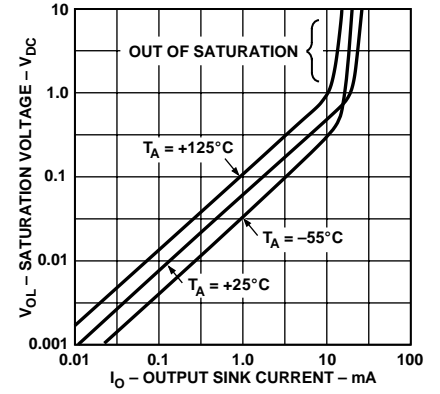


Figure 9. Output Voltage vs. Output Current and Temperature

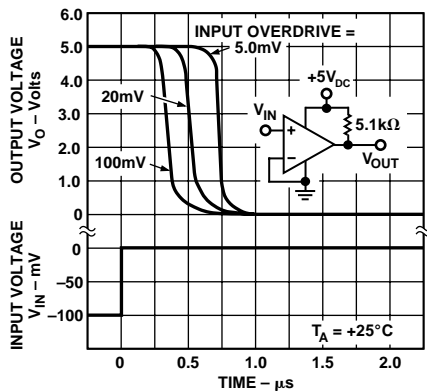


Figure 10. Response Time for Various Input Overdrives—Negative Transition

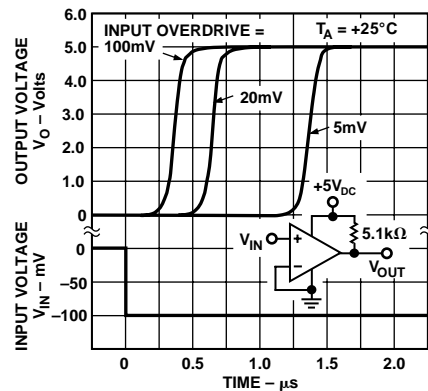


Figure 11. Response Time for Various Input Overdrives—Positive Transition

CMP04

TYPICAL APPLICATIONS

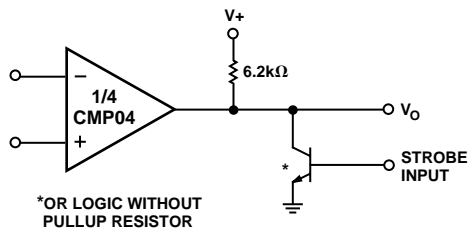


Figure 12. Output Strobing

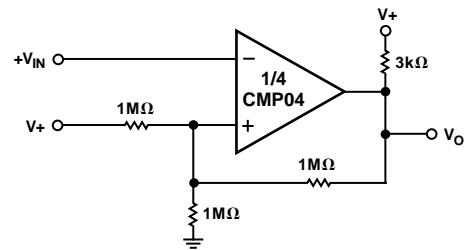


Figure 15. Inverting Comparator with Hysteresis

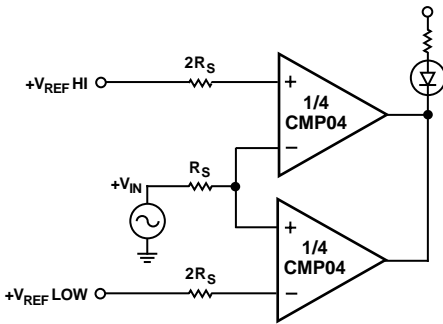


Figure 13. Limit Comparator

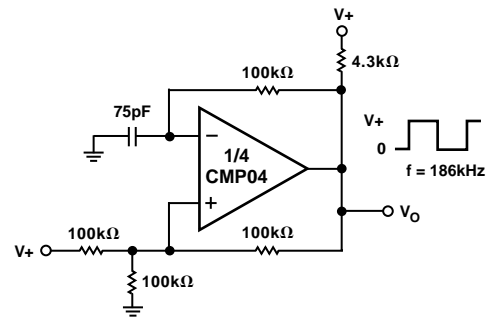


Figure 16. Square Wave Oscillator

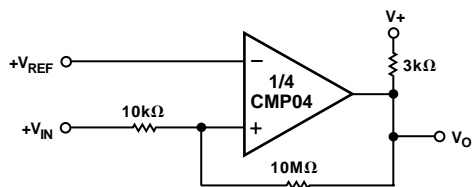


Figure 14. Noninverting Comparator with Hysteresis

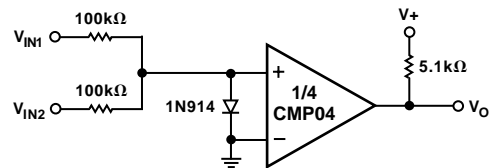


Figure 17. Comparing Input Voltages of Opposite Polarity

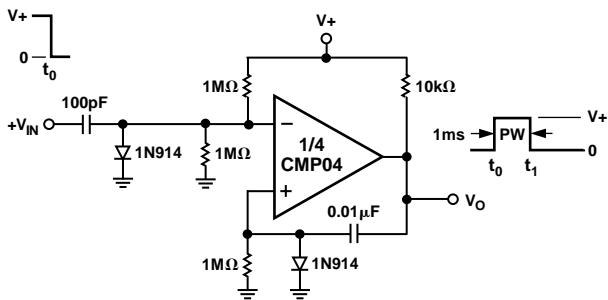


Figure 18. One-Shot Multivibrator

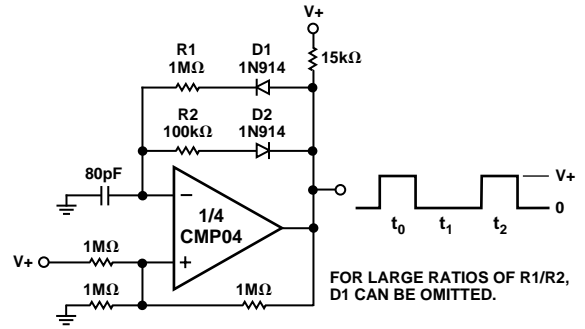


Figure 20. Pulse Generator

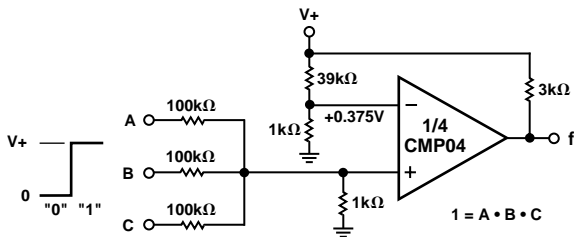


Figure 19. AND Gate

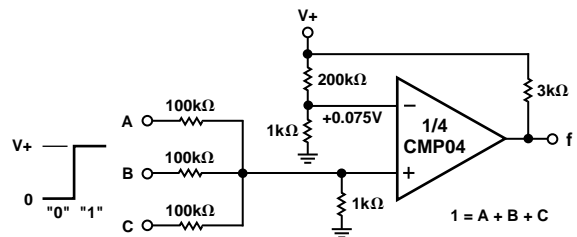


Figure 21. OR Gate

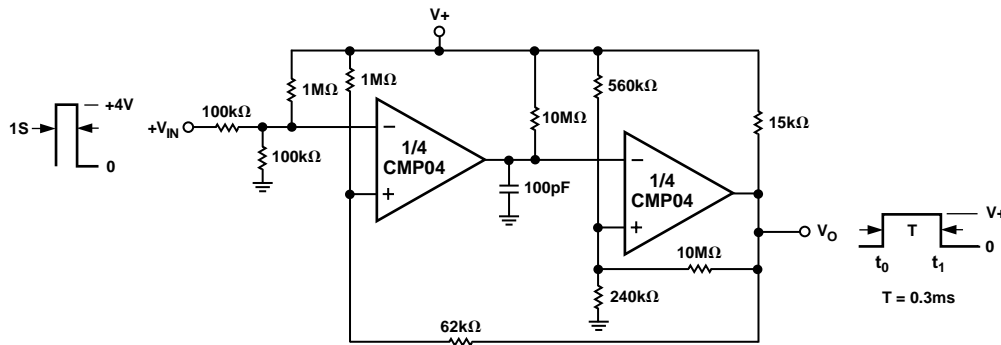


Figure 22. One-Shot Multivibrator with Input Lockout

CMP04

TYPICAL APPLICATIONS

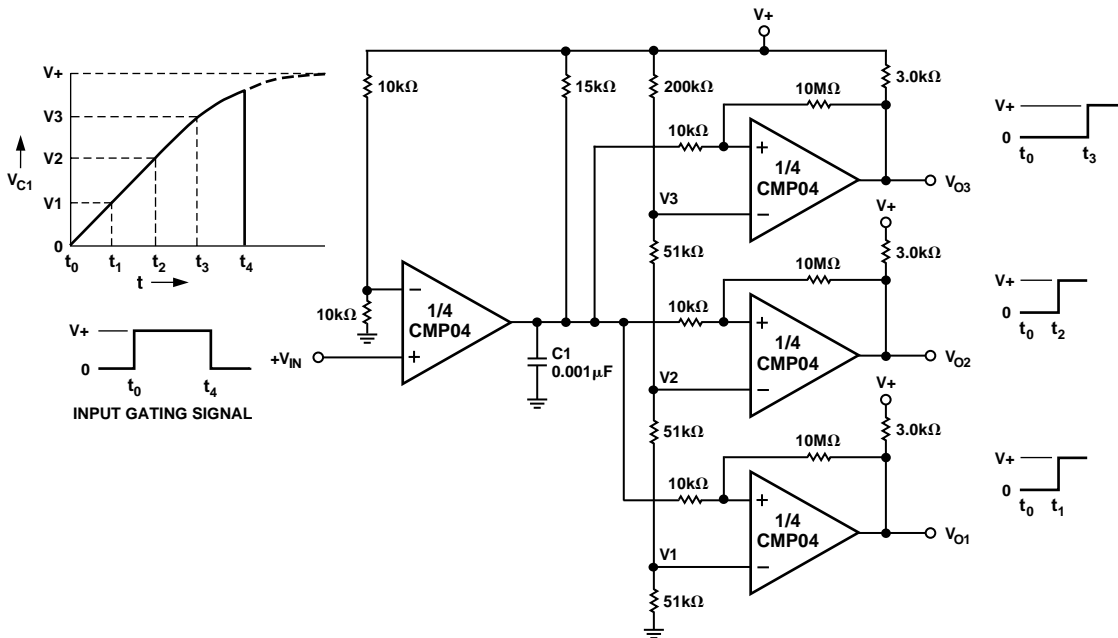
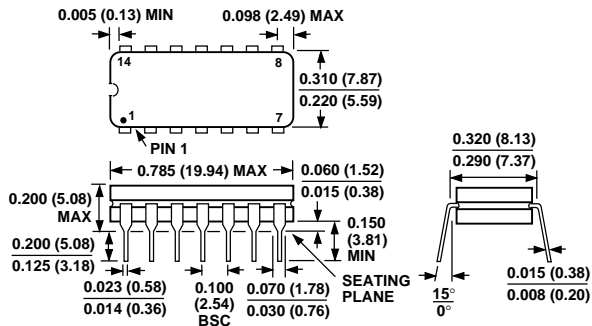


Figure 23. Time Delay Generator

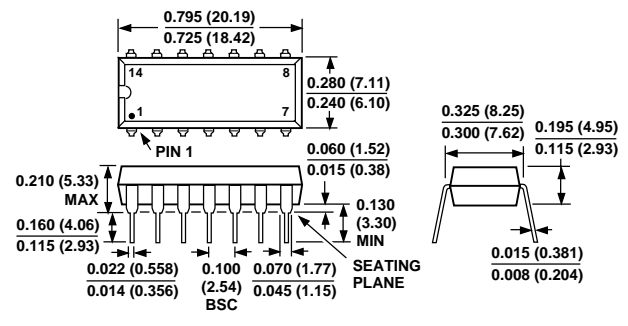
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

14-Lead Cerdip (Q-14)



14-Lead Plastic DIP (N-14)



14-Lead SOIC (R-14)

