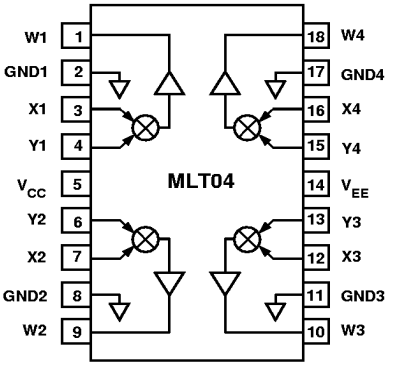
Four-Channel, Four-Quadrant Analog Multiplier

MLT04

FEATURES
- Four Independent Channels
- Voltage IN, Voltage OUT
- No External Parts Required
- 8 MHz Bandwidth
- Four-Quadrant Multiplication
- Voltage Output; W = (X × Y)/2.5 V
  - 0.2% Typical Linearity Error on X or Y Inputs
- Excellent Temperature Stability: 0.005%
- ±2.5 V Analog Input Range
- Operates from ±5 V Supplies
- Low Power Dissipation: 150 mW typ
- Spice Model Available

APPLICATIONS
- Geometry Correction in High-Resolution CRT Displays
- Waveform Modulation & Generation
- Voltage Controlled Amplifiers
- Automatic Gain Control
- Modulation and Demodulation

FUNCTIONAL BLOCK DIAGRAM
18-Lead Epoxy DIP (P Suffix)
18-Lead Wide Body SOIC (S Suffix)



W = (X • Y)/2.5V

GENERAL DESCRIPTION

The MLT04 is a complete, four-channel, voltage output analog multiplier packaged in an 18-pin DIP or SOIC-18. These complete multipliers are ideal for general purpose applications such as voltage controlled amplifiers, variable active filters, "zipper" noise free audio level adjustment, and automatic gain control. Other applications include cost-effective multiple-channel power calculations (I × V), polynomial correction generation, and low frequency modulation. The MLT04 multiplier is ideally suited for generating complex, high-order waveforms especially suitable for geometry correction in high-resolution CRT display systems.

Fabricated in a complementary bipolar process, the MLT04 includes four 4-quadrant multiplying cells which have been laser-trimmed for accuracy. A precision internal bandgap reference normalizes signal computation to a 0.4 scale factor. Drift over temperature is under 0.005%/°C. Spot noise voltage of 0.3 μV/√Hz results in a THD + Noise performance of 0.02% (LPF = 22 kHz) for the lower distortion Y channel. The four 8 MHz channels consume a total of 150 mW of quiescent power.

The MLT04 is available in 18-pin plastic DIP, and SOIC-18 surface mount packages. All parts are offered in the extended industrial temperature range (–40°C to +85°C).

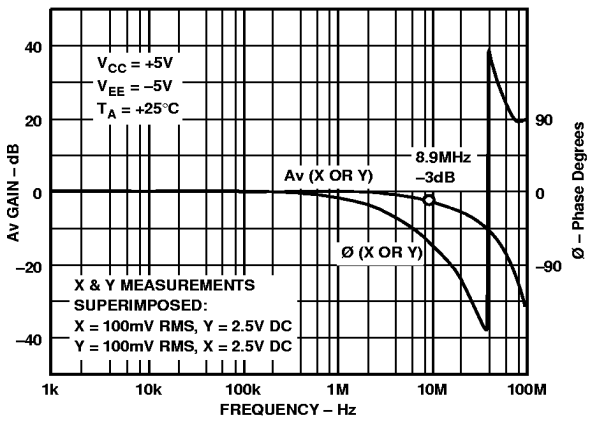


Figure 1. Gain & Phase vs. Frequency Response

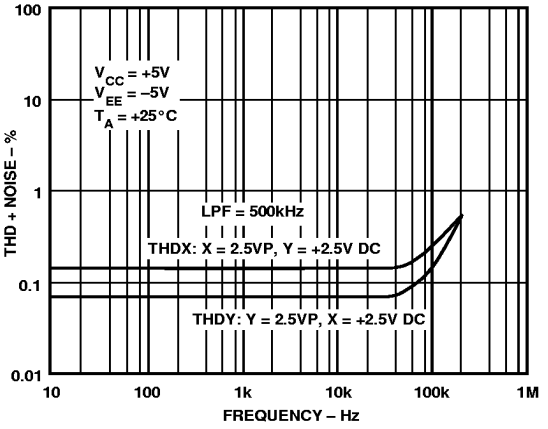


Figure 2. THD + Noise vs. Frequency

REV. B

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MLT04–SPECIFICATIONS (V_{CC} = +5 V, V_{EE} = –5 V, V_{IN} = ±2.5 V_P, R_L = 2 kΩ, T_A = +25°C unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
MULTIPLIER PERFORMANCE[1]						
Total Error[2] X	E_X	–2.5 V < X < +2.5 V, Y = +2.5 V	–5	±2	5	% FS
Total Error[2] Y	E_Y	–2.5 V < Y < +2.5 V, X = +2.5 V	–5	±2	5	% FS
Linearity Error[2] X	LE_X	–2.5 V < X < +2.5 V, Y = +2.5 V	–1	±0.2	+1	% FS
Linearity Error[2] Y	LE_Y	–2.5 V < Y < +2.5 V, X = +2.5 V	–1	±0.2	+1	% FS
Total Error Drift	TCE_X	X = –2.5 V, Y = 2.5 V, T_A = –40°C to +85°C		0.005		%/°C
Total Error Drift	TCE_Y	Y = –2.5 V, X = 2.5 V, T_A = –40°C to +85°C		0.005		%/°C
Scale Factor[3]	K	X = ±2.5 V, Y = ±2.5 V, T_A = –40°C to +85°C	0.38	0.40	0.42	1/V
Output Offset Voltage	Z_{OS}	X = 0 V, Y = 0 V, T_A = –40°C to +85°C	–50	±10	50	mV
Output Offset Drift	TCZ_{OS}	X = 0 V, Y = 0 V, T_A = –40°C to +85°C		50		µV/°C
Offset Voltage, X	X_{OS}	X = 0 V, Y = ±2.5 V, T_A = –40°C to +85°C	–50	±10.5	50	mV
Offset Voltage, Y	Y_{OS}	Y = 0 V, X = ±2.5 V, T_A = –40°C to +85°C	–50	±10.5	50	mV
DYNAMIC PERFORMANCE						
Small Signal Bandwidth	BW	V_{OUT} = 0.1 V rms		8		MHz
Slew Rate	SR	V_{OUT} = ±2.5 V	30	53		V/µs
Settling Time	t_S	V_{OUT} = Δ2.5 V to 1% Error Band		1		µs
AC Feedthrough	FT_{AC}	X = 0 V, Y = 1 V rms @ f = 100 kHz		–65		dB
Crosstalk @ 100 kHz	CT_{AC}	X = Y = 1 V rms Applied to Adjacent Channel		–90		dB
OUTPUTS						
Audio Band Noise	E_N	f = 10 Hz to 50 kHz		76		µV rms
Wide Band Noise	E_N	Noise BW = 1.9 MHz		380		µV rms
Spot Noise Voltage	e_N	f = 1 kHz		0.3		µV/√Hz
Total Harmonic Distortion	THD_X	f = 1 kHz, LPF = 22 kHz, Y = 2.5 V		0.1		%
	THD_Y	f = 1 kHz, LPF = 22 kHz, X = 2.5 V		0.02		%
Open Loop Output Resistance	R_{OUT}			40		Ω
Voltage Swing	V_{PK}	V_{CC} = +5 V, V_{EE} = –5 V	±3.0	±3.3		V_P
Short Circuit Current	I_{SC}			30		mA
INPUTS						
Analog Input Range	IVR	GND = 0 V	–2.5		+2.5	V
Bias Current	I_B	X = Y = 0 V		2.3	10	µA
Resistance	R_{IN}			1		MΩ
Capacitance	C_{IN}			3		pF
SQUARE PERFORMANCE						
Total Square Error	E_{SQ}	X = Y = 1		5		% FS
POWER SUPPLIES						
Positive Current	I_{CC}	V_{CC} = 5.25 V, V_{EE} = –5.25 V		15	20	mA
Negative Current	I_{EE}	V_{CC} = 5.25 V, V_{EE} = –5.25 V		15	20	mA
Power Dissipation	P_{DISS}	Calculated = 5 V × I_{CC} + 5 V × I_{EE}		150	200	mW
Supply Sensitivity	PSSR	X = Y = 0 V, V_{CC} = Δ5% or V_{EE} = Δ5%			10	mV/V
Supply Voltage Range	V_{RANGE}	For V_{CC} & V_{EE}	±4.75		±5.25	V

NOTES
[1]Specifications apply to all four multipliers.
[2]Error is measured as a percent of the ±2.5 V full scale, i.e., 1% FS = 25 mV.
[3]Scale Factor K is an internally set constant in the multiplier transfer equation W = K × X × Y.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltages V_{CC}, V_{EE} to GND	±7 V
Inputs X_I, Y_I	V_{CC}, V_{EE}
Outputs W_I	V_{CC}, V_{EE}
Operating Temperature Range	–40°C to +85°C
Maximum Junction Temperature (T_J max)	+150°C
Storage Temperature	–65°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C
Package Power Dissipation	(T_J max–T_A)/θ_{JA}
Thermal Resistance θ_{JA}	
PDIP-18 (N-18)	74°C/W
SOIC-18 (SOL-18)	89°C/W

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification are not implied.

ORDERING INFORMATION*

Model	Temperature Range	Package Description	Package Option
MLT04GP	–40°C to +85°C	18-Pin P-DIP	N-18
MLT04GS	–40°C to +85°C	18-Lead SOIC	SOL-18
MLT04GS-REEL	–40°C to +85°C	18-Lead SOIC	SOL-18
MLT04GBC	+25°C	Die	

*For die specifications contact your local Analog sales office. The MLT04 contains 211 transistors.

FUNCTIONAL DESCRIPTION

The MLT04 is a low cost quad, 4-quadrant analog multiplier with single-ended voltage inputs and voltage outputs. The functional block diagram for each of the multipliers is illustrated in Figure 3. Due to packaging constraints, access to internal nodes for externally adjusting scale factor, output offset voltage, or additional summing signals is not provided.

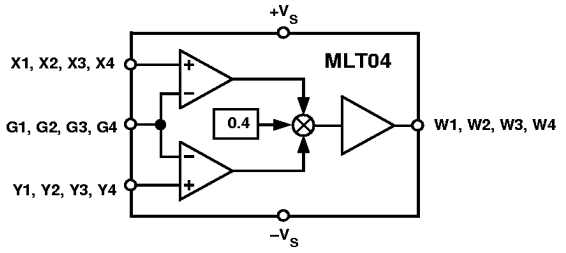


Figure 3. Functional Block Diagram of Each MLT04 Multiplier

Each of the MLT04's analog multipliers is based on a Gilbert cell multiplier configuration, a 1.23 V bandgap reference, and a unity-connected output amplifier. Multiplier scale factor is determined through a differential pair/trimmable resistor network external to the core. An equivalent circuit for each of the multipliers is shown in Figure 4.

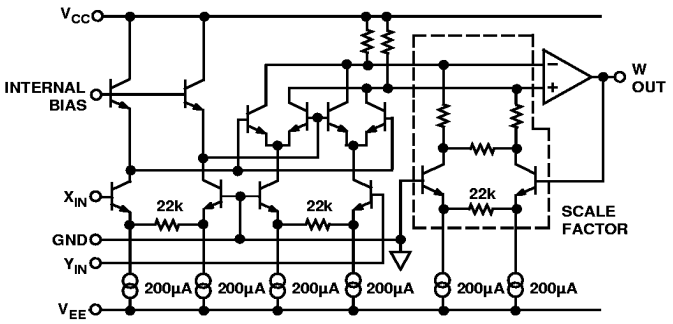


Figure 4. Equivalent Circuit for the MLT04

Details of each multiplier's output-stage amplifier are shown in Figure 5. The output stages idles at 200 µA, and the resistors in series with the emitters of the output stage are 25 Ω. The output stage can drive load capacitances up to 500 pF without oscillation. For loads greater than 500 pF, the outputs of the MLT04 should be isolated from the load capacitance with a 100 Ω resistor.

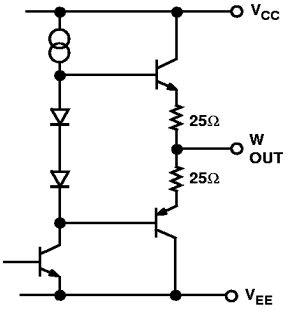


Figure 5. Equivalent Circuit for MLT04 Output Stages

ANALOG MULTIPLIER ERROR SOURCES

Multiplier errors consist primarily of input and output offsets, scale factor errors, and nonlinearity in the multiplying core. An expression for the output of a *real* analog multiplier is given by:

$$V_O = (K + \Delta K)\{(V_X + X_{OS})(V_Y + Y_{OS}) + Z_{OS} + f(X, Y)\}$$

where:
K = Multiplier Scale Factor
ΔK = Scale Factor Error
V_X = X-Input Signal
X_{OS} = X-Input Offset Voltage
V_Y = Y-Input Signal
Y_{OS} = Y-Input Offset Voltage
Z_{OS} = Multiplier Output Offset Voltage
$f(X, Y)$ = Nonlinearity

Executing the algebra to simplify the above expression yields expressions for all the errors in an analog multiplier:

Term	Description	Dependence on Input
KV_XV_Y	True Product	Goes to Zero As Either or Both Inputs Go to Zero
ΔKV_YV_Y	Scale-Factor Error	Goes to Zero at V_X, $V_Y = 0$
V_XY_{OS}	Linear "X" Feedthrough Due to Y-Input Offset	Proportional to V_X
V_YX_{OS}	Linear "Y" Feedthrough Due to X-Input Offset	Proportional to V_Y
$X_{OS}Y_{OS}$	Output Offset Due to X-, Y-Input Offsets	Independent of V_X, V_Y
Z_{OS}	Output Offset	Independent of V_X, V_Y
$f(X, Y)$	Nonlinearity	Depends on Both V_X, V_Y. Contains Terms Dependent on V_X, V_Y, Their Powers and Cross Products

As shown in the table, the primary static errors in an analog multiplier are input offset voltages, output offset voltage, scale factor, and nonlinearity. Of the four sources of error, only two are externally trimmable in the MLT04: the X- and Y-input offset voltages. Output offset voltage in the MLT04 is factory-trimmed to ±50 mV, and the scale factor is internally adjusted to ±2.5% of full scale. Input offset voltage errors can be eliminated by using the optional trim circuit of Figure 6. This scheme then reduces the net error to output offset, scale-factor (gain) error, and an irreducible nonlinearity component in the multiplying core.

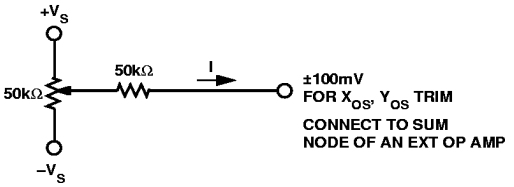


Figure 6. Optional Offset Voltage Trim Configuration

Feedthrough

In the ideal case, the output of the multiplier should be zero if either input is zero. In reality, some portion of the nonzero input will "feedthrough" the multiplier and appear at the output. This is caused by the product of the nonzero input and the offset voltage of the "zero" input. Introducing an offset equal to and opposite of the "zero" input offset voltage will null the linear component of the feedthrough. Residual feedthrough at the output of the multiplier is then irreducible core nonlinearity.

Typical X- and Y-input feedthrough curves for the MLT04 are shown in Figures 7 and 8, respectively. These curves illustrate MLT04 feedthrough after "zero" input offset voltage trim. Residual X-input feedthrough measures 0.08% of full scale, whereas residual Y-input feedthrough is almost immeasurable.

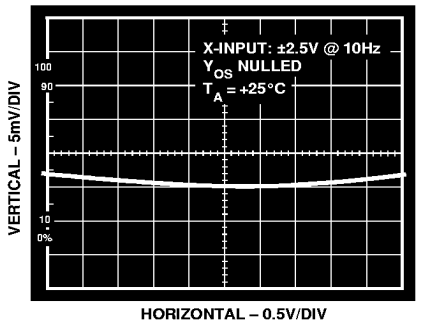


Figure 7. X-Input Feedthrough with Y_{OS} Nulled

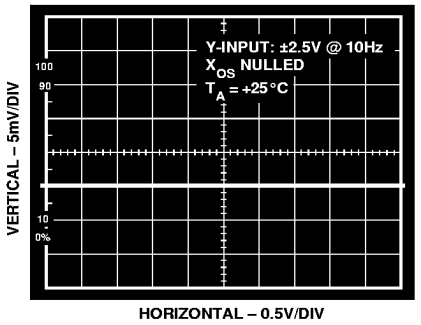


Figure 8. Y-Input Feedthrough with X_{OS} Nulled

Nonlinearity

Multiplier core nonlinearity is the irreducible component of error. It is the difference between actual performance and "best-straight-line" theoretical output, for all pairs of input values. It is expressed as a percentage of full scale with all other dc errors nulled. Typical X- and Y-input nonlinearities for the MLT04 are shown in Figures 9 through 12. Worst-case X-input nonlinearity measured less than 0.2%, and Y-input nonlinearity measured better than 0.06%. For modulator/demodulator or mixer applications it is, therefore, recommended that the carrier be connected to the X-input while the signal is applied to the Y-input.

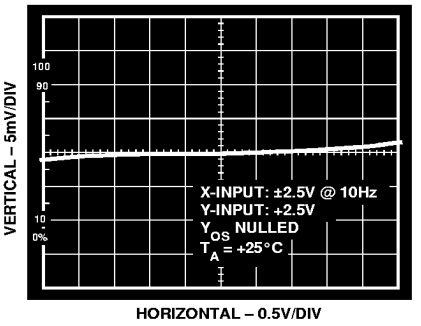


Figure 9. X-Input Nonlinearity @ Y = +2.5 V

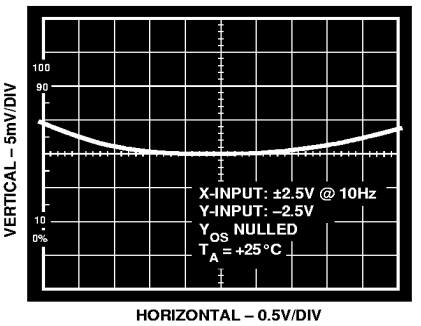


Figure 10. X-Input Nonlinearity @ Y = –2.5 V

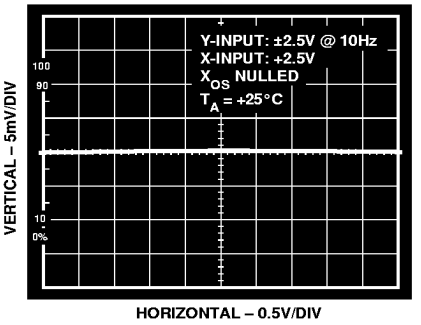


Figure 11. Y-Input Nonlinearity @ X = +2.5 V

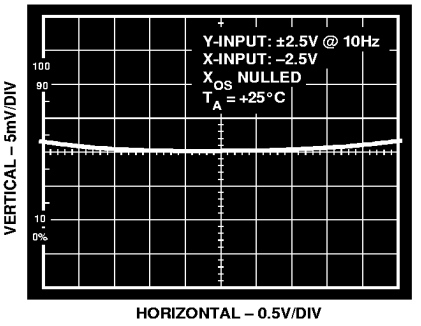


Figure 12. Y-Input Nonlinearity @ X = –2.5 V

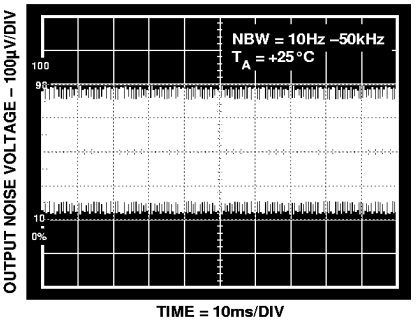


Figure 13. Broadband Noise

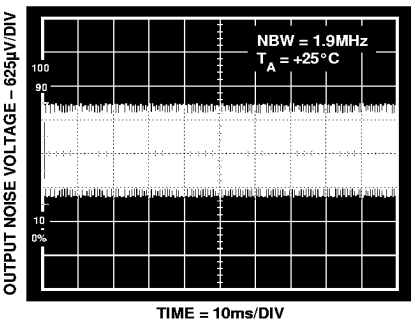


Figure 14. Broadband Noise

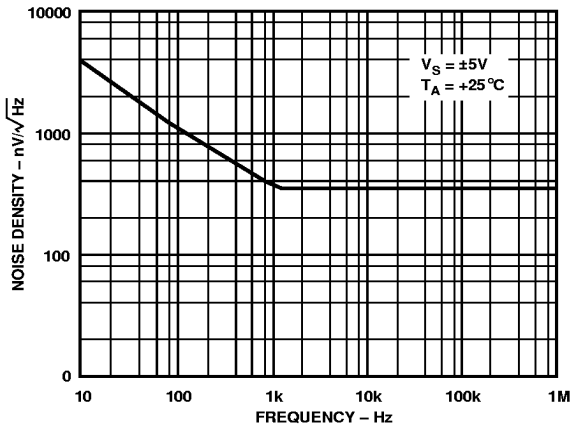


Figure 15. Noise Density vs. Frequency

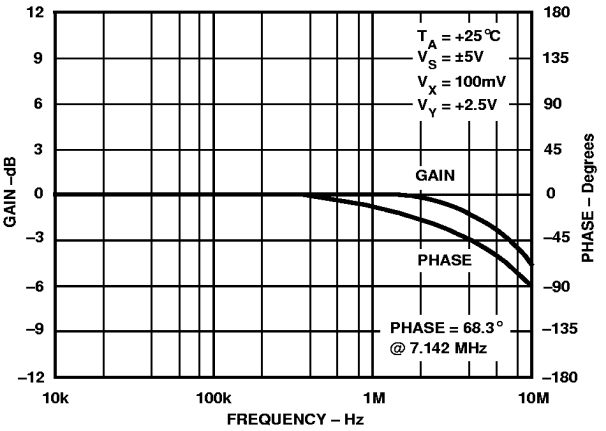


Figure 16. X-Input Gain and Phase vs. Frequency

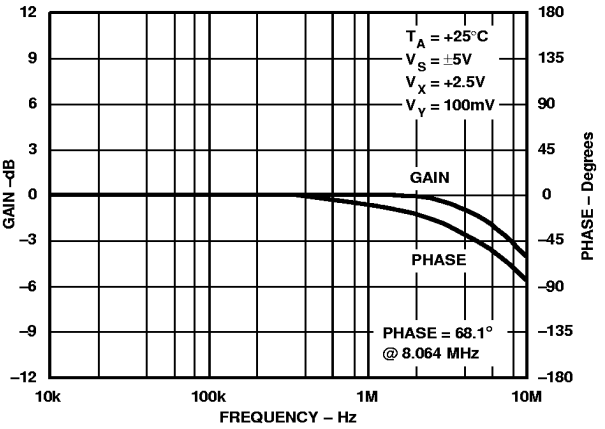


Figure 17. Y-Input Gain and Phase vs. Frequency

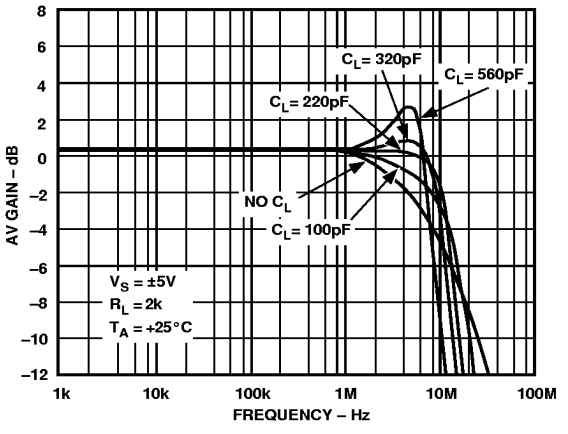


Figure 18. Amplitude Response vs. Capacitive Load

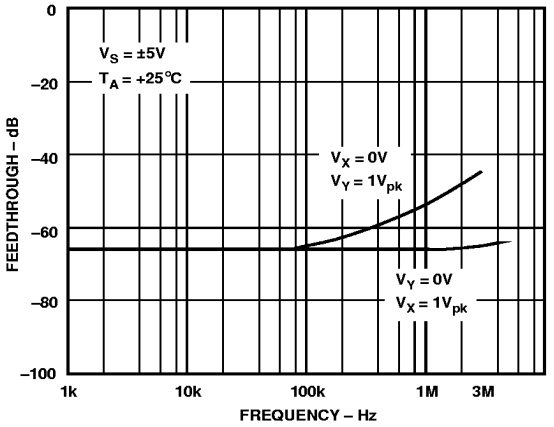


Figure 19. Feedthrough vs. Frequency

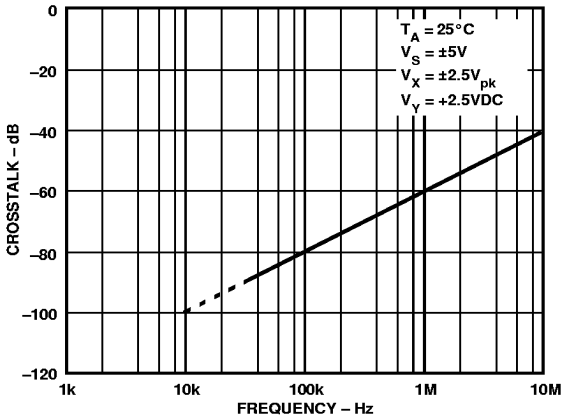


Figure 20. Crosstalk vs. Frequency

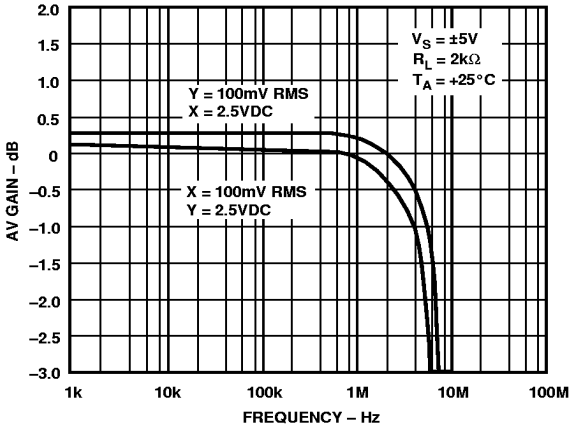


Figure 21. Gain Flatness vs. Frequency

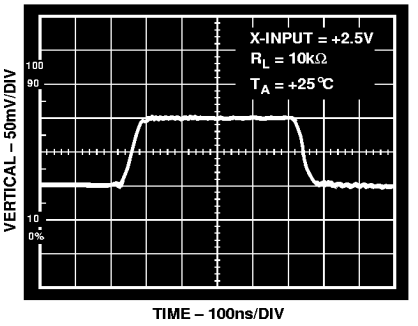


Figure 22. Y-Input Small-Signal Transient Response, C_L = 30 pF

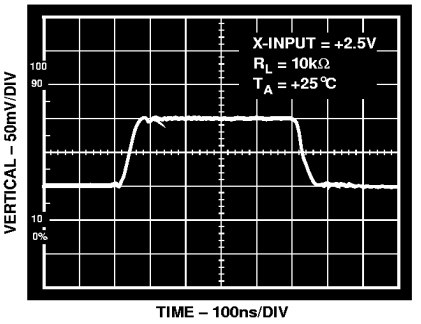


Figure 23. Y-Input Small-Signal Transient Response, C_L = 100 pF

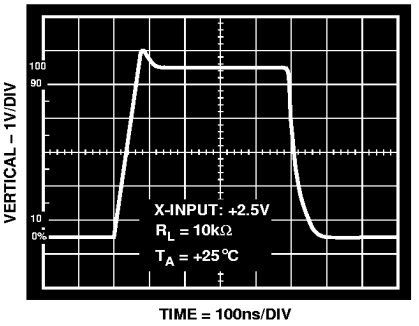


Figure 24. Y-Input Large-Signal Transient Response, C_L = 30 pF

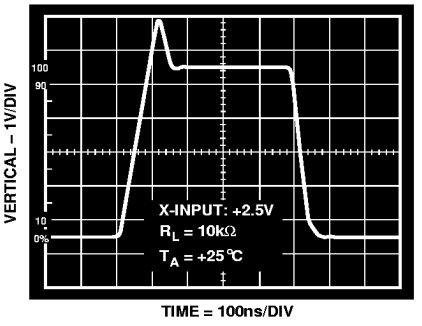


Figure 25. Y-Input Large-Signal Transient Response, C_L = 100 pF

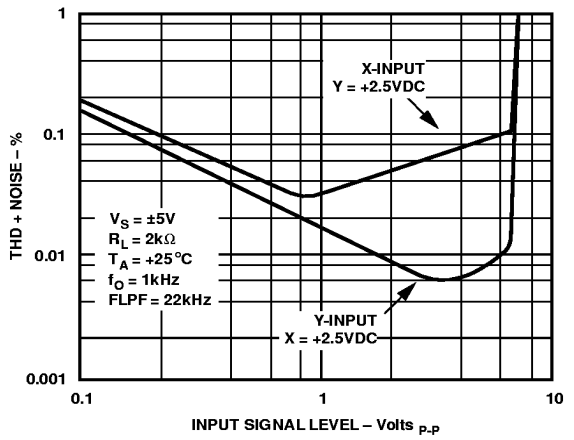


Figure 26. THD + Noise vs. Input Signal Level

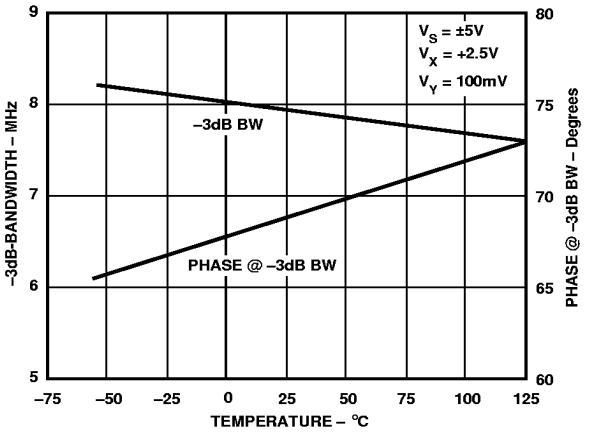


Figure 29. Y-Input Gain Bandwidth vs. Temperature

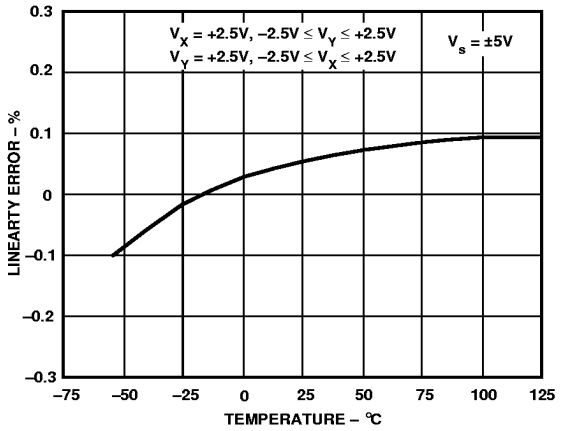


Figure 27. Linearity Error vs. Temperature

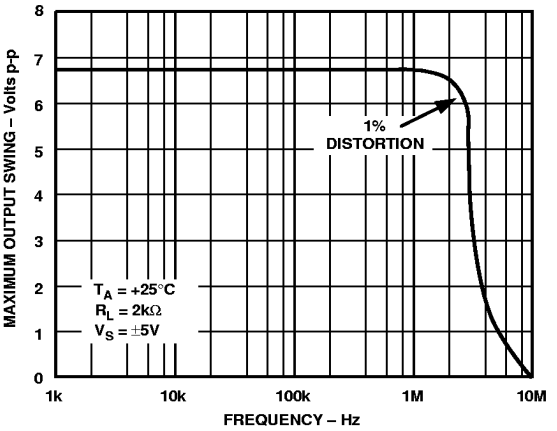


Figure 30. Maximum Output Swing vs. Frequency

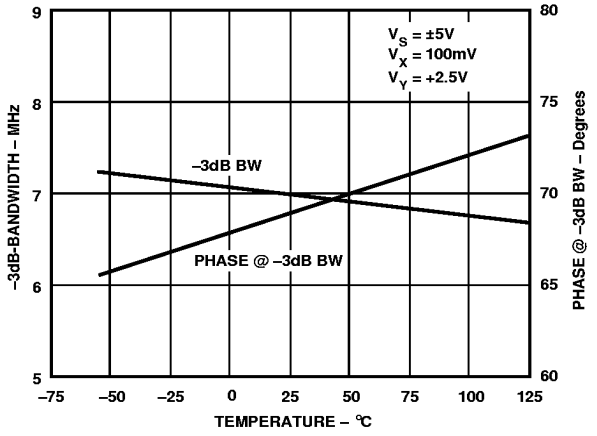


Figure 28. X-Input Gain Bandwidth vs. Temperature

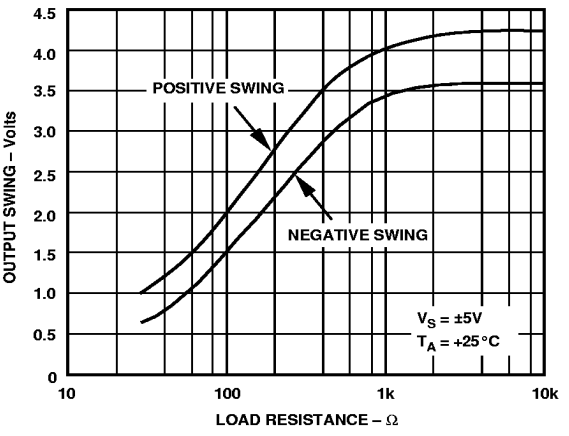


Figure 31. Maximum Output Swing vs. Resistive Load

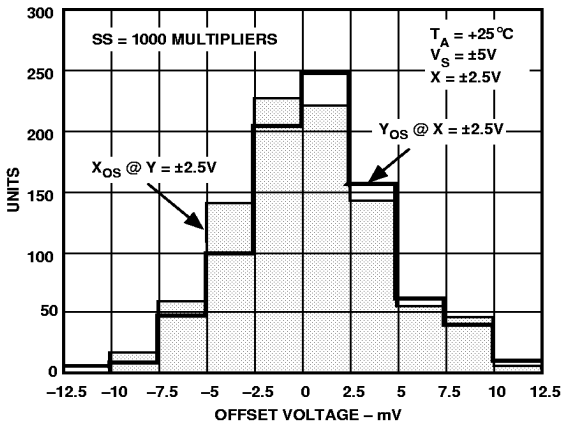


Figure 32. Offset Voltage Distribution

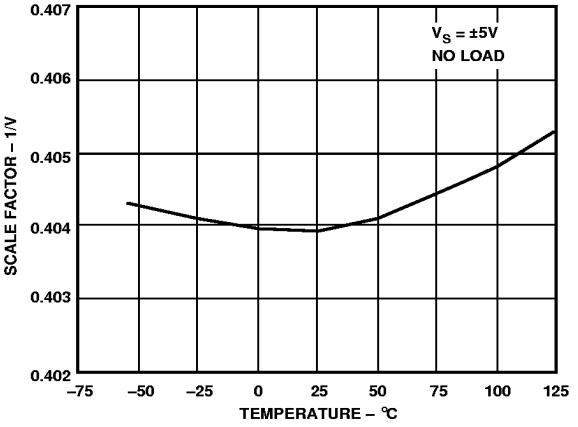


Figure 35. Scale Factor vs. Temperature

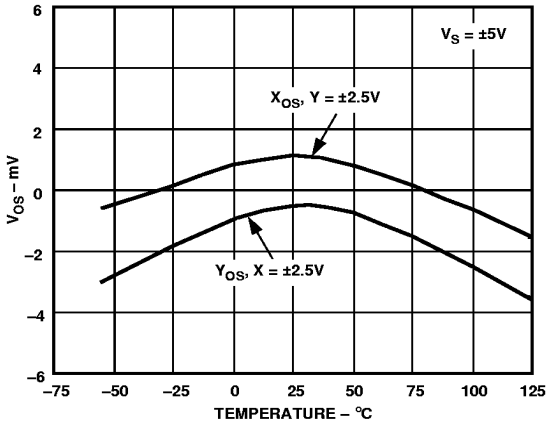


Figure 33. Offset Voltage vs. Temperature

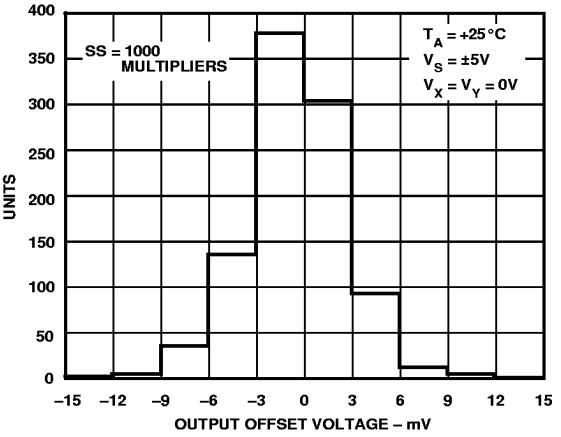


Figure 36. Output Offset Voltage (Z_{OS}) Distribution

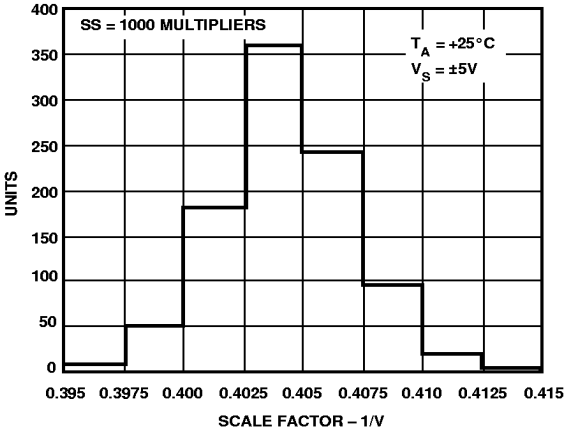


Figure 34. Scale Factor Distribution

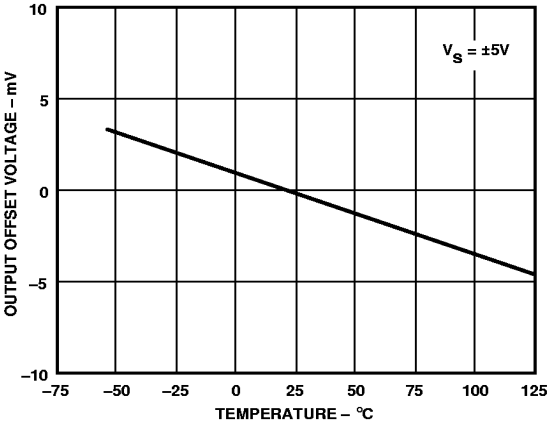


Figure 37. Output Offset Voltage (Z_{OS}) vs. Temperature

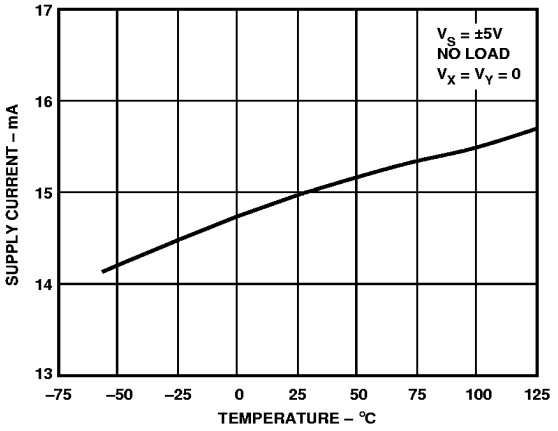


Figure 38. Supply Current vs. Temperature

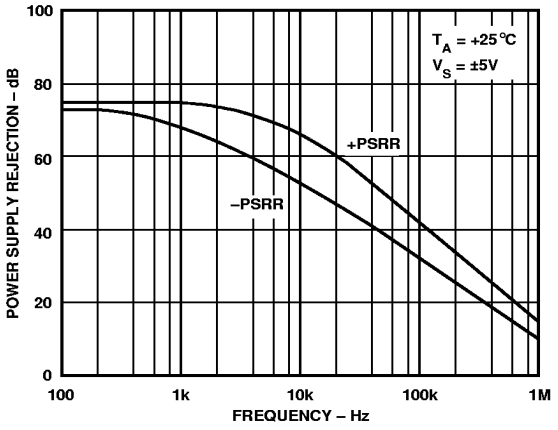


Figure 39. Power Supply Rejection vs. Frequency

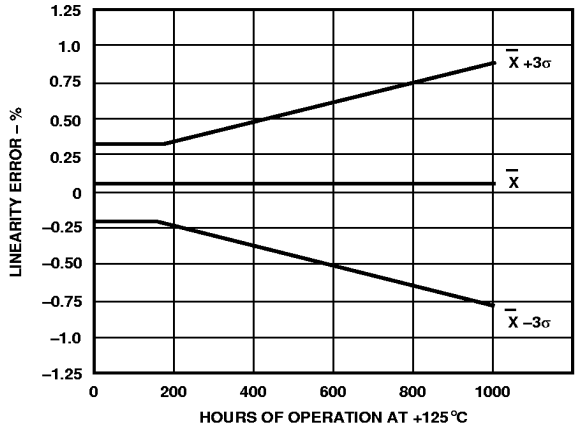


Figure 40. Linearity Error (LE) Distribution Accelerated by Burn-in

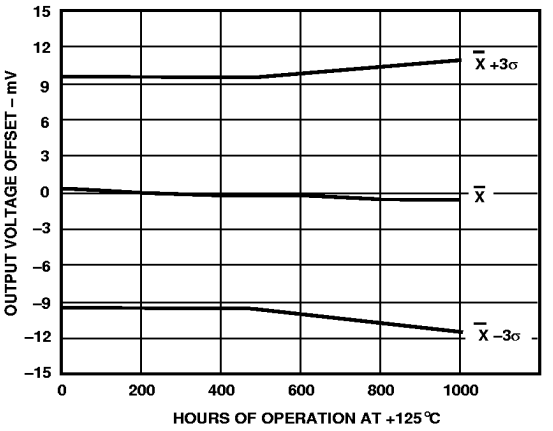


Figure 41. Output Voltage Offset (Z_{OS}) Distribution Accelerated by Burn-in

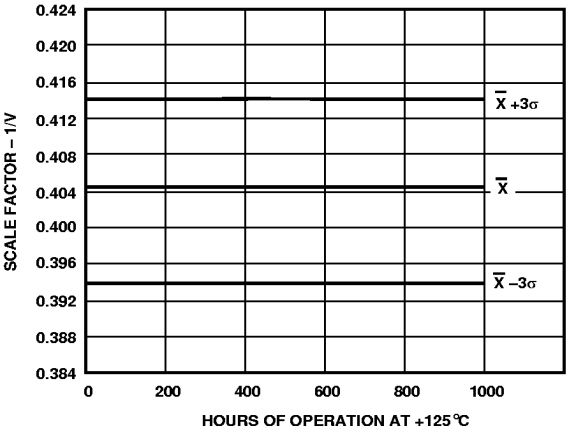


Figure 42. Scale Factor (K) Distribution Accelerated by Burn-in

APPLICATIONS

The MLT04 is well suited for such applications as modulation/demodulation, automatic gain control, power measurement, analog computation, voltage-controlled amplifiers, frequency doublers, and geometry correction in CRT displays.

Multiplier Connections

Figure 43 llustrates the basic connections for multiplication. Each of the four independent multipliers has single-ended voltage inputs (X, Y) and a low impedance voltage output (W). Also, each multiplier has its own dedicated ground connection (GND) which is connected to the circuit's analog common. For best performance, circuit layout should be compact with short component leads and well-bypassed supply voltage feeds. In applications where fewer than four multipliers are used, all unused analog inputs must be returned to the analog common.

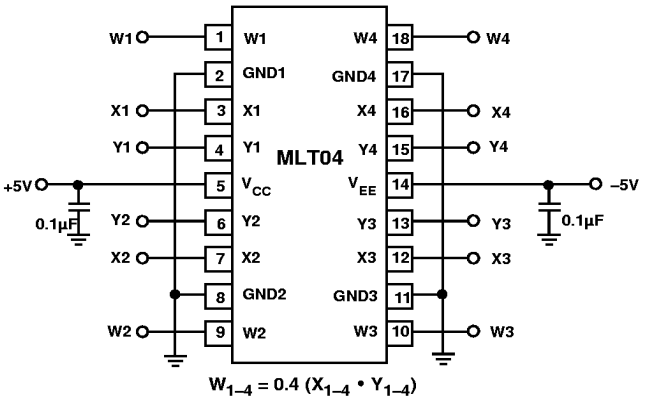


Figure 43. Basic Multiplier Connections

Squaring and Frequency Doubling

As shown in Figure 44, squaring of an input signal, V_{IN}, is achieved by connecting the X-and Y-inputs in parallel to produce an output of $V_{IN}^2/2.5$ V. The input may have either polarity, but the output will be positive.

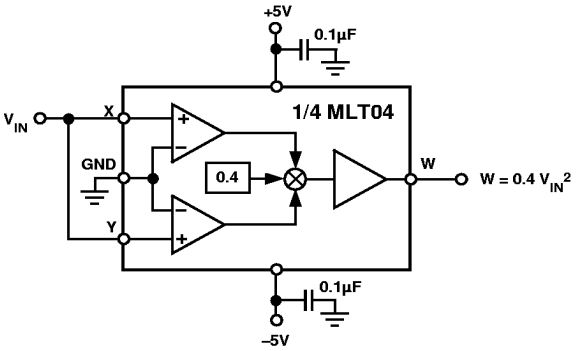


Figure 44. Connections for Squaring

When the input is a sine wave given by V_{IN} sin ωt, the squaring circuit behaves as a frequency doubler because of the trigonometric identity:

$$\frac{(V_{IN}\sin\omega t)^2}{2.5V} = \frac{V_{IN}{}^2}{2.5V}\left(\frac{1}{2}\right)(1-\cos 2\omega t)$$

The equation shows a dc term at the output which will vary strongly with the amplitude of the input, V_{IN}. The output dc offset can be eliminated by capacitively coupling the MLT04's output with a high-pass filter. For optimal spectral performance, the filter's cutoff frequency should be chosen to eliminate the input fundamental frequency.

A source of error in this configuration is the offset voltages of the X and Y inputs. The input offset voltages produce cross products with the input signal to distort the output waveform. To circumvent this problem, Figure 45 illustrates the use of inverting amplifiers configured with an OP285 to provide a means by which the X- and Y-input offsets can be trimmed.

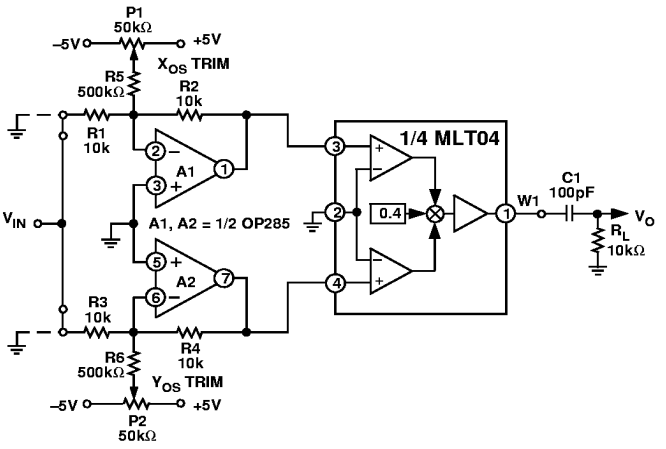


Figure 45. Frequency Doubler with Input Offset Voltage Trims

Feedback Divider Connections

The most commonly used analog divider circuit is the "inverted multiplier" configuration. As illustrated in Figure 46, an "inverted multiplier" analog divider can be configured with a multiplier operating in the feedback loop of an operational amplifier. The general form of the transfer function for this circuit configuration is given by:

$$V_O = -2.5V \times \left(\frac{R2}{R1}\right) \times \frac{V_{IN}}{V_X}$$

Here, the multiplier operates as a voltage-controlled potentiometer that adjusts the loop gain of the op amp relative to a control signal, V_X. As the control signal to the multiplier decreases, the output of the multiplier decreases as well. This has the effect of reducing negative feedback which, in turn, decreases the amplifier's loop gain. The result is higher closed-loop gain and reduced circuit bandwidth. As V_X is increased, the output of the multiplier increases which generates more negative feedback — closed-loop gain drops and circuit bandwidth increases. An example of an "inverted multiplier" analog divider frequency response is shown in Figure 47.

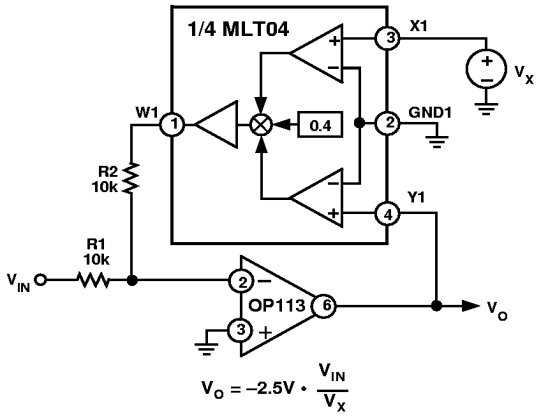


Figure 46. "Inverted-Multiplier" Configuration for Analog Division

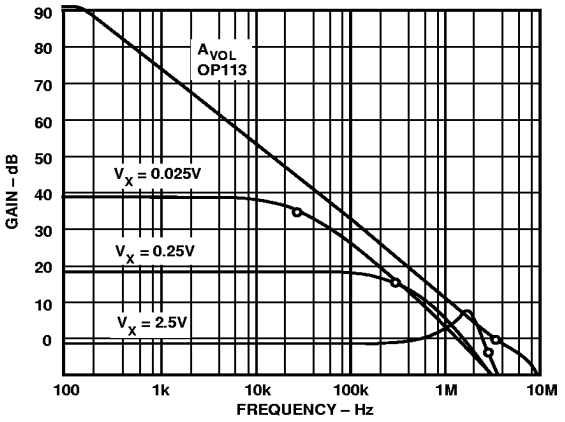


Figure 47. Signal-Dependent Feedback Makes Variables Out of Amplifier Bandwidth and Stability

Although this technique works well with almost any operational amplifier, there is one caveat: for best circuit stability, the unity-gain crossover frequency of the operational amplifier should be equal to or less than the MLT04's 8 MHz bandwidth.

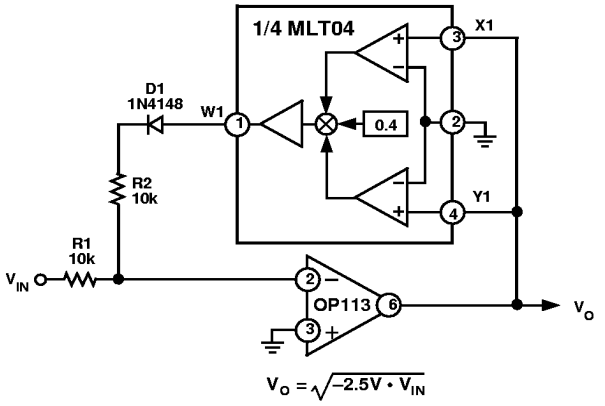
Connection for Square Rooting

Another application of the "inverted multiplier" configuration is the square-root function. As shown in Figure 48, both inputs of the MLT04 are wired together and are used as the output of the circuit. Because the circuit configuration exhibits the following generalized transfer function:

$$V_O = \sqrt{-2.5 \times \left(\frac{R2}{R1}\right) \times V_{IN}}$$

the input signal voltage is limited to the range $-2.5\ V \le V_{IN} < 0$. To prevent circuit latchup due to positive feedback or input signal polarity reversal, a 1N4148-type junction diode is used in series with the output of the multiplier.

Figure 48. Connections for Square Rooting



Voltage-Controlled Low-Pass Filter

The circuit in Figure 49 illustrates how to construct a voltage-controlled low-pass filter with an analog multiplier. The advantage with this approach over conventional active-filter configurations is that the overall characteristic cut-off frequency, ω_O, will be directly proportional to a multiplying input voltage. This permits the construction of filters in which the capacitors are adjustable (directly or inversely) by a control voltage. Hence, the frequency scale of a filter can be manipulated by means of a single voltage without affecting any other parameters. The general form of the circuit's transfer function is given by:

$$\frac{V_O}{V_{IN}} = -\left(\frac{R2}{R1}\right)\left\{\frac{1}{s\left(\frac{R2+R1}{R1}\right)\left(\frac{2.5RC}{V_X}\right)+1}\right\}$$

In this circuit, the ratio of R2 to R1 sets the passband gain, and the break frequency of the filter, ω_{LP}, is given by:

$$\omega_{LP} = \left(\frac{R1}{R1+R2}\right)\left(\frac{V_X}{2.5RC}\right)$$

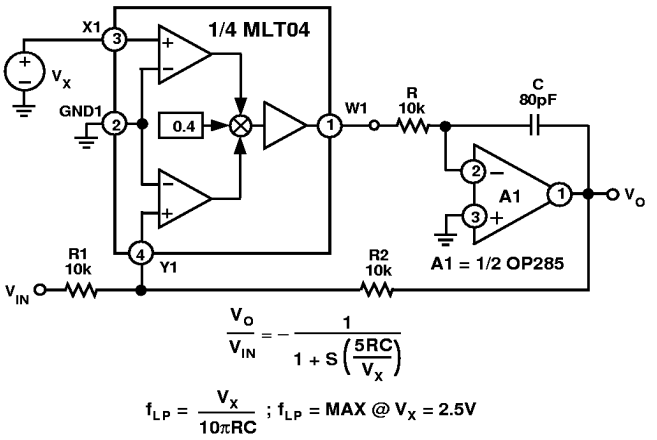


Figure 49. A Voltage-Controlled Low-Pass Filter

For example, if R1 = R2 = 10 kΩ , R = 10 kΩ , and C = 80 pF,

then the output of the circuit has a pole at frequencies from 1 kHz to 100 kHz for V_X ranging from 25 mV to 2.5 V. The performance of this low-pass filter is illustrated in Figure 20.

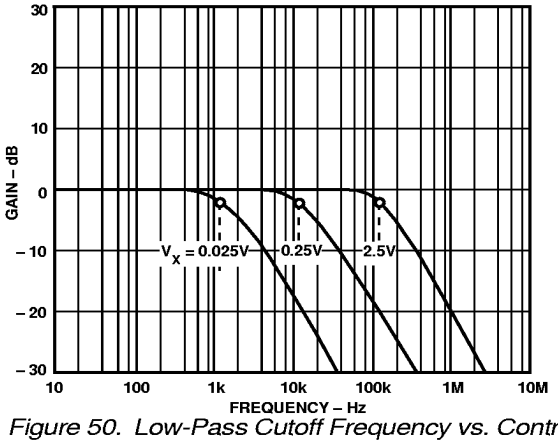


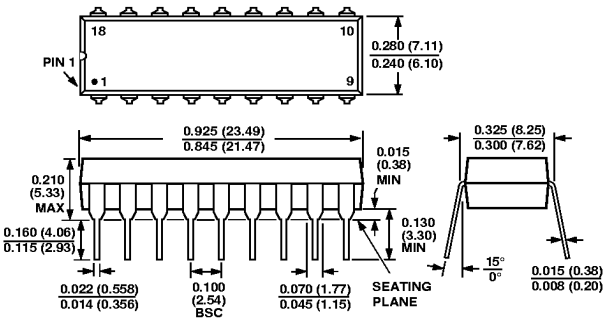
Figure 50. Low-Pass Cutoff Frequency vs. Control Voltage, V_X

With this approach, it is possible to construct parametric biquad filters whose parameters (center frequency, passband gain, and Q) can be adjusted with dc control voltages.

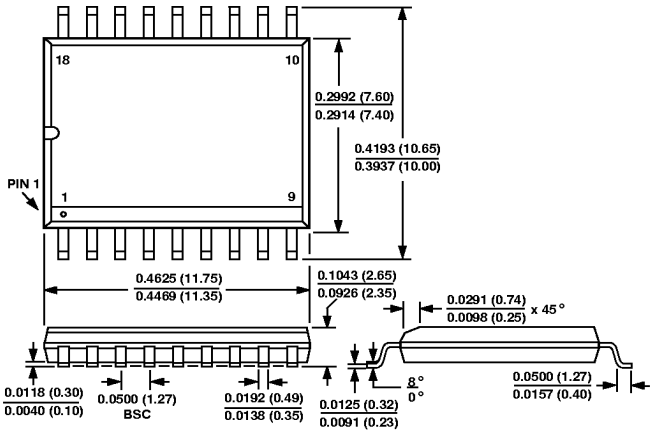
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

18-Lead Epoxy DIP (P Suffix)



18-Lead Wide-Body SOL (S Suffix)



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