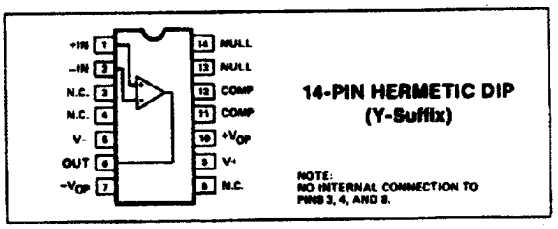
High-Output-Current Operational Amplifier ($A_{VCL} \geq 5$)

OP-50

FEATURES

- Open-Loop Gain ..... 10,000,000V/V Min
- Low Input Offset Voltage ..... 25μV Max
- Low Input Bias Current ..... 5nA Max
- Excellent TCV_{OS} ..... 0.3μV/°C Max
- High CMRR ..... 126dB Min
- High PSRR ..... 126dB Min
- Low Noise ..... 5.5nV/$\sqrt{Hz}$ @ f = 10Hz
  ..... 4.5nV/$\sqrt{Hz}$ @ f = 1kHz
- High Output Current ..... ±50mA
- Drives Capacitive Loads up to 10nF
- On-Board Thermal Shutdown Circuit
- Available in Die Form

PIN CONNECTIONS



14-PIN HERMETIC DIP
(Y-Suffix)

NOTE:
NO INTERNAL CONNECTION TO PINS 3, 4, AND 8.

ORDERING INFORMATION†

T_A = 25°C V_{OS} MAX (μV)	PACKAGE CERDIP 14-PIN	OPERATING TEMPERATURE RANGE
25	OP-50AY*	MIL
100	OP-50BY*	MIL
25	OP-50EY	IND
100	OP-50FY	IND

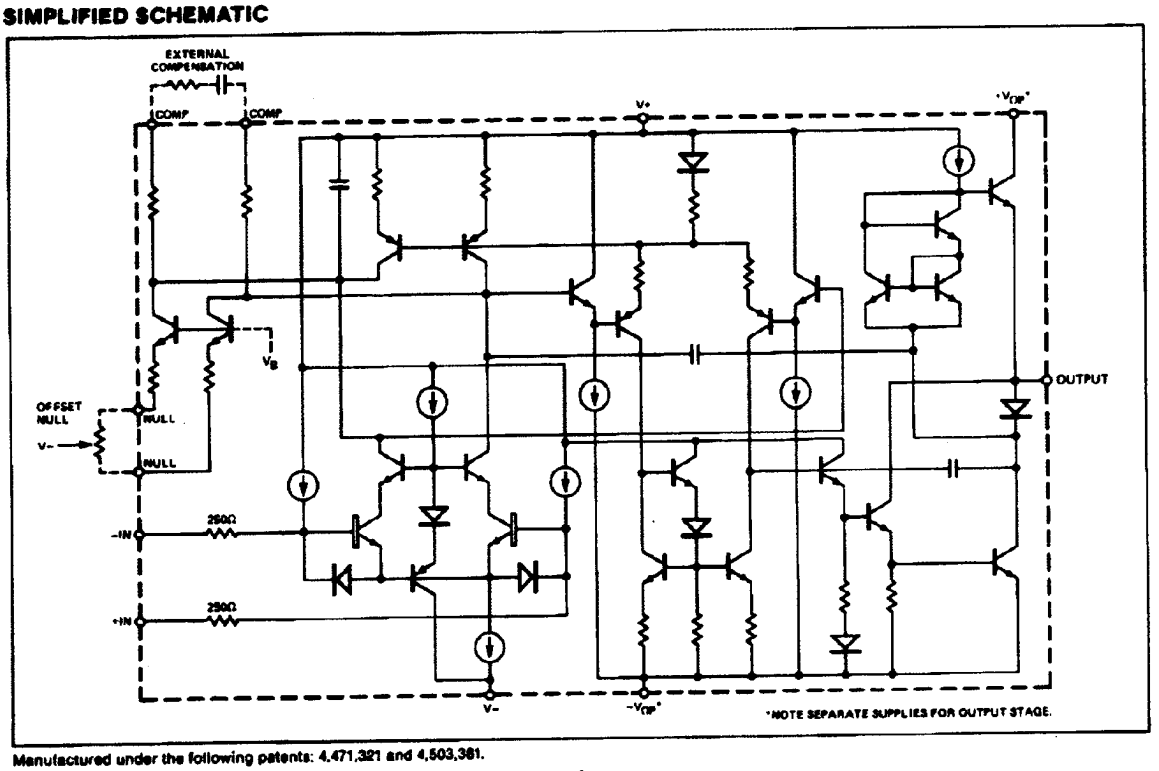
* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

GENERAL DESCRIPTION

The OP-50 eliminates the need for an output buffer in applications which require high load-driving capability coupled with premium amplifier performance. The output stage can drive ±50mA into 50Ω loads. In addition, the output is stable with capacitive loads of up to 10nF. This load driving ability makes the OP-50 ideal for amplifying small signals for transmission through long cables. The amplifier features open-loop voltage gain of over 10 million with common-mode rejection and power supply rejection of greater than 126dB (A/E grades).

SIMPLIFIED SCHEMATIC



Manufactured under the following patents: 4,471,321 and 4,503,381.

OP-50

The OP-50 is stable for closed-loop gains above 50, and can be externally compensated for closed-loop gains in the range of 5 to 50. The amplifier is designed for use in high-gain and/or high-output-current applications. For example, an OP-07 coupled with an output buffer can be replaced by a single OP-50 amplifier.

Ion-implanted superbeta transistors, combined with a patented input bias current cancellation circuit, provide an input bias current of only 5nA and input offset current of 1nA. Over the full military temperature range, input bias current and input offset current for an A-grade device does not exceed 8nA and 3nA, respectively. Input offset voltages are trimmed to a maximum of 25μV (A/E grades) and 100μV (B/F grades) using PMI's zener-zapping technique. This low offset eliminates the need for an offset trimpot in most applications.

Low voltage-noise, typically 4.5nV/$\sqrt{Hz}$ at 1kHz, is achieved in the OP-50 with minimum sacrifice of input protection. Overload protection is provided by input resistors of 250Ω and emitter-base diodes. The input resistors provide current limit protection against differential inputs of up to ±10V; and the diodes prevent avalanche breakdown which could degrade the I_B, I_{OS}, and matching of the input stage transistors. External resistors can be added to the input to guard against higher input voltages; however, the added resistors will degrade noise voltage performance. When minimum noise voltage is required, source resistance should be kept below a few hundred ohms.

Separate output-stage power supply pins are provided on the OP-50 to allow control of device power dissipation and output voltage swing. The maximum voltage which may be applied across the power supply pins is ±18V. The guaranteed specifications are based on operating both stages at ±15V; however, there is minimal effect on DC performance when the main amplifier is operated at ±15V and the output stage is operated at a reduced voltage. When operating both the main amplifier and the output stage at the same voltages, the corresponding power supply pins may be tied together. Decoupling capacitors are recommended between the power supply pins and analog ground. It is necessary to use decoupling capacitors on each power supply pin when operating the output stage at supply voltages less than the amplifier supply voltage. Do not operate the output-stage negative power supply pin at a more negative voltage than the negative supply pin (V–).

A thermally-symmetric die layout, which differs from other op amp designs by the positioning of more devices along the center line, provides the OP-50 with a thermal drift of less than 0.3μV/°C. This layout feature is critical to the maintenance of high open-loop gain when driving large-current loads and dissipating hundreds of milliwatts in the device. The use of a heatsink is recommended to reduce internal temperature rise when operating at high output power levels. The use of standard dual-in-line package heatsinks will help to dissipate heat to the environment. Other techniques, such as the use of external voltage-dropping resistors, allow heat to be dissipated outside of the package. See Figure 5, "Driving 50Ω Loads", in the applications section.

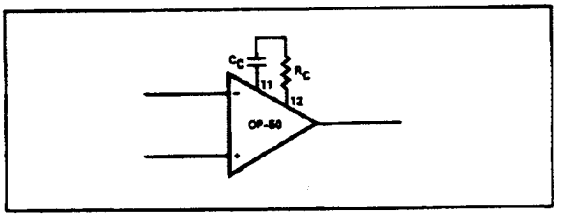
A thermal-shutdown circuit protects the OP-50 from overdissipation. When the die temperature reaches approximately 165°C, the output stage automatically shuts down. The amplifier input stage remains fully operational, thereby protecting the signal source from any loading changes caused by a complete shutdown.

COMPENSATION FOR GAINS BETWEEN 5 AND 50

The OP-50 can be compensated for inverting gains between 5 and 50 using a series resistor and capacitor. These values can be adjusted to minimize overshoot for a given application. The recommended compensation is:

GAIN RANGE	R_C	C_C
$5 \le A_{VCL} \le 20$	560Ω	4.7nF
$20 \le A_{VCL} \le 50$	3.3kΩ	1nF
$A_{VCL} \ge 50$	No compensation required	

COMPENSATION



ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (Note 2) ..... ±18V
Input Voltage ..... Supply Voltage
Differential Input Voltage (Note 3) ..... ±10V
Differential Input Current (Note 3) ..... ±20mA
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range ..... –65°C to +150°C
Operating Temperature Range
OP-50A, B ..... –55°C to +125°C
OP-50E, F ..... –25°C to +85°C
Lead Temperature (Soldering, 60 sec) ..... 300°C
Junction Temperature (T_J) ..... –65°C to +150C

PACKAGE TYPE	θ_{JA} (NOTE 4)	θ_{JC}	UNITS
14-Pin Hermetic DIP (Y)	99	12	°C/W

NOTES:
1. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Supply voltage rating applies to all power supply pins. No device pins should be connected to a voltage more negative than the supply to V–, pin 5.
3. The OP-50's inputs are protected by 250Ω series resistors and protection diodes. If the differential input voltage exceeds ±10V, the input current must be limited to ±20mA.
4. θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for CerDIP package.

ELECTRICAL CHARACTERISTICS at $V+ = +V_{OP} = +15V$, $V- = -V_{OP} = -15V$, $T_A = 25°C$, no compensation, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-50A/E MIN	OP-50A/E TYP	OP-50A/E MAX	OP-50B/F MIN	OP-50B/F TYP	OP-50B/F MAX	UNITS
Input Offset Voltage	V_{OS}		—	10	25	—	50	100	μV
Input Bias Current	I_B		—	±1	±5	—	±1	±10	nA
Input Offset Current	I_{OS}		—	0.1	1	—	0.1	3	nA
Input Voltage Range	IVR	CMRR ≥ 100dB	±12	—	—	±12	—	—	V
Output Voltage Swing	V_O	$R_l \geq 500\Omega$ $R_L \geq 50\Omega$ (Note 1)	±13 ±2.5	±13.4 ±4.0	— —	±13 ±2.5	±13.4 ±4.0	— —	V
Output Voltage Swing	V_O	$V+ = +V_{OP} = +5V$, $V- = -V_{OP} = -5V$ $R_L = 500\Omega$ $R_L = 50\Omega$	 ±3.5 ±2.5	 ±3.8 ±2.8	 — —	 ±3.5 ±2.5	 ±3.8 ±2.8	 — —	V
Slew Rate	SR	$R_L \geq 2k\Omega$ $R_C = 560\Omega$ $C_C = 4.7nF$	2.5	3.0	—	2.5	3.0	—	V/μs
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$	126	140	—	110	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 15V$	—	0.1	0.5	—	0.5	1	μV/V
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$, $R_L = 1k\Omega$	10	20	—	7.5	15	—	V/μV
Gain-Bandwidth Product	GBW	$A_{VCL} = 50$ (Note 2)	15	25	—	15	25	—	MHz
Offset Voltage Range Adjust		$R_P = 100k\Omega$	±1.0	±2.5	—	±1.0	±2.5	—	mV
Input Noise Voltage	e_{np-p}	f = 0.1Hz to 10Hz	—	0.12	—	—	0.12	—	μV_{p-p}
Noise Voltage Density	e_n	f = 10Hz f = 1kHz (Note 3)	— —	5.5 4.5	8.5 6.0	— —	5.5 4.5	8.5 6.0	$nV/\sqrt{Hz}$
Noise Current	i_{np-p}	f = 0.1Hz to 10Hz	—	2	—	—	2	—	pA_{p-p}
Noise Current Density	i_n	f = 100Hz f = 1kHz	— —	0.3 0.23	— —	— —	0.3 0.23	— —	$pA/\sqrt{Hz}$
Quiescent Supply Current	I_{SY}	No Load	—	2.6	3.3	—	2.6	3.3	mA
Positive Current Limit	$+I_{SC}$	Output shorted to Ground	60	95	120	60	95	120	mA
Negative Current Limit	$-I_{SC}$	Output shorted to Ground	60	85	120	60	85	120	mA
Differential-Mode Input Resistance	R_{IND}		—	2	—	—	2	—	MΩ
Common-Mode Input Resistance	R_{INCM}		—	20	—	—	20	—	GΩ
Capacitive Load Capability	C_L	$A_{VCL} \geq 5$ $R_C = 560\Omega$ (Note 2) $C_C = 4.7nF$	10	—	—	10	—	—	nF
Settling-Time	t_s	Settling to 0.01%, $V_O = 20V_{p-p}$ $A_{VCL} = 500$ $A_{VCL} = 1000$	 — —	 30 60	 — —	 — —	 30 60	 — —	μs

NOTES:
1. Guaranteed by current limit tests.
2. Guaranteed by design.
3. Sample tested.

OP-50

ELECTRICAL CHARACTERISTICS at V+ = $+V_{OP}$ = +15V, V− = $-V_{OP}$ = −15V, −25°C ≤ T_A ≤ +85°C, no compensation, unless otherwise noted.

			OP-50E			OP-50F			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		—	20	45	—	50	150	µV
Input Offset Voltage Drift	TCV_{OS}	(Note 1)	—	0.15	0.3	—	0.3	1	µV/°C
Input Bias Current	I_B		—	±2	±7	—	±2	±25	nA
Input Offset Current	I_{OS}		—	0.2	2.5	—	0.2	20	nA
Input Offset Current Drift	TCI_{OS}		—	3	—	—	5	—	pA/°C
Input Bias Current Drift	TCI_B		—	20	—	—	50	—	pA/°C
Input Voltage Range	IVR	CMRR ≥ 100dB	±11.5	—	—	±11.5	—	—	V
Output Voltage Swing	V_O	R_L ≥ 500Ω	±12	±13.4	—	±12	±13.4	—	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±10V	120	130	—	105	120	—	dB
Power Supply Rejection Ratio	PSRR	V_S = ±5V to ±15V	—	0.5	1.25	—	0.5	1.25	µV/V
Quiescent Supply Current	I_{SY}	No Load	—	2.8	4	—	2.8	4	mA
Open-Loop Gain	A_{VO}	V_{OUT} = ±10V, R_L = 1kΩ (Note 2)	4	15	—	4	15	—	V/µV

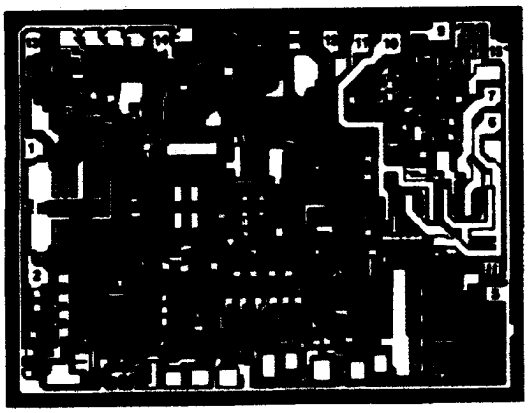
NOTES:
1. TCV_{OS} tested on E grade, guaranteed by design on F grade specification.
2. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at V+ = $+V_{OP}$ = +15V, V− = $-V_{OP}$ = −15V, −55°C ≤ T_A ≤ +125°C, no compensation, unless otherwise noted.

			OP-50A			OP-50B			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		—	20	55	—	50	200	µV
Input Offset Voltage Drift	TCV_{OS}		—	0.15	0.3	—	0.3	1	µV/°C
Input Bias Current	I_B		—	±2	±8	—	±2	±20	nA
Input Offset Current	I_{OS}		—	0.5	3	—	0.5	12	nA
Input Offset Current Drift	TCI_{OS}		—	3	—	—	5	—	pA/°C
Input Bias Current Drift	TCI_B		—	20	—	—	50	—	pA/°C
Input Voltage Range	IVR	CMRR ≥ 100dB	±11.5	—	—	±11.5	—	—	V
Output Voltage Swing	V_O	R_L > 500Ω	±12	±13.2	—	±12	±13.2	—	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±10V	120	130	—	105	120	—	dB
Power Supply Rejection Ratio	PSRR	V_S = ±5V to ±15V	—	0.5	1.25	—	0.5	1.25	µV/V
Quiescent Supply Current	I_{SY}	No Load	—	2.8	4	—	2.8	4	mA
Open-Loop Gain	A_{VO}	V_O = ±10V, R_L = 1kΩ (Note 1)	4	10	—	4	10	—	V/µV

NOTE:
1. Tested at +125°C, guaranteed by design at −55°C.

DICE CHARACTERISTICS



DIE SIZE 0.149 × 0.111 inch, 16,539 sq. mils
(3.78 × 2.82 mm, 10.66 sq. mm)

1. NONINVERTING INPUT
2. INVERTING INPUT
5. V–
6. OUTPUT
7. $-V_{OP}$
9. V+
10. $+V_{OP}$
11. COMPENSATION
12. COMPENSATION
13. NULL
14. NULL
15. V– (OPTIONAL BONDING PAD)*

WAFER TEST LIMITS at V+ = $+V_{OP}$ = +15V, V– = $-V_{OP}$ = –15V, T_A = 25°C, no compensation, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-50G LIMIT	UNITS
Input Offset Voltage	V_{OS}		100	µV MAX
Input Bias Current	I_B		±10	nA MAX
Input Offset Current	I_{OS}		3	nA MAX
Output Voltage Swing	V_O	$R_L \geq 500\Omega$	±13	V MIN
Output Voltage Swing	V_O	V+ = $+V_{OP}$ = +5V, V– = $-V_{OP}$ = –5V R_L = 500Ω R_L = 50Ω	±3.5 ±2.5	V MIN
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±10V	110	dB MIN
Power Supply Rejection Ratio	PSRR	V_S = ±5V to ±15V	1	µV/V MAX
Large-Signal Voltage Gain	A_{VO}	V_O = ±10V, R_L = 1kΩ	7.5	V/µV MIN
Positive Current Limit	$+I_{SC}$	Output shorted to Ground	60	mA MIN
Negative Current Limit	$-I_{SC}$	Output shorted to Ground	60	mA MIN
Quiescent Supply Current	I_{SY}	No Load	3.3	mA MAX

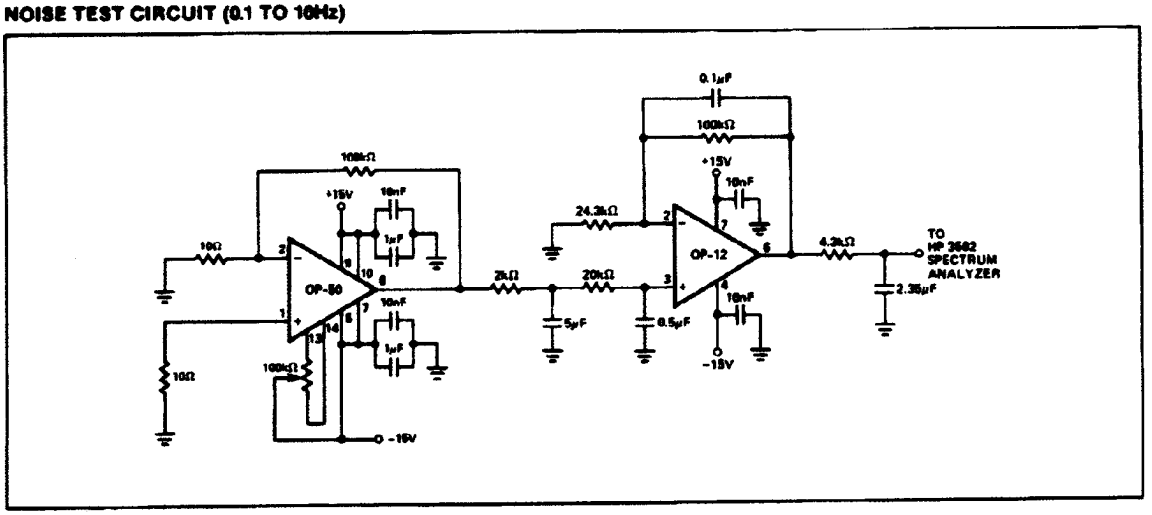
NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

OP-50

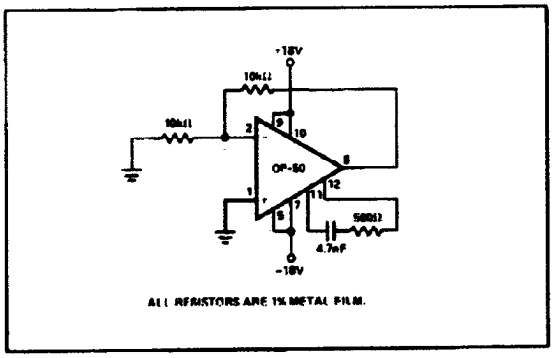
TYPICAL ELECTRICAL CHARACTERISTICS at $V+ = +V_{OP} = +15V$, $V- = -V_{OP} = -15V$, $T_A = 25°C$, no compensation, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-50G TYPICAL	UNITS
Slew Rate	SR	$R_L \geq 2k\Omega$ $R_C = 560\Omega$ $C_C = 4.7nF$	3	V/μs
Noise Voltage Density	e_n	f = 10Hz f = 1kHz	5.5 4.5	$nV/\sqrt{Hz}$
Input Noise Voltage	e_{np-p}	f = 0.1Hz to 10Hz	0.12	μV_{p-p}
Noise Current Density	i_n	f = 10Hz f = 1kHz	0.2 0.15	$pA/\sqrt{Hz}$
Capacitive Load Capability	C_L	$A_{VCL} \geq 5$ $R_C = 560\Omega$ $C_C = 4.7nF$	10	nF

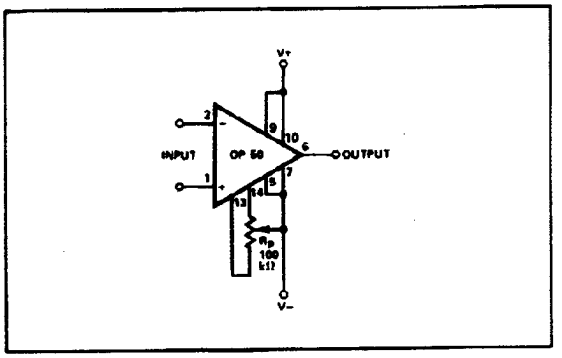
NOISE TEST CIRCUIT (0.1 TO 10Hz)



BURN-IN CIRCUIT

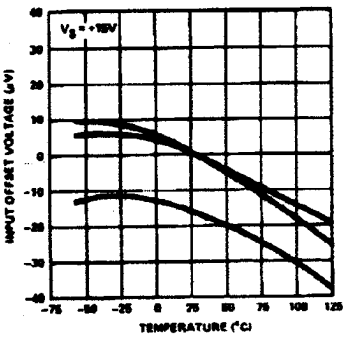


OFFSET NULLING CIRCUIT

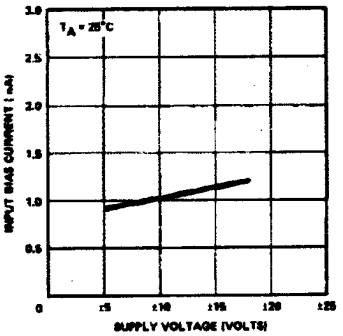


TYPICAL PERFORMANCE CHARACTERISTICS

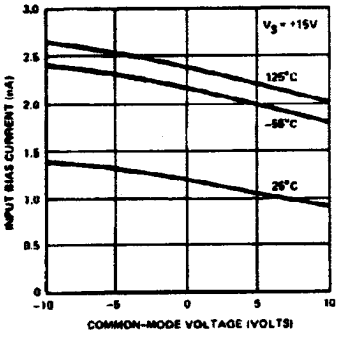
INPUT OFFSET VOLTAGE vs TEMPERATURE



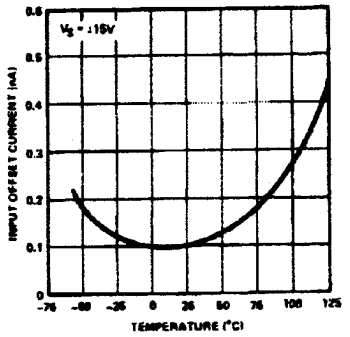
INPUT BIAS CURRENT vs SUPPLY VOLTAGE



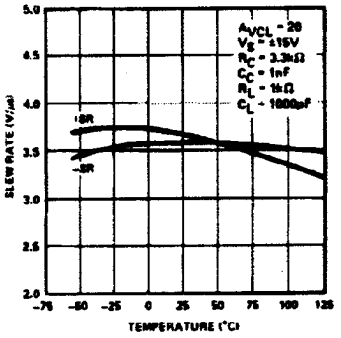
INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE



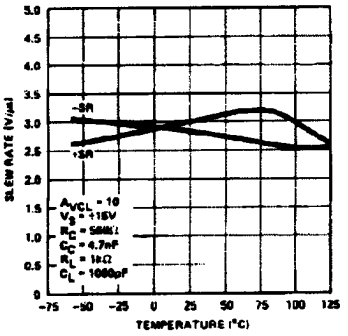
INPUT OFFSET CURRENT vs TEMPERATURE



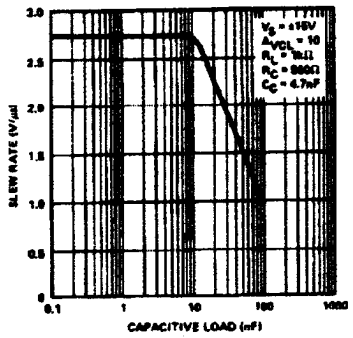
SLEW RATE vs TEMPERATURE



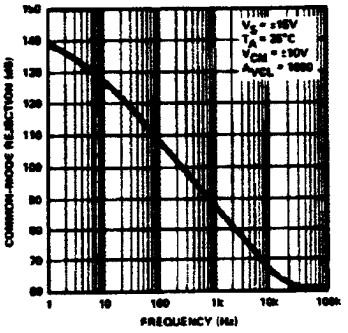
SLEW RATE vs TEMPERATURE



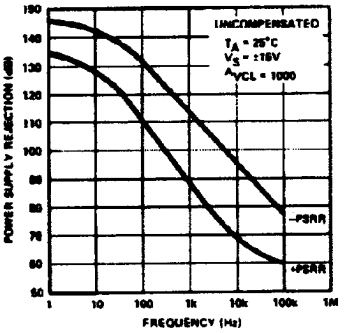
SLEW RATE vs CAPACITIVE LOAD



CMRR vs FREQUENCY



PSRR vs FREQUENCY

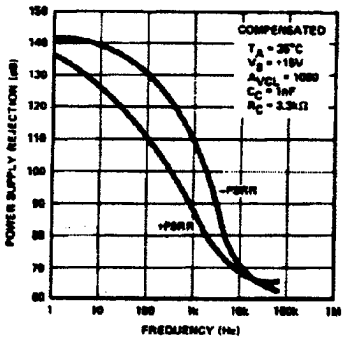


NOTE:
The symbol $\pm V_S$ is used to indicate the supply voltages when the main amplifier and the output stage are being operated at the same voltages.

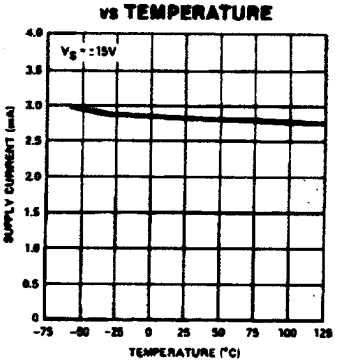
OP-50

TYPICAL PERFORMANCE CHARACTERISTICS

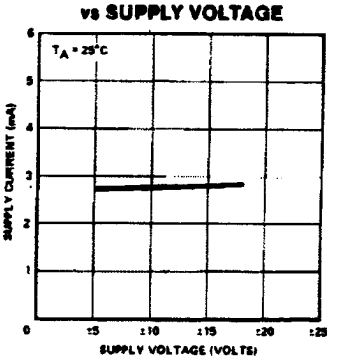
PSRR vs FREQUENCY



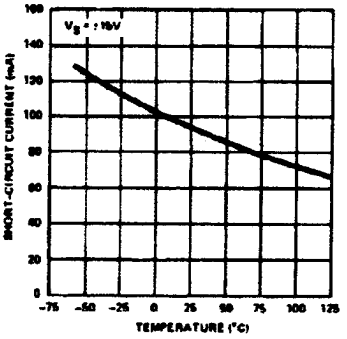
SUPPLY CURRENT vs TEMPERATURE



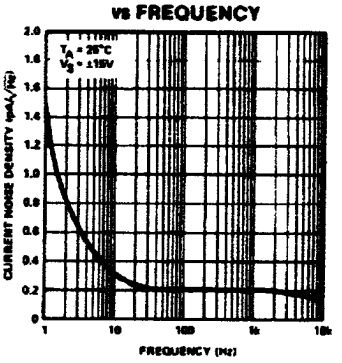
SUPPLY CURRENT vs SUPPLY VOLTAGE



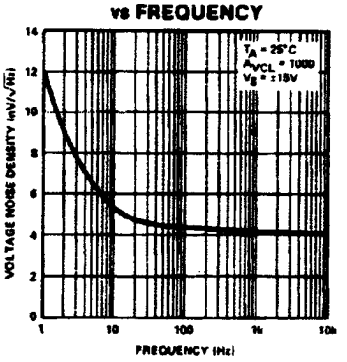
SHORT-CIRCUIT CURRENT vs TEMPERATURE



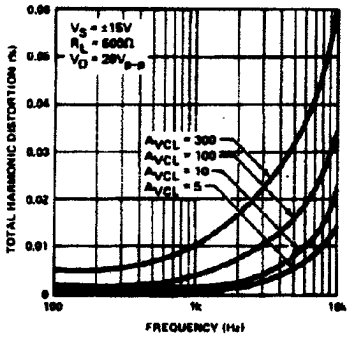
CURRENT NOISE DENSITY vs FREQUENCY



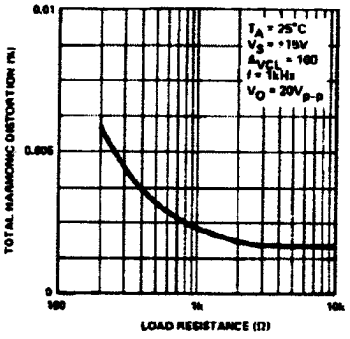
VOLTAGE NOISE DENSITY vs FREQUENCY



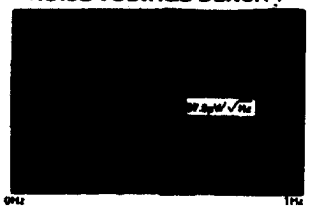
TOTAL HARMONIC DISTORTION vs FREQUENCY



TOTAL HARMONIC DISTORTION vs LOAD RESISTANCE



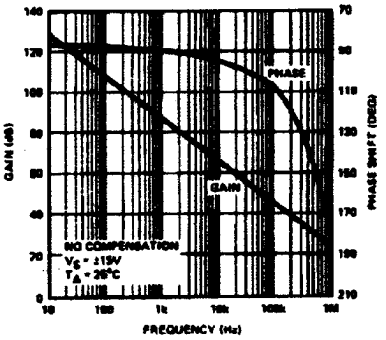
0 TO 1Hz NOISE VOLTAGE DENSITY



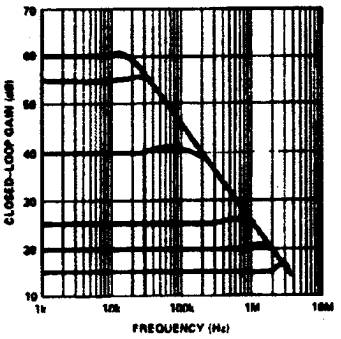
80.0μV FULL SCALE
10.0μV/DIV VERTICAL
A_{VCL} = 10,000

TYPICAL PERFORMANCE CHARACTERISTICS

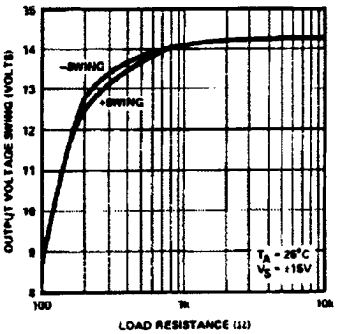
GAIN, PHASE SHIFT vs FREQUENCY



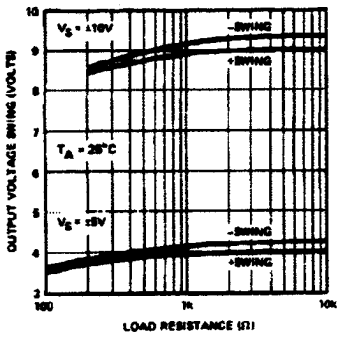
CLOSED-LOOP GAIN vs FREQUENCY



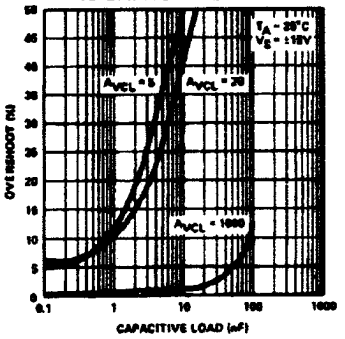
OUTPUT VOLTAGE SWING vs LOAD RESISTANCE



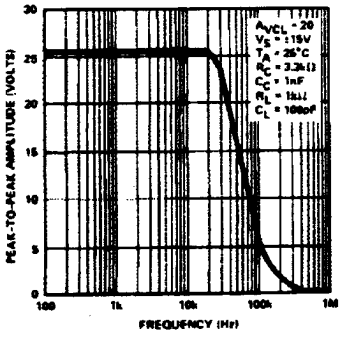
OUTPUT VOLTAGE SWING vs LOAD RESISTANCE



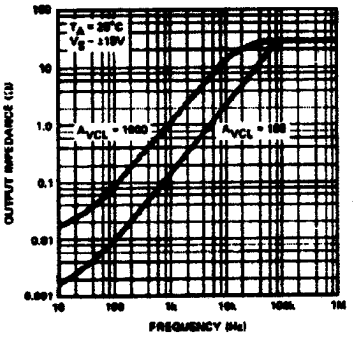
SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD



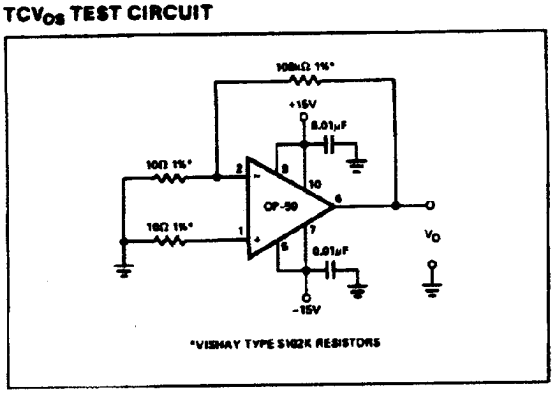
MAXIMUM OUTPUT SWING vs FREQUENCY



OUTPUT IMPEDANCE vs FREQUENCY



TCV_{OS} TEST CIRCUIT



APPLICATIONS INFORMATION

HIGH-SENSITIVITY VOLTAGE COMPARATOR

A comparator capable of resolving a submicrovolt difference signal is shown in Figure 1. The OP-50, operating without feedback, drives a second gain stage which generates a TTL-compatible output signal. Schottky-clamp diodes prevent overdriving of the long-tailed transistor pair and stop saturation of the output transistor. Power supply voltage is set to ±5V to lower the quiescent power dissipation and minimize thermal feedback due to output stage dissipation. Operating from ±5V supplies also reduces the OP-50 rise and fall times as the output slews over a reduced voltage range. This, in turn, reduces the output response time.

It is common practice with voltage comparators to ground one input terminal and to use a single-ended input. The historic reason is poor common-mode rejection on the input stage. In contrast, the OP-50 has very high common-mode rejection and is capable of detecting microvolt level differences in the presence of large common-mode signals.

The comparator is not fast, but it is very sensitive and can detect signal differences as low as 0.3μV. With large input overdrives, the circuit responds in approximately 3μs. If sharp transitions are needed, the use of a TTL Schmitt-trigger input is recommended. A table of Response Time vs. Input Overdrive is shown below.

INPUT OVERDRIVE	100mV	10mV	1mV	100μV	10μV
Positive Output Delay	3.2μs	5μs	40μs	340μs	2.4ms
Negative Output Delay	1.8μs	5μs	50μs	380μs	4.5ms

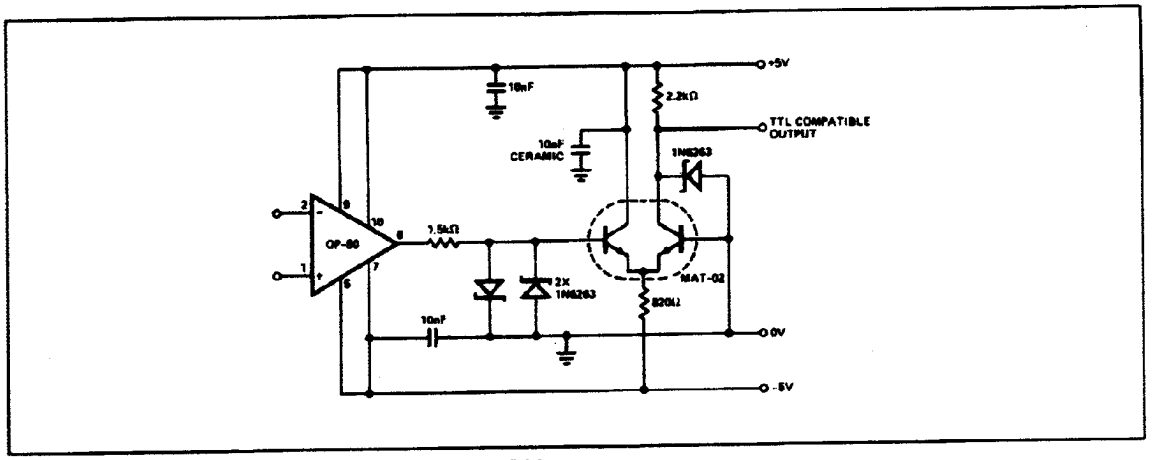


FIGURE 1: HIGH-SENSITIVITY VOLTAGE COMPARATOR

INTEGRATOR AND UNITY-GAIN BUFFER

Figure 2 shows a method of obtaining unity-gain in a buffer configuration. The R1 and C1 network provides input compensation to circumvent the minimum gain requirement. Figure 3 shows the same technique applied in the inverting mode to form a high precision integrator.

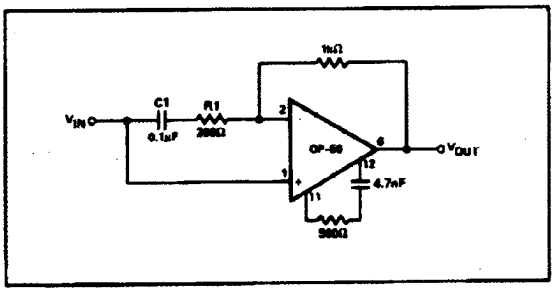


FIGURE 2: UNITY GAIN BUFFER

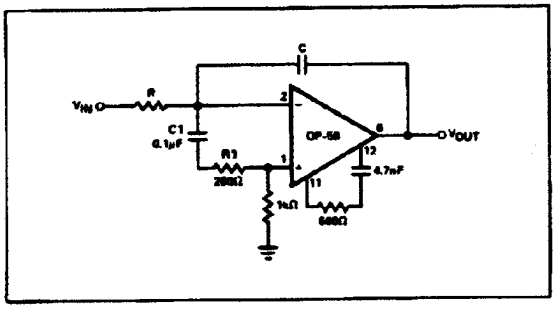


FIGURE 3: INTEGRATOR

20mA CURRENT SOURCE

The 20mA current source exploits the high output current and high linearity capabilities of the OP-50. Five precision resistors and a trim potentiometer are required in this circuit configuration, known as the Howland Current Pump. The trim potentiometer is used to balance the resistive feedback dividers. This maximizes the current-source output impedance. Compensation is selected for a voltage gain of 10.

Compliance is better than ±11V at an output current of 20mA and the trimmed output resistance is typically 2MΩ with $R_L \leq 500\Omega$. The transfer function is given by:

$$I_{OUT} = \frac{V_{IN\ (DIFF)} \times 10.1}{101}\ \text{Amps}$$

$V_{IN\ (DIFF)}$ is the differential input voltage. For the resistor values shown in Figure 4, the maximum $V_{IN\ (DIFF)}$ is 200mV.

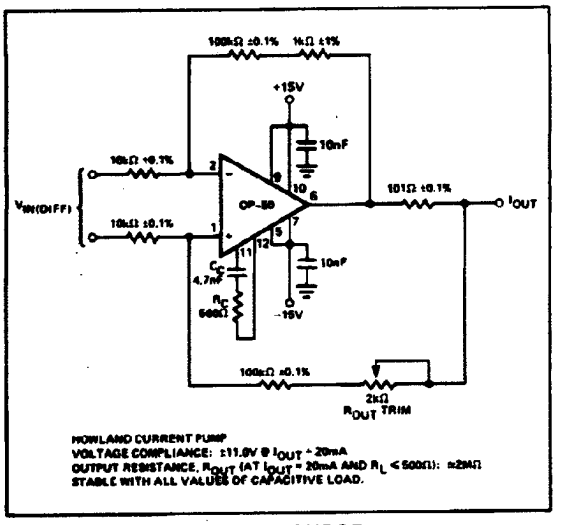


FIGURE 4: 20mA CURRENT SOURCE

DRIVING 50Ω LOADS

The OP-50 can provide up to 50mA into a 50Ω load and up to 26mA into a 500Ω load. The output is stable driving capacitive loads of up to 10nF.

Applications that make use of the high output current capability of the OP-50 will cause increased power dissipation in the amplifier. To reduce internal dissipation in these applications, external voltage dropping resistors can be connected in series with the output-stage power supply pins. As shown in Figure 5, 130Ω resistors can be attached to pin 7 ($-V_{OP}$) and to pin 10 ($+V_{OP}$). To maintain stability and specified performance levels, 0.047μF decoupling capacitors should be used as indicated from pin 7 and pin 10 to ground.

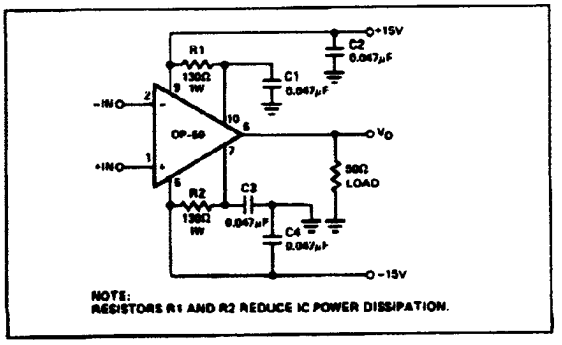


FIGURE 5: DRIVING 50Ω LOADS