Programmable Frequency Sweep and Output Burst Waveform Generator

Preliminary Technical Data

AD5930

FEATURES

- **Programmable frequency profile—no external components necessary**
- **Ouput frequency up to 25 Mhz**
- **Burst and listen capability**
- **Predefined frequency profile minimizes number of DSP/µcontroller writes**
- **Sinusoidal/triangular/square wave outputs**
- **Automatic or single pin control of frequency stepping**
- **Frequency starts at known phase—increments at 0° phase or phase continuous**
- **Powerdown mode (20 µA)**
- **+2.3 V to +5.5 V power supply**
- **Extended temperature range –40°C to +105°C**
- **20-lead TSSOP**

APPLICATIONS

- **Frequency Sweeping/Radar**
- **Network/Impedance Measurements**
- **Incremental Frequency stimulus**
- **Sensory Applications—Proximity and Motion**
- **BFSK**
- **Frequency Bursting/Pulse Trains**

GENERAL DESCRIPTION

The AD5930[1] is a waveform generator with programmable frequency sweep and output burst capability. Utilizing embedded digital processing allowing enhanced frequency control the device generates synthesized analog or digital frequency-stepped waveforms. Because frequency profiles are preprogrammed continuous write cycles are eliminated, thereby freeing up valuable DSP/µController resources. Waveforms start from a known phase and are incremented phase conti0nuously allowing phase shifts to be easily determined. Consuming only 8mA the AD5930 provides a convenient low power solution to waveform generation.

The AD5930 can be operated in three modes. In continuous output mode the device outputs the required frequency for a defined length of time and then steps to the next frequency. The length of time the device outputs a particular frequency can be either preprogrammed and the device increments the frequency automatically or alternatively can be incremented externally via the CTRL pin. In Burst mode, the device outputs it's frequency for a length of time and then returns to midscale for a further predefined length of time before stepping to the next frequency. In MSB mode a digital output is generated.

(continued on Page 3)

[1] Protected by US Patent Number 6747583, other patents pending.

FUNCTIONAL BLOCK DIAGRAM

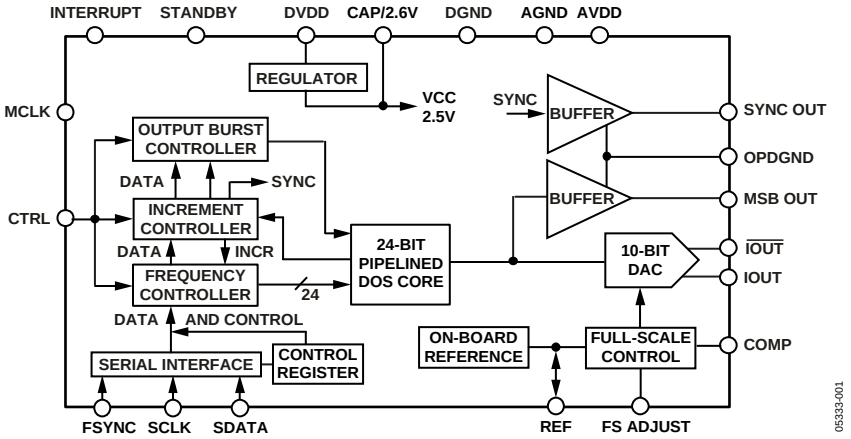

Figure 1.

Rev. PrF

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REVISION HISTORY

2/05—Revision PrF: Preliminary Version

GENERAL DESCRIPTION

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To program the device, the user enters the start frequency, the increment step size, the number of increments to be made and the time interval the part stays at each frequency. The frequency profile can be initiated by toggling the CTRL pin.

A number of different sweep profiles are offered. Frequencies can be stepped in triangular-sweep mode continuously sweeping up and down through the frequency range or in saw-sweep mode sweeping up but returning to the initial frequency before initiating the sweep again. In addition a single frequency or burst can generate without any sweep.

The AD5930 is written to via a 3-wire serial interface, which operates at clock rates up to 40 MHz. The device operates with a power supply from 2.3 V to 5.5 V and has a standby function which allows sections of the device that are not being used to be powered down.

The AD5930 is available in a 20-lead TSSOP package.

SPECIFICATIONS

AV_{DD} = DV_{DD} = +2.3 V to +5.5 V; AGND = DGND = 0 V; T_A = T_{MIN} to T_{MAX}; R_{SET} = 6.8 kΩ, R_{LOAD} = 200 Ω for IOUT and IOUTB, unless otherwise noted.

Table 1.

	Y Grade[2]				
Parameter	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
SIGNAL DAC SPECIFICATIONS					
Resolution		10		Bits	
Update Rate			50	MSPS	
Iout Fullscale[3]		3.124	4.0	mA	
Vout peak-to-peak		0.6		V	
Vout offset		30		mV	From 0V to the trough of the waveform
Output Compliance			0.8	V	AVDD = 2.3 V, Internal reference used
DC Accuracy:					
Integral Nonlinearity (INL)		±1		LSB	
Differential nonlinearity (DNL)		±0.5		LSB	
DDS SPECIFICATIONS					
Dynamic Specifications:					
Signal to Noise Ratio	55	60		dB	f_{MCLK} = 50 MHz, f_{OUT} = f_{MCLK}/4096
Total Harmonic Distortion		−66	−56	dBc	f_{MCLK} = 50 MHz, f_{OUT} = f_{MCLK}/4096
Spurious Free Dynamic Range (SFDR):					
Wideband (0 to Nyquist)		−60	−56	dBc	f_{MCLK} = 50 MHz, f_{OUT} = f_{MCLK}/50
NarrowBand (± 200 kHz)		−78	−67	dBc	f_{MCLK} = 50 MHz, f_{OUT} = f_{MCLK}/50
Clock Feedthrough		−50		dBc	
Wake Up Time		1		ms	
OUTPUT BUFFER					
Vout peak-to peak		DV_{DD}		V	Squarewave on MSB OUT
Output Rise/Fall Time		12		ns	
Output Jitter		120		ps rms	When DAC data MSB is output
VOLTAGE REFERENCE					
Internal Reference	1.12	1.18	1.24	V	
External Reference Range			1.3	V	
REFOUT Input Impedance		1		k Ω	
Reference TC		100		ppm/°C	
LOGIC INPUTS					
Input current			10	µA	
V_{INH}, input high voltage	1.7			V	Vdd = 2.3 V to 2.7 V
	2.0			V	Vdd = 2.7 V to 5.5 V
V_{INL}, input low voltage			0.7	V	Vdd = 2.3 V to 2.7 V
			0.8	V	Vdd = 2.7 V to 5.5 V
C_{IN}, input capacitance[3]		3		pF	
LOGIC OUTPUTS					
V_{OHL}, output high voltage	DV_{DD} − 0.8 V			V	I_{SINK} = 1 mA
V_{OL}, output low voltage			0.4	V	I_{SINK} = 1 mA
Floating-state O/P capacitance		8		pF	

Parameter	Y Grade[2]			Unit	Test Conditions/Comments
	Min	Typ	Max		
POWER REQUIREMENTS					f_{MCLK} = 50 MHz, $f_{OUT} = f_{MCLK}/7$
AVDD/DVDD	2.3		5.5	V	
I_{AA}		3.8	5	MA	
I_{DD}		2.0	3	mA	
$I_{AA} + I_{DD}$		5.8	8	mA	
Low Power Sleep Mode		20		µA	All outputs powered down, MCLK =0MHz, Serial interface active

[2] Operating temperature range is as follows: Y Version: −40°C to + 105°C; typical specifications are at 25°C.
[3] Guaranteed by Design.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Rating
AVDD to AGND	−0.3 V to +6 V
DVDD to DGND	−0.3 V to +6 V
AGND to DGND.	−0.3 V to +0.3 V
CAP/2.5V to DGND	2.75 V
Digital I/O Voltage to DGND	−0.3 V to DVDD + 0.3 V
Analog I/O Voltage to AGND	−0.3 V to AVDD + 0.3 V
Operating Temperature Range	
Extended (Y Version)	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	+150°C
TSSOP Package	
θ_{JA} Thermal Impedance	143°C/W
θ_{JC} Thermal Impedance	45°C/W
Lead Temperature, Soldering (10 sec)	300°C
IR Reflow, Peak Temperature	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTIONAL DESCRIPTIONS

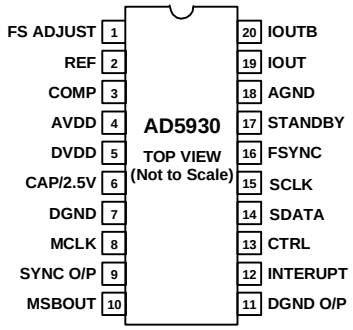

Figure 2.

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	FSADJUST	Full-Scale Adjust Control. A resistor (R_{SET}) must be connected externally between this pin and AGND. This determines the magnitude of the full-scale DAC current. The relationship between R_{SET} and the full-scale current is as follows: $IOUT_{FULL\text{-}SCALE} = 18 \times V_{REFOUT}/R_{SET}$ V_{REFOUT} = 1.20 V nominal, R_{SET} = 6.8 kΩ typical
2	REF	Voltage Reference, can be an input or an output. The AD5930 has an internal 1.20 V reference, which is made available at this pin. Alternatively, this reference can be overdriven by an external reference, with a voltage range as given in the specifications. A 10 nF decoupling capacitor should be connected between REF and AGND.
3	COMP	DAC Bias Pin. This pin is used for de-coupling the DAC bias voltage to AVDD.
4	AVDD	Positive power supply for the analog section. AVDD can have a value from +2.3 V to +5.5 V. A 0.1 µF decoupling capacitor should be connected between AVDD and AGND.
5	DVDD	Positive power supply for the digital section. DVDD can have a value from +2.3 V to +5.5 V. A 0.1 µF decoupling capacitor should be connected between DVDD and DGND.
6	CAP/2.5V	The digital circuitry operates from a +2.5 V power supply. This +2.5 V is generated from DVDD using an on board regulator. The regulator requires a decoupling capacitor of typically 100 nF which is connected from CAP/2.5 V to DGND. If DVDD is equal to or less than +2.7 V, CAP/2.5 V can be shorted to DVDD.
7	DGND	Ground for all Digital Circuitry (excluding digital output buffers).
8	MCLK	Digital Clock Input. DDS output frequencies are expressed as a binary fraction of the frequency of MCLK. The output frequency accuracy and phase noise are determined by this clock.
9	SYNC O/P	Digital Output for Sweep Status information. User selectable for "End of Sweep" (EOS), or Frequency Increments through the control register (SYNCOP bit). This pin must be enabled through setting control register bit SYNCOPEN to 1.
10	MSB OUT	Digital Output. The inverted MSB of the DAC data is available at this pin. This output pin must be enabled by setting bit OPBITEN in the control register to 1.
11	OPDGND	Separate DGND connection for digital output buffers. Connect to DGND.
12	INTERUPT	Digital Input. This pins acts as an interupt during a frequency sweep. A Low to High transition is sampled by the internal MCLK, which resets internal state machines. This results in the DAC output going to midscale.
13	CTRL	Digital Input. Triple Function pin for Initalisation, Start and External frequency Increments. A low-to-high transition, sampled by the internal MCLK, is used to initalise and start internal state machines, which then execute the pre-programmed frequency sweep sequence. When in Auto-Increment mode, a single pulse executes the entire sweep sequence, while in External – Increment mode, each frequency increment is triggered by low-to-high transitions.
14	SDATA	Serial Data Input. The 16-bit serial data word is applied to this input, with the register address first followed by the MSB to LSBs of the data.
15	SCLK	Serial Clock Input. Data is clocked into the AD9834 on each falling SCLK edge.
16	FSYNC	Active Low Control Input. This is the frame synchronisation signal for the serial data. When FSYNC is taken low, the internal logic is informed that a new word is being loaded into the device.
17	STANDBY	Active high digital input. When this pin is high, the internal MCLK is disabled, and the reference, DAC and regulator are powered down. This resultsin a shutdown current of typically 20 µA.
18	AGND	Ground for all Analog Circuitry.

Pin No.	Mnemonic	Description
19	IOUT	Current Output. This is a high impedance current source output. A load resistor of nominally 200 Ω should be connected between IOUT and AGND. A 20 pF capacitor to AGND is also recommended to act as a low-pass filter and to reduce clock feedthrough. In conjuction with IOUTB, a differential signal is available.
20	IOUTB	Current Output. IOUTB is the complimentary of IOUT. This pin should preferably be tied through an external load resistor of 200 Ω to AGND but can be tied directly to AGND. A 20 pF capacitor to AGND is also recommended as a low-pass filter and to reduce clock feedthrough. In conjuction with IOUT, a differential signal is available.

TERMINOLOGY

Integral Nonlinearity
This is the maximum deviation of any code from a straight line passing through the endpoints of the transfer function. The endpoints of the transfer function are zero scale, a point 0.5 LSB below the first code transition (000 . . . 00 to 000 . . . 01) and full scale, a point 0.5 LSB above the last code transition (111 . . . 10 to 111 . . . 11). The error is expressed in LSBs.

Differential Nonlinearity
This is the difference between the measured and ideal 1 LSB change between two adjacent codes in the DAC. A specified differential nonlinearity of ±1 LSB maximium ensures monotonicity.

Output Compliance
The output compliance refers to the maximum voltage that can be generated at the output of the DAC to meet the specifications. When voltages greater than that specified for the output compliance are generated, the AD9834 may not meet the specifications listed in the data sheet.

Spurious Free Dynamic Range
Along with the frequency of interest, harmonics of the fundamental frequency and images of the frequencies are present at the output of a DDS device. The spurious free dynamic range (SFDR) refers to the largest spur or harmonic which is present in the band of interest. The wide band SFDR gives the magnitude of the largest harmonic or spur relative to the magnitude of the fundamental frequency in the 0 to Nyquist bandwidth. The narrow band SFDR gives the attenuation of the largest spur or harmonic in a bandwidth of ±200 kHz about the fundamental frequency.

Total Harmonic Distortion
Total Harmonic Distortion (THD) is the ratio of the rms sum of harmonics to the rms value of the fundamental. For the AD5930, THD is defined as:

$$THD(\text{dB}) = 20\log\frac{\sqrt{V_2^{\,2} + V_3^{\,2} + V_4^{\,2} + V_5^{\,2} + V_6^{\,2}}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonic.

Signal-to-Noise Ratio (SNR)
S/N is the ratio of the rms value of the measured output signal to the rms sum of all other spectral components below the Nyquist frequency. The value for SNR is expressed in decibels.

Clock Feedthrough
There will be feedthrough from the MCLK input to the analog output. Clock feedthrough refers to the magnitude of the MCLK signal relative to the fundamental frequency in the AD5930's output spectrum.

DETAILED OPERATION

The AD5930 is a General Purpose Synthesized Waveform Generator capable of providing digitally programmable Waveform Sequences in both the frequency and time domain. The device contains embedded digital processing to provide a repetitive sweep of a user-programmable frequency profile allowing enhanced frequency control. Because the device is pre-programmable, it eliminates continuous write cycles from a DSP/microcontroller in generating a particular waveform.

The frequency profile is defined by a Start Frequency (F_{START}), a Frequency Increment (Δf) and the number of increments per Sweep (N_{INCR}). The Increment interval between frequency increments, (t_{INT}), is either user-programmable and frequency automatically incremented by the device or externally controlled via a hardware pin. For automatic update the interval profile can either be for a fixed number of clock periods or for a fixed number of output waveform cycles.

In the auto-increment mode, a single pulse at the CTRL pin starts and executes the frequency sweep. In the external-increment mode the CTRL pin also starts the sweep but the frequency increment interval is determined by the time interval between sequential 0 /1 transitions on the CTRL pin. Furthermore, the CTRL pin can be used to directly control the burst profile, where during the input high time, the output waveform is present, and during the input low-time, the output is reset to midscale

The frequency profile can be swept in two different modes:

Saw Sweep or
Triangular (Up/Down) Sweep

In the case of a saw-sweep, the AD5930 sweeps repeatedly between sweep-start to Sweep-end, i.e. from F_{START} incrementally to ($F_{START} + N_{INCR} \times \Delta f$), and then returns directly to F_{START} to begin again. This is shown in Figure 3. This gives a saw-sweep cycle time of $(N_{INCR} + 1) \times T_{INCR}$.

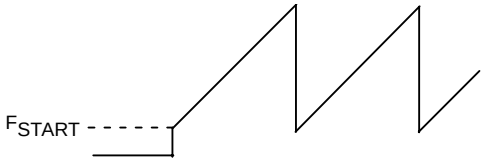

Figure 3. Saw sweep

In the case of a triangular sweep, the AD5930 sweeps repeatedly between sweep-start to Sweep-end, that is. from FSTART incrementally to (FSTART + NINCR × Δf), and then returning to FSTART in a decremental manner. This is shown in Figure 4. The triangular-sweep cycle time time is given by (2 × NINCR) × TINCR.

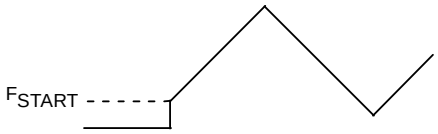

Figure 4. Triangular Sweep

The AD5930 offers two possible output modes: Continuous Output Mode and Burst Output mode. Both of these modes are illustrated in Figure 5.

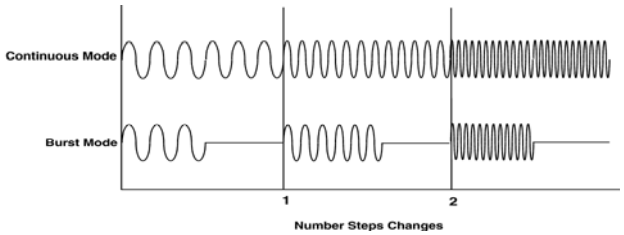

Figure 5. Continuous Mode and Burst Modes of the AD5930

In Continuous Output mode, each frequency of the sweep is available for the length of time programmed into the Time Interval (t_{INT}) register. This means the frequency swept output signal is continuously available, and is therefore phase continuous at all frequency increments.

In Burst Output Mode the AD5930 provides a programmable burst of the waveform output for a fixed length of time (T_{BURST}) within the programmed Increment interval (T_{INT}), after which the output is reset back to midscale and remains there until the next frequency increment. The beginning of each frequency increment is at midscale (Phase 0 Rad) and lasts for the programmed duration, after which it is reset back to midscale and remains there until the next frequency increment. This is very useful in applications where the user needs to burst a frequency for a set period, and then perhaps 'listen' for a response before incrementing to the next frequency. Also, because each frequency is starting from midscale, the phase of the signal is always known.

The AD5930 offers two digital outputs, available from the MSB OUT pin and the SYNC O/P pin. The inverted MSB of the DAC data is available at the MSB OUT pin, this could be used as a coarse clock. The SYNC O/P can be used to give the status of the sweep. It is user selectable for the End of the Sweep, or to output a $4 \times T_{CLOCK}$ pulse at frequency increments.

FUNCTIONAL DESCRIPTION

Serial Interface

The AD5930 has a standard 3-wire serial interface, which is compatible with SPI, QSPI, MICROWIRE and DSP interface standards.

Data is loaded into the device as a 16-bit word under the control of a serial clock input, SCLK. The timing diagram for this operation is given in Figure 4.

The FSYNC input is a level triggered input that acts as a frame synchronization and chip enable. Data can only be transferred into the device when FSYNC is low. To start the serial data transfer, FSYNC should be taken low, observing the minimum FSYNC to SCLK falling edge setup time, t_7. After FSYNC goes low, serial data will be shifted into the device's input shift register on the falling edges of SCLK for 16 clock pulses.

FSYNC may be taken high after the sixteenth falling edge of SCLK, observing the minimum SCLK falling edge to FSYNC rising edge time, t_8.Alternatively, FSYNC can be kept low for a multiple of 16 SCLK pulses, and then brought high at the end of the data transfer. In this way, a continuous stream of 16 bit words can be loaded while FSYNC is held low, FSYNC only going high after the 16th SCLK falling edge of the last word loaded.

The SCLK can be continuous or, alternatively, the SCLK can idle high or low between write operations.

Powering Up the AD5930

When the AD5930 is powered up, the part is in an-defined state, and therefore must be reset before use. The 8 registers (control and frequency) will contain invalid data and, therefore, should all be set to a known value by the user. The control register should be the first register to be programmed, as this sets up the part. Note that a write to the control register will automatically reset the internal state machines, and will provide an analog output of midscale as it provides the same function as the INTERRUPT pin. Typically, this is followed by a serial loading of all the required sweep parameters. The DAC output remains at midscale until a sweep is started using the CTRL pin.

OUTPUTS FROM THE AD5930

The AD5930 offers a variety of outputs from the chip. The analog outputs are available from the IOUT/IOUTB pins, and include a sinewave and a triangle output. The square-wave output is available from the MSB OUT pin.

Sinusoidal Output: The SIN ROM is used to convert the phase information from the frequency and phase registers into amplitude information, which results in a sinusoidal signal at the output. To have a sinusoidal output from the IOUT/IOUTB pins, set the bit SINE/TRI (D9) = 1.

Triangle Output: The SIN ROM can be bypassed so that the truncated digital output from the NCO is sent to the DAC. In this case, the output is no longer sinusoidal. The DAC produces 10-bit linear triangular function. To have a triangle output from the IOUT/IOUTB pins, set the bit SINE/TRI (D9) = 0.
Note that the DAC ENABLE bit (D10) must be "1" (that is. the DAC is enabled) when using these pins.

Digital Outputs: The digital outputs are available from the MSB OUT pin and the SYNCOP pin. The inverse of the MSB of the DAC data is available at the MSB OUT pin. The MSB OUT pin must be enabled before use. The enabling/disabling of this pin is controlled by the bit MSBOUTEN (D8) in the control register. When MSBOUTEN = 1, this pin is enabled. This is useful as a synthesised clock source.

PROGRAMMING THE AD5930

The AD5930 is designed to provide automatic frequency sweeps when the CTRL pin is triggered. The automatic sweep is controlled by a set of registers, the addresses of which are given in the table below. The function of each register is described in the subsequent pages.

Table 4. Regsister Adresseses

Register Address					
D15	D14	D13	D12	Mnemonic	Name
0	0	0	0	C_{REG}	Control Bits
0	0	0	1	N_{INCR}	Number of Increments
0	0	1	0	Δf	Lower 12 bits of Delta Frequency
0	0	1	1	Δf	Higher 12 bits of Delta Frequency
0	1			T_{INT}	Increment Interval
1	0			T_{BURST}	Burst Interval
1	1	0	0	F_{START}	Lower 12 bits of Start Frequency
1	1	0	1	F_{START}	Higher 12 bits of Start Frequency
1	1	1	0		Reserved
1	1	1	1		Reserved

The Control Register

The AD5930 contains a 12-bit control register which sets up the operating modes of the AD5930. The different functions and the various output options from the AD5930 are controlled by this register. Table 5 below describes the individual bits of the control register.

To address the control register, D15 to D12 of the 16-bit serial word must be set to '0' .

Table 5.Control Register

D15	D14	D13	D12	D11 D0
0	0	0	0	CONTROL BITS

Table 6. Description of bits in the Control Register

Bit	Name	Function
D15–D12	ADDR	Register Address bits.
D11	B24	Two write operations are required to load a complete word into the F_{START} register and the Δf register. B24 = '1' allows a complete word to be loaded into a frequency register in two consecutive writes. The first write contains the 12 LSBs of the frequency word and the next write will contain the 12 MSBs. Refer to Table 4 for the appropriate addresses. The write to the destination register occurs after both words have been loaded, so the register never holds an intermediate value. When B24 = '0' the 24-bit F_{START} /Δf register operates as 2 12-bit registers, one containing the 12 MSBs and the other containing the 12 LSBs. This means that the 12 MSBs of the frequency word can be altered independent of the 12 LSBs and vice versa. This is useful if the complete 24 bit update is not required. To alter the 12 MSBs or the 12 LSBs, a single write is made to the appropriate register address. Refer to Table 4 for the appropriate addresses.
D10	DAC ENABLE	When DAC ENABLE = '1', the DAC is enabled. When DAC ENABLE = '0', the DAC is powered down. This is useful if a user is just using the MSB of the DAC data (available at the MSBOUT pin), and wants to save power.
D9	SINE/TRI	The function of this bit is to control what is available at the IOUT/IOUT pins. When SINE/TRI = '1' the SIN ROM is used to convert the phase information into amplitude information which results in a sinusoidal signal at the output (See Table 4). When SINE/TRI = '0', the SIN ROM is bypassed, resulting in a triangular (up-down) output from the DAC.
D8	MSBOUTEN	When MSBOUTEN = '1', the MSBOUT pin is enabled. When MSBOUTEN = '0', the MSBOUT is disabled (tri-state).
D7	CW/BURST	When CW/BURST = '1', the AD5930 outputs each frequency continuously for the length of time (T_{CLOCK}) or number of output waveform cycles (T_{CYCLE}) specified in the appropriate register. When CW/BURST = '0', the AD5930 bursts each frequency for the length of time/number of cycles specified in the burst register (B_{CLOCK} or B_{CYCLE}). For the remainder of the time within each increment window ($T_{CLOCK} - B_{CLOCK}$) or ($T_{CYCLE} - B_{CYCLE}$) the AD5930 outputs a DC value of midscale. In external increment mode, it is defined by the pulse widths on the CTRL pin.
D6	INT/EX BURST	This bit is active when D7 = 0 and is also used in conjunction with D5. When the user is incrementing the frequency externally (D5 = 1), D6 dictates whether the user is controlling the burst internally or externally. When INT/EXT BURST = '1' the output burst is controlled externally through the CTRL pin. This is useful if the user is using an external source to trigger the frequency increments and the burst interval is also to be determined externally. When the bit INT/EXT BURST = '0' the output burst is controlled internally. The burst is pre-programmed by the user into the B_{CLOCK} or B_{CYCLE} register (the burst interval can either be clock based or for a specified number of output cycles). When D5 = 0, this bit is ignored.
D5	INT/EX INCR	When INT/EX INCR = '1' the frequency increments are triggered externally through the CTRL pin. When INT/EX INCR = '0', the frequency increments are triggered automatically.
D4	MODE	The function of this bit is to control what type of frequency sweep is carried out. When MODE = '1', the frequency profile is a saw-sweep. When MODE = '0', the frequency profile is a triangular (Up-Down) Sweep.
D3	SYNCSEL	User selectable for "End of Sweep" (EOS), or Frequency Increments When SYNCSEL = '1', the SYNCOP pin outputs a high level the End of the sweep and returns to zero at the start of the subsequent sweep. When SYNCSEL= '0', the SYNCOP outputs a pulse of $4 \times T_{CLOCK}$ only at each positive frequency increment.
D2	SYNCOUTEN	When SYNCOUTEN= '1', the SYNC output is available at the pin SYNCOP. When SYNCOUTEN= '0', the SYNCOP pin is disabled (tri-state).
D1	Reserved	This bit must always be set to 1.
D0	Reserved	This bit must always be set to 1.

SETTING UP THE SWEEP

As stated previously, the AD5930 requires certain registers to be programmed to enable a frequency sweep. The frequency profile is described by data for the Start Frequency (F_{START}), the Frequency Increment (Δf) and for the number of increments per Sweep (N_{INCR}). The Increment interval (T_{INT}) between frequency increments during the sweep is user-programmable, and can either be for a fixed number of clock periods or for a fixed number of output waveform cycles. The following section discusses these registers in more detail.

Start Frequency (F_{START})

To start a frequency sweep, the user needs to tell the AD5930 what frequency to start sweeping from. This frequency is stored in a 24-bit register called F_{START}. If the user wishes to alter the entire contents of the F_{START} register, two consecutive writes must be preformed, one to the LSBs and the other to the MSBs. Note that for an entire write to this register, the control bit B24 (D11) should be set to '1'. With the LSBs programmed first.

Table 7. F_{START} Register Bits

D15	D14	D13	D12	D11 D0
1	1	0	0	12 LSBs of F_{START} <11….0>
1	1	0	1	12 MSBs of F_{START} <23….12>

In some applications, the user does not need to alter all 24 bits of the F_{START} register. By setting the control bit B24 (D11) to '0', the 24-bit register operates as two 12-bit registers, one containing the 12 MSBs and the other containing the 12 LSBs. This means that the 12MSBs of the F_{START} word can be altered independently of the 12 LSBs, and vice versa. The addresses of both the LSBs and the MSBs of this register is given in Table 7.

Frequency Increments (Δf)

The value in the Δf register sets the Increment frequency for the sweep and is added incrementally to the current frequency being output. Note that the increment frequency can be positive or negative, thereby giving an increasing or decreasing frequency sweep.

At the start of a sweep, the frequency contained in the F_{START} register will be output. Next, the frequency (F_{START} + Δ f) will be output. This will be followed by (F_{START} + Δ f + Δf) and so on. Multiplying the Δf value by the number of Increments (N_{INCR}), and adding it to the start frequency (F_{START}), will give the final frequency in the sweep. Mathematically this final frequency /stop frequency is represented by F_{START} + (N_{INCR} × Δ f). The Δf register is a 23-bit register, and requires two 16-bit writes to be programmed. Table 8 gives the addresses associated with both the MSB and LSB registers of the Δf word.

Table 8. Δf Register Bits

D15	D14	D13	D12	D11	D10	D0	Sweep Direction
0	0	1	0	12 LSBs of Δf <11….0>			n/a
0	0	1	1	0	11 MSBs of Δf <22….12>		Positive Δf (F_{START} + Δf)
0	0	1	1	1	11 MSBs of Δf <22….12>		Negative Δf (F_{START} - Δf)

Number of Increments (N_{INCR})

An End frequency, or a maximum/minimum frequency before the sweep changes direction is not required on the AD5930. Instead, this End frequency is calculated by multiplying the frequency Increment value (Δf) value by the number of Frequency Steps (N_{INCR}), and adding it to/subtracting it from the start frequency (F_{START})., i.e. F_{START} + (N_{INCR} × Δ f).
The N_{INCR} register is a 12 bit register, with the address shown in the table below.

Table 9. N_{INCR} Register Bits

D15	D14	D13	D12	D11	D0
0	0	0	1	12 bits of N_{INCR}	<11….0>

The number of increments is programmed in binary fashion, with 000000000010 representing the minimum number of frequency increments (2 increments), and 111111111111 representing the maximum number of increments (4095).

Table 10. N_{INCR} Data Bits

D11		D0	No. of Increments
0000	0000	0010	2 frequency increments. This is a minimum number of Frequency Increments
0000	0000	0011	3 frequency increments.
0000	0000	0100	4 frequency increments.
	…		…
1111	1111	1110	4094 frequency increments.
1111	1111	1111	4095 frequency increments.

Increment Interval (T_{INT})

The increment interval dictates the duration for which the DAC output signal for each individual frequency of the Frequency sweep will be available. The AD5930 offers the user two choices:

- To have the duration as a multiple of cycles of the output frequency.
- To have the duration as a multiple of MCLK periods.

This is selected by Bit D13 in the T_{INT} register as shown in Table 11.

Table 11. t_{INT} Register Bits

D15	D14	D13	D12	D11	D10 D0
0	1	0	x	x	11 bits <10 …..0> Fixed number of output waveform cycles
0	1	1	x	x	11 bits <10 ….0> Fixed number of clock periods

Programming of this register is in binary form with the minimum number being decimal 2. Note from the table above that there are 11 bits, <D10 to D0>, of the register available to program the time interval As an example, for MCLK = 50 MHz, each clock period/base interval is (1/50 MHz) = 20 ns. If, for example, each frequency needs to be output for 100ns, then <00000000101> or decimal 5 needs to be programmed to this register. Note that the AD5930 can output each frequency for a maximum duration of 2^{11} −1 (or 2047) times the increment interval. So for the MCLK = 50MHz example, a time interval of 20 ns × 2047 = 40 µs is maximum, with the minimum being 40 ns.

In the example above, the maximum time that an individual frequency can be output is 40 µs. For some applications, this may be insufficient. Therefore to cater for sweeps that need a longer Increment Interval, Time-base Multipliers are provided. In Table 11, D12 and D11 are dedicated to the Time-base Multipliers. A more detailed table of the Multiplier options is given in Table 12 below.

To explain this via an example, and again assuming an MCLK of 50 MHz. If a multiplier of 500 is used, then the base interval is now (1/(50 MHz) x 500)) = 10µs. Therefore, using a multiplier of 500, the maximum Increment Interval is 10 µs × 2^{11-1} = 20.5 ms. Therefore, as can be seen from the example above, the option of Time-base Multipliers gives the user great flexibility when programming the length of the frequency window as any frequency can be output for a minimum of 40 ns up to a maximum of 20.5 ms.

Table 12. Time-base Multiplier Values

D12	D11	Multiplier value
0	0	Multiply (1/MCLK) by 1
0	1	Multiply (1/MCLK) by 5
1	0	Multiply (1/MCLK) by 100
1	1	Multiply (1/MCLK) by 500

Length of Sweep Time

The length of time to complete a user-programmed frequency sweep is given by the following equation:

$$T_{SWEEP} = (1 + N_{INCR}) \times T_{INT}$$

Burst Time Resister(T_{BURST})

As described previously, the AD5930 offers the user the ability to output each frequency in the Sweep for length of time within the Increment Interval (T_{INT}), and then return to midscale for the remainder of the time (T_{INT} – T_{BURST}) before stepping to the next frequency. The Burst option must be enabled and this is done by setting bit D7 in the control register to '0'.
Similar to the Time Interval Register, the Burst register can

- have its duration as a multiple of cycles of the output frequency.
- have its duration as a multiple of MCLK periods.

The address for this register is given in Table 13.

Table 13. C_{BURST}/ F_{BURST} Register Bits

D15	D14	D13	D12	D11	D10 D0
1	0	0	x	x	11 bits of <0….10> Fixed number of output waveform cycles
1	0	1	x	x	11 bits of <0….10> Fixed number of clock periods

However, note that when using both the Increment Interval (T_{INT}) and Burst Time Register (T_{BURST}), the settings for D13 should be the same. In instances where they differ, the AD5930 will default to the value programmed into the T_{INT} register. Similarly for bits 12 and 11, the Time-base multiplier bits, these will always default to the value programmed into the T_{INT} register.

ACTIVATING AND CONTROLLING THE SWEEP

After the registers have been programmed, a 0->1 transition on the CTRL pin starts the sweep. The sweep will always start from the frequency programmed into the F_{START} register, it will change by the value in the ΔF register, and will increment by the number of steps in the N_{INCR} register. But both the Time Interval of each frequency and the Burst duration of each frequency can be controlled internally using the registers t_{INT} and t_{BURST} or externally using the CTRL pin. The options available are described below.

Auto-Increment, Auto-Burst Control

The values in the T_{INT} and T_{BURST} registers are used to control the sweep. The AD5930 will burst each frequency for the length of time programmed in the T_{BURST} register, and will output midscale for the remainder of the interval time (T_{INT} – T_{BURST}). To setup the AD5930 to this mode, D7 in the control register must be set to '0'; bit D6 must be set to '0' and bit D5 must be set to '0'.

External Increment, Auto-Burst Control

The Time Interval, t_{INT}, is set by the pulse rate on the CTRL pin. The first 0->1 transition on the pin starts the sweep. Each subsequent 0->1 transition on the CTRL pin increments the output frequency by the value programmed into the ΔF register. For each Increment Interval, the AD5930 will output each frequency for the length of time programmed into the T_{BURST} register, and will output midscale until the CTRL pin is pulsed again. Note that for this mode. The values programmed into D13, D12 and D11 of the T_{BURST} register are used.

External Increment, External Burst Control

Both the Increment Interval (T_{INT}) and the Burst Interval (T_{BURST}) are controlled by the CTRL pin. A 0->1 transition on the CTRL pin starts the sweep. The duration of CTRL high then dictates the length of time the AD5930 will burst that frequency. The low time of CTRL is the 'listen' time, that is, for how long the part will remain at midscale. Bringing the CTRL pin high again will initiate a frequency increment, and the pattern continues. For this mode, the settings for D13, D12 and D11 are ignored.

Setting Up the AD5930 to Operate in Continuous Mode

To operate the AD5930 in continuous mode, the CW/BURST bit (D7) in the control register must be set to '1'.

Setting Up the AD5930 to Operate in Burst Mode

To set up the AD5930 in BURST mode, the CW/BURST bit (D7) in the control register must be set to '0'.

OUTLINE DIMENSIONS

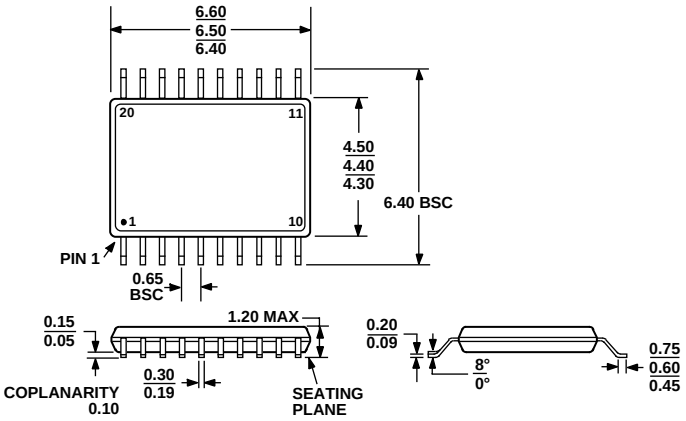

Figure 6. 20-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-20)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD5930YRU	−40 °C to +105 °C	20-Lead Thin Shrink Small Outline Package [TSSOP]	RU-20
AD5930YRU-REEL	−40 °C to +105 °C	20-Lead Thin Shrink Small Outline Package [TSSOP]	RU-20

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