10-Bit, 12-Channel Decimating LCD DECDRIVER® with Level Shifters

AD8385

FEATURES

- **High voltage drive to within 1.3 V of supply rails**
- **Output short-circuit protection**
- **High update rates**
  - **Fast, 100 Ms/s 10-bit input data update rate**
- **Static power dissipation: 1.84 W**
  - **Voltage controlled video reference (brightness), offset, and full-scale (contrast) output levels**
- **INV bit reverses polarity of video signal**
- **3.3 V logic, 9 V to 18 V analog supplies**
  - **Level shifters for panel timing signals**
- **High accuracy voltage outputs**
  - **Laser trimming eliminates the need for adjustments or calibration**
- **Flexible logic**
  - **STSQ/XFR allow parallel AD8385 operation**
- **Fast settling into capacitive loads**
  - **30 ns settling time to 0.25% into 150 pF load**
  - **Slew rate 460 V/µs**
- **Available in 100-lead 14 mm × 14 mm TQFP E-pad**

GENERAL DESCRIPTION

The AD8385 provides a fast, 10-bit, latched decimating digital input that drives 12 high voltage outputs. 10-bit input words are loaded into 12 separate high speed, bipolar DACs sequentially. Flexible digital input format allows several AD8385s to be used in parallel in high resolution displays. The output signal can be adjusted for dc reference, signal inversion, and contrast for maximum flexibility. Integrated level shifters convert timing signals from a 3 V timing controller to high voltage for LCD panel timing inputs. Two, serial, 8-bit DACs are integrated to provide dc reference signals. A 3-wire serial interface controls overload protection, output mode, and the serial DACs.

The AD8385 is fabricated on ADI's fast bipolar, 26 V XFHV process, which provides fast input logic, bipolar DACs with trimmed accuracy and fast settling, high voltage, precision drive amplifiers on the same chip.

The AD8385 dissipates 1.84 W nominal static power.

The AD8385 is offered in a 100-lead, 14 mm × 14 mm TQFP E-pad package and operates over the commercial temperature range of 0°C to 85°C.

FUNCTIONAL BLOCK DIAGRAM

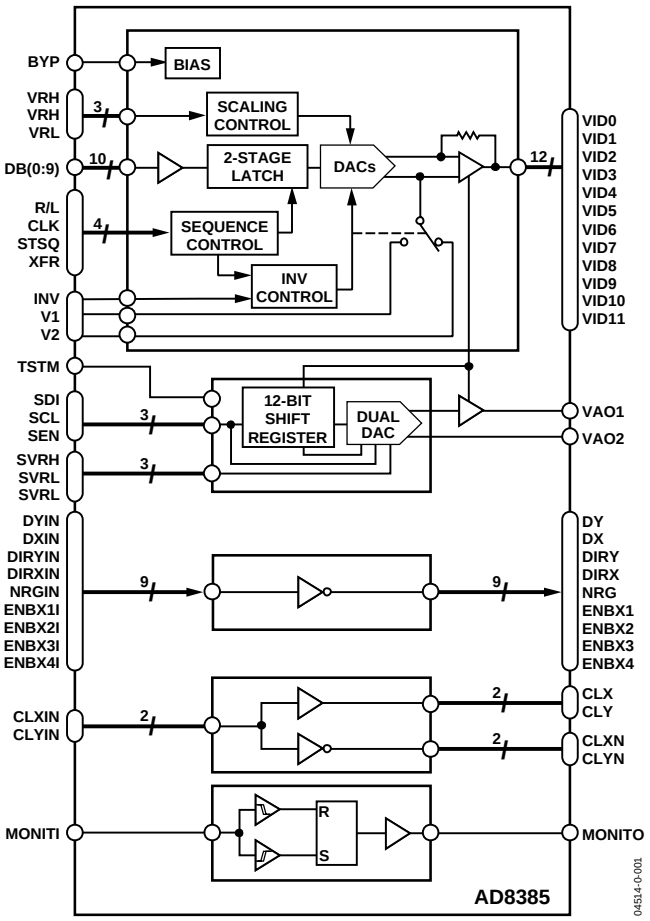

Figure 1.

Rev. 0

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REVISION HISTORY

1/05—Revision 0: Initial Version

SPECIFICATIONS

DECDRIVER SECTION

@ 25°C, AVCC = 15.5 V, DVCC = 3.3 V, $T_{A\ MIN}$ = 0°C, $T_{A\ MAX}$ = 85°C, VRH = 9.5 V, VRL = V1 = V2 = 7 V, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
VIDEO DC PERFORMANCE[1]	T_{MIN} to T_{MAX}				
VDE	DAC Code 450 to 800	–7.5		+7.5	mV
VCME	DAC Code 450 to 800	–3.5		+3.5	mV
VIDEO OUTPUT DYNAMIC PERFORMANCE	T_{MIN} to T_{MAX} , V_O = 5 V step, C_L = 150 pF				
Data Switching Slew Rate	20% to 80%		460		V/µs
Invert Switching Slew Rate	20% to 80%		560		V/µs
Data Switching Settling Time to 1%			19	24	ns
Data Switching Settling Time to 0.25%			30	50	ns
Invert Switching Settling Time to 1%			75	120	ns
Invert Switching Settling Time to 0.25%			250	500	ns
Invert Switching Overshoot			100	200	mV
CLK and Data Feedthrough[2]			10		mV p-p
All-Hostile Crosstalk[3]					
Amplitude			10		mV p-p
Glitch Duration			30		ns
DAC Transition Glitch Energy	DAC Code 511 to 512		0.3		nV-s
VIDEO OUTPUT CHARACTERISTICS					
Output Voltage Swing	AVCC – VOH, VOL – AGND		1.1	1.3	V
Output Voltage—Grounded Mode			0.25		V
Data Switching Delay: t_9[4]	50 % of VIDx	10	12	14	ns
INV Switching Delay: t_{10}[5]	50 % of VIDx	13	15	17	ns
INV to CLK Setup Time: t_{27}		0.5 f_{CLK}		5.5 f_{CLK}	ns
Output Current			100		mA
Output Resistance			22		Ω
REFERENCE INPUTS					
V1 Range	V2 ≥ (V1 – 0.25 V)	5		AVCC – 4	V
V2 Range	V2 ≥ (V1 – 0.25 V)	5		AVCC – 4	V
V1 Input Current			–5		µA
V2 Input Current			–27		µA
VRL Range	VRH ≥ VRL	V1 – 0.5		AVCC – 1.3	V
VRH Range	VRH ≥ VRL	VRL		AVCC	V
VRH to VRL Range	VFS =2 × (VRH – VRL)	0		2.75	V
VRH Input Resistance	To VRL		20		kΩ
VRL Bias Current			–0.2		µA
VRH Input Current			125		µA
RESOLUTION					
Coding	Binary	10			Bits

Parameter	Conditions	Min	Typ	Max	Unit
DIGITAL INPUT CHARACTERISTICS	Input t_r, t_f = 2 ns				
Max. Input Data Update Rate		100			Ms/s
Data Setup Time: t_1		0			ns
STSQ Setup Time: t_3		0			ns
XFR Setup Time: t_5		0			ns
Data Hold Time: t_2		3			ns
STSQ Hold Time: t_4		3			ns
XFR Hold Time: t_6		3			ns
CLK High Time: t_7		3			ns
CLK Low Time: t_8		2.5			ns
C_{IN}				3	pF
I_{IH}			0.05		µA
I_{IL}			–0.6		µA
V_{IH}		2			V
V_{IL}				0.8	V
V_{TH}			1.65		V

[1] VDE = differential error voltage; VCME = common-mode error voltage; VFS = full-scale output voltage = 2 × (VRH – VRL). See the Accuracy section.
[2] Measured on two outputs differentially as CLK and DB(0:9) are driven and XFR is held low.
[3] Measured on two outputs differentially as the other four are transitioning by 5 V. Measured for both states of INV.
[4] Measured from 50% of rising CLK edge to 50% of output change. Measurement is made for both states of INV.
[5] Measured from 50% of rising CLK edge that follows a valid XFR to 50% of output change. Refer to Figure 6 for the definition.

LEVEL SHIFTERS

@ 25°C, AVCC = 15.5 V, DVCC = 3.3 V, $T_{A\ MIN}$ = 0°C, $T_{A\ MAX}$ = 85°C, VRH = 9.5 V, VRL = V1 = V2 = 7 V, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
LEVEL SHIFTER LOGIC INPUTS					
C_{IN}				3	pF
I_{IH}			0.05	2	µA
I_{IL}		–2	–0.6		µA
V_{TH}			1.65		V
V_{IH}		2.0		DVCC	V
V_{IL}		DGND		0.8	V
LEVEL SHIFTER OUTPUTS	R_L > 10 kΩ				
V_{OH}			AVCC – 0.25		V
V_{OL}			0.25		V
LEVEL SHIFTER DYNAMIC PERFORMANCE	$T_{A\ MIN}$ to $T_{A\ MAX}$				
Output Rise, Fall Times—t_r, t_f					
DX, CLX, CLXN, ENBX[1–4]	C_L = 40 pF		18.5	30	ns
DY, CLY, CLYN	C_L = 40 pF		40	70	ns
DIRX, DIRY	C_L = 40 pF		102	200	ns
NRG	C_L = 200 pF		43	50	ns
NRG	C_L = 300 pF		61	100	ns
Propagation Delay Times—t_{11}, t_{12}, t_{13}, t_{14}					
DX, CLX, CLXN, ENBX[1–4]	C_L = 40 pF		20	50	ns
DY, CLY, CLYN	C_L = 40 pF		29	50	ns
DIRX, DIRY	C_L = 40 pF		70	100	ns
NRG	C_L = 200 pF		30	100	ns
NRG	C_L = 300 pF		37		ns
Output Skew					
ENBX[1-4]—t_{15}, t_{16}	C_L = 40 pF			2	ns
DX to ENBX[1–4]—t_{16}	C_L = 40 pF			2	ns
DX to CLX—t_{15}, t_{16}, t_{17}, t_{18}	C_L = 40 pF			10	ns
DY, CLY, CLYN—t_{15}, t_{16}, t_{17}, t_{18}	C_L = 40 pF			20	ns

LEVEL SHIFTING EDGE DETECTOR

@ 25°C, AVCC = 15.5 V, DVCC = 3.3 V, $T_{A\ MIN}$ = 0°C, $T_{A\ MAX}$ = 85°C, VRH = 9.5 V, VRL = V1 = V2 = 7 V, unless otherwise noted.

Table 3.

Parameter		Conditions	Min	Typ	Max	Unit
V_{IL}	Input Low Voltage		AGND		AGND + 0.75	V
V_{IH}	Input High Voltage		AVCC – 0.7		AVCC	V
$V_{TH\ LH}$	Input Rising Edge Threshold Voltage			AGND + 1		V
$V_{TH\ HL}$	Input Falling Edge Threshold Voltage			AVCC – 1		V
V_{OH}	Output High Voltage			DVCC – 0.25		V
V_{OL}	Output Low Voltage			0.25		V
I_{IH}	Input Current High State			1.2	2.5	µA
I_{IL}	Input Current Low State		–2.5	–1.2		µA
t_{19}	Input Rising Edge Propagation Delay Time	C_L = 10 pF		16		ns
Δt_{19}	t_{19} Variation with Temperature			2		ns
t_{20}	Input Falling Edge Propagation Delay Time	C_L = 10 pF		12		ns
Δt_{20}	t_{20} Variation with Temperature			2		ns
t_r	Output Rise Time	10% to 90%		5		ns
t_f	Output Fall Time	10% to 90%		6		ns

SERIAL INTERFACE

@ 25 C, AVCC = 15.5 V, DVCC = 3.3 V, $T_{A\ MIN}$ = 0°C, $T_{A\ MAX}$ = 85°C, SVFS = 5 V, SVRL = 4 V, SVRH = 9 V, unless otherwise noted.

Table 4.

Parameter	Conditions	Min	Typ	Max	Unit
SERIAL DAC REFERENCE INPUTS	SVFS = (SVRH – SVRL)				
SVRH Range	SVRL ≤ SVRH	SVRL + 1		AVCC – 3.5	V
SVRL Range	SVRL ≤ SVRH	AGND + 1.5		SVRH – 1	V
SVFS Range		1		8	V
SVRH Input Current	SVFS = 5 V		125	150	µA
SVRL Input Current	SVFS = 5 V	–2.8	–2.5		mA
SVRH Input Resistance			40		kΩ
SERIAL DAC ACCURACY					
DNL	SVFS = 5 V, R_L = ∞	–1.0		+1.0	LSB
INL	SVFS = 5 V, R_L = ∞	–1.5		+1.5	LSB
Output Offset Error		–2.0		+2.0	LSB
Scale Factor Error		–3		+3	LSB
SERIAL DAC LOGIC INPUTS	Input t_r, t_f = 10 ns				
C_{IN}				3	pF
$I_{IN\ LOW}$ Low Level Input Current			–0.6		µA
$I_{IN\ HIGH}$ High Level Input Current			0.05		µA
V_{TH} Input Threshold Voltage			1.65		V
V_{IH} Input High Voltage		2.0		DVCC	V
V_{IL} Input Low Voltage		DGND		0.8	V
SERIAL DAC OUTPUTS					
Maximum Output Voltage			SVRH – 1 LSB		V
Minimum Output Voltage			SVRL		V
VAO1—Grounded Mode			0.1		V
I_{OUT}			±30		mA
C_{LOAD} Low Range[1]				0.002	µF
C_{LOAD} High Range[1]		0.047			µF

Parameter	Conditions	Min	Typ	Max	Unit
SERIAL INTERFACE DYNAMIC PERFORMANCE					
SEN to SCL Setup Time, t_{20}		10			ns
SCL, High Level Pulse Width, t_{21}		10			ns
SCL, Low Level Pulse Width, t_{22}		10			ns
SDI Setup Time, t_{24}		10			ns
SDI Hold Time, t_{25}		10			ns
SCL to SEN Hold Time, t_{23}		10			ns
VAO1, VAO2 Settling Time, t_{26}	SVFS = 5 V, to 0.5%, C_L = 100 pF		1	2	ms
VAO1, VAO2 Settling Time, t_{26}	SVFS = 5 V, to 0.5%, C_L = 33 µF			15	ms

[1] Outputs VAO1 and VAO2 are designed to drive very high capacitive loads. For proper operation of these outputs, load capacitance must be ≤0.002 µF or ≥0.047 µF. Load capacitance in the range of 0.002 µF to 0.047 µF causes the output overshoot to exceed 100 mV.

POWER SUPPLIES

@ 25°C, AVCC = 15.5 V, DVCC = 3.3 V, $T_{A\ MIN}$ = 0°C, $T_{A\ MAX}$ = 85°C, SVFS = 5 V, SVRL = 4 V, SVRH = 9 V, unless otherwise noted.

Table 5.

AD8385 Power Supplies	Min	Typ	Max	Unit
DVCC, Operating Range	3	3.3	3.6	V
DVCC, Quiescent Current		56		mA
AVCC Operating Range	9		18	V
Total AVCC Quiescent Current		111		mA

OPERATING TEMPERATURE

@ 25°C, AVCC = 15.5 V, DVCC = 3.3 V, $T_{A\ MIN}$ = 0°C, $T_{A\ MAX}$ = 85°C, SVFS = 5 V, SVRL = 4 V, SVRH = 9 V, unless otherwise noted.

Table 6.

Parameter	Min	Typ	Max	Unit
Ambient Temperature Range, T_A[1]	0		75	°C
Ambient Temperature Range, T_A[2]	0		85	°C

[1] Operation at high ambient temperature requires a thermally-optimized PCB layout (see the Applications section), input data update rate not exceeding 85 MHz, black-to-white transition ≤ 4 V and C_L ≤ 150 pF. In systems with limited or no airflow, the maximum ambient operating temperature is limited to 75°C with the overload protection enabled. For operation above 75°C, see Endnote 2.

[2] In addition to the requirements stated in Endnote 1, operation at 85°C ambient temperature requires 200 lfm airflow or the overload protection disabled.

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
Supply Voltage	
AVCCx – AGNDx	18 V
DVCC – DGND	4.5 V
Input Voltage	
Maximum Digital Input Voltage	DVCC + 0.5 V
Minimum Digital Input Voltage	DGND – 0.5 V
Maximum Analog Input Voltage	AVCC + 0.5 V
Minimum Analog Input Voltage	AGND – 0.5 V
Internal Power Dissipation[1]	
TQFP E-Pad Package @ T_A = 25°C	5.00 W
Operating Temperature Range	0°C to 85°C
Storage Temperature Range	–65°C to 125°C
Lead Temperature Range (Soldering, 10 sec)	300°C

Stresses above those listed under the Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings for extended periods may reduce device reliability.

[1] 100-lead TQFP E-pad package: θ_{JA} = 20°C/W (still air), JEDEC STD, 4-layer PCB in still air.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

OVERLOAD PROTECTION

The AD8385 employs a 2-stage overload protection circuit with an enable/disable function that is programmable through the 3-wire serial interface. It consists of an output current limiter and a thermal shut down.

When enabled, the maximum current at any one output of the AD8385 is, on average, internally limited to 100 mA. In the event of a momentary short circuit between a video output and a power supply rail (VCC or AGND), the output current limit is sufficiently low to provide temporary protection.

The thermal shutdown debiases the output amplifier when the junction temperature reaches the internally set trip point. In the event of an extended short circuit between a video output and a power supply rail, the output amplifier current continues to switch between 0 mA and 100 mA typ, with a period determined by the thermal time constant and the hysteresis of the thermal trip point. Thermal shutdown provides long-term protection by limiting the average junction temperature to a safe level. When disabled, no overload protection is present.

EXPOSED PADDLE

To ensure optimal thermal performance, the exposed paddle must be electrically connected to an external plane such as AVCC or GND, as described in the Applications Circuit section.

MAXIMUM POWER DISSIPATION

The junction temperature limits the maximum power that can be safely dissipated by the AD8385. The maximum safe junction temperature for plastic encapsulated devices, determined by the glass transition temperature of the plastic, is approximately 150°C. Exceeding this limit can cause a temporary shift in the parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure.

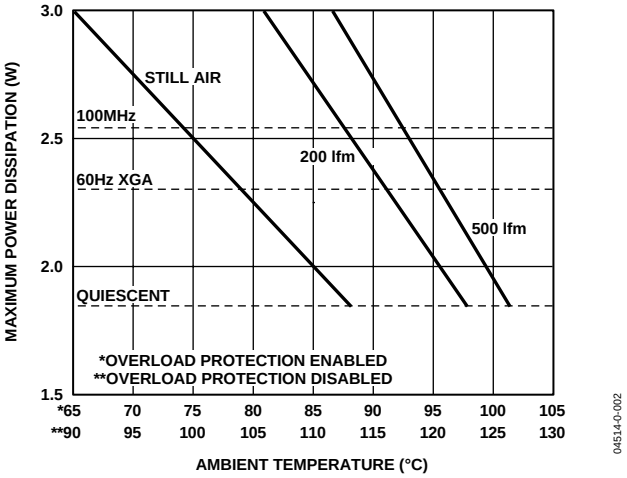
OPERATING TEMPERATURE RANGE

The maximum operating junction temperature is 150°C. The junction temperature trip point of the overload protection is 165°C. Production test guarantees a minimum junction temperature trip point of 125°C.

Consequently, the maximum guaranteed operating junction temperature is 125°C with the overload protection enabled, and 150°C with the overload protection disabled.

To ensure operation within the specified operating temperature range, the maximum power dissipation must be limited:

$$P_{DMAX} \approx \frac{\left(T_{JMAX} - T_A\right)}{\left(\theta_{JA} - 0.9 \times \sqrt[3]{Airflow\,in\,lfm}\right)}$$



AD8385 on a 4-layer JEDEC PCB with a thermally optimized landing pattern, as described in the Applications Circuit section.

Figure 2. Maximum Power Dissipation vs. Temperature

Note that the quiescent power dissipation of the AD8385 is 1.84 W when operating under the conditions specified in this data sheet. When driving a 12-channel XGA panel with an input capacitance of 150 pF, the AD8385 dissipates a total of 2.3 W when displaying 1 pixel wide alternating white and black vertical lines generated by a standard 60 Hz XGA input video. When the frequency of the pixel clock is raised to 100 MHz, the total power dissipation increases to 2.54 W. These specific power dissipations are shown in Figure 2 for reference.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

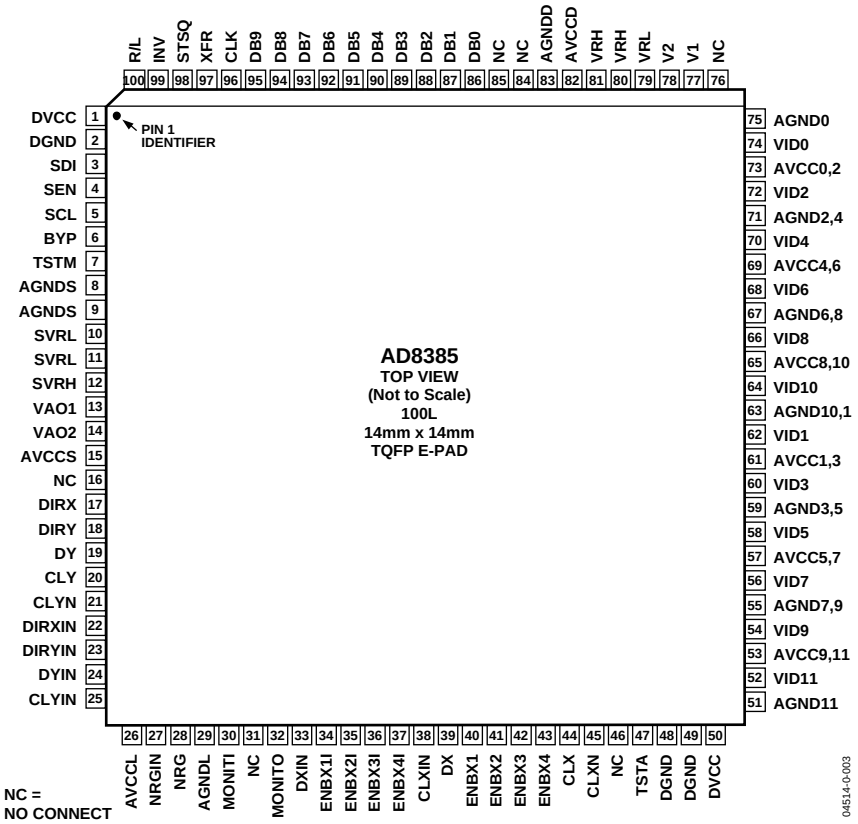


Figure 3. 100-Lead TQFP Package

Table 8. Pin Function Descriptions

Pin Name	Function	Description
DB(0:9)	Data Input	10-Bit Data Input. MSB = DB9.
CLK	Clock	Clock Input. Data is acquired on both edges of the CLK.
STSQ	Start Sequence	A new data loading sequence begins on the rising edge of CLK when this input was high on the preceding rising edge of CLK.
R/L	Right/Left Select	A new data loading sequence begins on the left, with Channel 0, when this input is low; a new data loading sequence begins on the right, with Channel 11 when this input is high.
XFR	Data Transfer	Data is transferred to the video outputs on the next rising edge of CLK when this input is high on the rising edge of CLK.
VID0–VID11	Analog Outputs	These pins are directly connected to the analog inputs of the LCD panel.
V1, V2	Reference Voltages	The voltage applied between V1 and AGND sets the white video level during INV = low. The voltage applied between V2 and AGND sets the white video level during INV = high.
VRH, VRL	Full-Scale References	The voltage applied between these pins sets the full-scale video output voltage.
INV	Invert	When this input is high, the analog output voltages are above V2. When low, the analog outputs voltages are below V1.
DVCC	Digital Power Supply	Digital Power Supply.
DGND	Digital Ground	This pin is normally connected to the digital ground plane.
AVCCx	Analog Power Supplies	Analog Power Supplies.
AGNDx	Analog Ground	Analog Supply Returns.
BYP	Bypass	A 0.1 µF capacitor connected between this pin and AGND ensures optimum settling time.
SVRH, SVRL	Serial DAC Reference Voltages	Reference Voltages for the Output Amplifiers of the Serial DACs.

Pin Name	Function	Description
SCL	Serial Interface Data Clock	Clock for the Serial Interface.
SDI	Serial Interface Data Input	While the SEN input is low, one 12-bit serial word is loaded into the serial interface on the rising edges of SCL. The first four bits select the function; the following eight bits are the data used in the serial DACs.
SEN	Serial Interface Enable	A falling edge of this input initiates a loading cycle. While this input is held low, the serial interface is enabled and data is loaded on every rising edge of SCL. The selected functions are updated on the rising edge of this input. While this input is held high, the serial interface is disabled.
VAO1, VAO2	Serial DAC Voltage Output	These output voltages are updated on the rising edge of the SEN input.
TSTM	Test Mode	When this input is low, the overload protection and output mode are determined by the function programmed into the serial interface. While this input is held high, the overload protection is forced to enabled and the output mode is forced to normal, regardless of function programmed into the serial interface.
TSTA	Test Pin	Connect this pin to DGND.
MONITI	Monitor Input	Logic Input of the Level Shifting Inverting Edge Detector.
MONITO	Monitor Output	Output of the Level Shifting Inverting Edge Detector.
DYIN, DIRYIN, DIRXIN, DXIN, NRGIN, ENBX(1–4)IN	Inverting Level Shifter Inputs	Logic Input of the Inverting Level Shifters.
DX, DY, DIRX, DIRY, NRG, ENBX(1–4)	Inverting Level Shifter Outputs	While the corresponding input voltage of these level shifters is below the threshold voltage, the output voltage at these pins is at VOH. While the corresponding input voltage of these level shifters is above the threshold voltage, the output voltage at these pins is at VOL.
CLXIN, CLYIN	Complementary Level Shifter Inputs	Logic Input of the Complementary Level Shifters.
CLX, CLXN, CLY, CLYN,	Complementary Level Shifter Outputs	While the corresponding input voltage of these level shifters is below the threshold voltage, the voltage at the noninverting output pins is at VOH and the voltage at the inverting outputs is at VOL. While the corresponding input voltage of these level shifters is above the threshold voltage, the voltage at the noninverting output pins is at VOL and the voltage at the inverting outputs is at VOH.

BLOCK DIAGRAMS AND TIMING DIAGRAMS

DECDRIVER SECTION

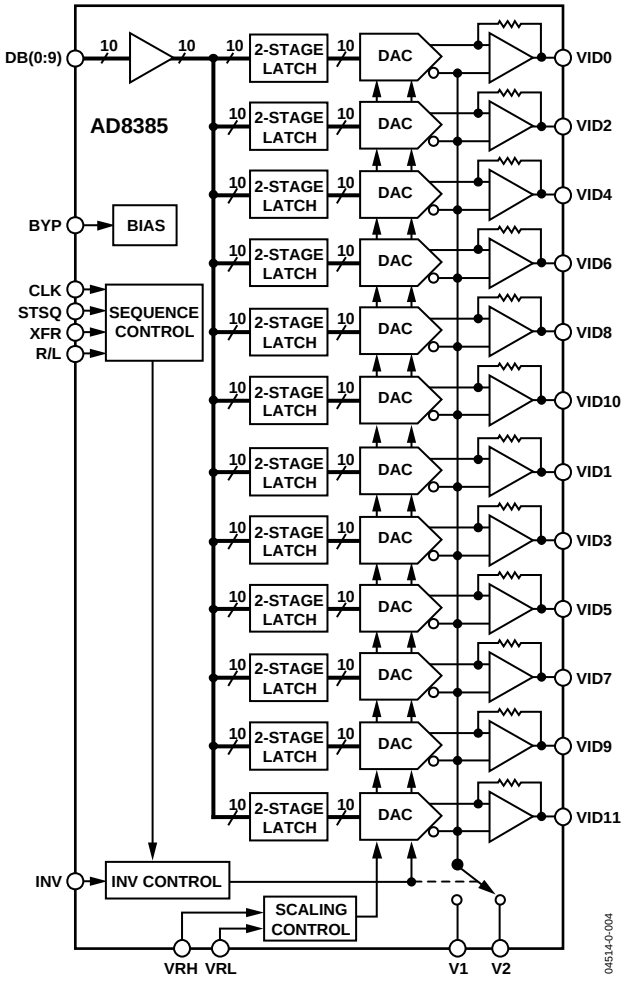


Figure 4. Block Diagram

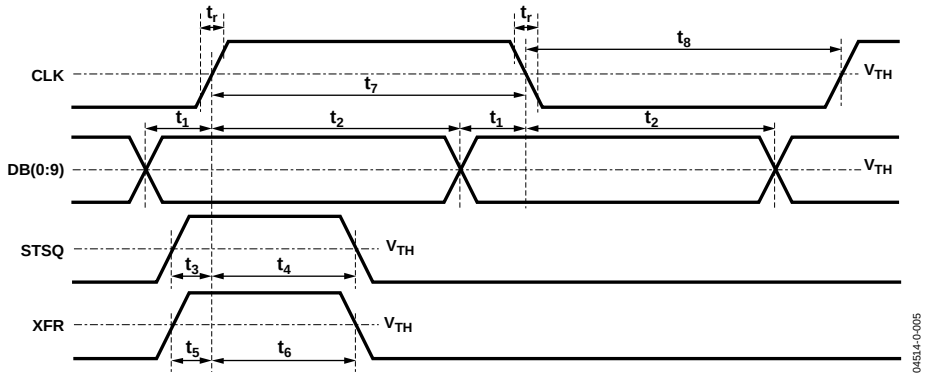


Figure 5. Input Timing

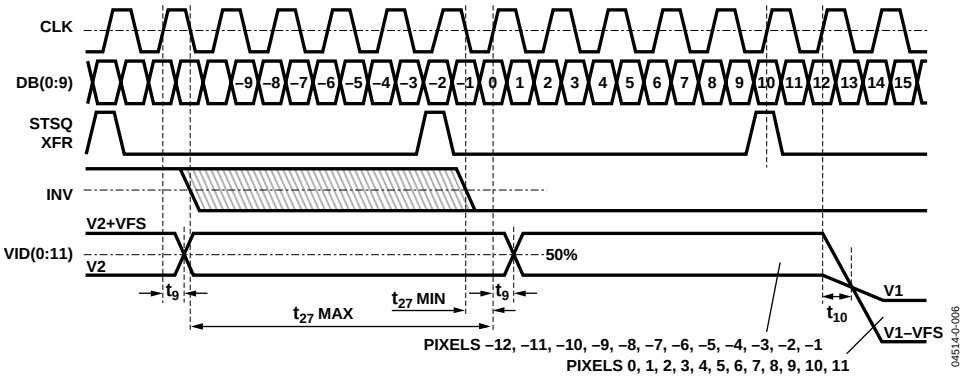


Figure 6. Output Timing (R/L = Low)

Table 9.

Parameter		Conditions	Min	Typ	Max	Unit
t_1	Data Setup Time	Input t_r, t_f = 2 ns	0			ns
t_2	Data Hold Time		3			ns
t_3	STSQ Setup Time		0			ns
t_4	STSQ Hold Time		3			ns
t_5	XFR Setup Time		0			ns
t_6	XFR Hold Time		3			ns
t_7	CLK High Time		3			ns
t_8	CLK Low Time		2.5			ns
t_9	Data Switching Delay		10	12	14	ns
t_{10}	Invert Switching Delay		13	15	17	ns
t_{27}	INV to CLK Setup Time		0.5/f_{CLK}		5.5/f_{CLK}	ns

LEVEL SHIFTERS

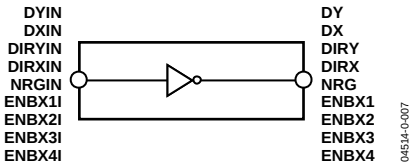


Figure 7. Level Shifter—Inverting

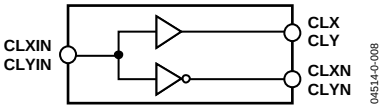


Figure 8. Level Shifter—Complementary

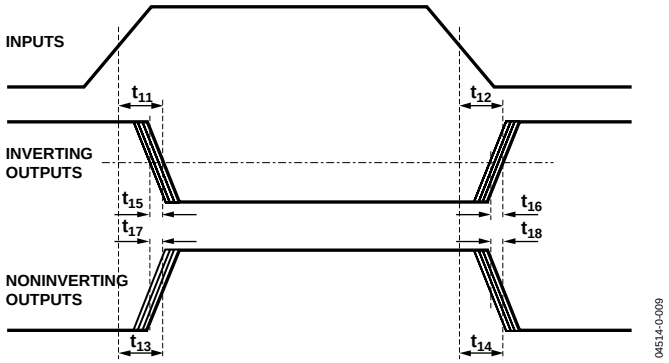


Figure 9. Inverting and Complementary Level Shifter Timing

Table 10. Level Shifter Timing

Parameter	Conditions	Min	Typ	Max	Unit
Output Rise, Fall Times, t_r, t_f	$T_{A\ MIN}$ to $T_{A\ MAX}$				
DX, CLX, CLXN, ENBX[1–4]	C_L = 40 pF		18.5	30	ns
DY, CLY, CLYN			40	70	ns
DIRX, DIRY			102	200	ns
NRG	C_L = 200 pF		43	50	ns
	C_L = 300 pF		61	100	ns
Propagation Delay Times—t_{11}, t_{12}, t_{13}, t_{14}	$T_{A\ MIN}$ to $T_{A\ MAX}$				
DX, CLX, CLXN, ENBX[1–4]	C_L = 40 pF		20	50	ns
DY, CLY, CLYN			29	50	ns
DIRX, DIRY			70	100	ns
NRG	C_L = 200 pF		30	100	ns
	C_L = 300 pF		37		ns
Propagation Delay Skew—t_{15}, t_{16}, t_{17}, t_{18}	$T_{A\ MIN}$ to $T_{A\ MAX}$, C_L = 40 pF				
ENBX[1–4]—t_{15}, t_{16}				2	ns
DX to ENBX[1–4]—t_{16}				2	
DX to CLX—t_{15}, t_{16}, t_{17}, t_{18}				10	ns
DY, CLY, CLYN—t_{15}, t_{16}, t_{17}, t_{18}				20	ns

LEVEL SHIFTING EDGE DETECTOR

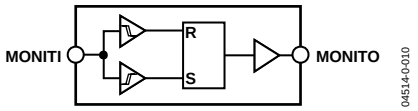


Figure 10. Level Shifting Edge Detector Block Diagram

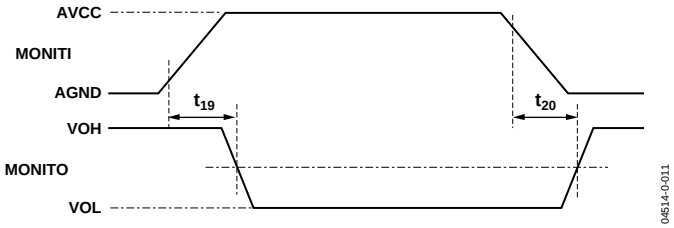


Figure 11. Level Shifting Edge Detector Timing

Table 11. Level Shifting Edge Detector, AVCC = 15.5 V, DVCC = 3.3 V, C_L = 10 pF, $T_{A\ MIN}$ = 25°C, $T_{A\ MAX}$ = 85°C

Parameter		Min	Typ	Max	Unit
V_{IL}	Input Low Voltage	AGND		AGND + 0.75	V
V_{IH}	Input High Voltage	AVCC – 0.7		AVCC	V
V_{TH} LH	Input Rising Edge Threshold Voltage		AGND + 1		V
V_{TH} HL	Input Falling Edge Threshold Voltage		AVCC – 1		V
V_{OH}	Output High Voltage		DVCC – 0.25		V
V_{OL}	Output Low Voltage		0.25		V
I_{IH}	Input Current High State		1.2	2.5	µA
I_{IL}	Input Current Low State	–2.5	–1.2		µA
t_{19}	Input Rising Edge Propagation Delay Time		16		ns
Δt_{19}	t_{19} Variation with Temperature		2		ns
t_{20}	Input Falling Edge Propagation Delay Time		12		ns
Δt_{20}	t_{20} Variation with Temperature		2		ns
t_r	Output Rise Time		5		ns
t_f	Output Fall Time		6		ns

SERIAL INTERFACE

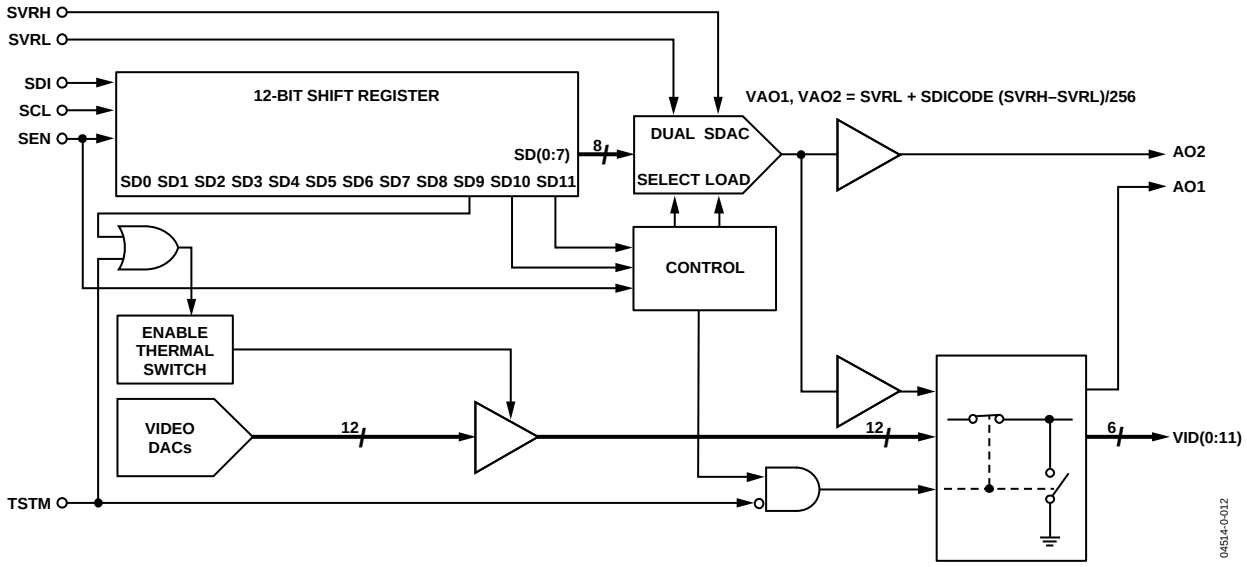


Figure 12. Serial Interface Block Diagram

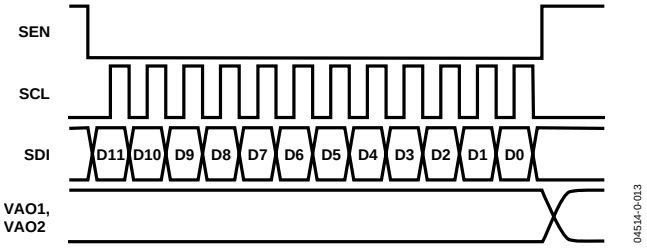


Figure 13. Serial Interface Timing

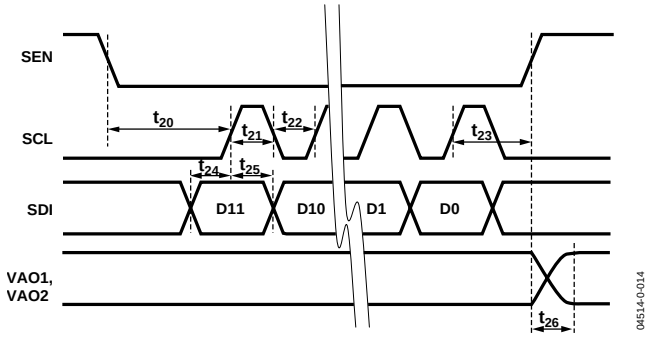


Figure 14. Serial Interface Timing

Table 12. Serial DAC Timing

Parameter	Conditions	Min	Typ	Max	Unit
SEN to SCL Setup Time, t_{20}		10			ns
SCL, High Level Pulse Width, t_{21}		10			ns
SCL, Low Level Pulse Width, t_{22}		10			ns
SDI Setup Time, t_{24}		10			ns
SDI Hold Time, t_{25}		10			ns
SCL to SEN Hold Time, t_{23}		10			ns
VAO1, VAO2 Settling Time, t_{26}	VFS = 5 V, to 0.5%, C_L = 100 pF		1	2	ms
	VFS = 5 V, to 0.5%, C_L = 33 µF			15	ms

FUNCTIONAL DESCRIPTION

The AD8385 is a system building block designed to directly drive the columns of LCD microdisplays of the type popularized for use in projection systems. It comprises 12 channels of precision, 10-bit digital-to-analog converters loaded from a single, high speed, 10-bit wide input. Precision current feedback amplifiers, providing well-damped pulse response and fast voltage settling into large capacitive loads, buffer the 12 outputs. Laser trimming at the wafer level ensures low absolute output errors and tight channel-to-channel matching. Tight part-to-part matching in high resolution systems is guaranteed by the use of external voltage references.

Three groups of level shifters convert digital inputs to high voltage outputs for direct connection to the control inputs of LCD panels.

An edge detector conditions a high voltage reference timing input from the LCD and converts it to digital levels for use in synchronizing timing controllers, such as the AD8389.

REFERENCE AND CONTROL INPUT

Start Sequence Control—Input Data Loading

A valid STSQ control input initiates a new 6-clock loading cycle during which 12 input data-words are loaded sequentially into 12 internal channels. Data is loaded on both the rising and falling edges of CLK. A new loading sequence begins on the current rising CLK edge only when STSQ is held high at the preceding rising CLK edge.

Right/Left Control—Input Data Loading

To facilitate image mirroring, the direction of the loading sequence is set by the R/L control.

A new loading sequence begins at Channel 0 and proceeds to Channel 11 when the R/L control is held low. It begins at Channel 11 and proceeds to Channel 0 when the R/L control is held high.

XFR Control—Data Transfer to Outputs

Data transfer to the outputs is initiated by the XFR control. Data is transferred to all outputs simultaneously on the rising CLK edge only when XFR is high during the preceding rising CLK edge.

V1, V2 Inputs—Voltage Reference Inputs

Two external analog voltage references set the levels of the outputs. V1 sets the output voltage at Code 1023 while the INV input is low, and V2 sets the output voltage at Code 1023 while the INV input is held high.

VRH, VRL Inputs—Full-Scale Video Reference Inputs

Twice the difference between these analog input voltages sets the full-scale output voltage VFS = 2 (VRH–VRL).

INV Control—Analog Output Inversion

The analog voltage equivalent of the input code is subtracted from (V2 + VFS) while INV is held high and added to (V1 – VFS) while INV is held low. Video inversion is delayed by 6 to 12 CLK cycles from the INV input.

TSTM Control—Test Mode

A low on this input allows serial interface control of the output operating mode and the thermal switch.

A high on this input turns the thermal switch on and releases the video outputs and VAO1 from grounded mode.

3-Wire Serial Interface—SDAC, Output, Thermal Switch Control

The serial interface controls two 8-bit serial DACs, the thermal switch of the overload protection circuit, and the video output operating mode via a 12-bit-wide serial word from a microprocessor. Four of the 12 bits select the function; the remaining 8 bits are the data for the serial DACs.

Table 13. Bit Definitions

Bit Name	Bit Functionality
SD(0:7)	8-bit SDAC data. MSB = SD7
SD8	Not used
SD9	Thermal switch control
SD10	Output operating mode, SDAC selection, and thermal switch control
SD11	Output operating mode and SDAC selection control

Table 14. Truth Table @ TSTM = Low

	SD				
SEN	11	10	9	8	Action
⌐↓	0	0	X	X	Load VAO2. No change to VAO1.
⌐↓	1	0	X	X	Load VAO1. Release video outputs from grounded mode. No change to VAO2.
⌐↓	0	1	0	X	Release video outputs and VAO1 from grounded mode. Disable thermal switch. No change to VAO1 and VAO2.
⌐↓	0	1	1	X	Release video outputs and VAO1 from grounded mode. Enable thermal switch. No change to VAO1 and VAO2.
⌐↓	1	1	0	X	Video outputs and VAO1 to grounded output mode. Disable thermal switch. No change to VAO1, VAO2.
⌐↓	1	1	1	X	Video outputs and VAO1 to grounded output mode. Enable thermal switch. No change to VAO1, VAO2.
↓	X	X	X	X	Start a serial interface loading cycle. No change to outputs.

Table 15. Truth Table @ TSTM = High. Thermal Switch Enabled. Grounded Output Disabled.

SEN	SD				Action
	11	10	9	8	
↓	0	0	X	X	Load VAO2. No change to VAO1.
↓	1	0	X	X	Load VAO1. No change to VAO2.
↓	X	1	X	X	No change to VAO1 and VAO2 data.
↑	X	X	X	X	Start a serial interface loading cycle. No change to outputs.

X = Don't Care.

OUTPUT OPERATING MODE

In normal operating mode, the voltage of the video outputs and VAO1 is determined by the inputs.

In grounded output mode, the video outputs and VAO1 are forced to (AGND + 0.1 V) typ.

OVERLOAD PROTECTION

The overload protection employs current limiters and a thermal switch to protect the video output pins against accidental shorts between any video output pin and AVCC or AGND.

The junction temperature trip point of the thermal switch is 165°C. Production test guarantees a minimum junction temperature trip point of 125°C. Consequently, the operating junction temperature should not be allowed to rise above 125°C with the thermal switch enabled.

For systems that operate at high internal ambient temperatures and require large capacitive loads to be driven by the AD8385 at high frequencies, junction temperatures above 125°C may be required. In such systems, the thermal switch should either be disabled or a minimum airflow of 200 lfm be maintained.

SERIAL DACS

Both serial DACs are loaded via the serial interface. The output voltage is determined by the following equation:

$$VAO1, VAO2 = SVRL + SD(0:7) \times (SVRH - SVRL)/256$$

Output *VAO1* is designed to drive very large capacitive loads, above 0.047 µF. Lower capacitive loads may result in excessive overshoot at *VAO1*.

Level Shifters

The characteristics of the level shifters are optimized based on their intended use.

Seven level shifters—DX, CLX, CLXN, and ENBX[1:4]—are optimized for the X direction and three—DY, CLY and CLYN—are optimized for the Y direction control signals.

One level shifter—NRG—is designed to drive a large capacitive load and is optimized for an X direction control signal. Two level shifters—DIRX and DIRY—are optimized for very low frequency control signals.

One level shifting edge detector—MONITI, MONITO—is optimized to condition a synchronizing feedback reference signal from the LCD.

THEORY OF OPERATION

TRANSFER FUNCTION AND ANALOG OUTPUT VOLTAGE

The DECDRIVER has two regions of operation where the video output voltages are either above reference voltage V*2* or below reference voltage V*1*. The transfer function defines the video output voltage as the function of the digital input code:

$$VIDx(n) = V2 + VFS \times (1 - n/1023), \text{ for INV = high}$$

$$VIDx(n) = V1 - VFS \times (1 - n/1023), \text{ for INV = low}$$

where:
n = input code
$VFS = 2 \times (VRH - VRL)$

A number of internal limits define the usable range of the video output voltages, VIDx. See Figure 15.

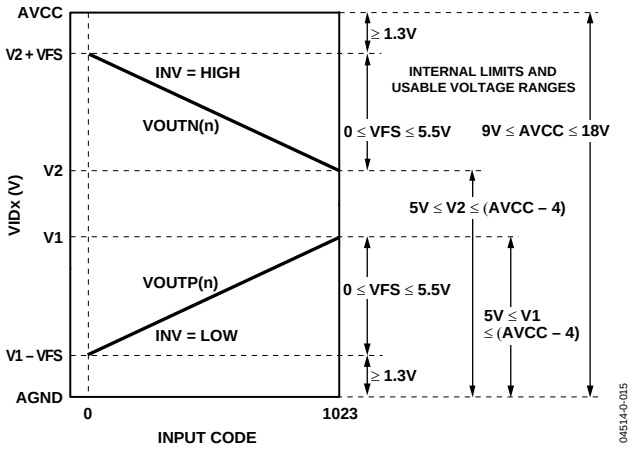


Figure 15. Transfer Function and Usable Voltage Ranges

ACCURACY

To best correlate transfer function errors to image artifacts, the overall accuracy of the DECDRIVER is defined by two parameters, VDE and VCME.

VDE, the differential error voltage, measures the difference between the rms value of the output and the rms value of the ideal. The defining expression is

$$VDE(n) = \frac{[VOUTN(n) - V2] - [VOUTP(n) - V1]}{2} - \left(1 - \frac{n}{1023}\right) \times VFS$$

VCME, the common-mode error voltage, measures ½ the dc bias of the output. The defining expression is

$$VCME(n) = \frac{1}{2}\left[\frac{1}{2}\left(VOUTN(n) + VOUTP(n)\right) - \frac{V1 + V2}{2}\right]$$

APPLICATIONS

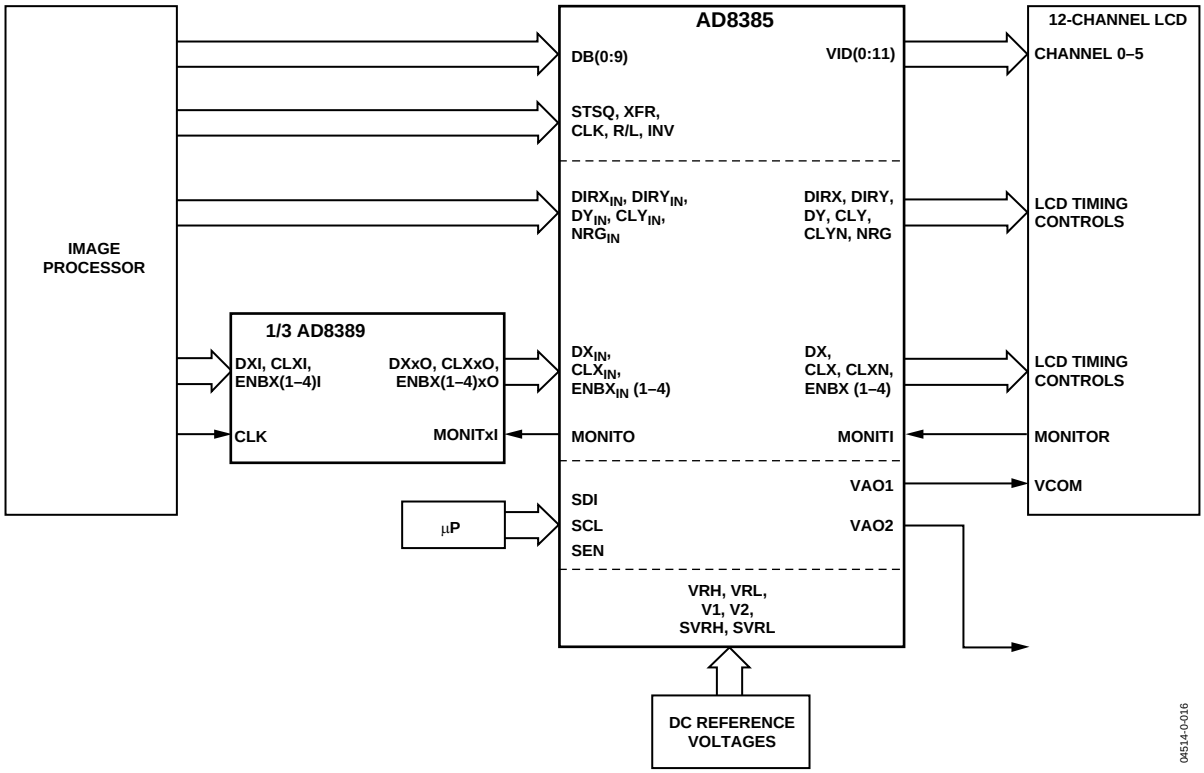


Figure 16. Typical Applications Circuit

OPTIMIZED RELIABILITY WITH THE THERMAL SWITCH

While internal current limiters provide short-term protection against temporary shorts at the outputs, the thermal switch must be enabled to protect against persistent shorts lasting for several seconds.

Initial Power-Up After Assembly or Repair Using a Service Jumper

To optimize reliability with the use of the thermal switch, the following sequence of operations is recommended:

1. Ensure that the TSTM pin is high on initial power-up by inserting a service jumper. See Figure 17.
2. Execute the initial power-up.
3. Identify any shorts at outputs.
4. Power down, repair shorts, and repeat the initial power-up sequence until proper system functionality is verified.
5. Remove service jumper.
6. Resume normal operation.

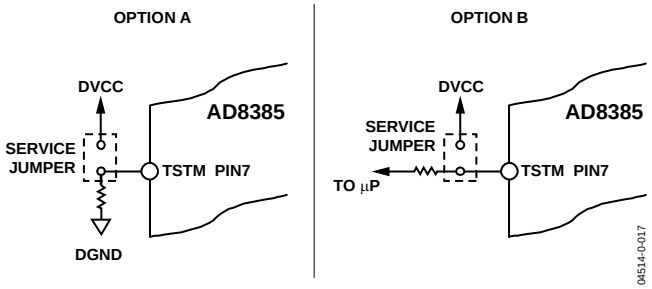


Figure 17. Service Jumper Location

Initial Power-Up after Assembly or Repair Using the Serial Interface

1. Immediately after power-up, send Code 011XXXXXXXXX through the serial interface to enable the thermal switch and disable the grounded output mode.
2. Identify any shorts at the outputs.
3. Power down, repair shorts, and repeat the initial power-up sequence until proper system functionality is verified.
4. Resume normal operation.

Power-Up During Normal Operation

The serial interface has no power-on reset. Code 010XXXXXXXXX, sent immediately following a power-up places, all outputs into normal operating mode and disables the thermal switch.

OPERATION IN HIGH AMBIENT TEMPERATURE

To extend the maximum operating junction temperature of the AD8385 to 150°C, keep the thermal switch disabled during normal operation. Code format X10XXXXXXXXX ensures a disabled thermal switch.

POWER SUPPLY SEQUENCING

As indicated in the Absolute Maximum Ratings, the voltage at any input pin cannot exceed its supply voltage by more than 0.5 V. To ensure compliance with the Absolute Maximum Ratings, the following power-up and power-down sequencing is recommended.

During power-up, initial application of nonzero voltages to any of the input pins must be delayed until the supply voltage ramps up to its highest operational input voltage.

During power-down, the voltage at any input pin must reach zero during a period not exceeding the hold-up time of the power supply.

Failure to comply with the Absolute Maximum Ratings, may result in functional failure or damage to the internal ESD diodes. Damaged ESD diodes can cause temporary parametric failures, which can result in image artifacts. Damaged ESD diodes cannot provide full ESD protection, reducing reliability.

Table 16.

Power-On	Power-Off
1. Apply power to supplies.	1. Remove power from I/Os.
2. Apply power to other I/Os.	2. Remove power from supplies.

VBIAS GENERATION—V1, V2 INPUT PIN FUNCTIONALITY

To avoid image flicker, a symmetrical ac voltage is required and a bias voltage of approximately 1 V minimum must be maintained across the pixels of HTPS LCDs. The AD8385 provides an internal and external method of maintaining this bias voltage.

Internal Bias Voltage Generation

Standard systems that internally generate the bias voltage reserve the uppermost code range for the bias voltage, and use the remaining code range to encode the video for gamma correction. A high degree of ac symmetry is guaranteed by the AD8385 in these systems.

The V1 and V2 inputs in these systems are tied together and are normally connected to VCOM, as shown in Figure 18.

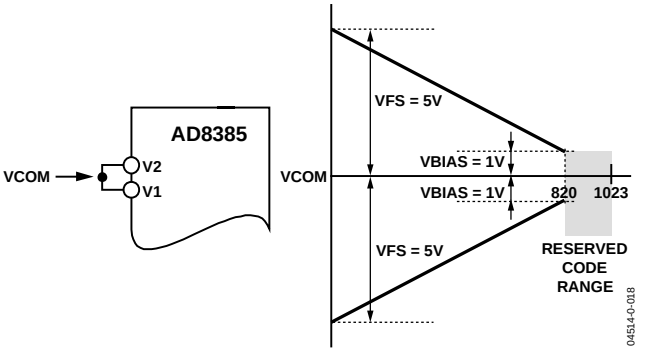


Figure 18. V1, V2 Connection and Transfer Function in a Typical Standard System

External Bias Voltage Generation

In systems that require improved brightness resolution and higher accuracy, the V1 and V2 inputs, connected to external voltage references, provide the necessary bias voltage (VBIAS) while allowing the full code range to be used for gamma correction.

To ensure a symmetrical ac voltage at the AD8385's outputs, VBIAS must remain constant for both states of INV. Therefore, V1 and V2 are defined as

$$V1 = VCOM - VBIAS$$

$$V2 = VCOM + VBIAS$$

APPLICATIONS CIRCUIT

The following circuit ensures VBIAS symmetry to within 1 mV with a minimum component count. Bypass capacitors are not shown for clarity.

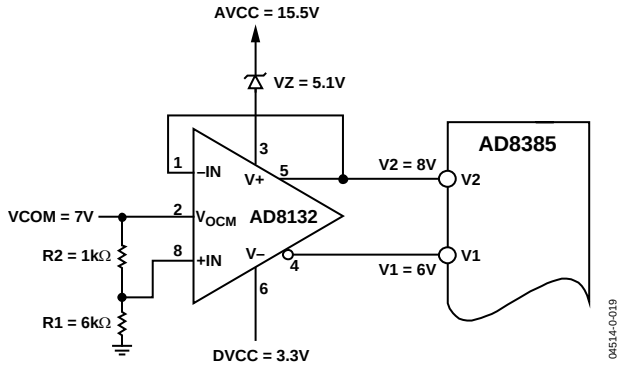


Figure 19. External VBIAS Generator with the AD8132

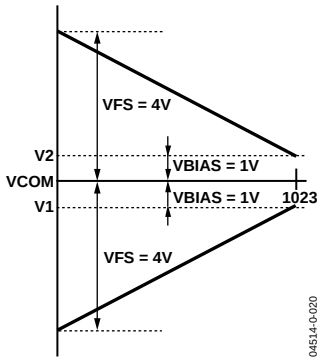


Figure 20. AD8385 Transfer Function in a Typical High Accuracy System

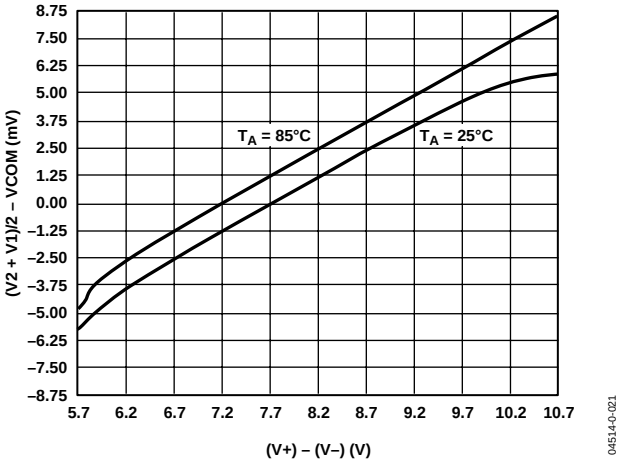


Figure 21. Typical Asymmetry at the Outputs of the AD8132 vs. Its Power Supply for the Application Circuit

Figure 21 shows that the AD8132 (Figure 19) typically produces a symmetrical output at 85°C when its supply, (V+) – (V–), is at 7.2 V.

PCB DESIGN FOR OPTIMIZED THERMAL PERFORMANCE

The total maximum power dissipation of the AD8385 is partly load-dependent. In a 12-channel 60 Hz XGA system running at a 65 MHz pixel rate, the total maximum power dissipation is 2.3 W at an LCD channel input capacitance of 150 pF. At a 100 MHz pixel rate, the total maximum power dissipation can exceed 3 W.

To limit the operating junction temperature at or below the guaranteed maximum, the package, in conjunction with the PCB, must effectively conduct heat away from the junction.

The AD8385 package is designed to provide enhanced thermal characteristics through the exposed die paddle on the bottom surface of the package. To take full advantage of this feature, the exposed paddle must be in direct thermal contact with the PCB, which then serves as a heat sink.

A thermally effective PCB must incorporate two thermal pads and a thermal via structure. The thermal pad on the top PCB layer provides a solderable contact surface on the top surface of the PCB. The thermal pad on the bottom PCB layer provides a surface in direct contact with the ambient. The thermal via structure provides a thermal path to the inner and bottom layers of the PCB to remove heat.

THERMAL PAD DESIGN

To minimize thermal performance degradation of production PCBs, the contact area between the thermal pad and the PCB should be maximized. Therefore, the size of the thermal pad on the top PCB layer should match the exposed paddle size. The second thermal pad of at least the same size should be placed on the bottom side of the PCB. At least one thermal pad should be in direct thermal contact with a plane such as AVCC or GND.

THERMAL VIA STRUCTURE DESIGN

Effective heat transfer from the top to the inner and bottom layers of the PCB requires thermal vias incorporated into the thermal pad design. Thermal performance increases logarithmically with the number of vias.

Near optimal thermal performance of production PCBs is attained only when tightly spaced thermal vias are placed on the full extent of the thermal pad.

AD8385 PCB DESIGN RECOMMENDATIONS

Top PCB Layer

- Pad size: 0.25 mm × 0.25 mm
- Pad pitch: 0.5 mm
- Thermal pad size: 6.5 mm × 6.5 mm
- Thermal via structure: 0.25 mm diameter vias on a 0.5 mm grid

Bottom PCB Layer

It is recommended that the bottom thermal pad be thermally connected to a plane. The connection should be direct such that the thermal pad becomes part of the plane.

The use of thermal spokes is not recommended when connecting the thermal pads or via structure to the AVCC plane.

Solder Masking

To minimize the formation of solder voids due to solder flowing into the via holes (solder wicking), the via diameter should be small. Optional solder masking of the via holes on the top layer of the PCB plugs the via holes, inhibiting solder flow into the holes. To optimize the thermal pad coverage, the solder mask diameter should be no more than 0.1 mm larger than the via hole diameter.

Solder Mask—Top Layer

- Pads: Set by the customer's PCB design rules
- Thermal vias: 0.25 mm diameter circular mask, centered on the vias.

Solder Mask—Bottom Layer

Set by the customer's PCB design rules.

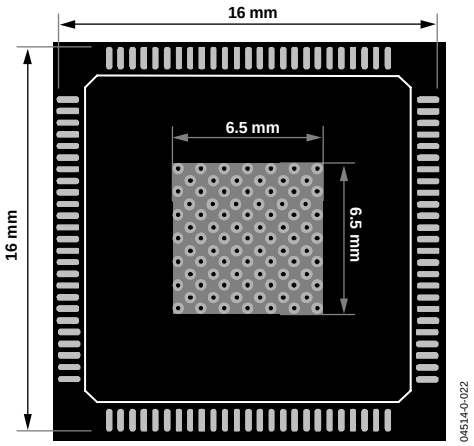


Figure 22. Land Pattern—Top Layer

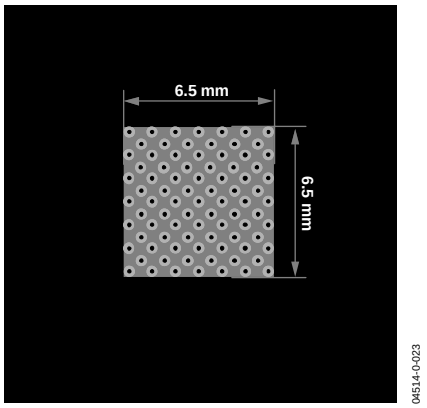


Figure 23. Land Pattern—Bottom Layer

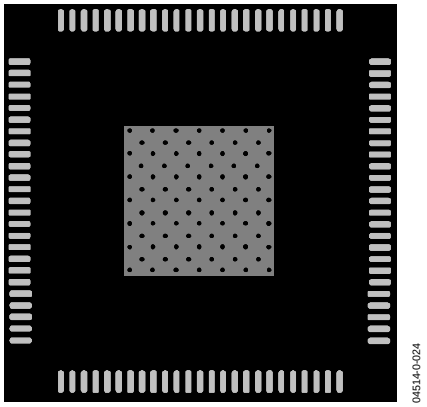


Figure 24. Solder Mask—Top Layer

OUTLINE DIMENSIONS

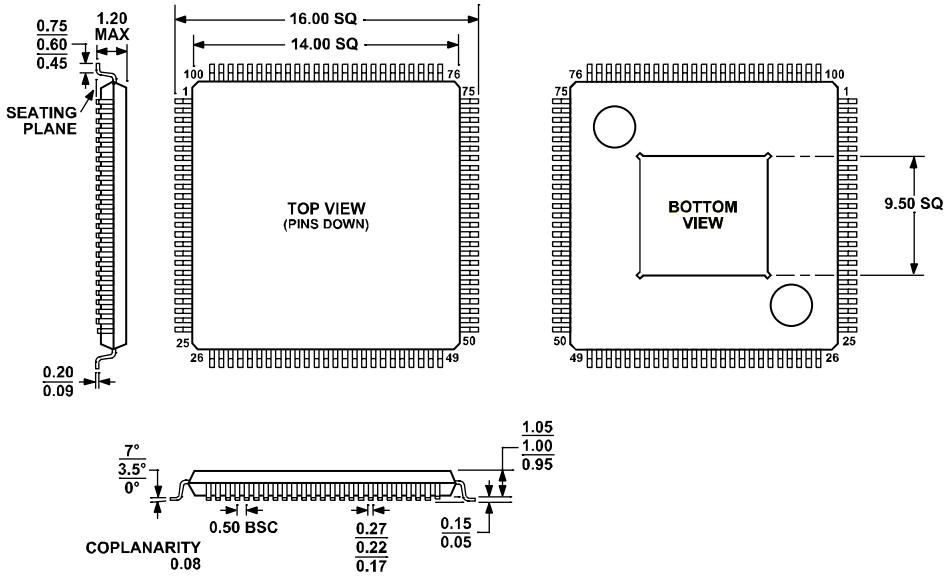


Figure 25. 100-Lead, Thermally Enhanced Thin Quad Flat Package (with Exposed Heat Sink) [TQFP_EP] (SV-100-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8385ASVZ[1]	0°C to 85°C	100-Lead TQFP_EP	SV-100-3

[1] Z = Pb-free part.

NOTES

D04514–0–1/05(0)