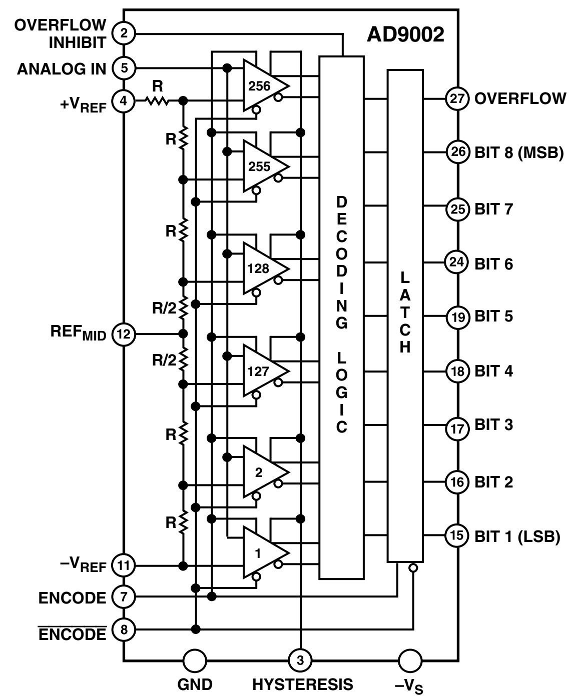
High-Speed 8-Bit Monolithic A/D Converter

AD9002

FEATURES
- 150 MSPS Encode Rate
- Low Input Capacitance: 17 pF
- Low Power: 750 mW
- –5.2 V Single Supply
- MIL-STD-883 Compliant Versions Available

APPLICATIONS
- Radar Systems
- Digital Oscilloscopes/ATE Equipment
- Laser/Radar Warning Receivers
- Digital Radio
- Electronic Warfare (ECM, ECCM, ESM)
- Communication/Signal Intelligence

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9002 is an 8-bit, high-speed, analog-to-digital converter. The AD9002 is fabricated in an advanced bipolar process that allows operation at sampling rates in excess of 150 megasamples/second. Functionally, the AD9002 is comprised of 256 parallel comparator stages whose outputs are decoded to drive the ECL compatible output latches.

An exceptionally wide large signal analog input bandwidth of 160 MHz is due to an innovative comparator design and very close attention to device layout considerations. The wide input bandwidth of the AD9002 allows very accurate acquisition of high speed pulse inputs, without an external track-and-hold. The comparator output decoding scheme minimizes false codes, which is critical to high speed linearity.

The AD9002 provides an external hysteresis control pin that can be used to optimize comparator sensitivity to further improve performance. Additionally, the AD9002's low power dissipation of 750 mW makes it usable over the full extended temperature range. The AD9002 also incorporates an overflow bit to indicate overrange inputs. This overflow output can be disabled with the overflow inhibit pin.

The AD9002 is available in two grades, one with 0.5 LSB linearity and one with 0.75 LSB linearity. Both versions are offered in an industrial grade, –25°C to +85°C, packaged in a 28-lead DIP and a 28-leaded JLCC. The military temperature range devices, –55°C to +125°C, are available in ceramic DIP and LCC packages and comply with MIL-STD-883 Class B.

REV. F

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AD9002–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (–V_S = –5.2 V; Differential Reference Voltage = 2.0 V; unless otherwise noted)

Parameter	Temp	AD9002AD/AJ			AD9002BD/BJ			AD9002SD/SE			AD9002TD/TE			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
RESOLUTION		8			8			8			8			Bits
DC ACCURACY														
Differential Linearity	25°C		0.6	0.75		0.4	0.5		0.6	0.75		0.4	0.5	LSB
	Full			1.0			0.75			1.0			0.75	LSB
Integral Linearity	25°C		0.6	1.0		0.4	0.5		0.6	1.0		0.4	0.5	LSB
	Full			1.2			1.2			1.2			1.2	LSB
No Missing Codes	Full		GUARANTEED			GUARANTEED			GUARANTEED			GUARANTEED		
INITIAL OFFSET ERROR														
Top of Reference Ladder	25°C		8	14		8	14		8	14		8	14	mV
	Full			17			17			17			17	mV
Bottom of Reference Ladder	25°C		4	10		4	10		4	10		4	10	mV
	Full			12			12			12			12	mV
Offset Drift Coefficient	Full		20			20			20			20		µV/°C
ANALOG INPUT														
Input Bias Current[1]	25°C		60	200		60	200		60	200		60	200	µA
	Full			200			200			200			200	µA
Input Resistance	25°C	25	200		25	200		25	200		25	200		kΩ
Input Capacitance	25°C		17	22		17	22		17	22		17	22	pF
Large Signal Bandwidth[2]	25°C		160			160			160			160		MHz
Input Slew Rate[3]	25°C		440			440			440			440		V/µs
REFERENCE INPUT														
Reference Ladder Resistance	25°C	40	80	110	40	80	110	40	80	110	40	80	110	Ω
Ladder Temperature Coefficient			0.25			0.25			0.25			0.25		Ω/°C
Reference Input Bandwidth	25°C		10			10			10			10		MHz
DYNAMIC PERFORMANCE														
Conversion Rate	25°C	125	150		125	150		125	150		125	150		MSPS
Aperture Delay	25°C		1.3			1.3			1.3			1.3		ns
Aperture Uncertainty (Jitter)	25°C		15			15			15			15		ps
Output Delay (t_{PD})[4, 5]	25°C	2.5	3.7	5.5	2.5	3.7	5.5	2.5	3.7	5.5	2.5	3.7	5.5	ns
Transient Response[6]	25°C		6			6			6			6		ns
Overvoltage Recovery Time[7]	25°C		6			6			6			6		ns
Output Rise Time[4]	25°C			3.0			3.0			3.0			3.0	ns
Output Fall Time[4]	25°C			2.5			2.5			2.5			2.5	ns
Output Time Skew[4, 8]	25°C		0.6			0.6			0.6			0.6		ns
ENCODE INPUT														
Logic “1” Voltage[4]	Full	–1.1			–1.1			–1.1			–1.1			V
Logic “0” Voltage[4]	Full			–1.5			–1.5			–1.5			–1.5	V
Logic “1” Current	Full			150			150			150			150	µA
Logic “0” Current	Full			120			120			120			120	µA
Input Capacitance	25°C		3			3			3			3		pF
Encode Pulsewidth (Low)[9]	25°C	1.5			1.5			1.5			1.5			ns
Encode Pulsewidth (High)[9]	25°C	1.5			1.5			1.5			1.5			ns
OVERFLOW INHIBIT INPUT														
0 V Input Current	Full		144	300		144	300		144	300		144	300	µA
AC LINEARITY[10]														
Effective Bits[11]	25°C		7.6			7.6			7.6			7.6		Bits
In-Band Harmonics														
dc to 1.23 MHz	25°C	48	55		48	55		48	55		48	55		dB
dc to 9.3 MHz	25°C		50			50			50			50		dB
dc to 19.3 MHz	25°C		44			44			44			44		dB
Signal-to-Noise Ratio[12]	25°C	46	47.6		46	47.6		46	47.6		46	47.6		dB
Two Tone Intermod Rejection[13]	25°C		60			60			60			60		dB
DIGITAL OUTPUTS[4]														
Logic “1” Voltage	Full	–1.1			–1.1			–1.1			–1.1			V
Logic “0” Voltage	Full			–1.5			–1.5			–1.5			–1.5	V
POWER SUPPLY[14]														
Supply Current (–5.2 V)	25°C		145	175		145	175		145	175		145	175	mA
	Full			200			200			200			200	mA
Nominal Power Dissipation	25°C		750			750			750			750		mW
Reference Ladder Dissipation	25°C		50			50			50			50		mW
Power Supply Rejection Ratio[15]	25°C		0.8	1.5		0.8	1.5		0.8	1.5		0.8	1.5	mV/V

NOTES
[1]Measured with AIN = 0 V.
[2]Measured by FFT analysis where fundamental is –3 dBc.
[3]Input slew rate derived from rise time (10 to 90%) of full scale input.
[4]0utputs terminated through 100 Ω to –2 V.
[5]Measured from ENCODE in to data out for LSB only.
[6]For full-scale step input, 8-bit accuracy is attained in specified time.
[7]Recovers to 8-bit accuracy in specified time after 150% full-scale input overvoltage.
[8]Output time skew includes high-to-low and low-to-high transitions as well as bit-to-bit time skew differences.
[9]ENCODE signal rise/fall times should be less than 10 ns for normal operation.
[10]Measured at 125 MSPS encode rate.
[11]Analog input frequency = 1.23 MHz.
[12]RMS signal to rms noise, with 1.23 MHz analog input signal.
[13]Input signals 1 V p-p @ 1.23 MHz and 1 V p-p @ 2.30 MHz.
[14]Supplies should remain stable within ±5% for normal operation.
[15]Measured at –5.2 V ±5%.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage ($-V_S$) . . . . –6 V
Analog-to-Digital Supply Voltage Differential . . . . 0.5 V
Analog Input Voltage . . . . $-V_S$ to +0.5 V
Digital Input Voltage . . . . $-V_S$ to 0 V
Reference Input Voltage ($+V_{REF} - V_{REF}$)[2] . . . –3.5 V to +0.1 V
Differential Reference Voltage . . . . 2.1 V
Reference Midpoint Current . . . . ±4 mA
ENCODE to $\overline{\text{ENCODE}}$ Differential Voltage . . . . 4 V
Digital Output Current . . . . 20 mA
Operating Temperature Range
  AD9002AD/BD/AJ/BJ . . . . –25°C to +85°C
  AD9002SE/SD/TD/TE . . . . –55°C to +125°C
Storage Temperature Range . . . . –65°C to +150°C
Junction Temperature[3] . . . . 150°C
Lead Soldering Temperature (10 sec) . . . . 300°C

NOTES
[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.
[2]$+V_{REF} \geq -V_{REF}$ under all circumstances.
[3]Maximum junction temperature (t_J max) should not exceed 175°C for ceramic packages, and 150°C for plastic packages:

$t_J = PD\ (\theta_{JA}) + t_A$
$PD\ (\theta_{JC}) + t_C$

where
PD = power dissipation
θ_{JA} = thermal impedance from junction to ambient (°C/W)
θ_{JC} = thermal impedance from junction to case (°C/W)
t_A = ambient temperature (°C)
t_C = case temperature (°C)

Typical thermal impedances are:
Ceramic DIP θ_{JA} = 56°C/W; θ_{JC} = 20°C/W
Ceramic LCC θ_{JA} = 69°C/W; θ_{JC} = 23°C/W
PLCC θ_{JA} = 60°C/W; θ_{JC} = 19°C/W.

Recommended Operating Conditions

Parameter	Input Voltage		
	Min	Nominal	Max
$-V_S$	–5.46	–5.20	–4.94
$+V_{REF}$	$-V_{REF}$	0.0 V	+0.1
$-V_{REF}$	–2.1	–2.0	$+V_{REF}$
Analog Input	$-V_{REF}$		$+V_{REF}$

EXPLANATION OF TEST LEVELS

Test Level I – 100% production tested.
Test Level II – 100% production tested at 25°C, and sample tested at specified temperatures.
Test Level III – Sample tested only.
Test Level IV – Parameter is guaranteed by design and characterization testing.
Test Level V – Parameter is a typical value only.
Test Level VI – All devices are 100% production tested at 25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

ORDERING GUIDE

Model	Linearity	Temperature Range	Package Option*
AD9002AD	0.75 LSB	–25°C to +85°C	D-28
AD9002BD	0.50 LSB	–25°C to +85°C	D-28
AD9002AJ	0.75 LSB	–25°C to +85°C	J-28
AD9002BJ	0.50 LSB	–25°C to +85°C	J-28
AD9002SD/883B	0.75 LSB	–55°C to +125°C	D-28
AD9002SE/883B	0.75 LSB	–55°C to +125°C	E-28A
AD9002TD/883B	0.50 LSB	–55°C to +125°C	D-28
AD9002TE/883B	0.50 LSB	–55°C to +125°C	E-28A

*D = Ceramic DIP; E = Leadless Ceramic Chip Carrier; J = Ceramic Chip Carrier, J-Formed Leads.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9002 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

FUNCTIONAL DESCRIPTION

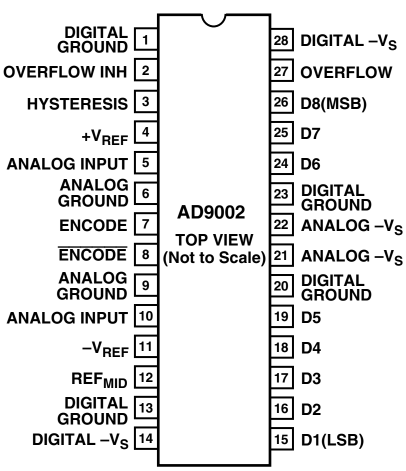
Pin #	Mnemonic	Description
1	DIGITAL GROUND	One of four digital ground pins. All digital ground pins should be connected together.
2	OVERFLOW INH	OVERFLOW INHIBIT controls the data output polarity for overvoltage inputs.

Analog Input	Overflow Enabled (Floating or –5.2 V) of D1–D8	Overflow Inhibited (GND) of D1–D8
$V_{IN} > +V_{REF}$	1 0 0 0 0 0 0 0 0	0 1 1 1 1 1 1 1 1
$V_{IN} \leq +V_{REF}$	0 X X X X X X X X	0 X X X X X X X X

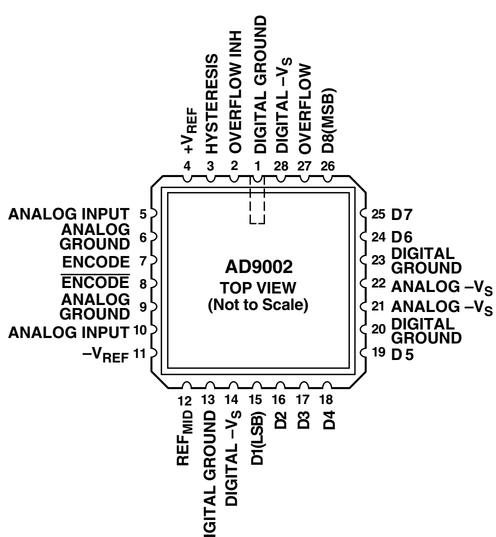
Pin #	Mnemonic	Description
3	HYSTERESIS	The Hysteresis control voltage varies the comparator hysteresis from 0 mV to 10 mV, for a change from –5.2 V to –2.2 V at the Hysteresis control pin. Normally converted to –5.2 V.
4	$+V_{REF}$	The most positive reference voltage for the internal resistor ladder.
5	ANALOG INPUT	One of two analog input pins. Both analog input pins should be connected together.
6	ANALOG GROUND	One of two analog ground pins. Both analog ground pins should be connected together.
7	ENCODE	Noninverted input of the differential encode input. This pin is driven in conjunction with $\overline{\text{ENCODE}}$. Data is latched on the rising edge of the ENCODE signal.
8	$\overline{\text{ENCODE}}$	Inverted input of the differential encode input. This pin is driven in conjunction with ENCODE.
9	ANALOG GROUND	One of two analog ground pins. Both analog ground pins should be connected together.
10	ANALOG INPUT	One of two analog input pins. Both analog inputs should be connected together.
11	$-V_{REF}$	The most negative reference voltage for the internal resistor ladder.
12	REF_{MID}	The midpoint tap on the internal resistor ladder.
13	DIGITAL GROUND	One of four digital ground pins. All digital ground pins should be connected together.
14	DIGITAL $-V_S$	One of two negative digital supply pins (nominally –5.2 V). Both digital supply pins should be connected together.
15	D1 (LSB)	Digital Data Output
16–19	D2–D5	Digital Data Output
20	DIGITAL GROUND	One of four digital ground pins. All digital ground pins should be connected together.
21, 22	ANALOG $-V_S$	One of two negative analog supply pins (nominally –5.2 V). Both analog supply pins should be connected together
23	DIGITAL GROUND	One of four digital ground pins. All digital ground pins should be connected together.
24, 25	D6, D7	Digital Data Output
26	D8 (MSB)	Digital Data Output
27	OVERFLOW	Overflow data output. Logic high indicates an input overvoltage ($V_{IN} > +V_{REF}$) if OVERFLOW INHIBIT is enabled (overflow enabled, –5.2 V). See OVERFLOW INHIBIT.
28	DIGITAL $-V_S$	One of two negative digital supply pins (nominally –5.2 V). Both digital supply pins should be connected together.

PIN DESIGNATIONS

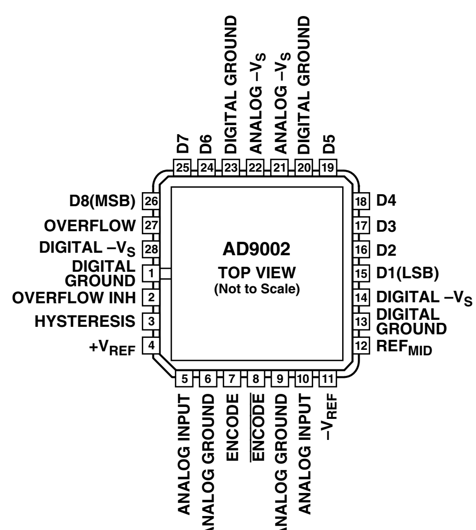
DIP



LCC



JLCC



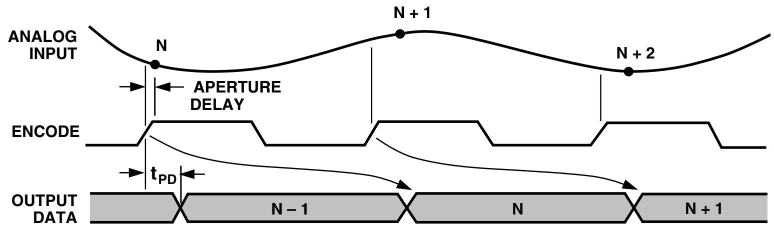


Figure 1. Timing Diagram

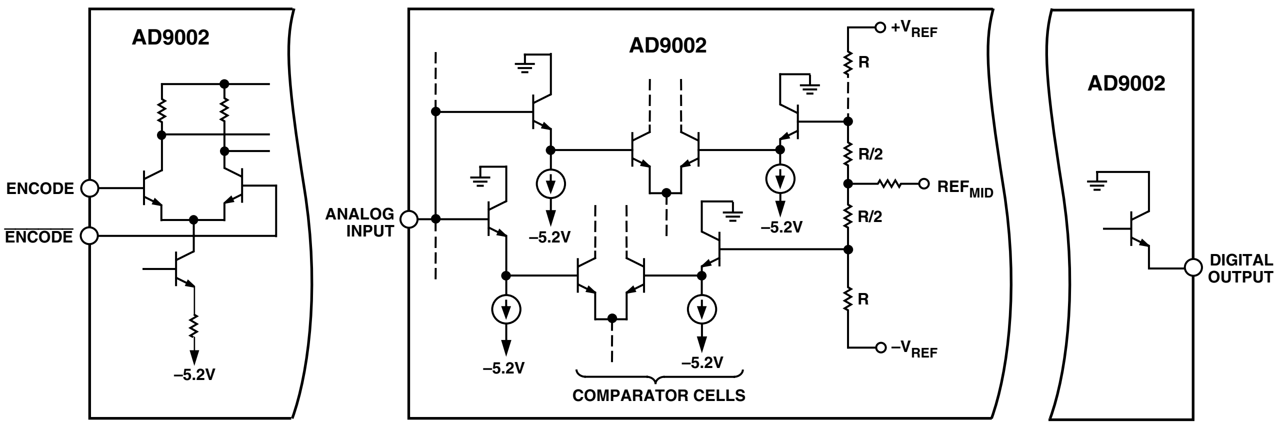


Figure 2. Input/Output Circuits

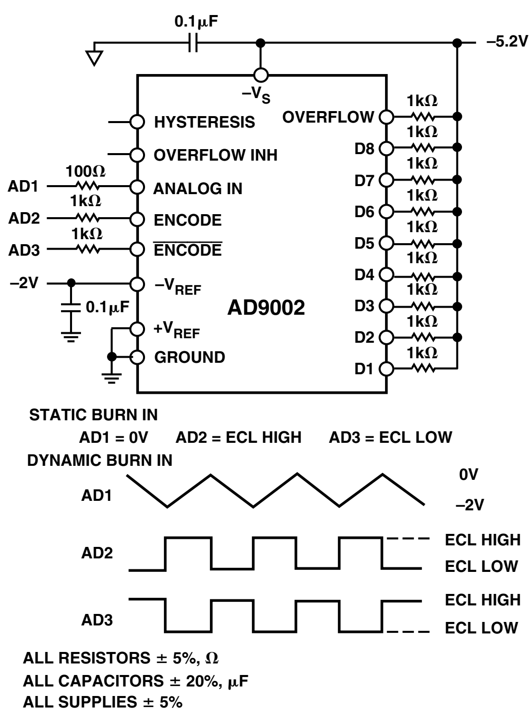


Figure 3. Burn-in Diagram

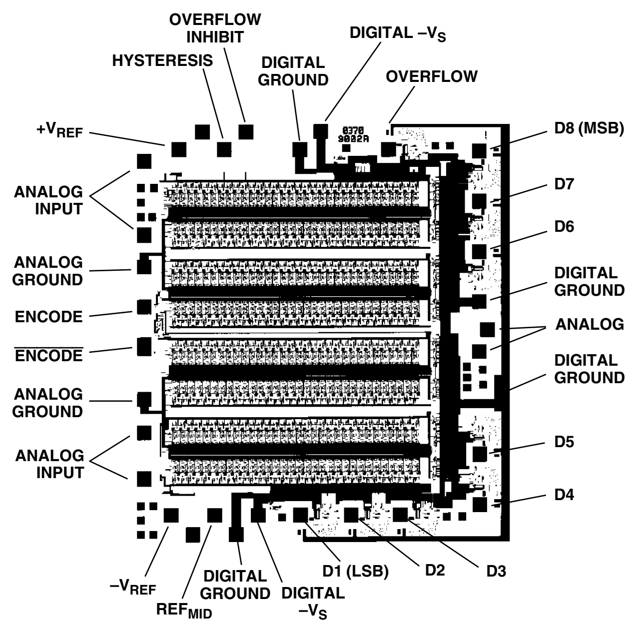


Figure 4. Die Layout and Mechanical Information

Die Dimensions . . . . 106 × 114 × 15 (±2) mils
Pad Dimensions . . . . 4 × 4 mils
Metalization . . . . Gold
Backing . . . . None
Substrate Potential . . . . $–V_S$
Passivation . . . . .Nitride
Die Attach . . . . Gold Eutectic (Ceramic)
. . . . Epoxy (Plastic)
Bond Wire . . . . 1-1.3 mil Gold; Gold Ball Bonding

APPLICATION INFORMATION

The AD9002 is compatible with all standard ECL logic families, including 10K and 10KH. 100K ECL's logic levels are temperature compensated, and are therefore compatible with the AD9002 (and most other ECL device families) only over a limited temperature range. To operate at the highest encode rates, the supporting logic around the AD9002 will need to be equally fast. Whichever of the ECL logic families is used, special care must be exercised to keep digital switching noise away from the analog circuits around the AD9002. The two most critical items are digital supply lines and digital ground return.

The input capacitance of the AD9002 is an exceptionally low 17 pF. This allows the use of a wide range of input amplifiers, both hybrid and monolithic. To take full advantage of the wide input bandwidth of the AD9002, a hybrid amplifier such as the AD9610 will be required. For those applications that do not require the full input bandwidth of the AD9002, more traditional monolithic amplifiers, such as the AD846, will work very well. Overall performance with any amplifier can be improved by inserting a 10 Ω resistor in series with the amplifier output.

The output data is buffered through the ECL compatible output latches. All data is delayed by one clock cycle, in addition to the latch propagation delay (t_{PD}), before becoming available at the outputs. Both the analog-to-digital conversion cycle and the data transfer to the output latches are triggered on the rising edge of the differential, ECL compactible ENCODE signal (see timing diagram). In applications where only a single-ended signal is available, the AD96685, a high speed, ECL voltage comparator, can be employed to generate the differential signals. All ECL signals (including the overflow bit) should be terminated properly to avoid ringing and reflection.

The AD9002 also incorporates a HYSTERESIS control pin which provides from 0 mV to 10 mV of additional hysteresis in the comparator input stages. Adjustments in the HYSTERESIS control voltage may help improve noise immunity and overall performance in harsh environments.

The OVERFLOW INHIBIT pin of the AD9002 determines how the converter handles overrange inputs (AIN ≥ $+V_{REF}$). In the "enabled" state (floating at –5.2 V), the OVERFLOW output will be at logic HIGH and all other outputs will be at logic LOW for overrange inputs (return-to-zero operation). In the "inhibited" state (tied to ground), the OVERFLOW output will be at logic LOW, and all other outputs will be at logic HIGH for overrange inputs (nonreturn-to-zero operation).

The AD9002 provides outstanding error rate performance. This is due to tight control of comparator offset matching and a fault tolerant decoding stage. Additional improvements in error rate are possible through the addition of hysteresis (see HYSTERESIS control pin). This level of performance is extremely important in fault-sensitive applications such as digital radio (QAM).

Dramatic improvements in comparator design and construction give the AD9002 excellent dynamic characteristics, especially SNR (signal-to-noise ratio). The 160 MHz input bandwidth and low error rate performance give the AD9002 an SNR of 48 dB with a 1.23 MHz input. High SNR performance is particularly important in wide bandwidth applications, such as pulse signature analysis, commonly performed in advanced radar receivers.

LAYOUT SUGGESTIONS

Designs using the AD9002, like all high speed devices, must follow a few basic layout rules to insure optimum performance. Essentially, these guidelines are meant to avoid many of the problems associated with high speed designs. The first requirement is for a substantial ground plane around and under the AD9002. Separate ground plane areas for the digital and analog components may be useful, but these separate grounds should be connected together at the AD9002 to avoid the effects of "ground loop" currents.

The second area that requires an extra degree of attention involves the three reference inputs, $+V_{REF}$, REF_{MID}, and $–V_{REF}$. The $+V_{REF}$ input and the $–V_{REF}$ input should both be driven from a low impedance source (note that the $+V_{REF}$ input is typically tied to analog ground). A low drift amplifier should provide satisfactory results, even over an extended temperature range. Adjustments at the REF_{MID} input may be useful in improving the integral linearity by correcting any reference ladder skews. The application circuit shown below demonstrates a simple and effective means of driving the reference circuit.

The reference inputs should be adequately decoupled to ground through 0.1 µF chip capacitors to limit the effects of system noise on conversion accuracy. The power supply pins must also be decoupled to ground to improve noise immunity; 0.1 µF and 0.01 µF chip capacitors are recommended.

The analog input signal is brought into the AD9002 through two separate input pins. It is very important that the two input pins be driven symmetrically with equal length electrical connections. Otherwise, aperture delay errors may degrade converter performance at high frequencies.

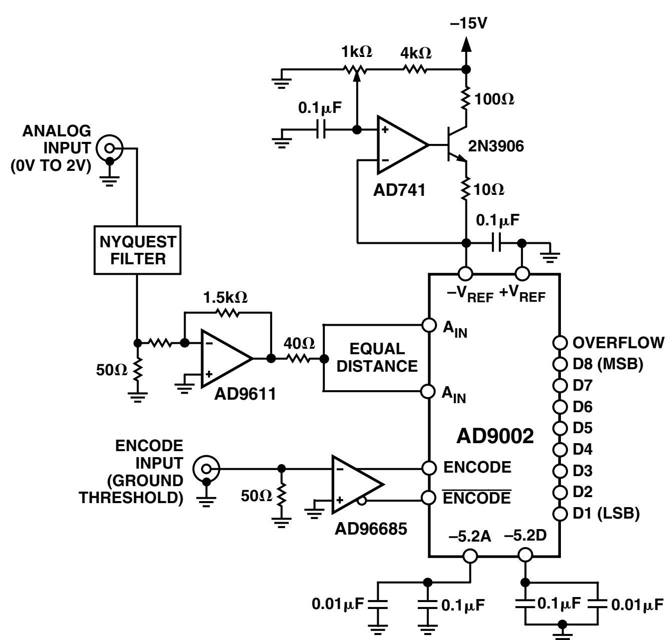


Figure 5. Typical Application

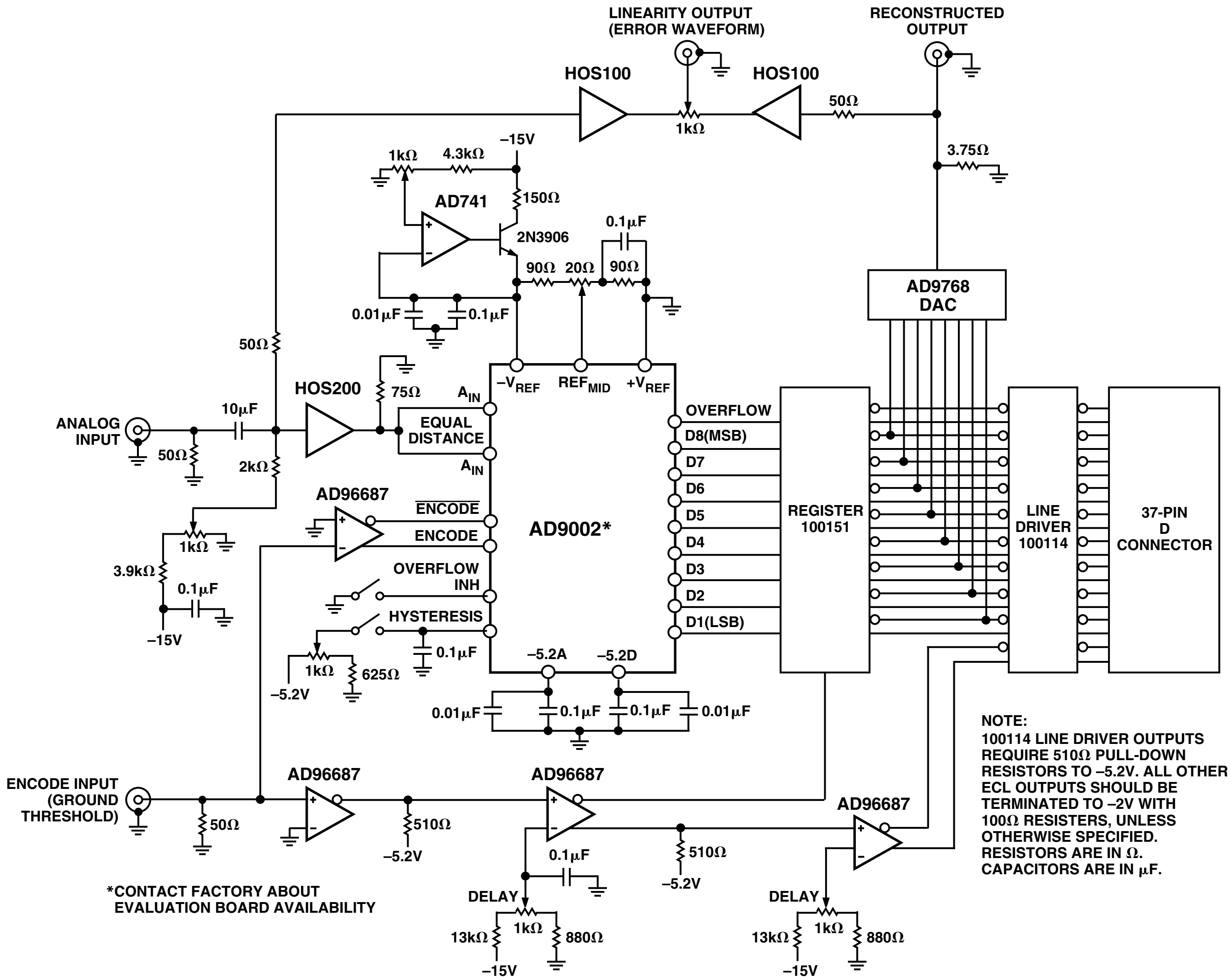


Figure 6. AD9002 Evaluation Circuit

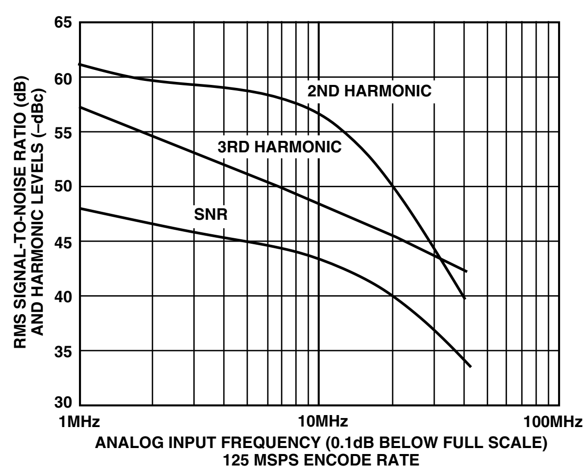
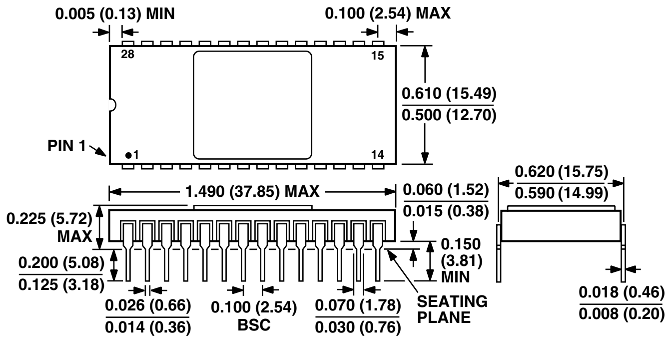


Figure 7. Dynamic Performance

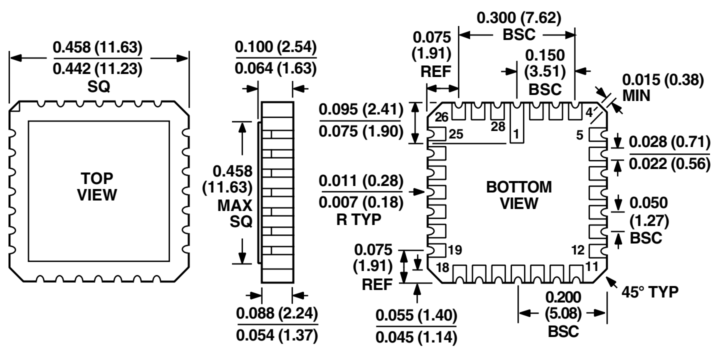
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

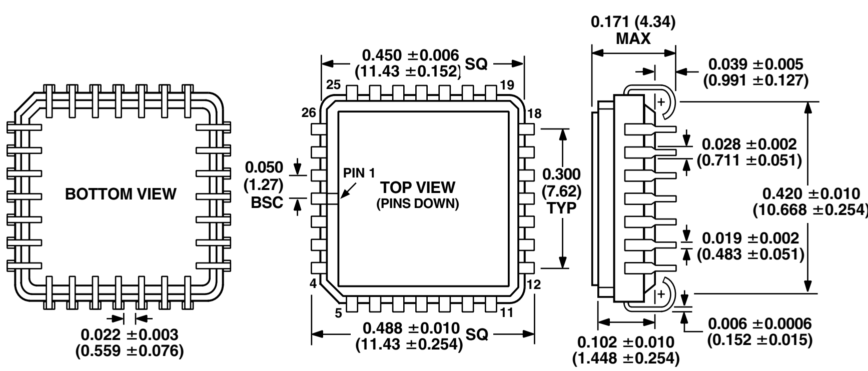
28-Lead Ceramic Side-Brazed DIP (D-28)



28-Lead Ceramic Leadless Chip Carrier (E-28A)



28-Leaded JLCC (J-28)



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Revision History

Location	Page
Data Sheet changed from REV. E to REV. F.	
Edit to ABSOLUTE MAXIMUM RATINGS	3