ANALOG DEVICES

High-Frequency Switch Mode Li-Ion Battery Charger

ADP3806

FEATURES

- Li-Ion Battery Charger
- Three Battery Voltage Options
  - Selectable 12.525 V/16.700 V
  - Selectable 12.600 V/16.800 V
  - Adjustable
- High End-of-Charge Voltage Accuracy
  - ±0.4% @ 25°C
  - ±0.6% @ 5°C to 55°C
  - ±0.7% @ 0°C to 85°C
- Programmable Charge Current with Rail-to-Rail Sensing
- System Current Sense with Reverse Input Protection
- Softstart Charge Current
- Undervoltage Lockout
- Bootstrapped Synchronous Drive for External NMOS
- Programmable Oscillator Frequency
- Oscillator SYNC Pin
- Low Current Flag
- Trickle Charge

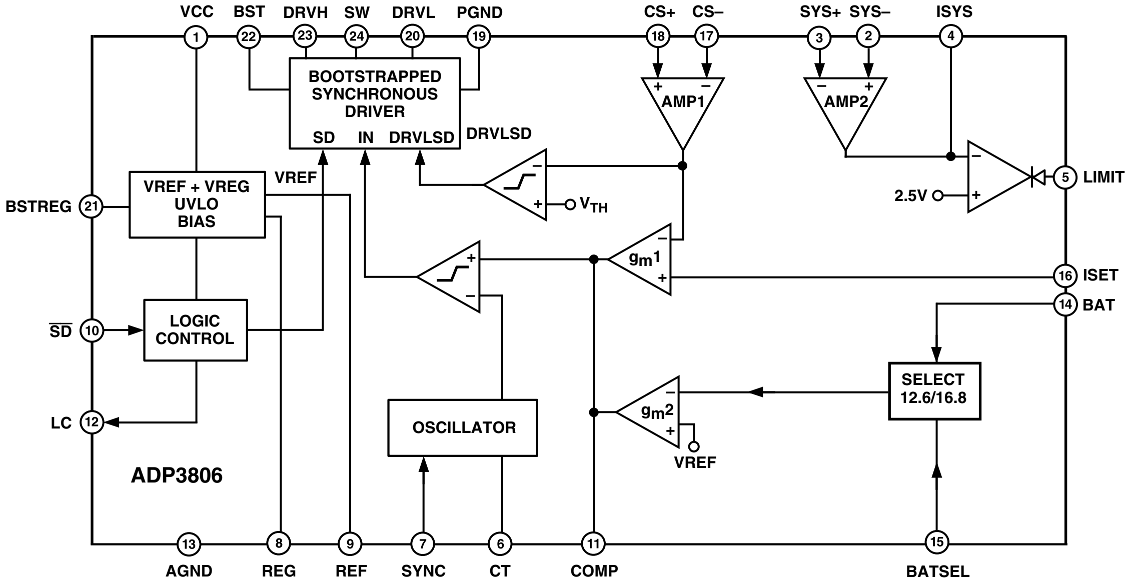
APPLICATIONS

- Portable Computers
- Fast Chargers

GENERAL DESCRIPTION

The ADP3806 is a complete Li-Ion battery-charging IC. The device combines high output voltage accuracy with constant current control to simplify the implementation of Constant-Current, Constant-Voltage (CCCV) chargers. The ADP3806 is available in three options. The ADP3806-12.6 guarantees the final battery voltage be selected to 12.6 V or 16.8 V ± 0.6%, the ADP3806-12.5 guarantees 12.525 V/16.7 V ± 0.6% and the ADP3806 is adjustable using two external resistors to set the battery voltage. The current sense amplifier has rail-to-rail inputs to accurately operate under low drop out and short circuit conditions. The charge current is programmable with a dc voltage on ISET. A second differential amplifier senses the system current across an external sense resistor and outputs a linear voltage on the ISYS pin. The bootstrapped synchronous driver allows the use of two NMOS transistors for lower system cost.

FUNCTIONAL BLOCK DIAGRAM


VCC
BST
DRVH
SW
DRVL
PGND
CS+
CS–
SYS+
SYS–
ISYS
1
22
23
24
20
19
18
17
3
2
4
BOOTSTRAPPED SYNCHRONOUS DRIVER
SD
IN
DRVLSD
DRVLSD
AMP1
AMP2
LIMIT
5
2.5V
VREF + VREG UVLO BIAS
VREF
BSTREG
21
V_{TH}
gm1
ISET
16
BAT
14
$\overline{SD}$
10
LOGIC CONTROL
SELECT 12.6/16.8
gm2
VREF
LC
12
OSCILLATOR
ADP3806
13
8
9
7
6
11
15
AGND
REG
REF
SYNC
CT
COMP
BATSEL

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ADP3806–SPECIFICATIONS (@ 0°C ≤ T_A ≤ 100°C, VCC = 16 V, unless otherwise noted.)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
BATTERY SENSE INPUT						
ADP3806-12.6 V and 16.8 V						
ADP3806-12.525 V and 16.7 V						
	T_A = 25°C, 13 V ≤ VCC ≤ 20 V	V_{BAT}	–0.4		+0.4	%
	5°C ≤ T_A ≤ 55°C	V_{BAT}	–0.6		+0.6	%
	0°C ≤ T_A ≤ 85°C	V_{BAT}	–0.7		+0.7	%
Input Resistance	Part in Operation	R_{BAT}	250	350		kΩ
Input Current	Part in Shutdown	$I_{BAT(SD)}$		0.2	1.0	μA
BATTERY SENSE INPUT						
ADP3806						
V_{BAT} = 2.5 V	T_A = 25°C, 13 V ≤ VCC ≤ 20 V	V_{BAT}	–0.5		+0.5	%
	0°C ≤ T_A ≤ 85°C	V_{BAT}	–0.7		+0.7	%
Input Current Operating	BATSEL = Open, Part in Operation			0.2	1.0	μA
Input Current Shutdown	BATSEL = 100 k to GND, Part in Shutdown			0.2	1.0	μA
OSCILLATOR						
Maximum Frequency[2]		f_{CT}	1000			kHz
Frequency Variation[3]	CT = 180 pF	f_{CT}	210	250	290	kHz
CT Charge Current		I_{CT}	125	150	175	μA
0% Duty Cycle Threshold	@ COMP Pin			1.0		V
Maximum Duty Cycle Threshold	@ COMP Pin			2.5		V
SYNC Input High		$SYNC_H$	2.2			V
SYNC Input Low		$SYNC_L$			0.8	V
SYNC Input Current		I_{SYNC}		0.2	1.0	μA
GATE DRIVE						
On Resistance	I_L = 10 mA	R_{ON}		6	10	Ω
Rise, Fall Time	C_L = 1 nF, DRVL and DRVH	t_r, t_f		35		ns
Overlap Protection Delay	DRVL Falling to DRVH Rising, DRVH Falling to DRVL Rising	t_{OP}		50		ns
SW Bias Current	Part in Shutdown, V_{SW} = 12.6 V			0.2	1.0	μA
BST Cap Refresh Threshold	$V_{BST} - V_{SW}$			3.7		V
CURRENT SENSE AMPLIFIER						
Input Common-Mode Range	V_{CS+} and $V_{CS–}$	$V_{CS(CM)}$	0.0		VCC + 0.3	V
Input Differential Mode Range	V_{CS}[4]	$V_{CS(DM)}$	0.0		160	mV
Input Offset Voltage[5]	0 V ≤ $V_{CS(CM)}$ ≤ VCC	$V_{CS(VOS)}$		1.0		mV
Gain[5]				25		V/V
Input Bias Current	0 V ≤ $V_{CS(CM)}$ ≤ VCC, Part in Operation	$V_{CS(IB)}$		50	100	μA
Input Offset Current	0 V ≤ $V_{CS(CM)}$ ≤ VCC	$V_{CS(IOS)}$		1.0	2.0	μA
Input Bias Current	Part in Shutdown			0.2	1.0	μA
DRVL Shutdown Threshold	Measured between V_{CS+} and V_{CS-}	$V_{CS(SD)}$		48		mV
SYSTEM CURRENT SENSE[6]						
Input Common-Mode Range	SYS+ and SYS–, I_L = 0 mA, V_{ISYS} = 3 V	$V_{SYS(CM)}$	4.0		VCC + 0.3	V
Input Differential Range	$(V_{SYS+}) - (V_{SYS–})$	$V_{SYS(DM)}$	0		100	mV
Input Offset Voltage				0.5		mV
Input Bias Current, SYS+	$V_{SYS(DM)}$ = 0 V, $V_{SYS(CM)}$ = 16 V	$I_{B(SYS+)}$		200	300	μA
Input Bias Current, SYS-	$V_{SYS(DM)}$ = 0 V, $V_{SYS(CM)}$ = 16 V	$I_{B(SYS–)}$		70	125	μA
Voltage Gain	10 V ≤ $V_{SYS(CM)}$ ≤ VCC + 0.3 V, I_L = 100 μA		48.5	50	51.5	V/V
Output Range	I_L = 1 mA[7], $V_{SYS(CM)}$ > 6 V	V_{ISYS}	0		5.0	V
Limit Output Threshold	V_{LIMIT} ≤ 0.2 V, 50 kΩ Pull-up to 5 V	$V_{TH(LIMIT)}$	2.3	2.5	2.7	V
Limit Output Voltage	V_{ISYS} > 2.65 V, I_{SINK} = 700 μA	$V_{O(LIMIT)}$		0.1	0.2	V

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
ISET INPUT						
Charge Current Programming Function	$0.0\ V < V_{ISET} \le 4.0\ V$	V_{ISET}/V_{CS}		25		V/V
Programming Function Accuracy	$V_{ISET} = 4.0\ V$, $1\ V \le V_{CS(CM)} \le 16V$		–5	±1.0	+5	%
	$V_{ISET} = 0.50\ V$, $1\ V \le V_{CS(CM)} \le 10V$		–30	±10	+30	%
ISET Bias Current	$0.0\ V \le V_{ISET} \le 4.0\ V$	I_B		0.2	1.0	µA
BATSEL INPUT						
$V_{BAT} = 12.6\ V$			2.0			V
$V_{BAT} = 16.8\ V$					0.8	V
BATSEL Input Current				0.2	5.0	µA
BOOST REGULATOR OUTPUT						
Output Voltage	$C_L = 0.1\ µF$	V_{BSTREG}	6.8	7.0	7.2	V
Output Current[10]		I_{BSTREG}	3.0	5.0		mA
ANALOG REGULATOR OUTPUT						
Output Voltage	$C_L = 10\ nF$	V_{REG}	5.8	6.0	6.2	V
Output Current[10]		I_{REG}	3.0	5.0		mA
PRECISION REFERENCE OUTPUT						
Output Voltage		V_{REF}	2.47	2.5	2.53	V
Output Current[10]		I_{REF}	0.5	1.1		mA
SHUTDOWN ($\overline{SD}$)						
ON		$\overline{SD}_H$	2.0			V
OFF		$\overline{SD}_L$			0.8	V
$\overline{SD}$ Input Current				0.2	1.0	µA
POWER SUPPLY						
ON Supply Current	No External Loads, UVLO ≤ VCC ≤ 20 V	I_{SYON}		6.0	8.0	mA
OFF Supply Current	No External Loads, VCC ≤ 20 V	I_{SYOFF}		1.0	5.0	µA
UVLO Threshold Voltage	Turn On	V_{UVLO}	5.65	6.0	6.25	V
UVLO Hysteresis	Turn Off		0.1	0.3	0.5	V
LC OUTPUT						
Output Voltage Low	High Current Mode[8], $I_{SINK} = 100\ µA$			0.1	0.4	V
Output Voltage High	Low Current Mode[9]			External		V
OUTPUT REVERSE LEAKAGE PROTECTION						
Leakage Current	VCC = Floating, $V_{BAT} = 12.6\ V$	I_{DISCH}		1	5	µA
OVERCURRENT COMPARATOR						
Overcurrent Threshold		$V_{CS(OC)}$		180		mV
Response Time	$V_{CS} > 180\ mV$ to COMP < 1 V	t_{OC}		2		µs
OVERVOLTAGE COMPARATOR						
Overvoltage Threshold		$V_{BAT(OV)}$		120		%
Response Time	$V_{BAT} > 120\%$ to COMP < 1 V	t_{OV}		2		µs

NOTES

[1] All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods.

[2] Guaranteed by design, not tested in production.

[3] If SYNC function is used, then f_{SYNC} must be greater than f_{CT}, but less than 120% of f_{CT}.

[4] $V_{CS} = (V_{CS+}) - (V_{CS-})$.

[5] Accuracy guaranteed by ISET INPUT, Programming Function Accuracy specification.

[6] System current sense is active during shutdown.

[7] Load current is supplied through SYS+ pin.

[8] $V_{BAT} < 93\%$ of final or $V_{CS} > 25\ mV$.

[9] $V_{BAT} \ge 93\%$ of final and $V_{CS} \le 25\ mV$.

[10] Guaranteed Output Current from 0 to Min specified value to maintain regulation.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

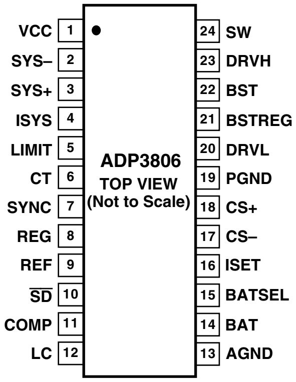
Input Voltage (VCC)	–0.3 V to +25 V
BAT, CS+, CS–	–0.3 V to VCC +0.3 V
SYS+, SYS–	–25 V to +25 V
BST	–0.3 V to +30 V
BST to SW	–0.3 V to +8 V
SW to PGND	–4 V to +25 V
DRVL to PGND	–0.3 V to +8 V
ISET, BATSEL, $\overline{SD}$, SYNC, CT, LIMIT, ISYS, LC	–0.3 V to +10 V
COMP	–0.3 V to +3 V
GND to PGND	–0.3 V to +0.3 V
Operating Ambient Temperature Range	0°C to 100°C
θ_{JA}	115°C/W
Operating Junction Temperature Range	0°C to 125°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature Range (Soldering 10 sec)	300°C

*This is a stress rating only, operation these limits can cause the device to be permanently damaged. Unless otherwise specified, all voltages are referenced to GND. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Battery Voltage	Package Description	Package Option
ADP3806JRU	Adjustable	TSSOP-24	RU-24
ADP3806JRU-12.5	12.525 V/ 16.7 V	TSSOP-24	RU-24
ADP3806JRU-12.6	12.600 V/ 16.8 V	TSSOP-24	RU-24

PIN CONFIGURATION
24-Lead TSSOP



PIN FUNCTION DESCRIPTIONS

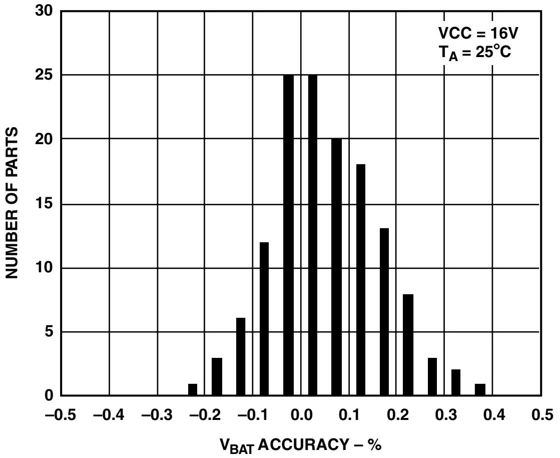
Pin No.	Mnemonic	Function
1	VCC	Supply Voltage
2	SYS–	Negative System Current Sense Input
3	SYS+	Positive System Current Sense Input
4	ISYS	System Current Sense Output
5	LIMIT	System Current Sense Limit Output
6	CT	Oscillator Timing Capacitor
7	SYNC	Oscillator Synchronization Pin
8	REG	6.0 V Analog Regulator Output
9	REF	2.5 V Precision Reference Output
10	$\overline{SD}$	Shutdown Control Input
11	COMP	External Compensation Node
12	LC	Low Current Output
13	AGND	Analog Ground
14	BAT	Battery Sense Input. 2.5 V for ADP3806, 12.525 V/16.7 V for ADP3806-12.5, or 12.6 V/16.8 V for ADP3806-12.6
15	BATSEL	Battery Voltage Sense Input High = 3 Cells, Low = 4 Cells
16	ISET	Charge Current Program Input
17	CS–	Negative Current Sense Input
18	CS+	Positive Current Sense Input
19	PGND	Power Ground
20	DRVL	Low Drive Output switches between REG and PGND
21	BSTREG	7.0 V Regulator Output for Boost
22	BST	Floating Bootstrap Supply for DRVH
23	DRVH	High Drive Output switches between SW and BST
24	SW	Buck Switching Node Reference for DRVH

CAUTION

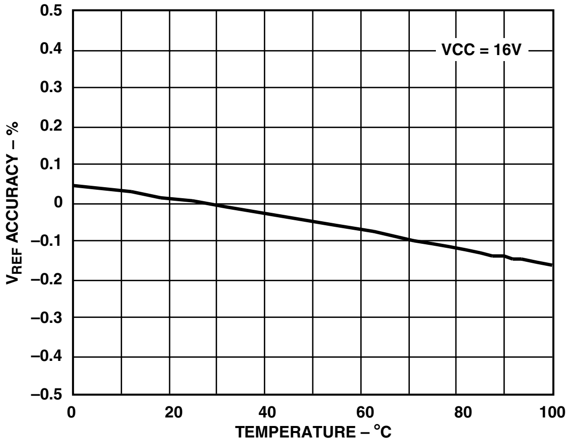
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADP3806 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

WARNING!
ESD SENSITIVE DEVICE

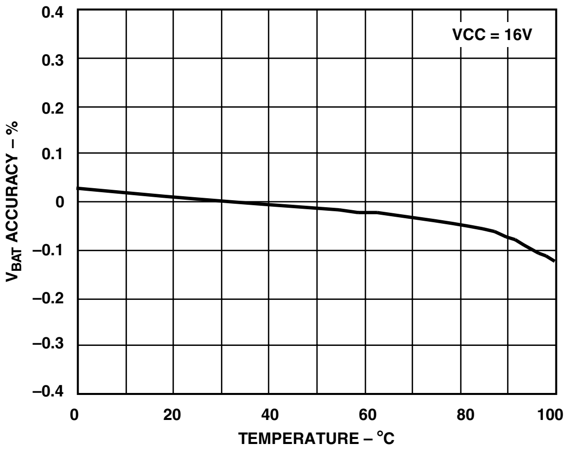
Typical Performance Characteristics–ADP3806



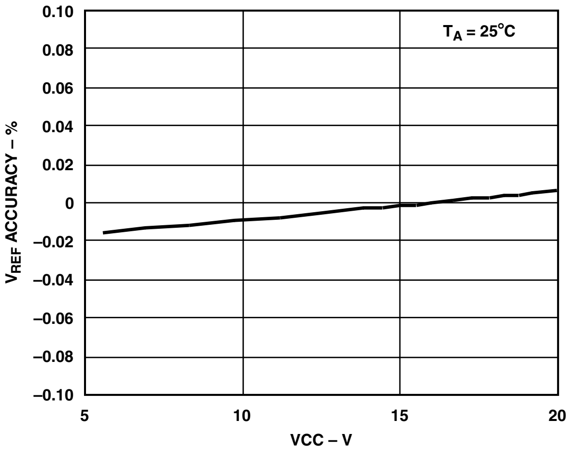
TPC 1. V_{BAT} Accuracy Distribution



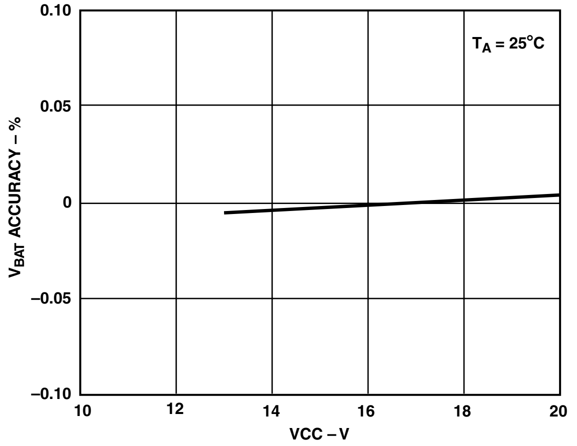
TPC 4. V_{REF} Accuracy vs. Temperature



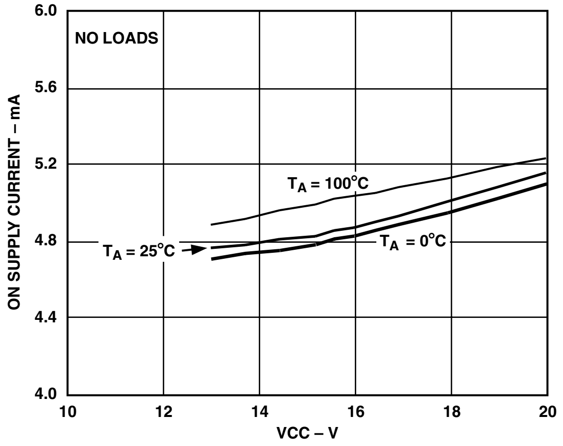
TPC 2. V_{BAT} Accuracy vs. Temperature



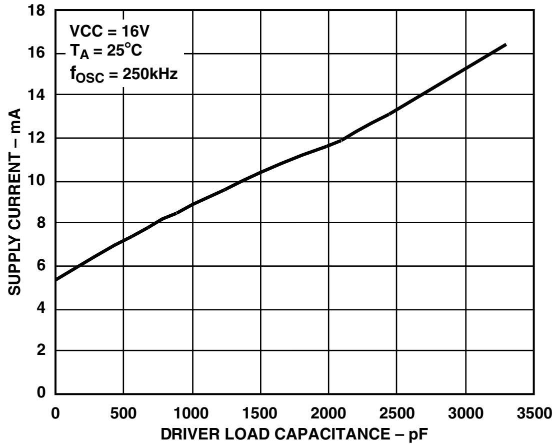
TPC 5. V_{REF} Accuracy vs. VCC



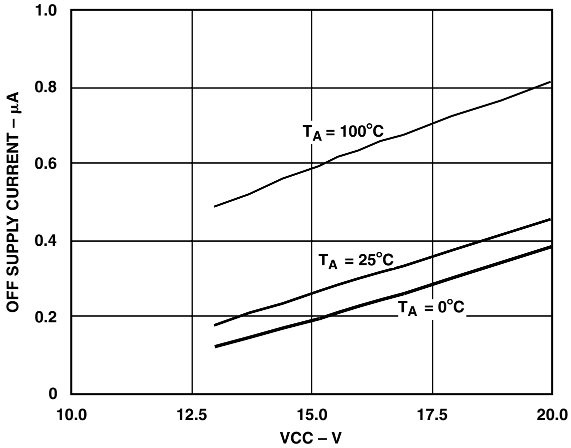
TPC 3. V_{BAT} Accuracy vs. Supply Voltage



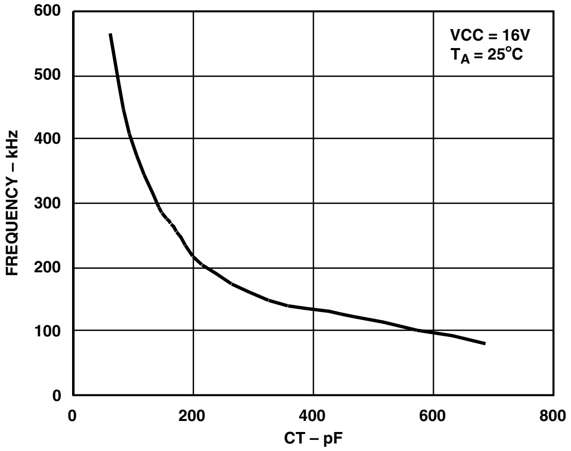
TPC 6. ON Supply Current vs. VCC



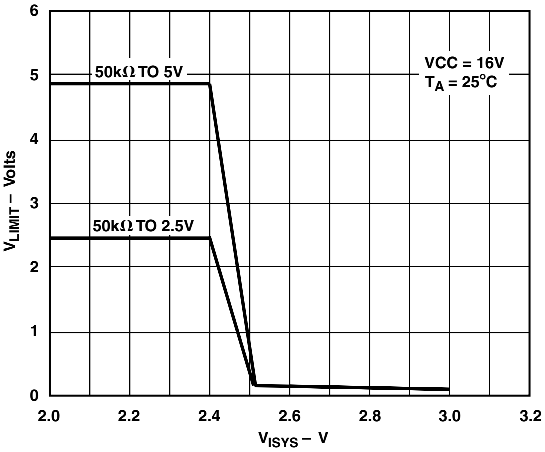
TPC 7. Supply Current vs. Driver Load Capacitance



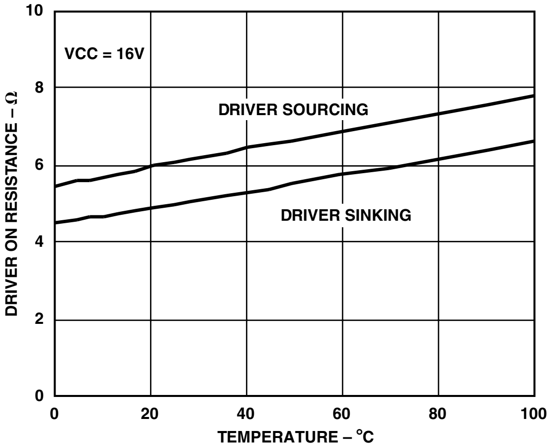
TPC 8. OFF Supply Current vs. VCC



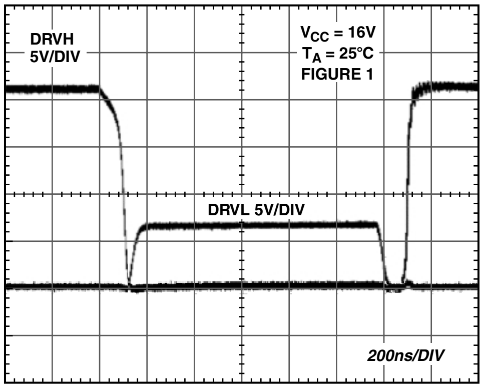
TPC 9. Oscillator Frequency vs. CT



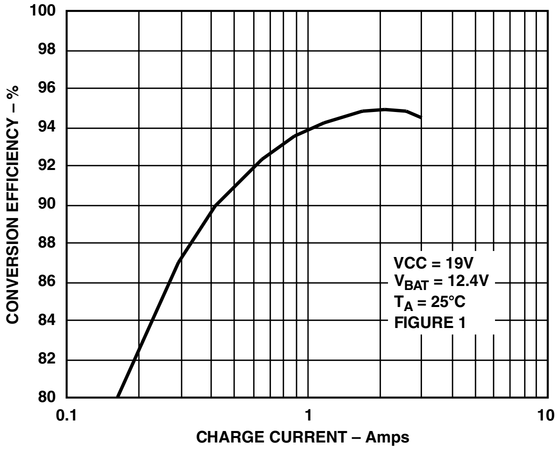
TPC 10. V_{LIMIT} vs. V_{ISYS}



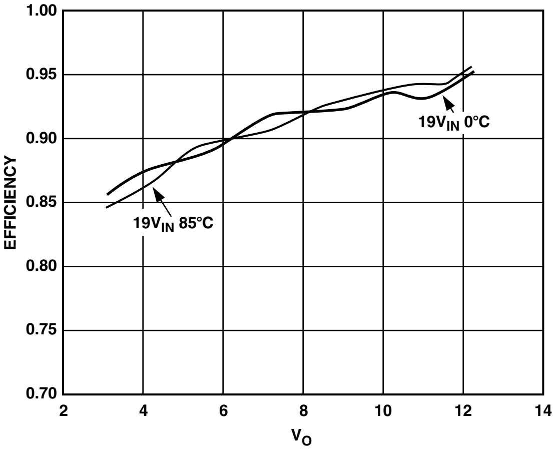
TPC 11. Driver On-Resistance vs. Temperature



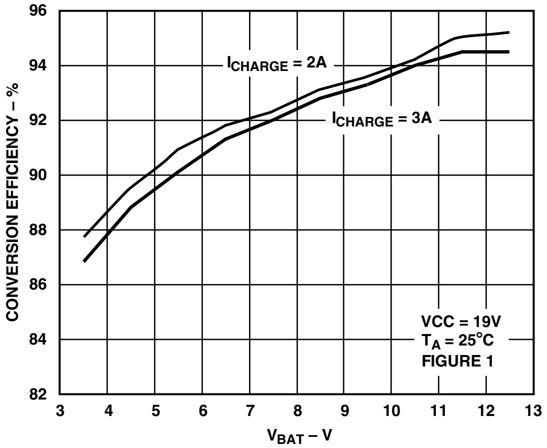
TPC 12. Driver Waveforms



TPC 13. *Conversion Efficiency vs. Charge Current*



TPC 15. *Conversion Efficiency vs. Battery Voltage at Temperatures*



TPC 14. *Conversion Efficiency vs. Battery Voltage*

THEORY OF OPERATION

The ADP3806 combines a bootstrapped synchronous switching driver with programmable current control and accurate final battery voltage control in a Constant Current, Constant Voltage (CCCV) Li-Ion battery charger. High accuracy voltage control is needed to safely charge Li-Ion batteries, which are typically specified at 4.2 V ± 1% per cell. For a typical notebook computer battery pack, three or four cells are in series giving a total voltage of 12.6 V or 16.8 V. The ADP3806 is available in three versions, a selectable 12.525 V/16.7 V output, a selectable 12.6 V/16.8 V output, and an adjustable output. The adjustable output can be programmed for a wide range of battery voltages using two external precision resistors.

Another requirement for safely charging Li-Ion batteries is accurate control of the charge current. The actual charge current depends on the number of cells in parallel within the battery pack. Typically this is in the range of 2 A to 3 A. The ADP3806 provides flexibility in programming the charge current over a wide range. An external resistor is used to sense the charge current and this voltage is compared to a DC input voltage. This programmability allows the current to be changed during charging. For example, the charge current can be reduced for trickle charging.

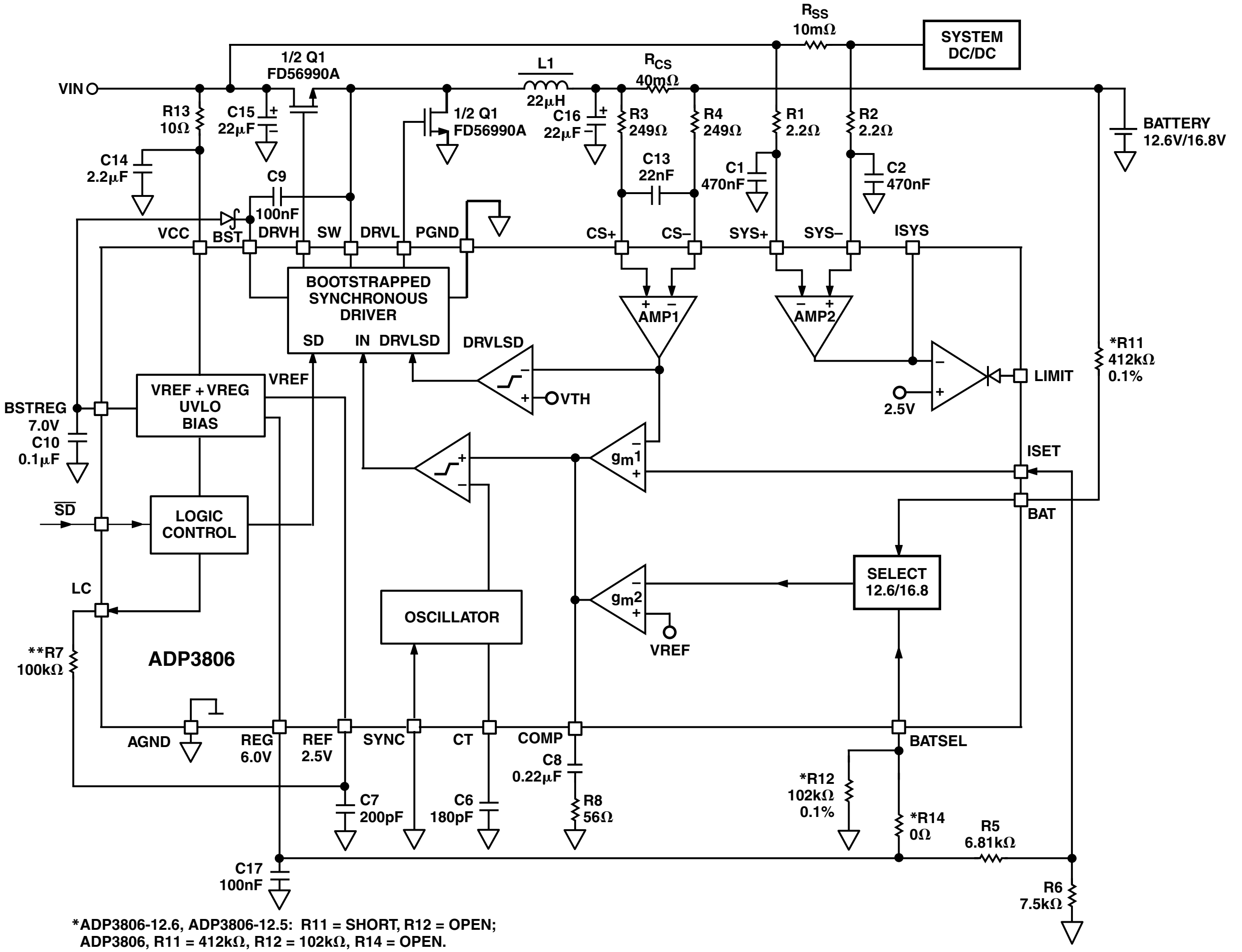
The synchronous driver provides high efficiency when charging at high currents. Efficiency is important mainly to reduce the amount of heat generated in the charger, but also to stay within the power limits of the AC adapter. With the addition of a bootstrapped high side driver, the ADP3806 drives two external power NMOS transistors for a simple, lower cost power stage.

The ADP3806 also provides an uncommitted current sense amplifier. This amplifier provides an analog output pin for monitoring the current through an external sense resistor. The amplifier can be used anywhere in the system that high side current sensing is needed.

Charge Current Control

AMP1 in Figure 1 has a differential input to amplify the voltage drop across an external sense resistor R_{CS}. The input common mode range is from ground to VCC allowing current control in short circuit and low drop-out conditions. The gain of AMP1 is internally set to 25 V/V for low voltage drop across the sense resistor. During CC mode, g_m1 forces the voltage at the output of AMP1 to be equal to the external voltage at the ISET pin. By choosing R_{CS} and V_{ISET} appropriately, a wide range of charge currents can be programmed:

$$I_{CHARGE} = \frac{V_{ISET}}{25 \times R_{CS}} \tag{1}$$



VIN
R13
10Ω
C15
22µF
1/2 Q1
FD56990A
C14
2.2µF
C9
100nF
1/2 Q1
FD56990A
L1
22µH
C16
22µF
RSS
10mΩ
SYSTEM DC/DC
RCS
40mΩ
R3
249Ω
R4
249Ω
C13
22nF
R1
2.2Ω
R2
2.2Ω
C1
470nF
C2
470nF
BATTERY
12.6V/16.8V
VCC
BST
DRVH
SW
DRVL
PGND
CS+
CS–
SYS+
SYS–
ISYS
BOOTSTRAPPED SYNCHRONOUS DRIVER
SD
IN
DRVLSD
DRVLSD
AMP1
AMP2
VTH
LIMIT
2.5V
*R11
412kΩ
0.1%
VREF
VREF + VREG UVLO BIAS
BSTREG
7.0V
C10
0.1µF
SD
LOGIC CONTROL
gm1
ISET
BAT
LC
OSCILLATOR
gm2
VREF
SELECT 12.6/16.8
**R7
100kΩ
ADP3806
AGND
REG
6.0V
REF
2.5V
SYNC
CT
COMP
C8
0.22µF
BATSEL
*R12
102kΩ
0.1%
*R14
0Ω
R5
6.81kΩ
C7
200pF
C6
180pF
R8
56Ω
C17
100nF
R6
7.5kΩ

*ADP3806-12.6, ADP3806-12.5: R11 = SHORT, R12 = OPEN;
ADP3806, R11 = 412kΩ, R12 = 102kΩ, R14 = OPEN.
**R7, OPEN IF LC FUNCTION IS NOT USED.

Figure 1. Typical Application

Typical values of R_{CS} are in the range from 25 mΩ to 50 mΩ, and the input range of ISET is from 0 V to 4 V. If, for example, a 3 A charger is required, R_{CS} could be set to 40 mΩ and V_{ISET} = 3 V. The power dissipation in R_{CS} should be kept below 500 mW. In this example, the power is a maximum of 360 mW. Once R_{CS} has been chosen, the charge current can be adjusted during operation with V_{ISET}. Lowering V_{ISET} to 125 mV gives a charge current of 125 mA for trickle charging. Components R3, R4, and C13 provide high-frequency filtering for the current sense signal.

Final Battery Voltage Control

As the battery approaches its final voltage, the ADP3806 switches from CC mode to CV mode. The change is achieved by the common output node of g_m1 and g_m2. Only one of the two outputs controls the voltage at the COMP pin. Both amplifiers can only pull down on COMP, such that when either amplifier has a positive differential input voltage, its output is not active. For example, when the battery voltage, V_{BAT}, is low, g_m2 does not control V_{COMP}. When the battery voltage reaches the desired final voltage, g_m2 takes control of the loop, and the charge current is reduced.

Amplifier g_m2 compares the battery voltage to the internal reference voltage of 2.5 V. In the case of the ADP3806-12.5 and ADP3806-12.6, an internal resistor divider sets the selectable final battery voltage.

When BATSEL is high, the final battery voltage is set to three cells (12.6 V or 12.525 V). BATSEL can be tied to REG for this state. When BATSEL is tied to ground, VBAT equals four cells (16.8 V or 16.7 V). BATSEL has a 2 μA pull-up current as a fail-safe to select three cells when it is left open.

The reference and internal resistor divider are referenced to the AGND pin, which should be connected close to the negative terminal of the battery to minimize sensing errors.

In contrast, the ADP3806 requires external, precision resistors. The divider ratio should be set to divide the desired final voltage down to 2.5 V at the BAT pin:

$$\frac{R11}{R12} = \frac{V_{BATTERY}}{2.5\,V} - 1 \qquad (2)$$

These resistors should have a parallel impedance of approximately 80 kΩ to minimize bias current errors. When the ADP3806 is in shutdown, an internal switch disconnects the BAT pin as shown in Figure 2. This disconnects the resistor, R11 from the battery and minimizes leakage. The resistance of the internal switch is less than 200 Ω.

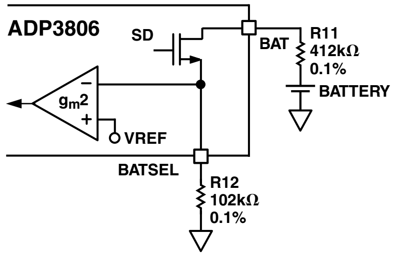


Figure 2. Battery Sense Disconnect Circuit

Oscillator and PWM

The oscillator generates a triangle waveform between 1 V and 2.5 V, which is compared to the voltage at the COMP pin, setting the duty cycle of the driver stage. When V_{COMP} is below 1 V, the duty cycle is zero. Above 2.5 V, the duty cycle reaches its maximum.

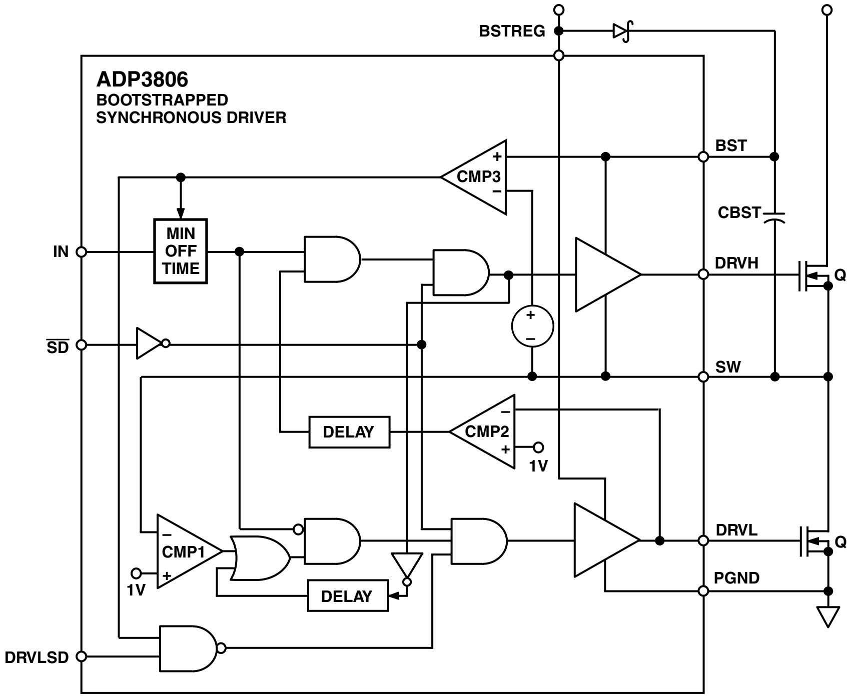


Figure 3. Bootstrapped Synchronous Driver

The oscillator frequency is set by the external capacitor at the CT pin and the internal current source of 150 μA according to the following formula:

$$f_{OSC} = \frac{150\ \mu A}{2.2 \times C_T \times 1.5\ V} \tag{3}$$

A 180 pF capacitor sets the frequency to 250 kHz. The frequency can also be synchronized to an external oscillator by applying a square wave input on SYNC. The SYNC function is designed to allow only increases in the oscillator frequency. The f_{SYNC} should be no more than 20% higher than f_{OSC}. The duty cycle of the SYNC input is not important and can be anywhere between 5% and 95%.

7 V Bootstrap Regulator

The driver stage is powered by the internal 7 V bootstrap regulator, which is available at the BSTREG pin. Because the switching currents are supplied by this regulator, decoupling must be added. A 0.1 μF capacitor should be placed close to the ADP3806, with the ground side connected close to the power ground pin, PGND. This supply is not recommended for use externally due to high switching noise.

Bootstrapped Synchronous Driver

The PWM comparator controls the state of the synchronous driver shown in Figure 3. A high output from the PWM comparator forces DRVH on and DRVL off. The drivers have an ON resistance of approximately 6 Ω for fast rise and fall times when driving external MOSFETs. Furthermore, the bootstrapped drive allows an external NMOS transistor for the main switch instead of a PMOS. An external boost diode should be connected between BSTREG and BST, and a boost capacitor of 0.1 μF must be added externally between BST and SW. The voltage between BST and SW is typically 6.5 V.

The DRVL pin switches between BSTREG and PGND. The 7 V output of BSTREG drives the external NMOS with high VGS to lower the ON resistance. PGND should be connected close to the source pin of the external synchronous NMOS. When DRVL is high, this turns on the lower NMOS and pulls the SW node to ground. At this point, the boost capacitor is charged up through the boost diode. When the PWM switches high, DRVL is turned off and DRVH turns on. DRVH switches between BST and SW. When DRVH is on, the SW pin is pulled up to the input supply (typically 16 V), and BST rises above this voltage by approximately 6.5 V.

Overlap protection is included in the driver to ensure that both external MOSFETs are not on at the same time. When DRVH turns off the upper MOSFET, the SW node goes low due to the inductor current. The ADP3806 monitors the SW voltage, and DRVL goes high to turn on the lower MOSFET when SW goes below 1 V. When DRVL turns off, an internal timer adds a delay of 50 ns before turning DRVH on.

When the charge current is low, the DRVLSD comparator signals the driver to turn off the low side MOSFET and DRVL is held low. As shown in Figure 1, the DRVLSD comparator looks at the output of AMP1. The DRVLSD threshold is set to 1.2 V, corresponding to 48 mV differential voltage between the CS pins. The driver stage monitors the voltage across the BST cap with CMP3. When this voltage is less than 4 V, CMP3 forces a minimum offtime of 200 ns. This ensures that the BST cap is charged even during DRVLSD. However, because a minimum off time is only forced when needed, the maximum duty cycle is greater than 99%.

2.5 V Precision Reference

The voltage at the BAT pin is compared to an internal precision, low temperature drift reference of 2.5 V. The reference is available externally at the REF pin. This pin should be bypassed with a 100 pF capacitor to the analog ground pin, AGND. The reference can be used as a precision voltage externally. However, the current draw should not be greater than 100 μA, and noisy, switching type loads should not be connected.

6 V Regulator

The 6 V regulator supplies power to most of the analog circuitry on the ADP3806. This regulator should be bypassed to AGND with a 0.1 μF capacitor. This reference has a 3 mA source capability to power external loads if needed.

LC

The ADP3806 provides a low current (LC) logic output to signal when the current sense voltage (V_{CS}) is below a fixed threshold and the battery voltage is greater than 95%. LC is an open drain output that is pulled low when V_{CS} is above the threshold. When the low current threshold condition is reached, LC is pulled high by an external resistor to REF or another appropriate pull-up voltage. To determine when LC goes low, an internal comparator senses when the current falls below 12.5% of full scale (20 mV across the CS pins). The comparator has hysteresis to prevent oscillation around the trip point.

To prevent false triggering (such as during soft-start), the comparator is only enabled when the battery voltage is within 5% of its final voltage. As the battery is charging up, the comparator will not go low even if the current falls below 12.5% as long as the battery voltage is below 95% of full scale. Once the battery has risen above 95%, the comparator is enabled. This pin can be used to indicate the end of the charge process.

System Current Sense

An uncommitted differential amplifier is provided for additional high side current sensing. This amplifier, AMP2, has a fixed gain of 50 V/V from the SYS+ and SYS– pins to the analog output at ISYS. ISYS has a 1 mA source capability to drive an external load. The common-mode range of the input pins is from 4 V to VCC. This amplifier is the only part of the ADP3806 that remains active during shutdown. The power to this block is derived from the bias current on the SYS+ and SYS– pins.

A separate comparator at the LIMIT pin signals when the voltage on the ISYS pin exceeds 2.5 V typically. The internal comparator has an open drain output, which produces the function shown in the TPC 10 graph of V_{LIMIT} versus V_{ISYS}. The LIMIT pin should be externally pulled up to 5 V, 2.5 V, or other voltage as needed through a resistor. This graph was taken with a 50 kΩ pull-up resistor to 5 V and to 2.5 V. When ISYS is below 2.4 V, the LIMIT pin has high output impedance. The open drain output is capable of sinking 700 μA when the threshold is exceeded. This comparator is turned off during shutdown to conserve power.

Shutdown

A high impedance CMOS logic input is provided to turn off the ADP3806. When the voltage on $\overline{SD}$ is less than 0.8 V, the ADP3806 is placed in low power shutdown. With the exception of the system current sense amplifier, AMP2, all other circuitry is turned off. The reference and regulators are pulled to ground during shutdown and all switching is stopped. During this state, the supply current is less than 5 μA. Also, the BAT, CS+, CS–, and SW pins go to high impedance to minimize current drain from the battery.

UVLO

Under-Voltage Lock-Out, UVLO, is included in the ADP3806 to ensure proper start-up. As VCC rises above 1 V, the reference and regulators will track VCC until they reach their final voltages. However, the rest of the circuitry is held off by the UVLO comparator. The UVLO comparator monitors both regulators to ensure that they are above 5 V before turning on the main charger circuitry. This occurs when VCC reaches 6 V. Monitoring the regulator outputs makes sure that the charger circuitry and driver stage have sufficient voltage to operate normally. The UVLO comparator includes 300 mV of hysteresis to prevent oscillations near the threshold.

Startup Sequence

During a startup from either $\overline{SD}$ going high or VCC exceeding the UVLO threshold, the ADP3806 initiates a soft-start sequence. The soft-start timing is set by the compensation capacitor at the COMP pin and an internal 40 μA source. Initially, both DRVH and DRVL are held low until V_{COMP} reaches 1 V. This delay time is set by:

$$t_{DELAY} = \frac{C_{COMP} \times 1\,V}{40\ \mu A} \qquad (4)$$

For a 0.22 μF COMP capacitor, t_{DELAY} is 5 ms. After this initial delay, the duty cycle is very low and then ramps up to its final value with the same ramp rate given for t_{DELAY}. For example, if V_{IN} is 16 V and the battery is 10 V when charging is started, the duty cycle will be approximately 65%, corresponding to a V_{COMP} of ~2 V. The time for the duty cycle to ramp from 0% at V_{COMP} = 1 V to 65% at V_{COMP} = 2 V is approximately 5 ms. Because the charge current is equal to zero at first, DRVLSD is active and DRVL will not turn on. However, if the BST cap is discharged, DRVL will be forced on for a minimum ON time of 200 ns each clock period until the BST cap is charged to greater than 4 V. Typically the BST cap is charged in 5 to 10 clock cycles.

Loop Feed Forward

As the startup sequence discussion shows, the response time at COMP is slowed by the large compensation capacitor. To speed up the response, two comparators can quickly feed forward around the normal control loop and pull the COMP node down to limit any over shoot in either short circuit or overvoltage conditions. The overvoltage comparator has a trip point set to 20% higher than the final battery voltage. The overcurrent comparator threshold is set to 180 mV across the CS pins, which is 15% above the maximum programmable threshold. When these comparators are tripped, a normal soft-start sequence is initiated. The overvoltage comparator is valuable when the battery is removed during charging. In this case, the current in the inductor causes the output voltage to spike up, and the comparator limits the maximum voltage. Neither of these comparators affect the loop under normal charging conditions.

APPLICATION INFORMATION

Design Procedure

Please refer to Figure 1, the typical application circuit, for the following description. The design follows that of a buck converter. With Li-Ion cells it is important to have a regulator with accurate output voltage control.

Battery Voltage Settings: The ADP3806 has three options for voltage selection:

1. 12.525 V/16.7 V as selectable fixed voltages.
2. 12.6 V/16.8 V as selectable fixed voltages.
3. Adjustable.

When using the fixed versions, R11 should be a short or 0 Ω wire jumper and R12 should be an open circuit. When using the adjustable version, the following equation gives the ratio of the two resistors:

$$\frac{R11}{R12} = \left(\frac{V_{BAT}}{2.5}\right) - 1 \qquad (5)$$

Often 0.1% resistors are required to maintain the overall accuracy budget in the design.

***Inductor Selection*:** Usually the inductor is chosen based on the assumption that the inductor ripple current is ±15% of the maximum output dc current at maximum input voltage. As long as the inductor used has a value close to this, the system should work fine. The final choice affects the trade-offs between cost, size, and efficiency. For example, the lower the inductance, the size is smaller but ripple current is higher. This situation, if taken too far, will lead to higher ac losses in the core and the windings. Conversely, a higher inductance results in lower ripple current and smaller output filter capacitors, but the transient response will be slower. With these considerations the required inductance can be found from:

$$L_1 = \frac{V_{IN,\,MAX} - V_{BAT}}{\Delta I} \times D_{MIN} \times T_S \qquad (6)$$

where the maximum input voltage $V_{IN,\,MAX}$ is used with the minimum duty ratio D_{MIN}. The duty ratio is defined as the ratio of the output voltage to the input voltage, V_{BAT}/V_{IN}. The ripple current is found from:

$$\Delta I = 0.3 \times I_{BAT,\,MAX} \qquad (7)$$

the maximum peak-to-peak ripple is 30%, that is 0.3, and maximum battery current, $I_{BAT,\,MAX}$ is used.

For example, with $V_{IN,\,MAX}$ = 19 V, V_{BAT} = 12.6 V, $I_{BAT,\,MAX}$ = 3A, and T_S = 4 μs, the value of L_1 is calculated as 18.9 μH. Choosing the closest standard value gives L_1 = 22 μH.

***Output Capacitor Selection*:** An output capacitor is needed in the charger circuit to absorb the switching frequency ripple current and smooth the output voltage. The RMS value of the output ripple current is given by:

$$I_{RMS} = \frac{V_{IN,\,MAX}}{fL_1\sqrt{12}} D\left(1 - D\right) \qquad (8)$$

The maximum value occurs when the duty cycle is 0.5. Thus:

$$I_{RMS\_MAX} = 0.072\frac{V_{IN,\,MAX}}{fL_1} \qquad (9)$$

For an input voltage of 19 V and a 22 µH inductance, the maximum RMS current is 0.26A. A typical 10 µF or 22 µF ceramic capacitor is a good choice to absorb this current.

***Input Capacitor Ripple*:** As is the case with a normal buck converter, the pulse current at the input has a high rms component. Therefore, since the input capacitor has to absorb this current ripple, it must have an appropriate rms current rating. The maximum input rms current is given by:

$$I_{RMS} = \frac{P_{BAT}}{\eta \times D \times V_{IN}} \times \frac{\sqrt{D(1-D)}}{D} \qquad (10)$$

where η is the estimated converter efficiency (approximately 90%, 0.9) and P_{BAT} is the maximum battery power consumed. This is a worst-case calculation and, depending on total charge time, the calculated number could be relaxed. Consult the capacitor manufacturer for further technical information.

***Decoupling the VCC Pin*:** It is a good idea to use an RC filter (R13 and C14) from the input voltage to the IC both to filter out switching noise and to supply bypass to the chip. During layout, this capacitor should be placed as close to the IC as possible. Values between 0.1 µF and 2.2 µF are recommended.

***Current-Sense Filtering*:** During normal circuit operation the current-sense signals can have high-frequency transients that need filtering to ensure proper operation. In the case of the CS+ and CS– inputs, the resistors (R3 and R4) are set to 249 Ω while the filter capacitor (C13) value is 22 nF. For the system current sense circuits, common mode filtering from SYS+ and SYS– to ground is needed. 470 nF ceramic capacitors (C1, C2) with 2.2 Ω resistors (R1, R2) will often due. These time constants can be adjusted in the laboratory if required, but represent a good starting point.

***MOSFET Selection*:** One of the features of the ADP3806 is that it allows use of a high-side NMOS switch instead of a more costly PMOS device. The converter also uses synchronous rectification for optimal efficiency. In order to use a high-side NMOS, an internal bootstrap regulator automatically generates a 7 V supply across C9.

Maximum output current determines the $R_{DS(ON)}$ requirement for the two power MOSFETs. When the ADP3806 is operating in continuous mode, the simplifying assumption can be made that one of the two MOSFETs is always conducting the load current. The power dissipation for each MOSFET is given by:

Upper MOS

$$P_{DISS} = R_{DS(ON)} \times (I_{BAT} \times \sqrt{D})^2 + V_{IN} \times I_{BAT} \times \sqrt{D} \times T_{SW} \times f \qquad (11)$$

Lower MOS

$$P_{DISS} = R_{DS(ON)} \times (I_{BAT} \times \sqrt{1-D})^2 + V_{IN} \times I_{BAT} \times \sqrt{1-D} \times T_{SW} \times f \qquad (12)$$

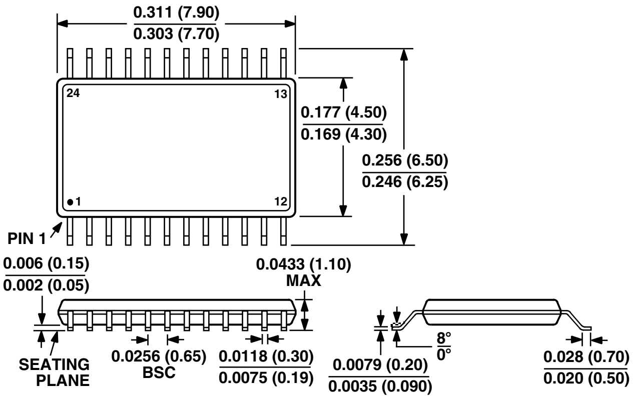
Where f is the switching frequency and T_{SW} is the switch transition time, usually 10 ns. The first term accounts for conduction losses while the second term estimates switching losses. Using these equations and the manufacturer's data sheets, the proper device can be selected.

A Schottky diode D1 in parallel with Q2 conducts only during dead time between the two power MOSFETs. D1's purpose is to prevent the body-diode of the lower N-channel MOSFET from turning on which could cost as much as 1% in efficiency. One option is to use a combined MOSFET with the Schottky diode in a single package–these integrated packages often work better in practice. Examples are the IRF7807D2 and the Si4832.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

24-Lead Thin Shrink SO Package (TSSOP) (RU-24)



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