320 mA Switched Capacitor Voltage Doubler

ADP3610

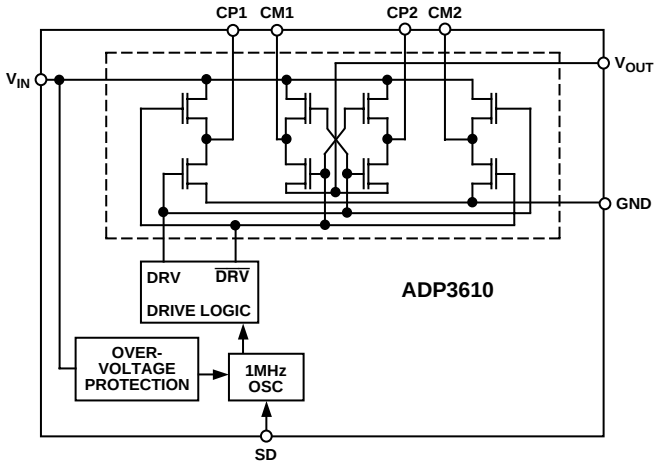
FEATURES

Push-Pull Charge Pump Doubler Reduces Output Ripple
+3.0 V to +3.6 V Operation
V_{OUT} > +5.4 V @ 320 mA Maximum Load
Output Impedance, $R_{TOTAL} \leq 1.66\ \Omega$
Shutdown Capability
Overvoltage Protection: V_{IN} > +4 V
Operating Temperature Range: –20°C to +85°C
Thermally Enhanced 16-Lead TSSOP Package

APPLICATIONS

High Current Doublers
LCD Panels
Cellular Phones
Inductorless Boost Converters

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADP3610 is a push-pull switched-capacitor converter voltage doubler. The term "push-pull" refers to two charge pumps working in parallel and in opposing phase to deliver charge to support the output voltage. When one capacitor is pumping charge to the output, the other is recharging. This technique minimizes voltage loss and output voltage ripple.

The converter accommodates input voltages from +3 V to +3.6 V and can provide 320 mA using 2.2 µF MLCC pump capacitors. Converter operation can be enabled or disabled simply by an input signal. The package is enhanced with Analog Devices' proprietary Thermal Coastline feature, which allows up to 980 mW of power dissipation at room temperature. The exceptionally thin TSSOP-16 package and the requirement of only capacitors (no inductors) to support the converter operation allows slim designs, e.g., for TFT or LCD display panels.

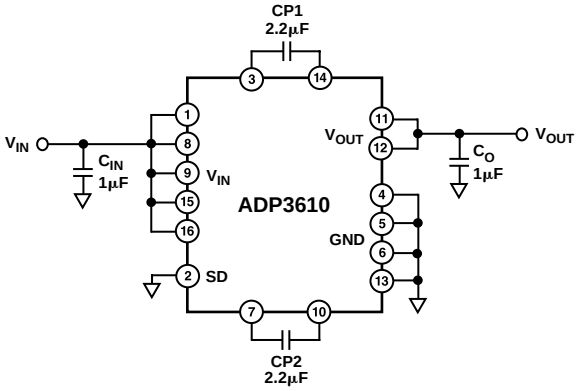


Figure 1. Typical Application Circuit

REV. A

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ADP3610–SPECIFICATIONS ($-20°C \le T_A \le +85°C$, $V_{IN} = +3.3$ V, CP1 = CP2 = 2.2 µF, C_O = 1 µF, SD = GND, unless otherwise noted)[1, 2, 3]

Parameter	Symbol	Condition	Min	Typ	Max	Units
OPERATING SUPPLY RANGE	V_{IN}		3.0		3.6	V
QUIESCENT CURRENT	I_Q	SD = V_{IN}		0.3		µA
		SD = GND, I_L = 0 mA		8.6	10	mA
INPUT OVP THRESHOLD	V_{OVP}			4		V
TOTAL OUTPUT IMPEDANCE	R_{TOTAL}[4]	I_O = 0 mA to 320 mA		1	1.66	Ω
OUTPUT VOLTAGE	V_O	I_O = 240 mA, V_{IN} = +3 V	5.6	5.75		V
		I_O = 320 mA, V_{IN} = +3 V	5.47	5.65		V
		I_O = 240 mA, V_{IN} = +3.3 V	6.2	6.35		V
		I_O = 320 mA, V_{IN} = +3.3 V	6.07	6.27		V
OUTPUT CURRENT	I_O		320			mA
OUTPUT SWITCHING FREQUENCY	f_{SW}		400	560	650	kHz
SD INPUT						
Logic Input High	V_{IH}		2.0			V
Input Current	I_{IH}			0.1		µA
Logic Input Low	V_{IL}				0.8	V
Input Current	I_{IL}			0.1		µA

NOTES
[1]Capacitors in the test circuit are multilayer ceramic type.
[2]All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods.
[3]Junction temperature is influenced by ambient temperature, device mounting and heatsinking, and power dissipation which is a function of I/O voltages and load.
[4]R_{TOTAL} includes the switch resistance, and the equivalent series resistance of the 2.2 µF (X7R) MLCC pump capacitors.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Input Voltage (V+ to GND) . . . . . +4.0 V
Output Short Circuit to GND (<1 A) . . . . . 60 sec
Power Dissipation
θ_{JA}[2] . . . . . +102°C/W
Operating Ambient Temperature Range . . . . –20°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature Range (Soldering 10 sec) . . . . . +300°C
Vapor Phase (60 sec) . . . . . +215°C
Infrared (15 sec) . . . . . +220°C

NOTES
[1]This is a stress rating only; operation beyond these limits can cause the device to be permanently damaged.
[2]θ_{JA} is specified for worst case conditions with device soldered on a FR-4, 1 oz. copper clad four layer circuit board.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADP3610ARU	–20°C to +85°C	Thin Shrink Small Outline Package (TSSOP-16)	RU-16

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADP3610 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

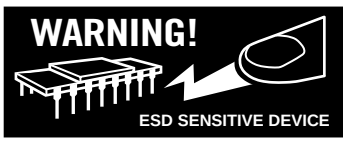


Table I. Other Members of ADP36xx Family[1]

Model	Output Current	Package Options[2]	Comments
ADP3603	50 mA	SO-8	Nom –3 V ± 3% Inverter
ADP3604	120 mA	SO-8	Nom –3 V ± 3% Inverter
ADP3605-3	120 mA	SO-8, TSSOP-14	Nom –3 V ± 5% Inverter
ADP3607-5	50 mA	SO-8	Nom 5 V ± 5% Boost
ADP3607	50 mA	SO-8	Adjustable ± 5% Boost

NOTES
[1]See individual data sheets for detailed ordering information.
[2]SO = Small Outline; TSSOP = Thin Shrink Small Outline Package.

Table II. Alternative Capacitor Technologies

Type	Life	High Freq	Temp	Size	Cost
Aluminum Electrolytic Capacitor	Fair	Fair	Fair	Small	Low
Multilayer Ceramic Capacitor	Long	Good	Poor*	Fair	High
Solid Tantalum Capacitor	Above Avg	Avg	Avg	Avg	Avg
OS-CON Capacitor	Above Avg	Good	Good	Good	Avg

*Refer to capacitor manufacturer's data sheet for operation below 0°C.

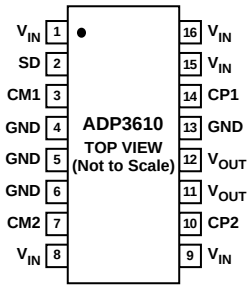
Table III. Recommended Capacitor Manufacturers

Manufacturer	Capacitor	Capacitor Type
Sprague	672D, 673D, 674D, 678D	Aluminum Electrolytic
Sprague	675D, 173D, 199D	Tantalum
Nichicon	PF and PL	Aluminum Electrolytic
Mallory	TDC and TDL	Tantalum
TOKIN	MLCC	Multilayer Ceramic
MuRata	GRM	Multilayer Ceramic

PIN FUNCTION DESCRIPTIONS

Pin	Name	Function
1, 8, 9, 15, 16	V_{IN}	Input Voltage. **Pins 1, 8, 9, 15 and 16 must be connected together for proper operation.**
2	SD	Shutdown. A logic low input allows normal operation. A logic high input shuts the device off.
3	CM1	Pump Capacitor C1 Negative Input
4, 5, 6, 13	GND	Ground. **Pins 4, 5, 6, and 13 must be connected together for proper operation.**
7	CM2	Pump Capacitor C2 Negative Input
10	CP2	Pump Capacitor C2 Positive Input
11, 12	V_{OUT}	Output Voltage. **Pins 11 and 12 must be connected together for proper operation**.
14	CP1	Pump Capacitor C1 Positive Input

PIN CONFIGURATION



ADP3610–Typical Performance Characteristics

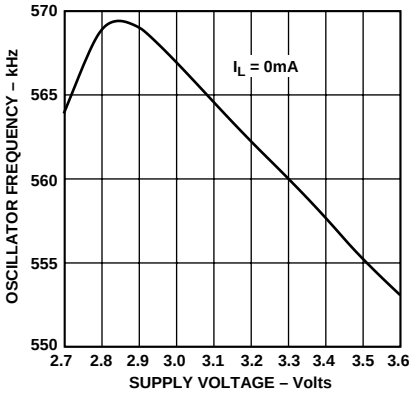


Figure 2. Oscillator Frequency vs. Supply Voltage

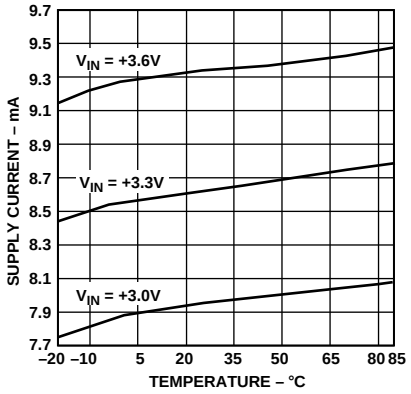


Figure 3. Supply Current vs. Temperature

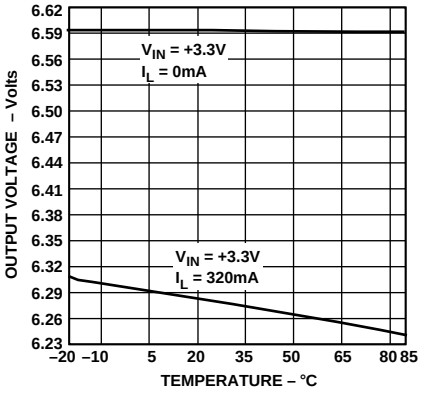


Figure 4. Output Voltage vs. Temperature, V_{IN} = +3.3 V

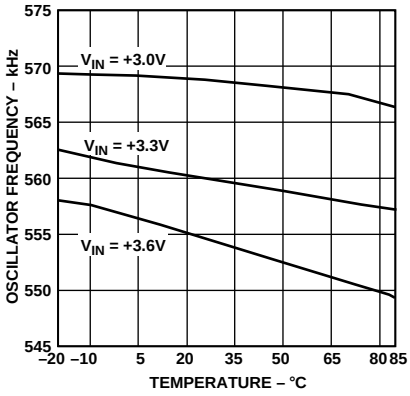


Figure 5. Oscillator Frequency vs. Temperature

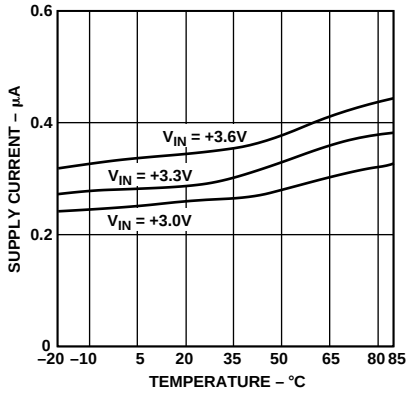


Figure 6. Supply Current in Shutdown Mode vs. Temperature

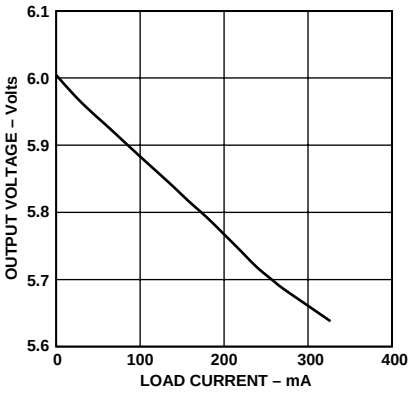


Figure 7. Output Voltage vs. Load Current for V_{IN} = +3.0 V

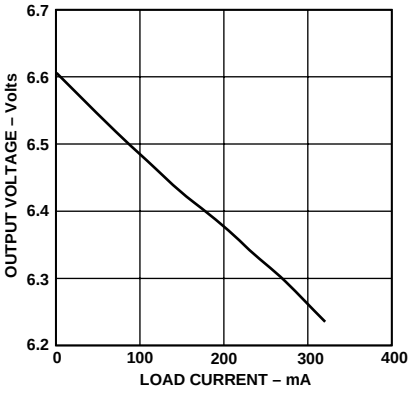


Figure 8. Output Voltage vs. Load Current for V_{IN} = +3.3 V

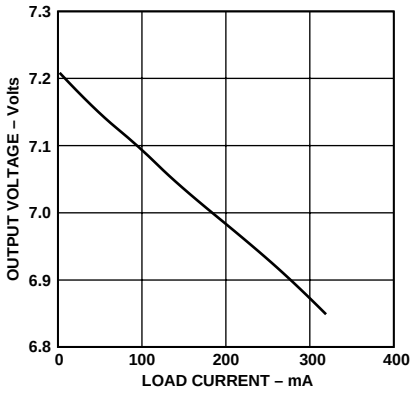


Figure 9. Output Voltage vs. Load Current for V_{IN} = +3.6 V

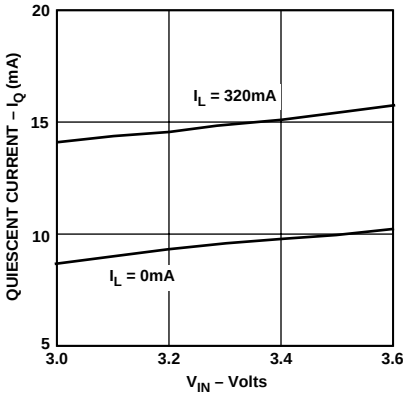


Figure 10. Quiescent Current vs. Input Voltage

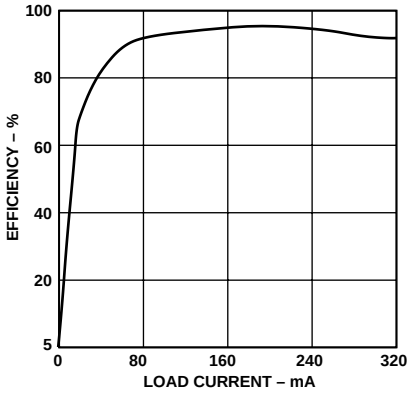


Figure 11. Efficiency vs. Load Current, V_{IN} = +3.3 V

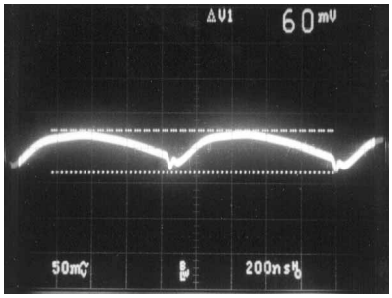


Figure 12. Output Voltage Ripple (I_O = 320 mA, CP1 = CP2 = 2.2 μF, C_O = 1 μF)

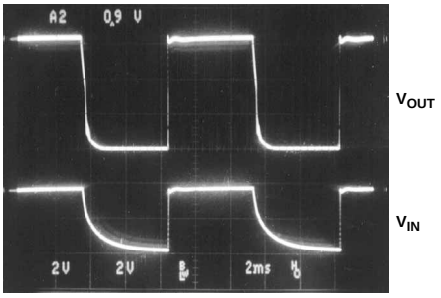


Figure 13. Start-Up Under Full Load (V_{IN} = +3.6 V, I_O = 320 mA)

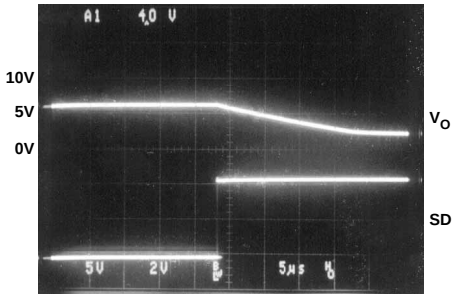


Figure 14. Shutdown at Full Load (V_{IN} = +3.3 V, I_O = 320 mA)

THEORY OF OPERATION

The ADP3610 is an unregulated switched capacitor voltage doubler that provides an output voltage greater than 5.4 V from a +3.0 V to +3.6 V input. The unique push-pull voltage doubling architecture allows it to deliver a maximum of 320 mA output current. A typical application circuit, as shown in Figure 20, requires five small external capacitors. The ADP3610 has an internal 1 MHz oscillator that is divided by two and used to generate two nonoverlapping phase clocks.

The basic principle behind a conventional switched capacitor voltage doubler is shown in Figure 15. During phase one, S1 and S2 are ON, charging the pump capacitor to the input voltage. In phase two, switches S1 and S2 are turned OFF and S3 and S4 are turned ON. During phase two, the pump capacitor is placed in series with the input voltage, thereby charging the output capacitor to the sum of input voltage and pump capacitor voltage, resulting in voltage doubling at the output terminal.

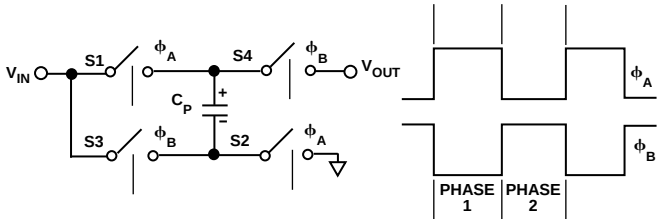


Figure 15. Conventional Voltage Doubler Configuration

The ADP3610 has two sets of switched capacitor voltage doublers connected in parallel delivering charge to the output as shown in Figure 16.

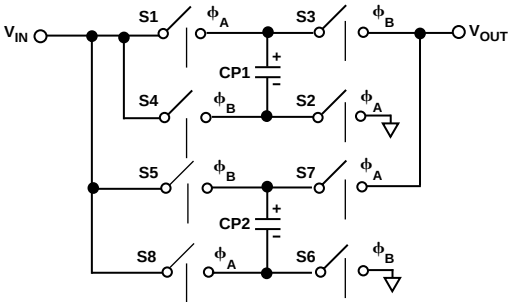


Figure 16. Switch Configuration Charging the Pump Capacitor

The two voltage doublers run in opposite phases, i.e., when one pump capacitor is being charged, the other is charging the output, as shown in Figure 17. In this architecture, one of the pump capacitors is always delivering charge to the output. As a result, output ripple is at a frequency that is double the switching frequency. This allows the use of a smaller output capacitor compared to a conventional voltage doubler.

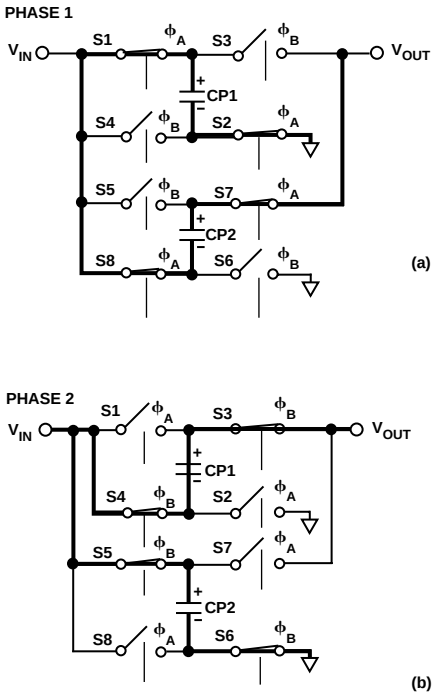


Figure 17. (a) Phase 1 "Push" Charging (b) Phase 2 "Pull" Charging

Overvoltage Protection

The input voltage is scaled with a resistor network and compared to the bandgap reference voltage of 1.25 V by a 50 mV hysteresis comparator. When the input voltage exceeds 4.0 V, the overvoltage protection signal stops the oscillator.

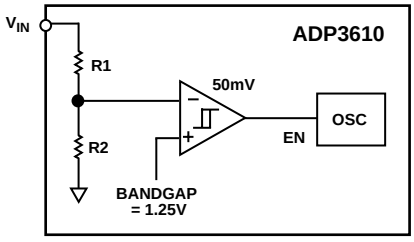


Figure 18. Overvoltage Protection

Shutdown Mode

The ADP3610's output can be disabled by pulling the SD pin high to a TTL/CMOS logic compatible level which will stop the internal oscillator. In shutdown mode, all analog circuitry including overvoltage protection is shut off, thereby reducing the quiescent current to 10 μA typical. Applying a digital low level or tying the SD pin to ground will turn on the output. If the shutdown feature is not used, SD pin should be tied to the ground pin. The output voltage in shutdown mode is approximately V_{IN} – 0.6 V.

APPLICATION INFORMATION

Capacitor Selection

The ADP3610's high internal oscillator frequency permits the use of small capacitors for both the pump and the output capacitors. For a given load current, factors affecting the output voltage performance are:

- Pump (CP) and output (C_O) capacitance
- ESR of the CP and C_O

When selecting the capacitors, keep in mind that not all manufacturers guarantee capacitor ESR in the range required by the circuit. In general, the capacitor's ESR is inversely proportional to its physical size, so larger capacitance values and higher voltage ratings tend to reduce ESR. Since the ESR is also a function of the operating frequency, when selecting a capacitor, make sure its value is rated at the circuit's operating frequency. Another factor affecting capacitor performance is temperature. Figure 19 illustrates the temperature effect on various capacitors. Aluminium electrolytic capacitors lose their capacitance at low temperatures and their ESR increases considerably. Some capacitor technologies do offer improved performance over temperature; for example, certain tantalum capacitors provide good low temperature ESR but at a higher cost. Table II provides the ratings for different types of capacitor technologies to help the designer select the right capacitors for the application. The exact values of C_{IN} and C_O are not critical. However, low ESR capacitors such as solid tantalum and multilayer ceramic capacitors are recommended to minimize voltage loss at high currents. Table III shows a partial list of the recommended low ESR capacitor manufacturers.

Input Capacitor

A small 1 µF input bypass capacitor, preferably with low ESR, such as tantalum or multilayer ceramic, is recommended to reduce noise and supply transients and supply part of the peak input current drawn by the ADP3610. A large capacitor is recommended if the input supply is connected to the ADP3610 through long leads, or if the pulse current drawn by the device might affect other circuitry through supply coupling.

Output Capacitor

The output capacitor (C_O) is alternately charged to the sum of input voltage and pump capacitor voltage when CP is switched in series with C_O. The ESR of C_O introduces steps in the V_{OUT} waveform whenever the charge pump charges C_O, which tends to increase V_{OUT} ripple. Thus, ceramic or tantalum capacitors are recommended for C_O to minimize ripple on the output. Note that as the capacitor value increases beyond the point where the dominant contribution to the output ripple is due to the ESR, no significant reduction in V_{OUT} ripple is achieved by added capacitance.

Multiple smaller capacitors can be connected in parallel to yield lower ESR and potential cost savings. For lighter loads, proportionally smaller capacitors are required. To reduce high frequency noise, bypass the output with a 0.1 µF ceramic capacitor.

Pump Capacitor

The ADP3610 alternately charges CP to the input voltage when it is switched in parallel with the input supply, and then transfers charge to C_O when it is switched in series with the input and connected to the output.

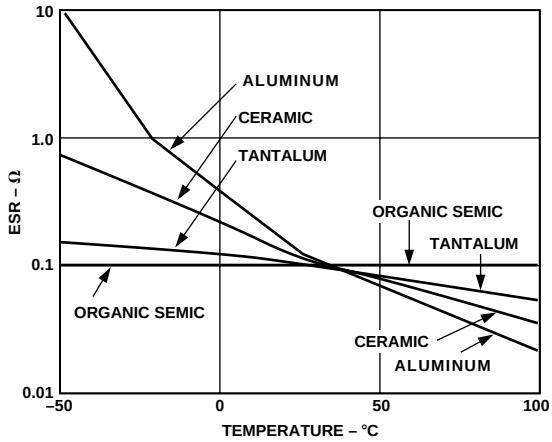


Figure 19. ESR vs. Temperature

Power Dissipation

The power dissipation of the ADP3610 circuit must be limited so the junction temperature of the device does not exceed the maximum junction temperature rating. Total power dissipation is calculated as follows:

$$P_D = (2\ V_{IN} - V_{OUT})\ I_{OUT} + V_{IN}\ (I_S)$$

Where I_{OUT} and I_S are output current and supply current, V_{IN} and V_{OUT} are input and output voltages respectively.

For example: assuming worst case conditions, V_{IN} = 3 *V*, V_{OUT} = 5.62 *V*, I_{OUT} = 320 *mA* and I_S = 14 *mA*. Calculated device power dissipation is:

$$P_D \approx (6\ V - 5.62\ V) \times 0.32 + 3 \times (0.014) = 163.6\ mW$$

The proprietary thermal coastline package used in the ADP3610 has a thermal resistance of 102°C/W. Therefore, the rise in junction temperature for this application would be:

$$T_{RISE} = 0.164\ W \times 102°C/W = 16.7°C$$

General Board Layout Guidelines

Since the ADP3610's internal switches turn on and off very fast, good PC board layout practices are critical to ensure optimal operation of the device. Improper layouts will result in poor load regulation, especially under heavy loads. Following these simple layout guidelines will improve output performance.

1. Use adequate ground and power traces or planes.
2. Use single point ground for device ground and input and output capacitor grounds.
3. Keep external components as close to the device as possible.
4. Use short traces from the input and output capacitors to the input and output pins respectively.
5. All multiple GND, V_{IN} and V_{OUT} pins must be connected together for proper operation.

Unregulated Voltage Doubler

Figure 20 shows a typical application for the ADP3610 in unregulated voltage doubling mode. The inherent limit on the output voltage for a voltage doubler is two times the input voltage. However, due to the losses in the switches and ESR of capacitors, this scaling factor is somewhat reduced. Figure 21 shows the magnitude of unregulated output voltage as the load current is increased from 0 mA to 320 mA. This gives a measure of the equivalent resistance R_{TOTAL}. R_{TOTAL} is comprised of internal switch resistance and ESR of the capacitors.

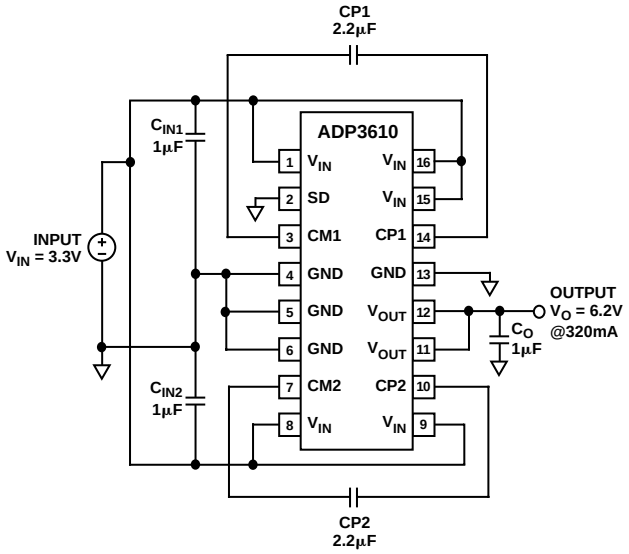


Figure 20. Unregulated Voltage Doubler

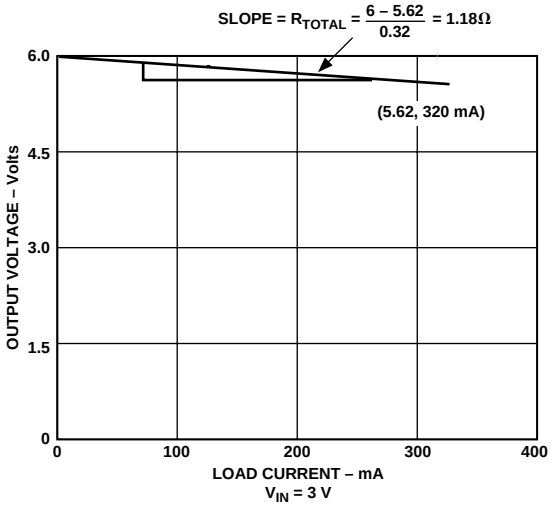


Figure 21. Load Regulation

TFT LCD System Design

The ADP3610 is very useful for applications like notebook LCD displays which require a low profile solution. Figure 22 shows a typical LCD display application. A TFT LCD display requires +5 V main voltage and +17 V and –5 V auxiliary voltages. The ADP3610 doubles the input voltage, which is then fed through a discrete linear regulator to generate +5 V. The main voltage is also fed to the ADP3605, which inverts the input voltage to generate –5 V. The CP+ node of the ADP3605 pump capacitor is fed to a diode-capacitor ladder network to quadruple the main voltage, i.e., $4 \times V_{MAIN} - 6 \times V_{DIODE} \approx 17$ V.

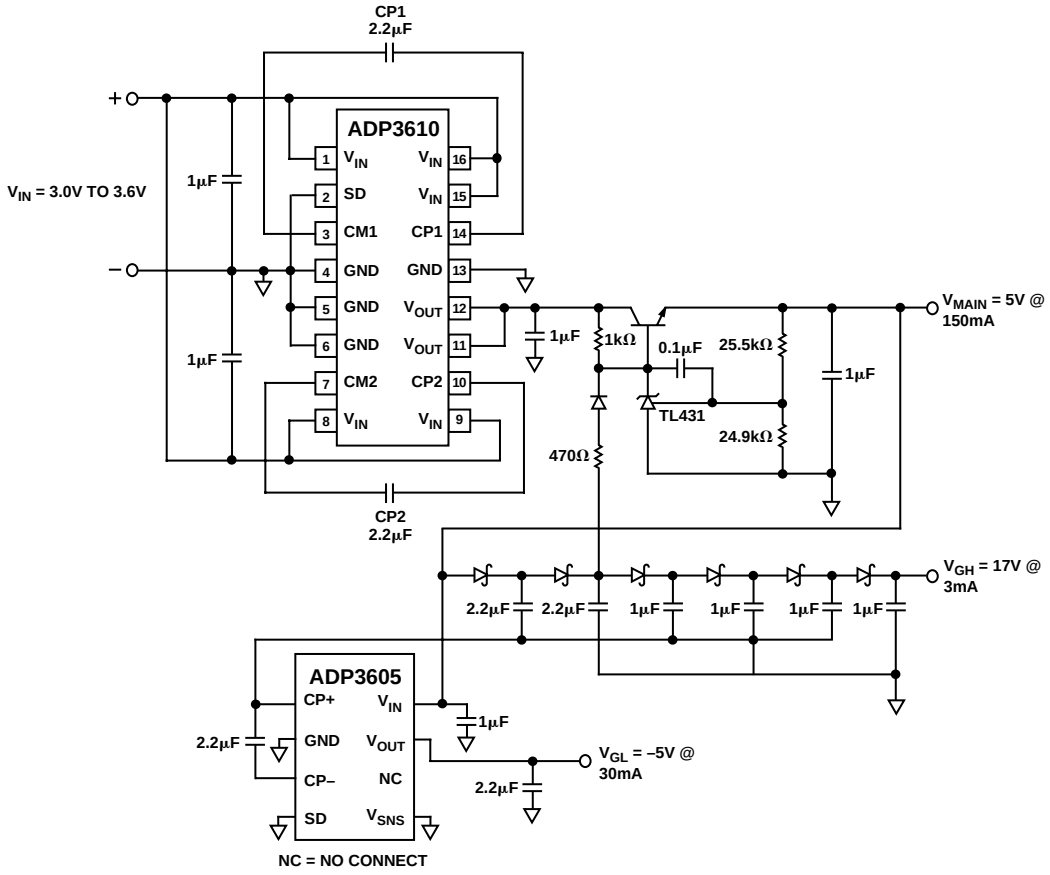
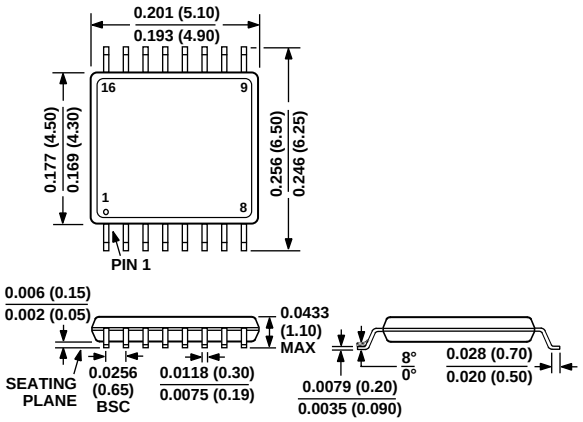


Figure 22. LCD Display Application

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-Lead Thin Shrink Small Outline Package (TSSOP)
(RU-16)



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