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+5V UPSTREAM CABLE LINE DRIVER

Preliminary Technical Data AD8328

FEATURES

Supports DOCSIS and EuroDOCSIS Standard for Reverse Path Transmission Systems
Gain Programmable in 1 dB Steps over a 59dB Range
Low Distortion at 60 dBmV Output
  –54 dBc SFDR at 21 MHz
  –52 dBc SFDR at 65 MHz
Output Noise Level @ Minimum Gain
  1.4nV/rtHz
Maintains 300Ω Output Impedance
  TX-Enable and Transmit-Disable Condition
Upper Bandwidth: 130 MHz (Full Gain Range)
5 V Supply Operation
Supports SPI Interfaces

APPLICATIONS

DOCSIS and EuroDOCSIS Cable Modems
CATV Set-Top Boxes
CATV Telephony Modems
Coaxial and Twisted Pair line driver

GENERAL DESCRIPTION

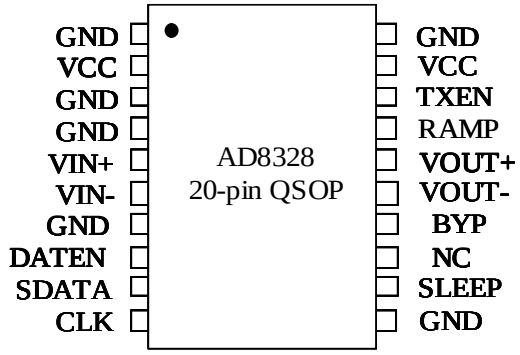
The AD8328 is a low-cost, digitally controlled, variable gain amplifier optimized for coaxial line driving applications such as cable modems that are designed to the MCNS-DOCSIS and EuroDOCSIS upstream standard. An 8-bit serial word determines the desired output gain over a 59dB range resulting in gain changes of 1dB/LSB.

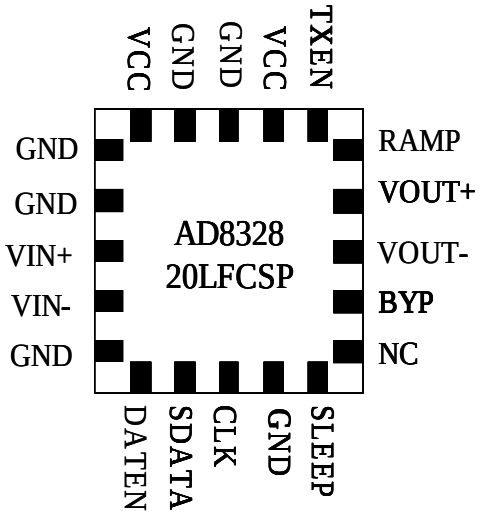
The AD8328 accepts a differential or single-ended input signal. The output is specified for driving a 75Ω load, through a 2:1 transformer.

Distortion performance of –52 dBc is achieved with an output level up to 60 dBmV at 65 MHz bandwidth over a wide temperature range.

This device has a sleep mode function that reduces the quiescent current to 2.6mA, and a full power down function which reduces power down current to 10μA.

The AD8328 is packaged in a low cost 20-lead LFCSP package and a 20-lead QSOP package. The AD8328 operates from a single 5V supply, and has an operational temperature range of –40°C to +85°C.





REV. PrA April 4, 2002

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AD8328–SPECIFICATIONS

(T_A = 25°C, V_S = 5 V, R_L = R_{IN} = 75 Ω, (using differential input) V_{IN} = 30 dBmV, V_{OUT} measured through a 2:1 transformer[1] with an insertion loss of 0.5 dB @ 10 MHz unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS					
Specified AC Input Voltage	Output = 60 dBmV, Max Gain		31		dBmV
Input Resistance	Single-Ended Input		800		Ω
	Differential Input		1600		Ω
Input Capacitance			2		pF
GAIN CONTROL INTERFACE					
Voltage Gain Range			59		dB
Maximum	Gain Code = 60 Dec		31		dB
Minimum	Gain Code = 1 Dec		–28		dB
Output Step Size					
T_A = -40°C to +85°C		0.6	1.0	1.4	dB/LSB
OUTPUT CHARACTERISTICS					
Bandwidth (–3 dB)	All Gain Codes (0-60 decimal codes)		130		MHz
Bandwidth Roll-Off	f = 65 MHz		1.0		dB
1 dB Compression Point	Max Gain, f = 10 MHz		TBD		dBm
Output Noise					
Maximum Gain	f = 10 MHz		160		nV/rtHz
Minimum Gain	f = 10 MHz		1.4		nV/rtHz
Transmit Disable	f = 10 MHz		1.4		nV/rtHz
Noise Figure	Max Gain, f = 10 MHz		TBD		
Differential Output Impedance	TX-Enable and TX-Disable		75 ± 30%[2]		Ω
OVERALL PERFORMANCE					
Second Order Harmonic Distortion	f = 21 MHz, P_{OUT} = 60 dBmV @Max Gain		–61	-55	dBc
T_A = -40°C to +85°C	f = 42 MHz, P_{OUT} = 60 dBmV @Max Gain		–61	-55	dBc
	f = 65 MHz, P_{OUT} = 60 dBmV @Max Gain		–59	-55	dBc
Third Order Harmonic Distortion	f = 21 MHz, P_{OUT} = 60 dBmV @Max Gain		–54	-50	dBc
T_A = -40°C to +85°C	f = 42 MHz, P_{OUT} = 60 dBmV @Max Gain		–52	-50	dBc
	f = 65 MHz, P_{OUT} = 60 dBmV @Max Gain		–52	-50	dBc
ACPR[3]			TBD		dBc
Isolation (Transmit Disable)	Max Gain, f = 65 MHz		–60		dBc
POWER CONTROL					
TX-Enable Settling Time	Max Gain, V_{IN} = 0		3.5		µs
TX-Disable Settling Time	Max Gain, V_{IN} = 0		3.5		µs
Output Switching Transients	Equivalent Output = 31 dBmV			7	mV p-p
	Equivalent Output = 60 dBmV			50	mV p-p
Output Settling					
Due to Gain Change	Min to Max Gain		TBD		ns
Due to Input Step Change	Max Gain, V_{IN} = 30 dBmV		TBD		ns
POWER SUPPLY					
Operating Range		4.75	5	5.25	V
Quiescent Current	Maximum Gain		125		mA
	Minimum Gain		24		mA
	Transmit Disable, TXEN = 0		2.6		mA
	Sleep Mode (Power-Down)		10		µA
OPERATING TEMPERATURE RANGE		–40		+85	°C

NOTES
[1]TOKO 458PT-1087 used for above specifications.
[2]Measured through a 2:1 transformer.
[3]V_{in} = 30dBmV, QPSK modulation, 160ksps symbol rate

LOGIC INPUTS (TTL/CMOS Compatible Logic) (DATEN, CLK, SDATA, TXEN, SLEEP, V_{CC} = 5 V: Full Temperature Range)

Parameter	Min	Typ	Max	Unit
Logic "1" Voltage	2.1		5.0	V
Logic "0" Voltage	0		0.8	V
Logic "1" Current (V_{INH} = 5 V) CLK, SDATA, DATEN	0		20	nA
Logic "0" Current (V_{INL} = 0 V) CLK, SDATA, DATEN	–600		–100	nA
Logic "1" Current (V_{INH} = 5 V) TXEN	50		190	µA
Logic "0" Current (V_{INL} = 0 V) TXEN	–250		–30	µA
Logic "1" Current (V_{INH} = 5 V) SLEEP	50		190	µA
Logic "0" Current (V_{INL} = 0 V) SLEEP	–250		–30	µA

TIMING REQUIREMENTS (Full Temperature Range, V_{CC} = 5 V, T_R = T_F = 4 ns, f_{CLK} = 8 MHz unless otherwise noted.)

Parameter	Min	Typ	Max	Unit
Clock Pulsewidth (T_{WH})	16.0			ns
Clock Period (T_C)	32.0			ns
Setup Time SDATA vs. Clock (T_{DS})	5.0			ns
Setup Time DATEN vs. Clock (T_{ES})	15.0			ns
Hold Time SDATA vs. Clock (T_{DH})	5.0			ns
Hold Time DATEN vs. Clock (T_{EH})	3.0			ns
Input Rise and Fall Times, SDATA, DATEN, Clock (T_R, T_F)			10	ns

AD8328

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage $+V_S$
- Pins TBD ..... 6 V

Input Voltages
- Pins TBD ..... ±0.5 V
- Pins TBD ..... –0.8 V to +5.5 V

Internal Power Dissipation
- LFCSP ..... TBD W
- QSOP ..... TBD W

Operating Temperature Range ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature, Soldering 60 seconds ..... 300°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description
AD8328ACP	–40°C to +85°C	20-Lead LFCSP
AD8328ACP-REEL	–40°C to +85°C	20-Lead LFCSP
AD8328ARQ	–40°C to +85°C	20-Lead QSOP
AD8328ARQ-REEL	–40°C to +85°C	20-Lead QSOP
AD8328-EVAL		Evaluation Board

*Thermal Resistance measured on SEMI standard 4-layer board.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8325 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTIONS (QSOP-20 Package)

Pin No.	Mnemonic	Description
8	DATEN	Data Enable Low Input. This port controls the 8-bit parallel data latch and shift register. A Logic 0-to-1 transition transfers the latched data to the attenuator core (updates the gain) and simultaneously inhibits serial data transfer into the register. A 1-to-0 transition inhibits the data latch (holds the previous gain state) and simultaneously enables the register for serial data load.
9	SDATA	Serial Data Input. This digital input allows for an 8-bit serial (gain) word to be loaded into the internal register with the MSB (Most Significant Bit) first.
10	CLK	Clock Input. The clock port controls the serial attenuator data transfer rate to the 8-bit master-slave register. A Logic 0-to-1 transition latches the data bit and a 1-to-0 transfers the data bit to the slave. This requires the input serial data word to be valid at or before this clock transition.
1, 3, 4, 7, 11, 20	GND	Common External Ground Reference.
2, 19	V_{CC}	Common Positive External Supply Voltage. A 0.1 µF capacitor must decouple each pin.
18	TXEN	Logic “0” disables forward transmission. Logic “1” enables forward transmission.
12	SLEEP	Low Power Sleep Mode. In the Sleep mode, the AD8328’s supply current is reduced to 1 µA. A Logic “0” powers down the part (High Z_{OUT} State) and a Logic “1” powers up the part.
15	VOUT–	Negative Output Signal.
16	VOUT+	Positive Output Signal.
14	BYP	Internal Bypass. This pin must be externally ac-coupled (0.1 µF cap).
17	RAMP	This is the external RAMP capacitor (OPTIONAL)
5	V_{IN+}	Noninverting Input. DC-biased to approximately $V_{CC}/2$. Should be ac-coupled with a 0.1 µF capacitor.
6	$V_{IN–}$	Inverting Input. DC-biased to approximately $V_{CC}/2$.