Dual MOSFET Driver with Bootstrapping

ADP3415

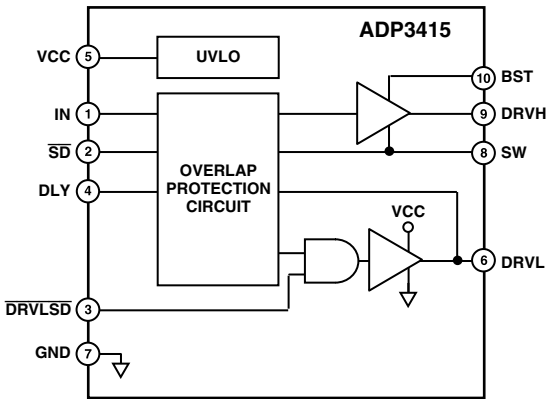
FEATURES

All-in-One Synchronous Buck Driver
One PWM Signal Generates Both Drives
Anticross-Conduction Protection Circuitry
Programmable Transition Delay
Zero-Crossing Synchronous Drive Control
Synchronous Override Control
Undervoltage Lockout
Shutdown Quiescent Current <100 μA

APPLICATIONS

Mobile Computing CPU Core Power Converters
Multiphase Desktop CPU Supplies
Single-Supply Synchronous Buck Converters
Standard-to-Synchronous Converter Adaptations

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADP3415 is a dual MOSFET driver optimized for driving two N-channel FETs that are the two switches in the non isolated synchronous buck power converter topology. The driver sizes are each optimized for performance in notebook PC regulators for CPUs in the 20 amp range. The high-side driver can be bootstrapped atop the switched node of the buck converter as needed to drive the upper switch, and is designed to accommodate the high voltage slew rate associated with high-performance, high-frequency switching. The ADP3415 has several features: an overlapping protection circuit (OPC), undervoltage lockout (UVLO) that holds the switches off until the driver is assured of having sufficient voltage for proper operation, a programmable transition delay, and a synchronous drive disable pin. The quiescent current, when the device is disabled, is less than 100 μA.

The ADP3415 is available in a 10-lead MSOP package.

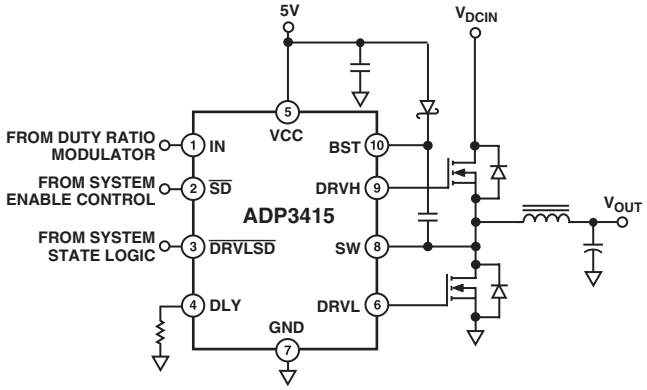


Figure 1. Typical Application Circuit

REV. 0

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ADP3415–SPECIFICATIONS[1] (T_A = 0°C to 100°C, V_{CC} = 5 V, $V_{BST} - V_{SW}$ = 5 V, $\overline{SD}$ = 5 V, $C_{DRVH} = C_{DRVL}$ = 3 nF, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SUPPLY (VCC)						
Quiescent Current[2]	I_{CCQ}					
Shutdown Mode		V_{SD} = 0.8 V		30	65	µA
Operating Mode		V_{SD} = 5 V, No Switching		1.2	2	mA
UNDERVOLTAGE LOCKOUT (UVLO)						
UVLO Threshold	V_{CCUVLO}		3.9	4.15	4.5	V
UVLO Hysteresis	$V_{CCHUVLO}$			0.05		V
LOW-SIDE DRIVER SHUTDOWN ($\overline{DRVLSD}$)						
Input Voltage High[3]	V_{IH}		2.0			V
Input Voltage Low[3]	V_{IL}				0.8	V
Propagation Delay[3, 4]	$tpdl_{DRVLSD}$			20	50	ns
(See Figure 3)	$tpdh_{DRVLSD}$			10	30	ns
SHUTDOWN ($\overline{SD}$)						
Input Voltage High[3]	V_{IH}		2.0			V
Input Voltage Low[3]	V_{IL}				0.8	V
INPUT (IN)						
Input Voltage High[3]	V_{IH}		2.0			V
Input Voltage Low[3]	V_{IL}				0.8	V
THERMAL SHUTDOWN(THSD)						
THSD Threshold	T_{SD}	$T_J = T_A$		165		°C
THSD Hysteresis	T_{HSD}	$T_J = T_A$		10		°C
HIGH-SIDE DRIVER (DRVH)						
Output Resistance, DRVH–BST				1.5	3.5	Ω
Output Resistance, DRVH–SW				0.85	2.0	Ω
DRVH Transition Times[4]	tr_{DRVH}	$V_{BST} - V_{SW}$ = 4.6 V		20	30	ns
(See Figure 4)	tf_{DRVH}			25	35	ns
DRVH Propagation Delay[4, 5]	$tpdh_{DRVH}$	$V_{BST} - V_{SW}$ = 4.6 V, V_{DLY} = 0 V	10	22	40	ns
(See Figure 4)	$tpdl_{DRVH}$			40	70	ns
LOW-SIDE DRIVER (DRVL)						
Output Resistance, DRVL–VCC				1.6	3.0	Ω
Output Resistance, DRVL–GND				1.0	3.0	Ω
DRVL Transition Times[4]	tr_{DRVL}	$V_{BST} - V_{SW}$ = 4.6 V		25	40	ns
(See Figure 4)	tf_{DRVL}	$V_{BST} - V_{SW}$ = 4.6 V		20	30	ns
DRVL Propagation Delay[4, 5, 6]	$tpdh_{DRVL}$	$V_{BST} - V_{SW}$ = 4.6 V	10	30	38	ns
(See Figure 4)	$tpdl_{DRVL}$	$V_{BST} - V_{SW}$ = 4.6 V		10	25	ns
SW Transition Timeout[7]	t_{SWTO}	$V_{BST} - V_{SW}$ = 4.6 V	130		300	ns
Zero-Crossing Threshold	V_{ZC}			1.6		V
DRVH TURN-ON DELAY TIMER						
Programmable Delay[8]	t_{DLY}	$0 \le R_{DLY} \le 100$ kΩ	0		100	ns
		$R_{DLY} > 100$ kΩ	100		200	ns
Delay Slope[4, 8]	$\Delta t_{DLY}/R_{DLY}$	$0 \le R_{DLY} \le 100$ kΩ	0.8	1.0	1.2	ns/kΩ

NOTES

[1]All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods.

[2]Including I_{BSTQ} quiescent current.

[3]The signal source driving the pin must have 70 µA (typ) pull-down strength to make a high-to-low transient, and 20 µA (typ) pull-up strength to make a low-to-high transient. The pin does not represent load (<100 nA) in static low (<0.8 V) and static high (>2.0 V) logic states (see TPC 3.) The pin can be driven with standard TTL logic level source.

[4]Guaranteed by characterization.

[5]For propagation delays, "tpdh" refers to the specified signal going high, "tpdl" refers to it going low.

[6]Propagation delay measured until DRVL begins its transition.

[7]The turn-on of DRVL is initiated after IN goes low by either V_{SW} crossing a ~1.6 V threshold or by expiration of t_{SWTO}.

[8]This delay represents a programmable extension to the propagation delay of DRVH assertion ($tpdh_{DRVH}$). The additional delay is a linear function of the range $0 \le R_{DLY} \le 100$ kΩ delay resistor tied from DLY to GND if its value is the specified resistance. The DLY pin may be grounded for no additional delay.

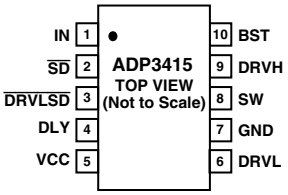
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

VCC to GND . . . . . –0.3 V to +7 V
BST to GND . . . . . –0.3 V to +30 V
BST to SW . . . . . –0.3 V to +7 V
SW to GND . . . . . –2.0 V to +25 V
SD, IN, DRVLSD to GND . . . . . –0.3 V to +7.3 V
Operating Ambient Temperature Range . . . . . 0°C to 100°C
Operating Junction Temperature Range . . . . . 0°C to 125°C
θ_{JA} . . . . . 155°C/W
θ_{JC} . . . . . 40°C/W
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . 300°C

*This is a stress rating only; operation beyond these limits can cause the device to be permanently damaged.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin	Mnemonic	Function
1	IN	TTL-Level Input Signal. Has primary control of the drive outputs.
2	$\overline{SD}$	Shutdown. When high, this pin enables normal operation. When low, DRVH and DRVL are forced low and the supply current (I_{CCQ}) is minimized as specified.
3	$\overline{DRVLSD}$	Drive-Low Shutdown. When $\overline{DRVLSD}$ is low, DRVL is kept low. When $\overline{DRVLSD}$ is high, DRVL is enabled and controlled by IN and by the adaptive OPC function.
4	DLY	High-Side Turn-On Delay. A resistor from this pin to ground programs an extended delay from turn-off of the lower FET to turn-on of the upper FET.
5	VCC	Input Supply. This pin should be bypassed to GND with a ~10 µF ceramic capacitor.
6	DRVL	Synchronous Rectifier Drive. Output drive for the lower (synchronous rectifier) FET.
7	GND	Ground. Should be directly connected to the ground plane, close to the source of the lower FET.
8	SW	This pin should be connected to the buck switching node, close to the upper FET's source. It is the floating return for the upper FET drive signal. Also, it is used to monitor the switched voltage for the OPC function.
9	DRVH	Buck Drive. Output drive for the upper (buck) FET.
10	BST	Floating Bootstrap Supply for the Upper FET. A capacitor connected between BST and SW pins holds this bootstrapped supply voltage for the high-side FET driver as it is switched. The capacitor should be a MLC type and should have substantially greater capacitance (e.g., ~ 20×) than the input capacitance of the upper FET.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Number of Units per Reel
ADP3415KRM-REEL	0°C to 100°C	Mini_SO Package (MSOP-10)	RM-10	3000
ADP3415KRM-REEL7	0°C to 100°C	Mini_SO Package (MSOP-10)	RM-10	1000

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADP3415 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

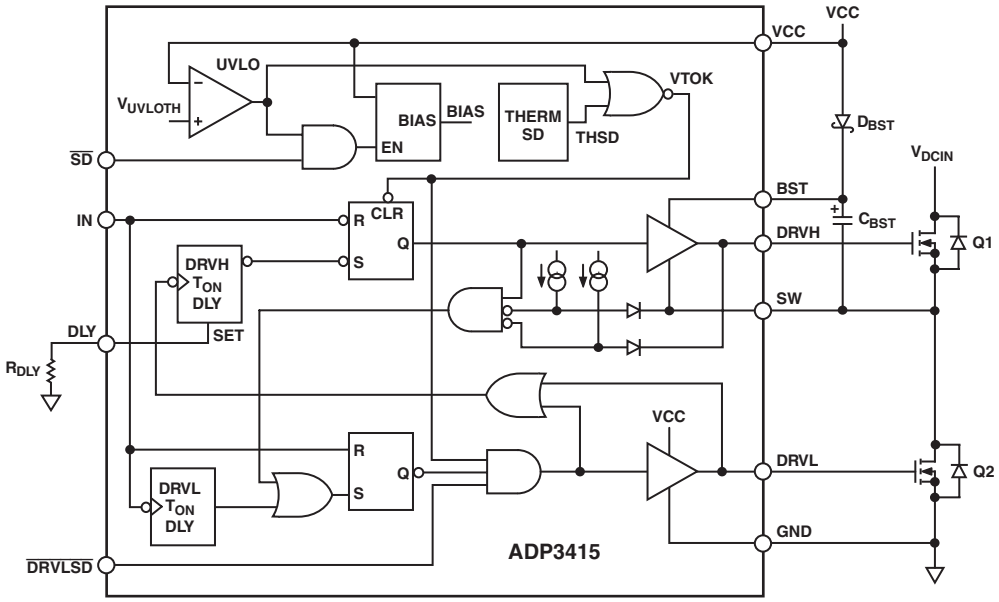


Figure 2. Functional Block Diagram

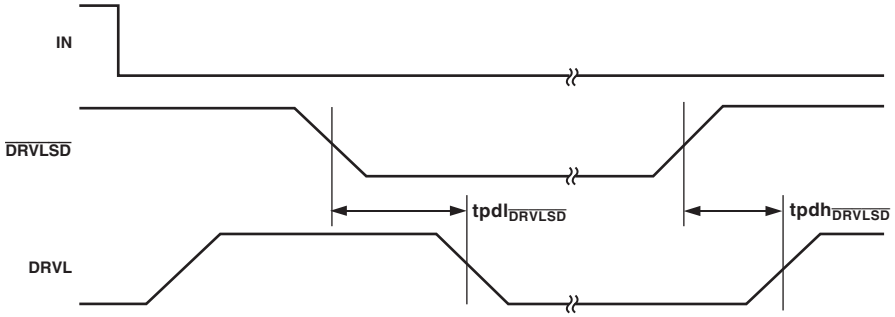


Figure 3. $\overline{DRVLSD}$ Propagation Delay

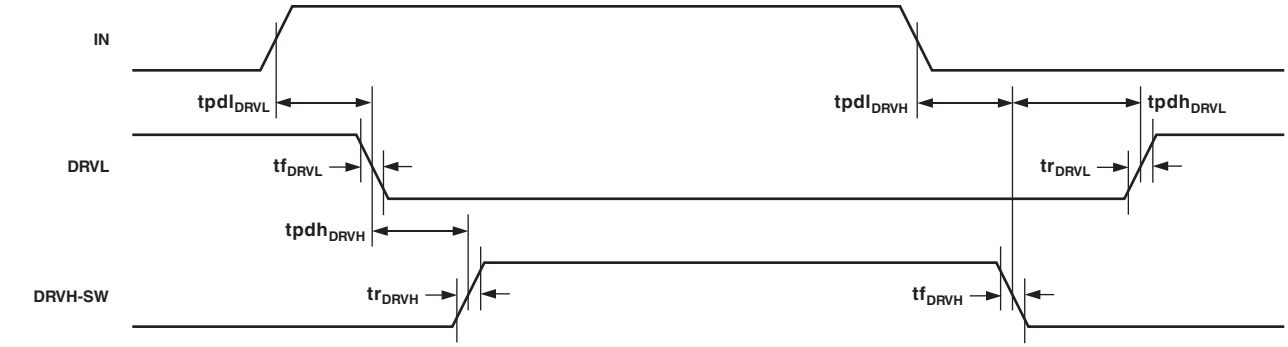


Figure 4. Switching Timing Diagram (Propagation Delay Referenced to 50%, Rise and Fall Time to 10% and 90% Points)

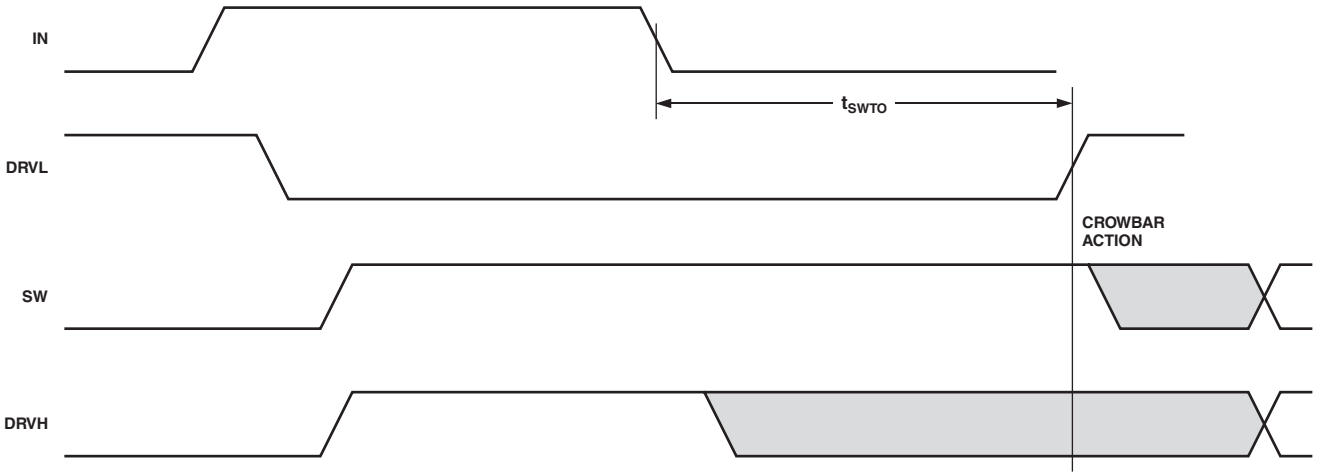
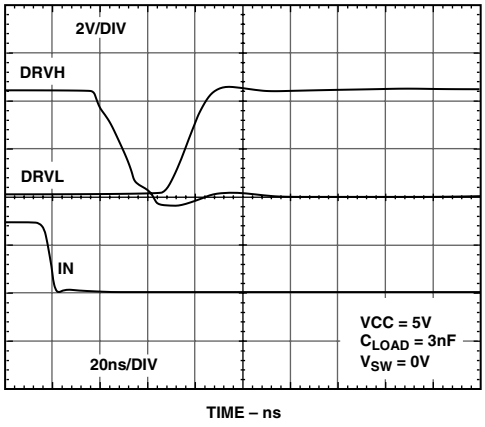
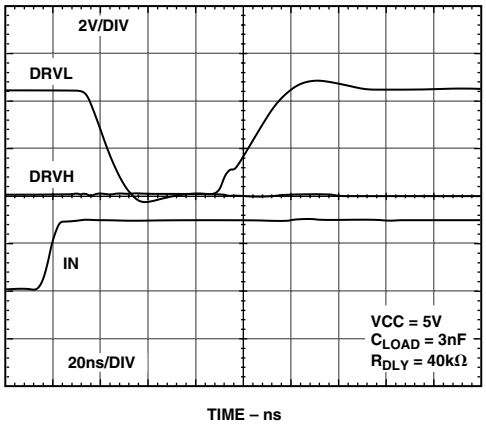


Figure 5. Switching Waveforms – SW Node Failure Mode – DRVL Timeout

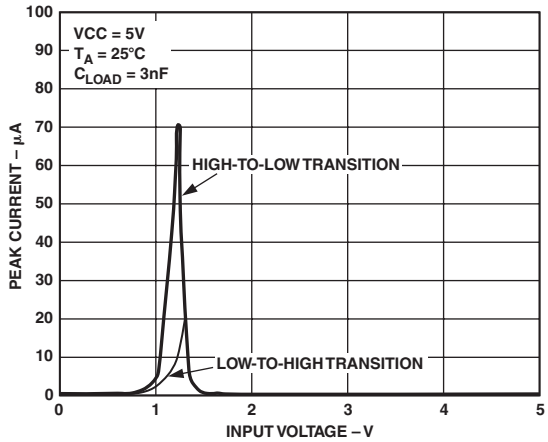
ADP3415–Typical Performance Characteristics



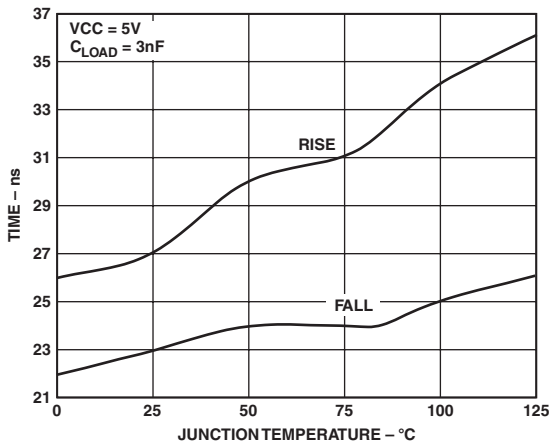
TPC 1. DRVH Fall and DRVL Rise Times



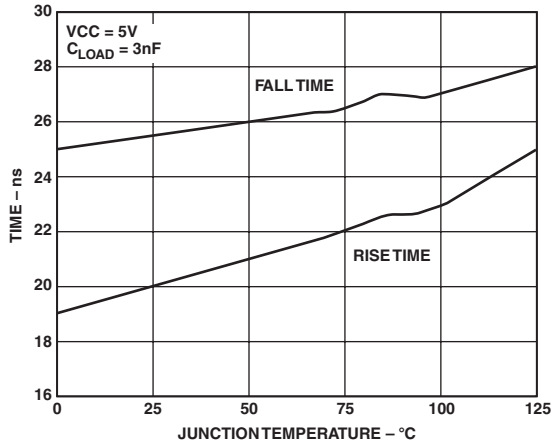
TPC 2. DRVL Fall and DRVH Rise Times



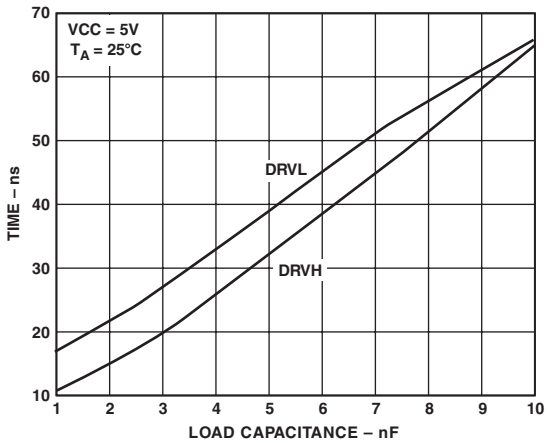
TPC 3. Input Voltage vs. Input Current



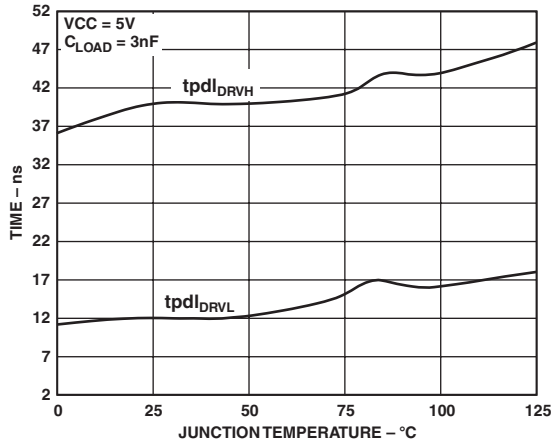
TPC 4. DRVL Rise and Fall Times vs. Temperature



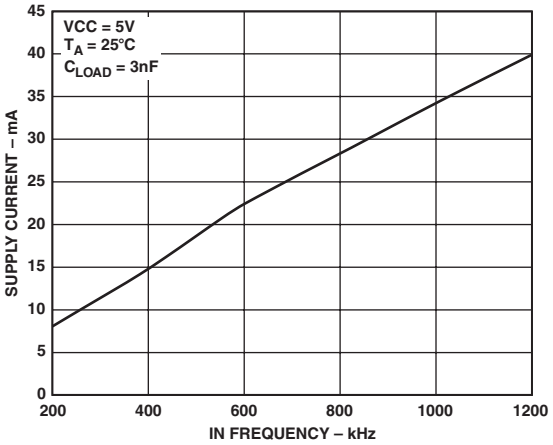
TPC 5. DRVH Rise and Fall Time vs. Temperature



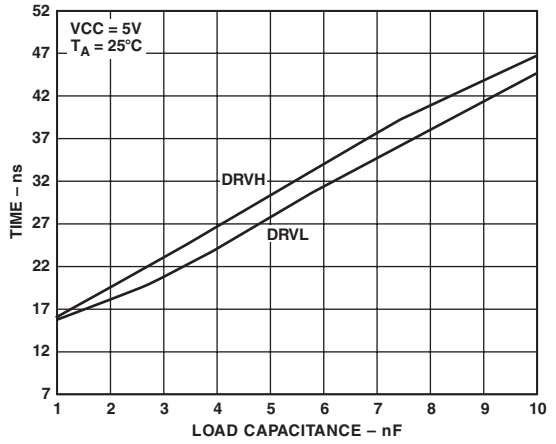
TPC 6. DRVH and DRVL Rise Time vs. Load Capacitance



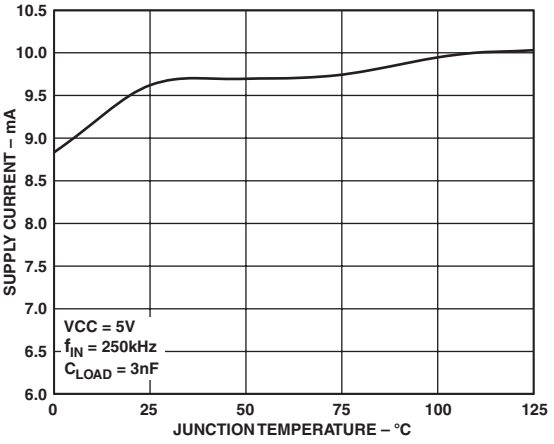
TPC 7. DRVH and DRVL Propagation Delay vs. Temperature



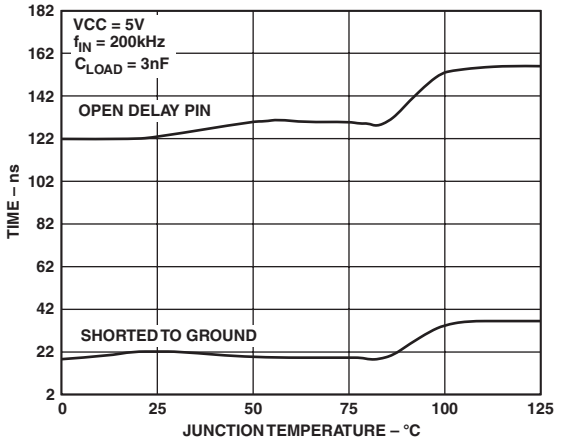
TPC 10. Supply Current vs. Frequency



TPC 8. DRVH and DRVL Fall Time vs. Load Capacitance



TPC 11. Supply Current vs. Temperature



TPC 9. $tpdh_{DRVH}$ vs. Temperature

THEORY OF OPERATION

The ADP3415 is a dual MOSFET driver optimized for driving two N-channel FETs in a synchronous buck converter topology. A single duty ratio modulation signal is all that is required to command the proper drive signal for the high-side and the low-side FETs.

A more detailed description of the ADP3415 and its features follows. Refer to the Functional Block Diagram (Figure 2).

Drive State Input

The drive state input, IN, should be connected to the duty ratio modulation signal of a switch-mode controller. IN can be driven by 2.5 V–5.0 V logic. The FETs will be driven so that the SW node follows the polarity of IN.

Low-Side Driver

The supply rails for the low-side driver, DRVL, are VCC and GND. In its conventional application it drives the gate of the synchronous rectifier FET.

When the driver is enabled, the driver's output is 180° out of phase with the duty ratio input aside from overlap protection circuit, propagation, and transition delays. When the driver is shut down or the entire ADP3415 is in shutdown or in under-voltage lockout, the low-side gate is held low.

High-Side Driver

The supply rail for the high-side driver, DRVH, is between the BST and SW pins, and is created by an external bootstrap supply circuit. In its conventional application it drives the gate of the (top) main buck converter FET.

The bootstrap circuit comprises a Schottky diode, D_{BST}, and bootstrap capacitor, C_{BST}. When the ADP3415 is starting up, the SW pin is at ground, so the bootstrap capacitor will charge up to VCC through D_{BST}. As the supply voltage ramps up and exceeds the UVLO threshold, the driver is enabled. When the input pin, IN, goes high, the high-side driver will begin to turn the high-side FET (Q1) ON by transferring charge from C_{BST} to the gate of the FET. As Q1 turns ON, the SW pin will rise up to V_{DCIN}, forcing the BST pin to $V_{DCIN} + V_{C(BST)}$, which is enough gate to source voltage to hold Q1 ON. To complete the cycle, when IN goes low, Q1 is switched OFF as DRVH discharges the gate to the voltage at the SW pin. When the low-side FET, Q2, turns ON, the SW pin is held at ground. This allows the bootstrap capacitor to charge up to VCC again.

The high-side driver's output is in phase with the duty ratio input. When the driver is in undervoltage lockout, the high-side gate is held low.

Overlap Protection Circuit

The overlap protection circuit (OPC) prevents both of the main power switches, Q1 and Q2, from being ON at the same time. This prevents excessive shoot-through currents from flowing through both power switches and minimizes the associated losses that can occur during their ON-OFF transitions. The overlap protection circuit accomplishes this by adaptively controlling the delay from Q1's turn OFF to Q2's turn ON, and by programming the delay from Q2's turn OFF to Q1's turn ON.

To prevent the overlap of the gate drives during Q1's turn OFF and Q2's turn ON, the overlap circuit monitors the voltage at the SW pin. When IN goes low, Q1 will begin to turn OFF (after a propagation delay), but before Q2 can turn ON the overlap protection circuit waits for the voltage at the SW pin to fall from V_{DCIN} to 1.6 V. Once the voltage on the SW pin has fallen to 1.6 V, Q2 will begin to turn ON. By waiting for the voltage on the SW pin to reach 1.6 V, the overlap protection circuit ensures that Q1 is OFF before Q2 turns on, regardless of variations in temperature, supply voltage, gate charge, and drive current. There is, however, a timeout circuit that will override the waiting period for the SW pin to reach 1.6 V. After the time-out period has expired, DRVL will be asserted regardless of the SW voltage.

To prevent the overlap of the gate drives during Q2's turn OFF and Q1's turn ON, the overlap circuit provides a programmable delay that is set by a resistor on the DLY pin. When IN goes high, Q2 will begin to turn OFF (after a propagation delay), but before Q1 can turn ON the overlap protection circuit waits for the voltage at DRVL to go low. Once the voltage at DRVL is low, the overlap protection circuit initiates a delay timer that is programmed by the external resistor R_{DLY}. The delay resistor adds an additional specified delay. The delay allows time for current to commutate from the body diode of Q2 to an external Schottky diode, which allows turnoff losses to be reduced. Although not as foolproof as the adaptive delay, the programmable delay adds a safety margin to account for variations in size, gate charge, and internal delay of the external power MOSFETs.

Low-Side Driver Shutdown

The low-side driver shutdown $\overline{\text{DRVLSD}}$ allows a control signal to shut down the synchronous rectifier. This signal should be modulated by system state logic to achieve maximum battery life under light load conditions and maximum efficiency under heavy load conditions. Under heavy load conditions, $\overline{\text{DRVLSD}}$ should be high so that the synchronous switch is modulated for maximum efficiency. Under light load conditions, $\overline{\text{DRVLSD}}$ should be low to prevent needless switching losses due to charge shuttling caused by polarity reversal of the inductor current when the average current is low.

When the $\overline{\text{DRVLSD}}$ input is low, the low-side driver stays low. When the $\overline{\text{DRVLSD}}$ input is high, the low-side driver is enabled and controlled by the driver signals as previously described.

Low-Side Driver Timeout Circuit

In normal operation, the DRVH signal tracks the IN signal and turns off the Q1 high-side switch with a few tens of ns $tpdl_{DRVH}$ delay following the falling edge of the input signal. When Q1 is turned off, then DRVL is allowed to go high, Q2 to turn on, and the SW node voltage to collapse to zero. But in a faulty scenario, such as the case of a high-side Q1 switch drain-source short circuit when even DRVH goes low, the SW node cannot fall to zero.

The ADP3415 has a timer circuit to address this scenario. Every time the IN goes low, a DRVL on-time delay timer gets triggered (see Figure 2). Should the SW node voltage not trigger the low-side turn-on, the DRVL on-time delay circuit will do it instead, when it times out with t_{SWTO} delay (see Figure 5.) If the high-side Q1 is still turned on, i.e., its drain is shorted to the source, the low-side Q2 turn-on will create a direct short circuit across the V_{DCIN} voltage rail, and the crowbar action will result in the fuse in the V_{DCIN} current patch blows. The opening of the fuse saves the load (CPU) from potential damage that the high-side switch short circuit could have caused.

Shutdown
For optimal system power management, when the output voltage is not needed, the ADP3415 can be shut down to conserve power.

When the $\overline{SD}$ pin is high, the ADP3415 is enabled for normal operation. Pulling the $\overline{SD}$ pin low forces the DRVH and DRVL outputs low, turning the buck converter OFF and reducing the VCC supply current to less than 40 μA.

Undervoltage Lockout
The undervoltage lockout (UVLO) circuit holds both FET driver outputs low during VCC supply ramp-up. The UVLO logic becomes active and in control of the driver outputs at a supply voltage of no greater than 1.5 V. The UVLO circuit waits until the VCC supply has reached a voltage high enough to bias logic level FETs fully ON, around 4.1 V, before releasing control of the drivers to the control pins.

Thermal Shutdown
The thermal shutdown circuit protects the ADP3415 against damage due to excessive power dissipation. Under extreme conditions, high ambient temperature, and high power dissipation, the die temperature may rise up to the thermal shutdown threshold of 165°C. If the die temperature exceeds 165°C, the thermal shutdown circuit will turn the output drivers OFF. The drivers remain disabled until the junction temperature has decreased by 10°C, at which point the drivers are again enabled.

APPLICATION INFORMATION

Supply Capacitor Selection
For the supply input (VCC) of the ADP3415, a local bypass capacitor is recommended to reduce the noise and to supply some of the peak currents drawn. Use a 10 μF MLC capacitor. Keep the ceramic capacitor as close as possible to the ADP3415. Multilayer ceramic (MLC) capacitors provide the best combination of low ESR and small size, and can be obtained from the following vendors:

Murata	GRM235Y5V106Z16	www.murata.com
Taiyo-Yuden	EMK325F106ZF	www.t-yuden.com
Tokin	C23Y5V1C106ZP	www.tokin.com

Bootstrap Circuit
The bootstrap circuit requires a charge storage capacitor, C_{BST}, and a Schottky diode, D1, as shown in Figure 2. Selecting these components can be done after the high-side FET has been chosen.

The bootstrap capacitor must have a voltage rating that is able to handle the maximum battery voltage plus 5 V. The capacitance is determined using the following equation:

$$C_{BST} = \frac{Q_{GATE}}{\Delta V_{BST}} \quad (1)$$

where Q_{GATE} is the total gate charge of the high-side FET, and ΔV_{BST} is the voltage droop allowed on the high-side FET drive. For example, the IRFR8503 has a total gate charge of about 15 nC. For an allowed droop of 150 mV, the required bootstrap capacitance is 100 nF. Use an MLC capacitor.

A Schottky diode is recommended for the bootstrap diode due to its low forward drop, which maximizes the drive available for the high-side FET. The bootstrap diode must also be able to withstand the maximum battery voltage plus 5 V. The average forward current can be estimated by:

$$I_{F(AVG)} \approx Q_{GATE} \times f_{MAX} \quad (2)$$

where f_{MAX} is the maximum switching frequency of the controller.

Delay Resistor Selection
The delay resistor, R_{DLY}, is used to add an additional delay when the low-side FET drive turns off and when the high-side drive starts to turn on. The delay resistor programs a specified additional delay besides the 20 ns of fixed delay.

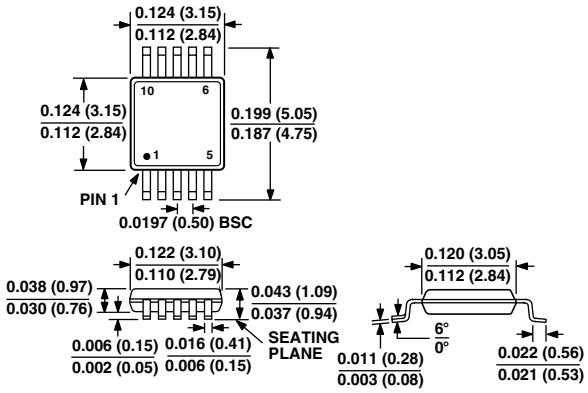
Printed Circuit Board Layout Considerations
Use the following general guidelines when designing printed circuit boards:

1. Trace out the high-current paths and use short, wide traces to make these connections.
2. The VCC bypass capacitor should be located as close as possible to VCC and GND pins.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

10-Lead Mini_SOIC Package (MSOP)
(RM-10)



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