

Complete 20 MSPS CCD Signal Processors AD9841A/AD9842A

FEATURES

20 MSPS Correlated Double Sampler (CDS) 4 dB ± 6 dB 6-Bit Pixel Gain Amplifier (*PxGA*®) 2 dB to 36 dB 10-Bit Variable Gain Amplifier (VGA) Low Noise Clamp Circuits Analog Preblanking Function 10-Bit (9841) or 12-Bit (9842) 20 MSPS A/D Converter Auxiliary Inputs with VGA and Input Clamp 3-Wire Serial Digital Interface 3 V Single Supply Operation Low Power: 65 mW @ 2.7 V Supply 48-Lead LOFP Package

APPLICATIONS Digital Still Cameras Digital Video Camcorders

PRODUCT DESCRIPTION

The AD9841A and AD9842A are complete analog signal processors for CCD applications. Both products feature a 20 MHz single-channel architecture designed to sample and condition the outputs of interlaced and progressive scan area CCD arrays. The AD9841A/AD9842A's signal chain consists of an input clamp, correlated double sampler (CDS), Pixel Gain Amplifier (*PxGA*), digitally controlled variable gain amplifier (VGA), black level clamp, and A/D converter. The AD9841A offers 10-bit ADC resolution, while the AD9842A contains a true 12-bit ADC. Additional input modes are provided for processing analog video signals.

The internal registers are programmed through a 3-wire serial digital interface. Programmable features include gain adjustment, black level adjustment, input configuration, and power-down modes.

The AD9841A and AD9842A operate from a single 3 V power supply, typically dissipate 78 mW, and are packaged in a 48-lead LQFP.



FUNCTIONAL BLOCK DIAGRAM

PxGA is a registered trademark of Analog Devices, Inc.

REV.0

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AD9841A/AD9842A-SPECIFICATIONS

GENERAL SPECIFICATIONS (T_{MIN} to T_{MAX} , AVDD = DVDD = 3.0 V, $f_{DATACLK}$ = 20 MHz, unless otherwise noted.)

Parameter	Min	Тур	Max	Unit
TEMPERATURE RANGE				
Operating	-20		+85	°C
Storage	-65		+150	°C
POWER SUPPLY VOLTAGE				
Analog, Digital, Digital Driver	2.7		3.6	V
POWER CONSUMPTION				
Normal Operation	(Specified	d Under Each M	ode of Operation)	
Power-Down Modes		20		
Fast Recovery Mode		30 5		mw
Standby Total Bourse Dourse		5		III W
		1		
MAXIMUM CLOCK RATE	20			MHz
A/D CONVERTER (AD9841A)				
Resolution	10			Bits
Differential Nonlinearity (DNL)		± 0.4	± 1.0	LSB
No Missing Codes	10			Bits Guaranteed
Full-Scale Input Voltage		2.0		V
Data Output Coding		Straight Binary		
A/D CONVERTER (AD9842A)				
Resolution	12			Bits
Differential Nonlinearity (DNL)		± 0.5	± 1.0	LSB
No Missing Codes	12			Bits Guaranteed
Full-Scale Input Voltage		2.0		V
Data Output Coding		Straight Binary		
VOLTAGE REFERENCE				
Reference Top Voltage (VRT)		2.0		V
Reference Bottom Voltage (VRB)		1.0		V

Specifications subject to change without notice.

DIGITAL SPECIFICATIONS (DRVDD = 2.7 V, C_L = 20 pF unless otherwise noted.)

Parameter	Symbol	Min	Тур	Max	Unit
LOGIC INPUTS					
High Level Input Voltage	V_{IH}	2.1			V
Low Level Input Voltage	V _{IL}			0.6	V
High Level Input Current	I _{IH}		10		μA
Low Level Input Current	I _{IL}		10		μA
Input Capacitance	C _{IN}		10		pF
LOGIC OUTPUTS					
High Level Output Voltage, I _{OH} = 2 mA	V _{OH}	2.2			V
Low Level Output Voltage, $I_{OL} = 2 \text{ mA}$	V _{OL}			0.5	V

AD9841A CCD-MODE SPECIFICATIONS $(T_{MIN} \text{ to } T_{MAX}, \text{ AVDD} = \text{DVDD} = 3.0 \text{ V}, f_{DATACLK} = f_{SHP} = f_{SHD} = 20 \text{ MHz}, \text{ unless otherwise noted.}$

Parameter	Min T	yp Max	Unit	Notes
POWER CONSUMPTION	78	3	mW	See TPC 1 for Power Curves
MAXIMUM CLOCK RATE	20		MHz	
CDS Gain Allowable CCD Reset Transient ¹ Max Input Range Before Saturation ¹ Max CCD Black Pixel Amplitude ¹	0 50 1.0 20	00	dB mV V p-p mV	See Input Waveform in Footnote 1 <i>PxGA</i> Gain at 4 dB
PIXEL GAIN AMPLIFIER (<i>PxGA</i>) Max Input Range Max Output Range Gain Control Resolution Gain Monotonicity Gain Range (Two's Complement Coding) Min Gain (<i>PxGA</i> Gain Code 32) Max Gain (<i>PxGA</i> Gain Code 31)	1.0 1.6 64 Gua -2 10	ranteed	V p-p V p-p Steps dB dB	<i>PxGA</i> Gain at 4 dB At Any <i>PxGA</i> Gain See Figure 28 for <i>PxGA</i> Gain Curve
VARIABLE GAIN AMPLIFIER (VGA) Max Input Range Max Output Range Gain Control Resolution Gain Monotonicity Gain Range Low Gain (VGA Gain Code 91) Max Gain (VGA Gain Code 1023)	1.6 2.0 . Guan 2 36	24 ranteed	V p-p V p-p Steps dB dB	See Figure 29 for VGA Gain Curve
BLACK LEVEL CLAMP Clamp Level Resolution Clamp Level Min Clamp Level Max Clamp Level	25 0 63	66 9.75	Steps LSB LSB	Measured at ADC Output
SYSTEM PERFORMANCEGain Accuracy, VGA Code 91 to 10232PxGA Gain AccuracyMin Gain (PxGA Register Code 32)Max Gain (PxGA Code 31)Peak Nonlinearity, 500 mV Input SignalPeak Nonlinearity, 800 mV Input SignalTotal Output NoisePower Supply Rejection (PSR)	-0.5 -1 0 11 12 0. 0. 40	+0.5 +1 13 1 4 2	dB dB % LSB rms dB	Specifications Include Entire Signal Chain Use Equations on Page 19 to Calculate Gain VGA Gain Fixed at 2 dB (Code 91) VGA Gain Fixed at 2 dB (Code 91) 12 dB Gain Applied 8 dB Gain Applied AC Grounded Input, 6 dB Gain Applied Measured with Step Change on Supply
POWER-UP RECOVERY TIME Fast Recovery Mode Reference Standby Mode Total Shutdown Mode Power-Off Condition	0. 1 3 15	1	ms ms ms ms	Normal Clock Signals Applied

NOTES

¹Input Signal Characteristics defined as follows:

/ 500mV TYP 200mV MAX OPTICAL BLACK PIXEL INPUT SIGNAL RANGE

 $^{2}PxGA$ gain fixed at 4 dB.

AD9841A/AD9842A-SPECIFICATIONS

AD9842A CCD-MODE SPECIFICATIONS $(T_{MIN} \text{ to } T_{MAX}, \text{ AVDD} = \text{DVDD} = 3.0 \text{ V}, f_{DATACLK} = f_{SHP} = f_{SHD} = 20 \text{ MHz}, \text{ unless otherwise noted}$

Parameter	Min	Тур	Max	Unit	Notes
POWER CONSUMPTION		78		mW	See TPC 1 for Power Curves
MAXIMUM CLOCK RATE	20			MHz	
CDS Gain Allowable CCD Reset Transient ¹ Max Input Range Before Saturation ¹ Max CCD Black Pixel Amplitude ¹	1.0	0 500 200		dB mV V p-p mV	See Input Waveform in Footnote 1 <i>PxGA</i> Gain at 4 dB
PIXEL GAIN AMPLIFIER (<i>PxGA</i>) Max Input Range Max Output Range Gain Control Resolution Gain Monotonicity Gain Range (Two's Complement Coding) Min Gain (<i>PxGA</i> Gain Code 32) Max Gain (<i>PxGA</i> Gain Code 31)	1.0 1.6 Gi	64 uarantee -2 10	d	V p-p V p-p Steps dB dB	See Figure 28 for <i>PxGA</i> Gain Curve
VARIABLE GAIN AMPLIFIER (VGA) Max Input Range Max Output Range Gain Control Resolution Gain Monotonicity Gain Range Low Gain (VGA Gain Code 91) Max Gain (VGA Gain Code 1023)	1.6 2.0 G	1024 Guaranteo 2 36	ed	V p-p V p-p Steps dB dB	See Figure 29 for VGA Gain Curve
BLACK LEVEL CLAMP Clamp Level Resolution Clamp Level Min Clamp Level Max Clamp Level		256 0 255		Steps LSB LSB	Measured at ADC Output
SYSTEM PERFORMANCE Gain Accuracy, (VGA Code 91 to 1023) ² PxGA Gain Accuracy Min Gain (PxGA Register Code 32) Max Gain (PxGA Code 31) Peak Nonlinearity, 500 mV Input Signal Total Output Noise Power Supply Rejection (PSR)	-0.5 -1 11	0 12 0.1 0.6 40	+0.5 +1 13	dB dB % LSB rms dB	Specifications Include Entire Signal Chain Use Equations on Page 19 to Calculate Gain VGA Gain Fixed at 2 dB (Code 91) VGA Gain Fixed at 2 dB (Code 91) 12 dB Gain Applied AC Grounded Input, 6 dB Gain Applied Measured with step change on supply
POWER-UP RECOVERY TIME Fast Recovery Mode Reference Standby Mode Total Shutdown Mode Power-Off Condition		0.1 1 3 15		ms ms ms ms	Normal Clock Signals Applied

NOTES

¹Input Signal Characteristics defined as follows:

500mV TYP 200mV MAX OPTICAL BLACK PIXEL INPUT SIGNAL RANGE

 $^{2}PxGA$ gain fixed at 4 dB.

AUX1-MODE SPECIFICATIONS (T_{MIN} to T_{MAX} , AVDD = DVDD = 3.0 V, $f_{DATACLK}$ = 20 MHz, unless otherwise noted.)

Parameter	Min	Тур	Max	Unit
POWER CONSUMPTION		60		mW
MAXIMUM CLOCK RATE	20			MHz
INPUT BUFFER Gain Max Input Range	1.0	0		dB V p-p
VGA Max Output Range Gain Control Resolution Coin (Selected Using VGA Gain Register)	2.0	1023		V p-p Steps
Min Gain Max Gain		0 36		dB dB

Specifications subject to change without notice.

AUX2-MODE SPECIFICATIONS (T_{MIN} to T_{MAX} , AVDD = DVDD = 3.0 V, $f_{DATACLK}$ = 20 MHz, unless otherwise noted.)

Parameter	Min	Тур	Max	Unit
POWER CONSUMPTION		mW		
MAXIMUM CLOCK RATE	20			MHz
INPUT BUFFER	(Sam	e as AUX1-MODE)		
VGA				
Max Output Range	2.0			V p-p
Gain Control Resolution		512		Steps
Gain (Selected Using VGA Gain Register)				
Min Gain		0		dB
Max Gain		18		dB
ACTIVE CLAMP (AD9841A)				
Clamp Level Resolution		256		Steps
Clamp Level (Measured at ADC Output)				-
Min Clamp Level		0		LSB
Max Clamp Level		63.75		LSB
ACTIVE CLAMP (AD9842A)				
Clamp Level Resolution		256		Steps
Clamp Level (Measured at ADC Output)				-
Min Clamp Level		0		LSB
Max Clamp Level		255		LSB

Parameter	Symbol	Min	Тур	Max	Unit
SAMPLE CLOCKS					
DATACLK, SHP, SHD Clock Period	t _{CONV}	48	50		ns
DATACLK Hi/Low Pulsewidth	t _{ADC}	20	25		ns
SHP Pulsewidth	t _{SHP}	7	12.5		ns
SHD Pulsewidth	t _{SHD}	7	12.5		ns
CLPDM Pulsewidth	t _{CDM}	4	10		Pixels
CLPOB Pulsewidth ¹	t _{COB}	2	20		Pixels
SHP Rising Edge to SHD Falling Edge	t _{S1}	0	12.5		ns
SHP Rising Edge to SHD Rising Edge	t _{S2}	20	25		ns
Internal Clock Delay	t _{ID}		3.0		ns
Inhibited Clock Period	t _{INH}	10			ns
DATA OUTPUTS					
Output Delay	t _{OD}		14.5	16	ns
Output Hold Time	t _H	7.0	7.6		ns
Pipeline Delay			9		Cycles
SERIAL INTERFACE					
Maximum SCK Frequency	f _{SCLK}	10			MHz
SL to SCK Setup Time	t _{LS}	10			ns
SCK to SL Hold Time	t _{LH}	10			ns
SDATA Valid to SCK Rising Edge Setup	t _{DS}	10			ns
SCK Falling Edge to SDATA Valid Hold	t _{DH}	10			ns
SCK Falling Edge to SDATA Valid Read	t _{DV}	10			ns

TIMING SPECIFICATIONS $(C_L = 20 \text{ pF}, f_{SAMP} = 20 \text{ MHz}, CCD-Mode Timing in Figures 5 and 6, AUX-Mode Timing in Figure 7. Serial Timing in Figures 21–24.)$

¹Minimum CLPOB pulsewidth is for functional operation only. Wider typical pulses are recommended to achieve low noise clamp performance.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Parameter	With Respect To	Min	Max	Unit
	AVSS	_0.3	+3.0	v
DVDD1 DVDD2	DVSS	-0.3	+3.9	v
DRVDD	DRVSS	-0.3	+3.9	v
Digital Outputs	DRVSS	-0.3	DRVDD + 0.3	v
SHP, SHD, DATACLK	DVSS	-0.3	DVDD + 0.3	v
CLPOB, CLPDM, PBLK	DVSS	-0.3	DVDD + 0.3	V
SCK, SL, SDATA	DVSS	-0.3	DVDD + 0.3	v
VRT, VRB, CMLEVEL	AVSS	-0.3	AVDD + 0.3	v
BYP1-4, CCDIN	AVSS	-0.3	AVDD + 0.3	V
Junction Temperature			150	°C
Lead Temperature			300	°C
(10 sec)				

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9841AJST	–20°C to +85°C	Thin Plastic Quad Flatpack (LQFP)	ST-48
AD9842AJST	–20°C to +85°C	Thin Plastic Quad Flatpack (LQFP)	ST-48

THERMAL CHARACTERISTICS Thermal Resistance

48-Lead LQFP Package $\theta_{IA} = 92^{\circ}C$

CAUTION _

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9841A/AD9842A features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



NOTES



PIN FUNCTION DESCRIPTIONS

Pin Number	Name	Туре	Description
1, 2	NC	NC	Internally Not Connected (AD9841A ONLY)
3-12	D0-D9	DO	Digital Data Outputs (AD9841A ONLY)
1-12	D0-D11	DO	Digital Data Outputs (AD9842A ONLY)
13	DRVDD	Р	Digital Output Driver Supply
14	DRVSS	Р	Digital Output Driver Ground
15, 41	DVSS	Р	Digital Ground
16	DATACLK	DI	Digital Data Output Latch Clock
17	DVDD1	Р	Digital Supply
18	HD	DI	Horizontal Drive. Used with VD for Color Steering Control
19	PBLK	DI	Preblanking Clock Input
20	CLPOB	DI	Black Level Clamp Clock Input
21	SHP	DI	CDS Sampling Clock for CCD's Reference Level
22	SHD	DI	CDS Sampling Clock for CCD's Data Level
23	CLPDM	DI	Input Clamp Clock Input
24	VD	DI	Vertical Drive. Used with HD for Color Steering Control
25, 26, 35	AVSS	Р	Analog Ground
27	AVDD1	Р	Analog Supply
28	BYP1	AO	Internal Bias Level Decoupling
29	BYP2	AO	Internal Bias Level Decoupling
30	CCDIN	AI	Analog Input for CCD Signal
31	NC	NC	Internally Not Connected
32	BYP4	AO	Internal Bias Level Decoupling
33	AVDD2	Р	Analog Supply
34	AUX2IN	AI	Analog Input
36	AUX1IN	AI	Analog Input
37	CML	AO	Internal Bias Level Decoupling
38	VRT	AO	A/D Converter Top Reference Voltage Decoupling
39	VRB	AO	A/D Converter Bottom Reference Voltage Decoupling
40	DVDD2	Р	Digital Supply
42	THREE-STATE	DI	Digital Output Disable. Active High
43	NC	NC	May be tied high or low. Do not leave floating.
44	STBY	DI	Standby Mode, Active High. Same as Serial Interface
45	NC	NC	Internally Not Connected. May be Tied High or Low
46	SL	DI	Serial Digital Interface Load Pulse
47	SDATA	DI	Serial Digital Interface Data
48	SCK	DI	Serial Digital Interface Clock

TYPE: AI = Analog Input, AO = Analog Output, DI = Digital Input, DO = Digital Output, P = Power.

DEFINITIONS OF SPECIFICATIONS DIFFERENTIAL NONLINEARITY (DNL)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Thus every code must have a finite width. No missing codes guaranteed to 12-bit resolution indicates that all 4096 codes, respectively, must be present over all operating conditions.

PEAK NONLINEARITY

Peak nonlinearity, a full signal chain specification, refers to the peak deviation of the output of the AD984x from a true straight line. The point used as "zero scale" occurs 1/2 LSB before the first code transition. "Positive full scale" is defined as a Level 1, 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each particular output code to the true straight line. The error is then expressed as a percentage of the 2 V ADC full-scale signal. The input signal is always appropriately gained up to fill the ADC's full-scale range.

TOTAL OUTPUT NOISE

The rms output noise is measured using histogram techniques. The standard deviation of the ADC output codes is calculated

EQUIVALENT INPUT CIRCUITS



Figure 1. Digital Inputs—SHP, SHD, DATACLK, CLPOB, CLPDM, HD, VD, PBLK, SCK, SL



Figure 2. Data Outputs-D0-D9 (D11)

in LSB, and represents the rms noise level of the total signal chain at the specified gain setting. The output noise can be converted to an equivalent voltage, using the relationship 1 LSB = (ADC Full Scale/2^N codes) when N is the bit resolution of the ADC. For the AD9842A, 1 LSB is 500 μ V, and for the AD9841A, 1 LSB is 2 mV.

POWER SUPPLY REJECTION (PSR)

The PSR is measured with a step change applied to the supply pins. This represents a very high frequency disturbance on the AD984xA's power supply. The PSR specification is calculated from the change in the data outputs for a given step change in the supply voltage.

INTERNAL DELAY FOR SHP/SHD

The internal delay (also called aperture delay) is the time delay that occurs from when a sampling edge is applied to the AD984xA until the actual sample of the input signal is held. Both SHP and SHD sample the input signal during the transition from low to high, so the internal delay is measured from each clock's rising edge to the instant the actual internal sample is taken.



Figure 3. CCDIN (Pin 30)



Figure 4. SDATA (Pin 47)

Typical Performance Characteristics-AD9841A/AD9842A



TPC 1. AD9841A/AD9842A Power vs. Sample Rate



TPC 2. AD9841A Typical DNL Performance



TPC 3. AD9841A Output Noise vs. VGA Gain



TPC 4. AD9842A Typical DNL Performance



TPC 5. AD9842A Output Noise vs. VGA Gain

CCD-MODE AND AUX MODE TIMING



1. RECOMMENDED PLACEMENT FOR DATACLK RISING EDGE IS BETWEEN THE SHD RISING EDGE AND NEXT SHP FALLING EDGE.

2. CCD SIGNAL IS SAMPLED AT SHP AND SHD RISING EDGES.

Figure 5. CCD-Mode Timing



1. CLPOB AND CLPDM WILL OVERWRITE PBLK. PBLK WILL NOT AFFECT CLAMP OPERATION IF OVERLAPPING CLPDM AND/OR CLPOB. 2. PBLK SIGNAL IS OPTIONAL. 3. DIGITAL OUTPUT DATA WILL BE ALL ZEROS DURING PBLK. OUTPUT DATA LATENCY IS 9 DATACLK CYCLES.

Figure 6. Typical CCD-Mode Line Clamp Timing



Figure 7. AUX-Mode Timing

PIXEL GAIN AMPLIFIER (PxGA) TIMING















Figure 11. PxGA Mode 2 (Interlace) Detailed Timing



NOTE: 0 = GAIN0, 1 = GAIN1, 2 = GAIN2

Figure 12. PxGA Mode 3 (3-Color) Frame/Line Gain Register Sequence



Figure 13. PxGA Mode 3 (3-Color) Detailed Timing



Figure 14. PxGA Mode 4 (4-Color) Frame/Line Gain Register Sequence



2. EVERY HD RISING EDGE WITH A PREVIOUS VD RISING EDGE WILL RESET TO 01230123.

Figure 15. PxGA Mode 4 (4-Color) Detailed Timing



Figure 16. PxGA Mode 5 (VD Selected) Frame/Line Gain Register Sequence



Figure 17. PxGA Mode 5 (VD Selected) Detailed Timing



Figure 18. PxGA Mode 6 (Mosaic Repeat) Frame/Line Gain Register Sequence







Figure 20. PxGA Mode 7 (User-Specified) Detailed Timing

SERIAL INTERFACE TIMING AND INTERNAL REGISTER DESCRIPTION

Register	A	ddr	ess		Data Bits									
Name	A	A1	A2	D 0	D 1	D2	D3	D 4	D5	D6	D 7	D 8	D9	D10
Operation	0	0	0	Chann CCD/	el Select AUX1/2	Power- Modes	Down	Software Reset	OB Clamp On/Off	0*	1**	0*	0*	0*
VGA Gain	1	0	0	LSB									MSB	Х
Clamp Level	0	1	0	LSB							MSB	X	X	X
Control	1	1	0	Color Selecti	Steering . on	Mode	PxGA On/Off	Clock Po SHP/SHI	larity Select for D/CLP/DATA	- .	0*	0*	Three- State	X
PxGA Gain0	0	0	1	LSB					MSB	X	X	X	X	Х
PxGA Gain1	1	0	1	LSB					MSB	X	X	X	X	X
PxGA Gain2	0	1	1	LSB					MSB	X	X	X	X	X
PxGA Gain3	1	1	1	LSB					MSB	X	X	X	X	Х

Table I. AD9841A/AD9842A Internal Register Map

*Internal use only. Must be set to zero.

**Must be set to one.



Figure 21. Serial Write Operation



1. RNW = READ-NOT WRITE. SET HIGH FOR READ OPERATION.

2. TEST BITS = INTERNAL USE ONLY. MUST BE SET LOW.

3. SERIAL DATA FROM THE SELECTED REGISTER IS VALID STARTING AFTER THE 5TH SCK FALLING EDGE, AND IS UPDATED ON SCK FALLING EDGES.

Figure 22. Serial Readback Operation



NOTES: 1. ANY NUMBER OF ADJACENT REGISTERS MAY BE LOADED SEQUENTIALLY, BEGINNING WITH THE LOWEST ADDRESS AND INCREMENTING ONE ADDRESS AT A TIME. 2. WHEN SEQUENTIALLY LOADING MULTIPLE REGISTERS, THE EXACT REGISTER LENGTH (SHOWN ABOVE) MUST BE USED FOR EACH REGISTER. 3. ALL LOADED REGISTERS WILL BE SIMULTANEOUSLY UPDATED WITH THE RISING EDGE OF SL.





Figure 24. Continuous Serial Write Operation to All PxGA Gain Registers

D 10	D9	D8	D 7	D6	Optical Black Clamp D5	Reset D4	Power-Down Modes D3 D2	Channel Selection D1 D0
0*	0*	0*	1**	0*	 Enable Clamping Disable Clamping 	0 Normal 1 Reset All Registers to Default	0 0 Normal Power 0 1 Fast Recovery 1 0 Standby 1 1 Total Power-Down	0 0 CCD Mode 0 1 AUX1 Mode 1 0 AUX2 Mode 1 1 Test Only

Table II.	Operation	Register	Contents	(Default	Value x000)
-----------	-----------	----------	----------	----------	-------------

*Must be set to zero.

**Set to one.

 Table III. VGA Gain Register Contents (Default Value x096)

D10	MSB D9	D8	D 7	D6	D5	D 4	D3	D2	D1	LSB D0	Gain (dB)
X	0	0	0	1	0 •	1	1	1	1	1	2.0 •
	1 1	1 1	1 1	1 1	• 1 1	1 1	1 1	1 1	1 1	0 1	• 35.965 36.0

D10	D9	D8	MSB D7	D6	D5	D 4	D3	D2	D1	LSB D0	Clamp Level (LSB)
x	Х	Х	0	0	0	0	0	0	0	0	0
			0	0	0	0	0	0	0	1	0.25
			0	0	0	0	0	0	1	0	0.5
						•					•
						•					•
						•					•
			1	1	1	1	1	1	1	0	63.5
			1	1	1	1	1	1	1	1	63.75

Table IV. AD9841A Clamp Level Register Contents (Default Value x080)

Table V. AD9842A Clamp Level Register Contents (Default Value x080)

D10	D9	D8	MSB D7	D6	D5	D 4	D3	D2	D 1	LSB D0	Clamp Level (LSB)
X	Х	Х	0	0	0	0	0	0	0	0	0
			0	0	0	0	0	0	0	1	1
			0	0	0	0	0	0	1	0	2
						•					•
						•					•
						•					•
			1	1	1	1	1	1	1	0	254
			1	1	1	1	1	1	1	1	255

Table VI. Control Register Contents (Default Value x000)

D10	Data Out D9	D8	D 7	DATACLK D6	CLP/PBLK D5	SHP/SHD D4	<i>PxGA</i> D3**	Col D2	or St D1	teering Modes D0
X	0 Enable 1 Three-State	0*	0*	0 Rising Edge Trigger 1 Falling Edge Trigger	0 Active Low 1 Active High	0 Active Low 1 Active High	0 Disable 1 Enable	0 0 0 1 1 1	0 0 1 1 0 0 1	 0 Steering Disabled 1 Mosaic Separate 0 Interlace 1 3-Color 0 4-Color 1 VD Selected 0 Mosaic Repeat

*Must be set to zero.

**When D3 = 0 (PxGA disabled) the PxGA gain is fixed to 4 dB.

Table VII. PxGA Gain Registers for Gain0, Gain1, Gain2, Gain3 (Default Value x000)

D10	D9	D8	D 7	D6	MSB D5	D 4	D3	D2	D1	LSB D0	Gain (dB)*
X	Х	Х	Х	Х	0	1	1	1	1	1	+10.0
							•				•
							•				•
							•				•
					0	0	0	0	0	0	+4.3
					1	1	1	1	1	1	+4.0
							•				•
							•				•
							•				•
					1	0	0	0	0	0	-2.0

*Control Register Bit D3 must be set High (PxGA Enable) to use the PxGA Gain Registers.

CIRCUIT DESCRIPTION AND OPERATION

The AD9841A and AD9842A signal processing chain is shown in Figure 25. Each processing step is essential in achieving a high-quality image from the raw CCD pixel data.

DC Restore

To reduce the large dc offset of the CCD output signal, a dcrestore circuit is used with an external 0.1 μ F series coupling capacitor. This restores the dc level of the CCD signal to approximately 1.5 V, to be compatible with the 3 V single supply of the AD984xA.

Correlated Double Sampler

The CDS circuit samples each CCD pixel twice to extract the video information and reject low-frequency noise. The timing shown in Figure 5 illustrates how the two CDS clocks, SHP and SHD, are used to sample the reference level and data level of the CCD signal respectively. The CCD signal is sampled on the rising edges of SHP and SHD. Placement of these two clock signals is critical in achieving the best performance from the CCD. An internal SHP/SHD delay (t_{ID}) of 3 ns is caused by internal propagation delays.

Input Clamp

A line-rate input clamping circuit is used to remove the CCD's optical black offset. This offset exists in the CCD's shielded black reference pixels. Unlike some AFE architectures, the AD984xA removes this offset in the input stage to minimize the

effect of a gain change on the system black level, usually called the "gain step." Another advantage of removing this offset at the input stage is to maximize system headroom. Some area CCDs have large black level offset voltages, which, if not corrected at the input stage, can significantly reduce the available headroom in the internal circuitry when higher VGA gain settings are used.

Horizontal timing is shown in Figure 6. It is recommended that the CLPDM pulse be used during valid CCD dark pixels. CLPDM may be used during the optical black pixels, either together with CLPOB or separately. The CLPDM pulse should be a minimum of 4 pixels wide.

PxGA

The PxGA provides separate gain adjustment for the individual color pixels. A programmable gain amplifier with four separate values, the PxGA has the capability to "multiplex" its gain value on a pixel-to-pixel basis. This allows lower output color pixels to be gained up to match higher output color pixels. Also, the PxGA may be used to adjust the colors for white balance, reducing the amount of digital processing that is needed. The four different gain values are switched according to the "Color Steering" circuitry. Seven different color steering modes for different types of CCD color filter arrays are programmed in the AD984xA's Control Register. For example, Mosaic Separate steering mode accommodates the popular "Bayer" arrangement of Red, Green, and Blue filters (see Figure 26).



Figure 25. AD9841A/AD9842A CCD-Mode Block Diagram



Figure 26. CCD Color Filter Example: Progressive Scan



Figure 27. CCD Color Filter Example: Interlaced

The same Bayer pattern can also be interlaced, and the VD Selected mode should be used with this type of CCD (see Figure 27). The Color Steering performs the proper multiplexing of the R, G, and B gain values (loaded into the PxGA gain registers), and is synchronized by the user with vertical (VD) and horizontal (HD) sync pulses. For more detailed information, see the PxGA Timing section. The PxGA gain for each of the four channels is variable from -2 dB to +10 dB, controlled in 64 steps through the serial interface. The PxGA gain curve is shown in Figure 28.



Figure 28. PxGA Gain Curve

Variable Gain Amplifier

The VGA stage provides a gain range of 2 dB to 36 dB, programmable with 10-bit resolution through the serial digital interface. Combined with 4 dB from the PxGA stage, the total gain range for the AD984xA is 6 dB to 40 dB. The minimum gain of 6 dB is needed to match a 1 V input signal with the ADC full-scale range of 2 V. When compared to 1 V full-scale systems (such as ADI's AD9803), the equivalent gain range is 0 dB to 34 dB.

The VGA gain curve is divided into two separate regions. When the VGA Gain Register code is between 0 and 511, the curve follows a (1 + x)/(1 - x) shape, which is similar to a "linear-indB" characteristic. From code 512 to code 1023, the curve follows a "linear-in-dB" shape. The exact VGA gain can be calculated for any Gain Register value by using the following two equations:

Code Range Gain Equation (dB)

 $\begin{array}{ll} 0-511 & Gain = 20 \log_{10} \left([658 + code] / [658 - code] \right) - 0.4 \\ 512 - 1023 & Gain = (0.0354) (code) - 0.4 \end{array}$

As shown in the CCD Mode Specifications, only the VGA gain range from 2 dB to 36 dB has tested and guaranteed accuracy. This corresponds to a VGA gain code range of 91 to 1023. The Gain Accuracy Specifications also include the PxGA gain of 4 dB, for a total gain range of 6 dB to 40 dB.



Figure 29. VGA Gain Curve (Gain from PxGA Not Included)

Optical Black Clamp

The optical black clamp loop is used to remove residual offsets in the signal chain, and to track low-frequency variations in the CCD's black level. During the optical black (shielded) pixel interval on each line, the ADC output is compared with a fixed black level reference, selected by the user in the Clamp Level Register. Any value between 0 LSB and 64 LSB (AD9841A) or 255 LSB (AD9842A) may be programmed, with 8-bit resolution. The resulting error signal is filtered to reduce noise, and the correction value is applied to the ADC input through a D/A converter. Normally, the optical black clamp loop is turned on once per horizontal line, but this loop can be updated more slowly to suit a particular application. If external digital clamping is used during the post processing, the AD984xA's optical black clamping may be disabled using Bit D5 in the Operation Register (see Serial Interface Timing and Internal Register Description section). When the loop is disabled, the Clamp Level Register may still be used to provide programmable offset adjustment.

Horizontal timing is shown in Figure 6. The CLPOB pulse should be placed during the CCD's optical black pixels. It is recommended that the CLPOB pulse duration be at least 20 pixels wide to minimize clamp noise. Shorter pulsewidths may be used, but clamp noise may increase, and the ability to track low-frequency variations in the black level will be reduced.

A/D Converter

The AD9841A and AD9842A use high-performance ADC architectures, optimized for high speed and low power. Differential Nonlinearity (DNL) performance is typically better than 0.5 LSB, as shown in TPCs 2 and 4. Instead of the 1 V full-scale range used by the earlier AD9801 and AD9803 products from Analog Devices, the AD984xA ADCs use a 2 V input range. Better noise performance results from using a larger ADC full-scale range (see TPCs 3 and 5).

AUX1 Mode

For applications that do not require CDS, the AD9841A/AD9842A can be configured to sample ac-coupled waveforms. Figure 30 shows the circuit configuration for using the AUX1 channel input (Pin 36). A single 0.1 μ F ac-coupling capacitor is needed between the input signal driver and the AUX1IN pin. An on-chip dc-bias circuit sets the average value of the input signal to approximately 0.4 V, which is referenced to the midscale code of the ADC. The VGA Gain register provides a gain range of 0 dB to 36 dB in this mode of operation (see VGA Gain Curve,

Figure 29). The VGA gains up the signal level with respect to the 0.4 V bias level. Signal levels above the bias level will be further increased to a higher ADC code, while signal levels below the bias level will be further decreased to a lower ADC code.

AUX2 Mode

For sampling video-type waveforms, such as NTSC and PAL signals, the AUX2 channel provides black level clamping, gain adjustment, and A/D conversion. Figure 31 shows the circuit configuration for using the AUX2 channel input (Pin 34). A external 0.1 μ F blocking capacitor is used with the on-chip video clamp circuit, to level-shift the input signal to a desired reference level. The clamp circuit automatically senses the most negative portion of the input signal, and adjusts the voltage across the input capacitor. This forces the black level of the input signal to be equal to the value programmed into the Clamp Level register (see Serial Interface Register Description). The VGA provides gain adjustment from 0 dB to 18 dB. The same VGA Gain register is used, but only the 9 MSBs of the gain register are used (see Table VIII.)



Figure 30. AUX1 Circuit Configuration



Figure 31. AUX2 Circuit Configuration

D 10	MSB D9	D 8	D 7	D6	D5	D 4	D3	D2	D 1	LSB D0	Gain (dB)
X	0	Х	Х	Х	Х	Х	Х	Х	Х	Х	0.0
	1	0	0	0	0	0	0	0	0	0	0.0
					•						•
					•						•
					•						•
	1	1	1	1	1	1	1	1	1	1	18.0

Table VIII. VGA Gain Register Used for AUX2-Mode

APPLICATIONS INFORMATION

The AD9841A and AD9842A are complete Analog Front End (AFE) products for digital still camera and camcorder applications. As shown in Figure 32, the CCD image (pixel) data is buffered and sent to the AD984xA analog input through a series input capacitor. The AD984xA performs the dc restoration, CDS, gain adjustment, black level correction, and analog-todigital conversion. The AD984xA's digital output data is then processed by the image processing ASIC. The internal registers of the AD984xA—used to control gain, offset level, and other functions—are programmed by the ASIC or microprocessor through a 3-wire serial digital interface. A system timing generator provides the clock signals for both the CCD and the AFE.



Figure 32. AD984xA System Applications Diagram



Figure 33. AD9841A Recommended Circuit Configuration for CCD-Mode



Figure 34. AD9842A Recommended Circuit Configuration for CCD-Mode

Internal Power-On Reset Circuitry

After power-on, the AD9842A will automatically reset all internal registers and perform internal calibration procedures. This takes approximately 1 ms to complete. During this time, normal clock signals and serial write operations may occur. However, serial register writes will be ignored until the internal reset operation is completed. Pin 43 (formerly RSTB on the AD9842A non-A) is no longer used for the reset operation. Toggling Pin 43 in the AD9842A will have no effect.

Grounding and Decoupling Recommendations

As shown in Figures 33 and 34, a single ground plane is recommended for the AD9841A/AD9842A. This ground plane should be as continuous as possible, particularly around Pins 25 through 39. This will ensure that all analog decoupling capacitors provide the lowest possible impedance path between the power and bypass pins and their respective ground pins. All decoupling capacitors should be located as close as possible to the package pins. A single clean power supply is recommended for the AD9841A/AD9842A, but a separate digital driver supply may be used for DRVDD (Pin 13). DRVDD should always be decoupled to DRVSS (Pin 14), which should be connected to the analog ground plane. Advantages of using a separate digital driver supply include using a lower voltage (2.7 V) to match levels with a 2.7 V ASIC, reducing digital power dissipation, and reducing potential noise coupling. If the digital outputs (Pins 3–12) must drive a load larger than 20 pF, buffering is recommended to reduce digital code transition noise. Alternatively, placing series resistors close to the digital output pins may also help reduce noise.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

