ANALOG DEVICES

High Speed, 3.3 V/5 V Quad 2:1 Mux/Demux (4-Bit, 1 of 2) Bus Switch
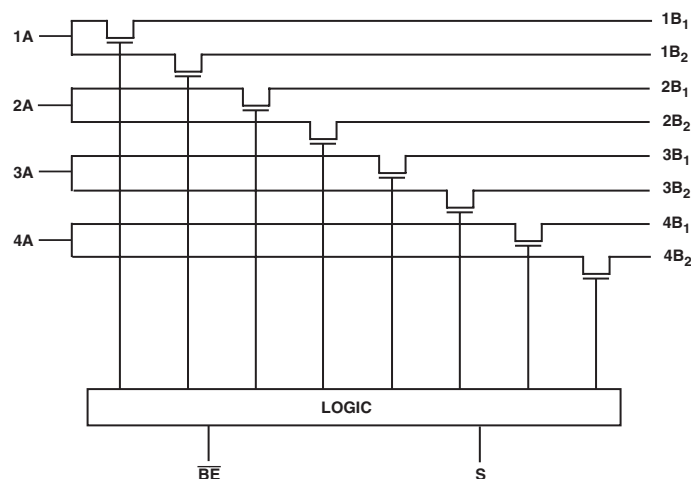
ADG3257

FEATURES
100 ps Propagation Delay through the Switch
2 Ω Switches Connect Inputs to Outputs
Data Rates up to 933 Mbps
Single 3.3 V/5 V Supply Operation
Level Translation Operation
Ultralow Quiescent Supply Current (1 nA Typical)
3.5 ns Switching
Standard '3257 Type Pinout

APPLICATIONS
Bus Switching
Bus Isolation
Level Translation
Memory Switching/Interleaving

FUNCTIONAL BLOCK DIAGRAM

GENERAL DESCRIPTION

The ADG3257 is a CMOS bus switch comprised of four 2:1 multiplexers/demultiplexers with high impedance outputs. The device is manufactured on a CMOS process. This provides low power dissipation yet high switching speed and very low ON resistance, allowing the inputs to be connected to the outputs without adding propagation delay or generating additional ground bounce noise.

The ADG3257 operates from a single 3.3 V/5 V supply. The control logic for each switch is shown in Table I. These switches are bidirectional when ON. In the OFF condition, signal levels are blocked up to the supplies.

This bus switch is suited to both switching and level translation applications. It may be used in applications requiring level translation from 3.3 V to 2.5 V when powered from 3.3 V. Additionally, with a diode connected in series with 5 V V_{DD}, the ADG3257 may also be used in applications requiring 5 V to 3.3 V level translation.

PRODUCT HIGHLIGHTS

1. 0.1 ns propagation delay through switch

2. 2 Ω switches connect inputs to outputs

3. Bidirectional operation

4. Ultralow power dissipation

5. 16-lead QSOP package

Table I. Truth Table

$\overline{BE}$	S	Function
H	X	DISABLE
L	L	A = B_1
L	H	A = B_2

REV. C

ADG3257–SPECIFICATIONS[1] (V_{CC} = 5.0 V ± 10%, GND = 0 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	Symbol	Conditions[2]	B Version Min	Typ[3]	Max	Unit
DC ELECTRICAL CHARACTERISTICS						
Input High Voltage	V_{INH}		2.4			V
Input Low Voltage	V_{INL}		−0.3		+0.8	V
Input Leakage Current	I_I	$0 \leq V_{IN} \leq 5.5$ V		±0.01	±1	µA
OFF State Leakage Current	I_{OZ}	$0 \leq A, B \leq V_{CC}$		±0.01	±1	µA
ON State Leakage Current	I_{OZ}	$0 \leq A, B \leq V_{CC}$		±0.01	±1	µA
Max Pass Voltage[4]	V_P	$V_{IN} = V_{CC} = 5$ V, $I_O = -5$ µA	3.9	4.2	4.4	V
CAPACITANCE[4]						
A Port OFF Capacitance	C_A OFF	f = 1 MHz		7		pF
B Port OFF Capacitance	C_B OFF	f = 1 MHz		5		pF
A, B Port ON Capacitance	C_A, C_B ON	f = 1 MHz		11		pF
Control Input Capacitance	C_{IN}	f = 1 MHz		4		pF
SWITCHING CHARACTERISTICS[4]						
Propagation Delay A to B or B to A t_{PD}	t_{PHL}, t_{PLH}[5]	$V_A = 0$ V, $C_L = 50$ pF			0.10	ns
Propagation Delay Matching[6]		$V_A = 0$ V, $C_L = 50$ pF		0.0075	0.035	ns
Bus Enable Time $\overline{BE}$ to A or B	t_{PZH}, t_{PZL}	$C_L = 50$ pF, $R_L = 500$ Ω	1	5	7.5	ns
Bus Disable Time $\overline{BE}$ to A or B	t_{PHZ}, t_{PLZ}	$C_L = 50$ pF, $R_L = 500$ Ω	1	3.5	7	ns
Bus Select Time S to A or B						
Enable	t_{SEL_EN}	$C_L = 50$ pF, $R_L = 500$ Ω		8	12	ns
Disable	t_{SEL_DIS}	$C_L = 50$ pF, $R_L = 500$ Ω		5	8	ns
Max Data Rate		$V_A = 2$ V p-p		933		Mbps
DIGITAL SWITCH						
ON Resistance	R_{ON}	$V_A = 0$ V				
		$I_O = 48$ mA, 15 mA, 8 mA, $T_A = 25°C$		2	3	Ω
		$I_O = 48$ mA, 15 mA, 8 mA			4	Ω
		$V_A = 2.4$ V				
		$I_O = 48$ mA, 15 mA, 8 mA, $T_A = 25°C$		3	5	Ω
		$I_O = 48$ mA, 15 mA, 8 mA			6	Ω
ON Resistance Matching	ΔR_{ON}	$V_A = 0$ V				
		48 mA, 15 mA, 8 mA, $T_A = 25°C$		0.15	0.35	Ω
		$V_A = 0$ V, 48 mA, 15 mA, 8 mA			0.7	Ω
POWER REQUIREMENTS						
V_{CC}			3.0		5.5	V
Quiescent Power Supply Current	I_{CC}	Digital Inputs = 0 V or V_{CC}		0.001	1	µA
Increase in I_{CC} per Input[7]	ΔI_{CC}	$V_{CC} = 5.5$ V, One Input at 3.0 V; Others at V_{CC} or GND			200	µA

NOTES
[1]Temperature range is as follows: B Version: −40°C to +85°C.
[2]See Test Circuits and Waveforms.
[3]All typical values are at $T_A = 25°C$, unless otherwise noted.
[4]Guaranteed by design, not subject to production test.
[5]The digital switch contributes no propagation delay other than the RC delay of the typical R_{ON} of the switch and the load capacitance when driven by an ideal voltage source. Since the time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the digital switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
[6]Propagation delay matching between channels is calculated from ON resistance matching of worst-case channel combinations and load capacitance.
[7]This current applies to the control pins only and represents the current required to switch internal capacitance at the specified frequency. The A and B ports contribute no significant ac or dc currents as they transition. This parameter is guaranteed by design, not subject to production test.

Specifications subject to change without notice.

REV. C

SPECIFICATIONS[1]

(V_{CC} = 3.3 V ± 10%, GND = 0 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	Symbol	Conditions[2]	B Version Min	B Version Typ[3]	B Version Max	Unit
DC ELECTRICAL CHARACTERISTICS						
Input High Voltage	V_{INH}		2.0			V
Input Low Voltage	V_{INL}		−0.3		+0.8	V
Input Leakage Current	I_I	$0 \leq V_{IN} \leq 3.6$ V		±0.01	±1	μA
OFF State Leakage Current	I_{OZ}	$0 \leq A, B \leq V_{CC}$		±0.01	±1	μA
ON State Leakage Current	I_{OZ}	$0 \leq A, B \leq V_{CC}$		±0.01	±1	μA
Max Pass Voltage[4]	V_P	$V_{IN} = V_{CC} = 3.3$ V, $I_O = -5$ μA	2.3	2.6	2.8	V
CAPACITANCE[4]						
A Port OFF Capacitance	C_A OFF	f = 1 MHz		7		pF
B Port OFF Capacitance	C_B OFF	f = 1 MHz		5		pF
A, B Port ON Capacitance	C_A, C_B ON	f = 1 MHz		11		pF
Control Input Capacitance	C_{IN}	f = 1 MHz		4		pF
SWITCHING CHARACTERISTICS[4]						
Propagation Delay A to B or B to A t_{PD}	t_{PHL}, t_{PLH}[5]	$V_A = 0$ V, $C_L = 50$ pF			0.10	ns
Propagation Delay Matching[6]		$V_A = 0$ V, $C_L = 50$ pF		0.01	0.04	ns
Bus Enable Time $\overline{BE}$ to A or B	t_{PZH}, t_{PZL}	$C_L = 50$ pF, $R_L = 500$ Ω	1	5.5	9	ns
Bus Disable Time $\overline{BE}$ to A or B	t_{PHZ}, t_{PLZ}	$C_L = 50$ pF, $R_L = 500$ Ω	1	4.5	8.5	ns
Bus Select Time S to A or B						
Enable	t_{SEL_EN}	$C_L = 50$ pF, $R_L = 500$ Ω		8	12	ns
Disable	t_{SEL_DIS}	$C_L = 50$ pF, $R_L = 500$ Ω		6	9	ns
Max Data Rate		$V_A = 2$ Vp-p		933		Mbps
DIGITAL SWITCH						
ON Resistance	R_{ON}	$V_A = 0$ V				
		$I_O = 15$ mA, 8 mA, $T_A = 25°C$		2	4	Ω
					4.5	Ω
		$V_A = 1.7$ V, $I_O = 15$ mA, $T_A = 25°C$		8	16.5	Ω
					18	Ω
		$V_A = 1.7$ V, $I_O = 8$ mA, $T_A = 25°C$		7	14	Ω
					17	Ω
ON Resistance Matching	ΔR_{ON}	$V_A = 0$ V, 15 mA, 8 mA, $T_A = 25°C$		0.2	0.4	Ω
		$V_A = 0$ V, 15 mA, 8 mA			0.8	Ω
POWER REQUIREMENTS						
V_{CC}			3.0		5.5	V
Quiescent Power Supply Current	I_{CC}	Digital Inputs = 0 V or V_{CC}		0.001	1	μA
Increase in I_{CC} per Input[7]	ΔI_{CC}	$V_{CC} = 3.3$ V, One Input at 3.0 V; Others at V_{CC} or GND			200	μA

NOTES

[1]Temperature range is as follows: B Version: −40°C to +85°C.
[2]See Test Circuits and Waveforms.
[3]All typical values are at $T_A = 25°C$, unless otherwise noted.
[4]Guaranteed by design, not subject to production test.
[5]The digital switch contributes no propagation delay other than the RC delay of the typical R_{ON} of the switch and the load capacitance when driven by an ideal voltage source. Since the time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the digital switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
[6]Propagation delay matching between channels is calculated from ON resistance matching of worst-case channel combinations and load capacitance.
[7]This current applies to the control pins only and represents the current required to switch internal capacitance at the specified frequency. The A and B ports contribute no significant ac or dc currents as they transition. This parameter is guaranteed by design, not subject to production test.

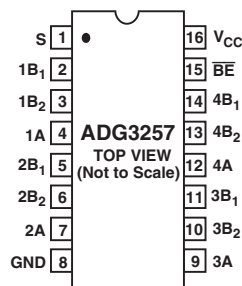Specifications subject to change without notice.

ADG3257

ABSOLUTE MAXIMUM RATINGS*

(T_A = 25°C, unless otherwise noted.)

V_{CC} to GND .... −0.3 V to +6 V
Digital Inputs to GND .... −0.3 V to +6 V
DC Input Voltage .... −0.3 V to +6 V
DC Output Current .... 100 mA
Operating Temperature Range
  Industrial (B Version) .... −40°C to +85°C
Storage Temperature Range .... −65°C to +150°C
Junction Temperature .... 150°C
QSOP Package
  θ_{JA} Thermal Impedance .... 149.97°C/W
Lead Temperature, Soldering (10 sec) .... 300°C
IR Reflow, Peak Temperature (<20 sec) .... 235°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

PIN CONFIGURATION

```
        ┌───┐ ┌───┐
    S  │1   •   16│ V_CC
   1B₁ │2       15│ BE
   1B₂ │3       14│ 4B₁
    1A │4  ADG3257  13│ 4B₂
   2B₁ │5  TOP VIEW 12│ 4A
       │  (Not to Scale)│
   2B₂ │6       11│ 3B₁
    2A │7       10│ 3B₂
   GND │8        9│ 3A
        └─────────┘
```

PIN FUNCTION DESCRIPTIONS

Mnemonic	Description
$\overline{BE}$	Output Enable (Active Low)
S	Port Select
Ax	Port A, Inputs or Outputs
Bx	Port B, Inputs or Outputs

ORDERING GUIDE

Model	Temperature Range	Package Descriptions	Package Option
ADG3257BRQ	−40°C to +85°C	RQ = 0.15" Quarter Size Outline Package (QSOP)	RQ-16

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG3257 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.
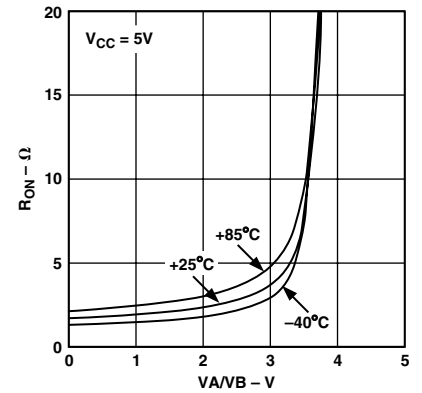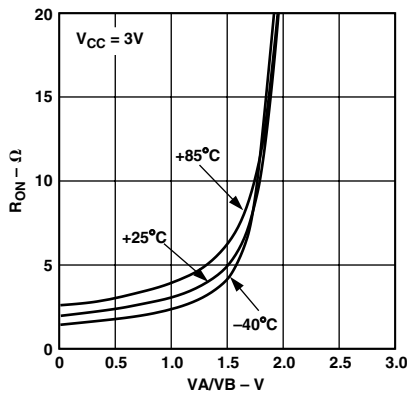
WARNING!

ESD SENSITIVE DEVICE

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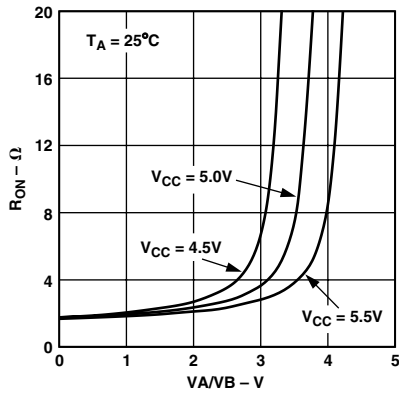
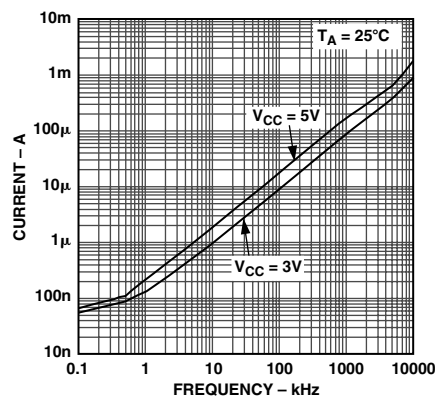TPC 1. ON Resistance vs. Input Voltage
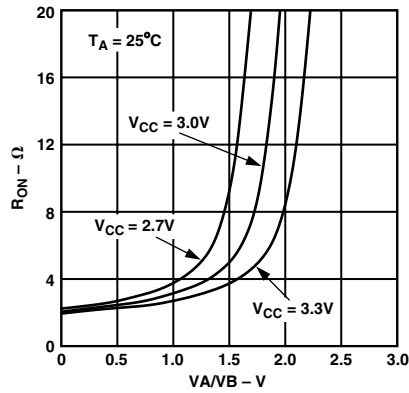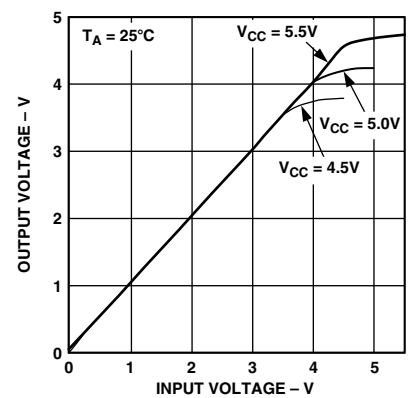
TPC 2. ON Resistance vs. Input Voltage

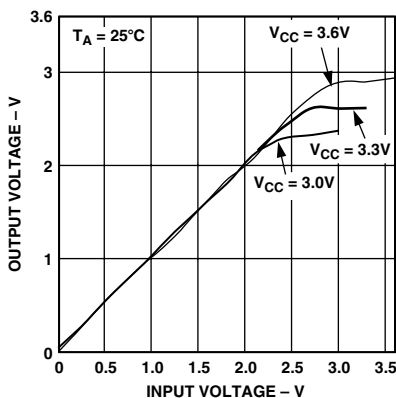TPC 3. ON Resistance vs. Input Voltage for Different Temperatures

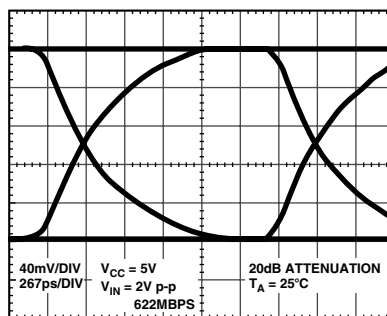TPC 4. ON Resistance vs. Input Voltage for Different Temperatures

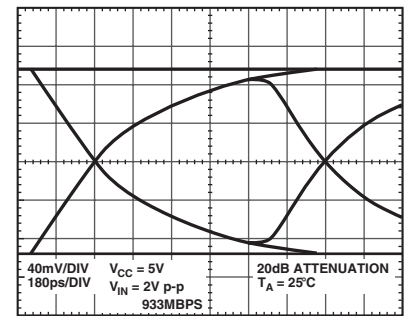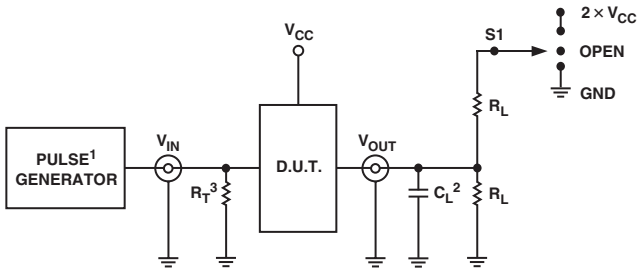TPC 5. I_{CC} vs. Enable Frequency

TPC 6. Max Pass Voltage

TPC 7. Max Pass Voltage

TPC 8. 622 Mbps Eye Diagram

TPC 9. 933 Mbps Eye Diagram

ADG3257

Figure 1. Load Circuit
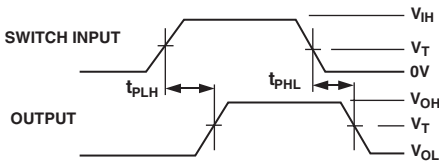
Figure 2. Propagation Delay
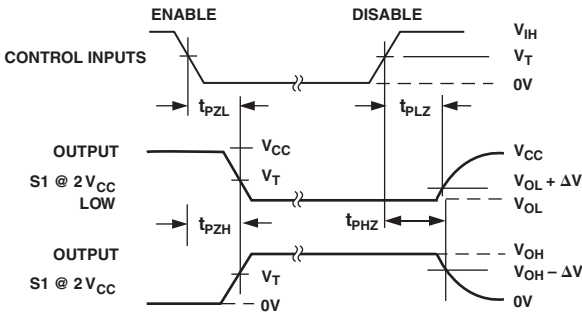
Figure 3. Select, Enable, and Disable Times

Table II. Switch S1 Condition

Test	S1
t_{PLH}, t_{PHL}	OPEN
t_{PLZ}, t_{PZL}	$2 \times V_{CC}$
t_{PHZ}, t_{PZH}	GND
t_{SEL}	OPEN

Table III. Test Conditions

Symbol	V_{CC} = 5 V ±10%	V_{CC} = 3.3 V ±10%	Unit
R_L	500	500	Ω
V_Δ	300	300	mV
C_L	50	50	pF

APPLICATIONS

Mixed Voltage Operation, Level Translation

Bus switches can be used to provide a solution for mixed voltage systems where interfacing bidirectionally between 5 V and 3 V devices is required. To interface between 5 V and 3.3 V buses, an external diode is placed in series with the 5 V power supply as shown in Figure 4.
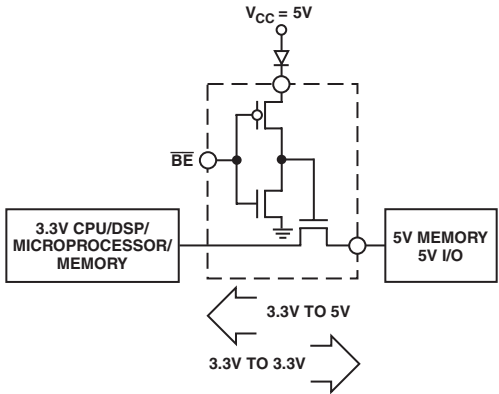

Figure 4. Level Translation Between 5 V and 3.3 V Devices

The diode drops the internal gate voltage down to 4.3 V. The bus switch limits the voltage present on the output to V_{CC} − external diode drop = V_{TH}.

Therefore, assuming a diode drop of 0.7 V and a V_{TH} of 1 V, the output voltage would be limited to 3.3 V with a logic high.
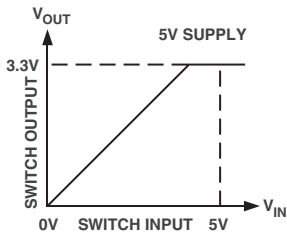

Figure 5. Input Voltage to Output Voltage

Similarly, the device could be used to translate bidirectionally between 3.3 V to 2.5 V systems. In this case, there is no need for an external diode. The internal V_{TH} drop is 1 V, so with a V_{CC} = 3.3 V the bus switch will limit the output voltage to V_{CC} − 1 V = 2.3 V.
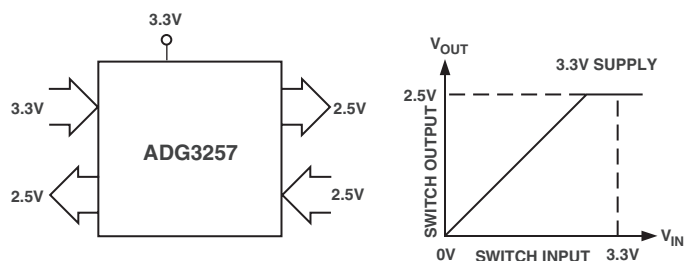
Figure 6. 3.3 V to 2.5 V Level Translation Using the ADG3257 Bus Switch

Memory Switching

This quad bus switch may be used to allow switching between different memory banks, thus allowing additional memory and decreasing capacitive loading. Figure 7 illustrates the ADG3257 in such an application.
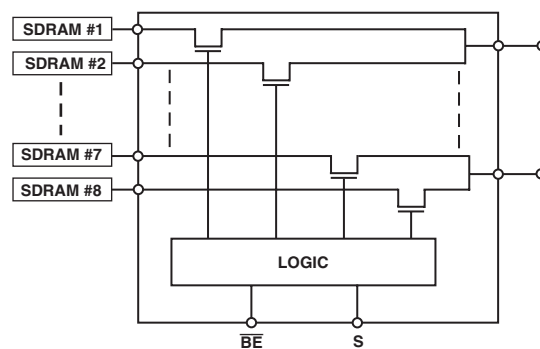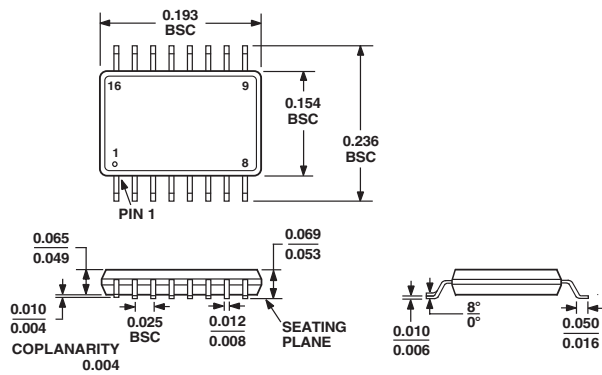

Figure 7. Allows Additional Memory Modules without Added Drive or Delay

ADG3257

OUTLINE DIMENSIONS

16-Lead Shrink Small Outline Package [QSOP]
(RQ-16)
Dimensions shown in inches

0.193
BSC

16   9

0.154
BSC

0.236
BSC

1   8

PIN 1

0.065
0.049

0.069
0.053

0.010
0.004

0.025
BSC

0.012
0.008

SEATING
PLANE

COPLANARITY
0.004

0.010
0.006

8°
0°

0.050
0.016

COMPLIANT TO JEDEC STANDARDS MO-137AB

Revision History