Complete 10-Bit, 25 MHz CCD Signal Processor

AD9943

FEATURES

25 MSPS Correlated Double Sampler (CDS)
6 dB to 40 dB 10-Bit Variable Gain Amplifier (VGA)
Low Noise Optical Black Clamp Circuit
Preblanking Function
10-Bit, 25 MSPS A/D Converter
No Missing Codes Guaranteed
3-Wire Serial Digital Interface
3 V Single-Supply Operation
Space-Saving 32-Lead 5 mm × 5 mm LFCSP Package

APPLICATIONS

Digital Still Cameras
Digital Video Camcorders
PC Cameras
Portable CCD Imaging Devices
CCTV Cameras

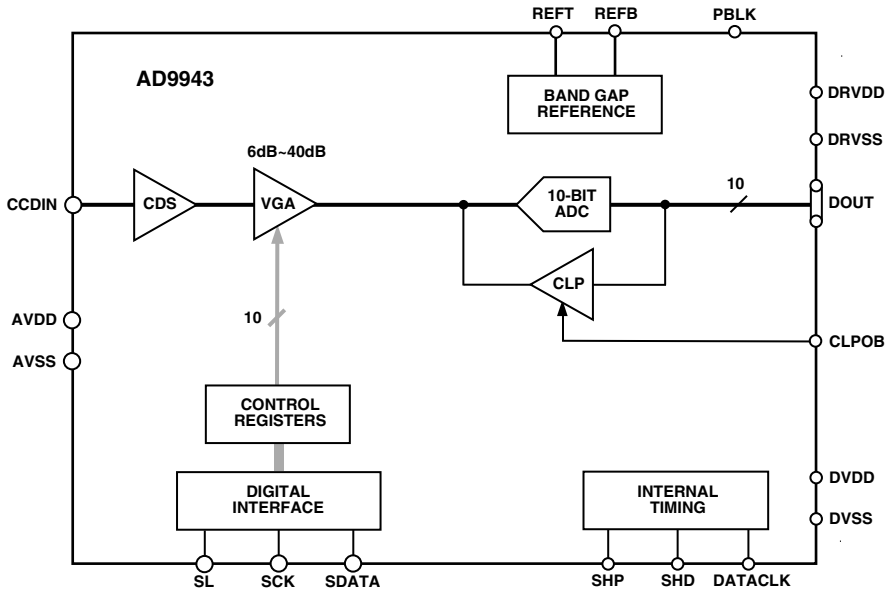
GENERAL DESCRIPTION

The AD9943 is a complete analog signal processor for CCD applications. It features a 25 MHz single-channel architecture designed to sample and condition the outputs of interlaced and progressive scan area CCD arrays. The AD9943's signal chain consists of a correlated double sampler (CDS), digitally controlled variable gain amplifier (VGA), black level clamp, and a 10-bit A/D converter.

The internal registers are programmed through a 3-wire serial digital interface. Programmable features include gain adjustment, black level adjustment, input clock polarity, and power-down modes.

The AD9943 operates from a single 3 V power supply, typically dissipates 79 mW, and is packaged in a space-saving 32-lead LFCSP.

FUNCTIONAL BLOCK DIAGRAM



REV. 0

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AD9943–SPECIFICATIONS

GENERAL SPECIFICATIONS (T_{MIN} to T_{MAX}, AVDD = DVDD = DRVDD = 3.0 V, f_{SAMP}= 25 MHz, unless otherwise noted.)

Parameter	Min	Typ	Max	Unit
TEMPERATURE RANGE				
Operating	–20		+85	°C
Storage	–65		+150	°C
POWER SUPPLY VOLTAGE				
Analog, Digital, Digital Driver	2.7		3.6	V
POWER CONSUMPTION				
Normal Operation		79		mW
Power-Down Mode		150		µW
MAXIMUM CLOCK RATE	25			MHz

Specifications subject to change without notice.

DIGITAL SPECIFICATIONS (DRVDD = DVDD = 2.7 V, C_L = 20 pF, unless otherwise noted.)

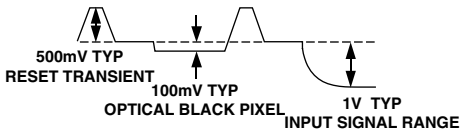
Parameter	Symbol	Min	Typ	Max	Unit
LOGIC INPUTS					
High Level Input Voltage	V_{IH}	2.1			V
Low Level Input Voltage	V_{IL}			0.6	V
High Level Input Current	I_{IH}		10		µA
Low Level Input Current	I_{IL}		10		µA
Input Capacitance	C_{IN}		10		pF
LOGIC OUTPUTS					
High Level Output Voltage, I_{OH} = 2 mA	V_{OH}	2.2			V
Low Level Output Voltage, I_{OL} = 2 mA	V_{OL}			0.5	V

Specifications subject to change without notice.

SYSTEM SPECIFICATIONS (T_{MIN} to T_{MAX}, AVDD = DVDD = DRVDD = 3.0 V, f_{SAMP} = 25 MHz, unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Notes
CDS					
Max Input Range before Saturation*		1.0		V p-p	
Allowable CCD Reset Transient*		500		mV	See Input Waveform in Footnote
Max CCD Black Pixel Amplitude*		100		mV	
VARIABLE GAIN AMPLIFIER (VGA)					
Gain Control Resolution		1024		Steps	
Gain Monotonicity		Guaranteed			
Gain Range					
Min Gain		5.3		dB	See Figure 7 for VGA Gain Curve
Max Gain	40.0	41.5		dB	See Variable Gain Amplifier section for VGA Gain Equation
BLACK LEVEL CLAMP					
Clamp Level Resolution		256		Steps	
Clamp Level					Measured at ADC Output
Min Clamp Level		0		LSB	
Max Clamp Level		63.75		LSB	
A/D CONVERTER					
Resolution	10			Bits	
Differential Nonlinearity (DNL)		±0.3		LSB	
No Missing Codes		Guaranteed			
Data Output Coding		Straight Binary			
Full-Scale Input Voltage		2.0		V	
VOLTAGE REFERENCE					
Reference Top Voltage (REFT)		2.0		V	
Reference Bottom Voltage (REFB)		1.0		V	
SYSTEM PERFORMANCE					Specifications Include Entire Signal Chain
Gain Range					
Low Gain (VGA Code = 0)		5.3		dB	
Max Gain (VGA Code = 1023)	40.0	41.5		dB	
Gain Accuracy		±1.0		dB	
Peak Nonlinearity 500 mV Input Signal		0.1		%	
Total Output Noise		0.3		LSB rms	12 dB Gain Applied
Power Supply Rejection (PSR)		50		dB	AC Grounded Input, 6 dB Gain Applied

*Input Signal Characteristics defined as follows:



Specifications subject to change without notice.

TIMING SPECIFICATIONS (C_L = 20 pF, f_{SAMP} = 25 MHz, CCD Mode Timing in Figures 8 and 9, Serial Timing in Figures 4 and 5.)

Parameter	Symbol	Min	Typ	Max	Unit
SAMPLE CLOCKS					
DATACLK, SHP, SHD Clock Period	t_{CONV}	40			ns
DATACLK High/Low Pulsewidth	t_{ADC}	16	20		ns
SHP Pulsewidth	t_{SHP}		10		ns
SHD Pulsewidth	t_{SHD}		10		ns
CLPOB Pulsewidth*	t_{COB}	2	20		Pixels
SHP Rising Edge to SHD Falling Edge	t_{S1}		10		ns
SHP Rising Edge to SHD Rising Edge	t_{S2}	16	20		ns
Internal Clock Delay	t_{ID}		3.0		ns
DATA OUTPUTS					
Output Delay	t_{OD}		9.5		ns
Pipeline Delay			9		Cycles
SERIAL INTERFACE					
Maximum SCK Frequency	f_{SCLK}	10			MHz
SL to SCK Setup Time	t_{LS}	10			ns
SCK to SL Hold Time	t_{LH}	10			ns
SDATA Valid to SCK Rising Edge Setup	t_{DS}	10			ns
SCK Falling Edge to SDATA Valid Hold	t_{DH}	10			ns

*Minimum CLPOB pulsewidth is for functional operation only. Wider typical pulses are recommended to achieve low noise clamp performance.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Parameter	With Respect To	Min	Max	Unit
AVDD	AVSS	–0.3	+3.9	V
DVDD	DVSS	–0.3	+3.9	V
DRVDD	DRVSS	–0.3	+3.9	V
Digital Outputs	DRVSS	–0.3	DRVDD + 0.3	V
SHP, SHD, DATACLK	DVSS	–0.3	DVDD + 0.3	V
CLPOB, PBLK	DVSS	–0.3	DVDD + 0.3	V
SCK, SL, SDATA	DVSS	–0.3	DVDD + 0.3	V
REFT, REFB, CCDIN	AVSS	–0.3	AVDD + 0.3	V
Junction Temperature			150	°C
Lead Temperature (10 sec)			300	°C

*Stresses above those listed in Absolute Maximum Ratings may cause permanent change to the device. This is a stress rating only; functional operation of the device at these or any other conditions above these listed in the operational section is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9943	–20°C to +85°C	Lead Frame Chip Scale (LFCSP)	CP-32

THERMAL CHARACTERISTICS

Thermal Resistance (with exposed bottom pad soldered to board GND)

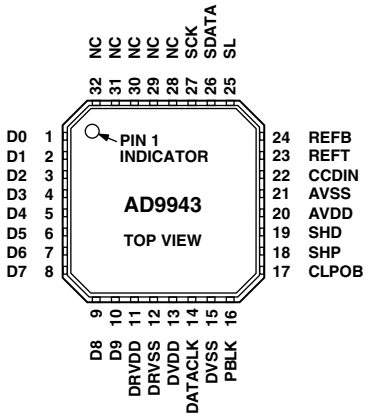
32-Lead LFCSP Package

θ_{JA} = 27.7°C/W

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9943 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTION

Pin No.	Mnemonic	Type	Description
1–10	D0–D9	DO	Digital Data Outputs
11	DRVDD	P	Digital Output Driver Supply
12	DRVSS	P	Digital Output Driver Ground
13	DVDD	P	Digital Supply
14	DATACLK	DI	Digital Data Output Latch Clock
15	DVSS	P	Digital Supply Ground
16	PBLK	DI	Preblanking Clock Input
17	CLPOB	DI	Black Level Clamp Clock Input
18	SHP	DI	CDS Sampling Clock for CCD's Reference Level
19	SHD	DI	CDS Sampling Clock for CCD's Data Level
20	AVDD	P	Analog Supply
21	AVSS	P	Analog Ground
22	CCDIN	AI	Analog Input for CCD Signal
23	REFT	AO	A/D Converter Top Reference Voltage Decoupling
24	REFB	AO	A/D Converter Bottom Reference Voltage Decoupling
25	SL	DI	Serial Digital Interface Load Pulse
26	SDATA	DI	Serial Digital Interface Data Input
27	SCK	DI	Serial Digital Interface Clock Input
28	NC	NC	Internally Pulled Down. Float or connect to GND.
29	NC	NC	Internally Pulled Down. Float or connect to GND.
30	NC	NC	Internally Pulled Down. Float or connect to GND.
31	NC	NC	Internally Not Connected
32	NC	NC	Internally Not Connected

TYPE: AI = Analog Input, AO = Analog Output, DI = Digital Input, DO = Digital Output, P = Power.

DEFINITIONS OF SPECIFICATIONS

Differential Nonlinearity (DNL)
An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Thus every code must have a finite width. No missing codes guaranteed to 10-bit resolution indicates that all 1024 codes, respectively, must be present over all operating conditions.

Peak Nonlinearity
Peak nonlinearity, a full signal chain specification, refers to the peak deviation of the output of the AD9943 from a true straight line. The point used as zero scale occurs 1/2 LSB before the first code transition. Positive full scale is defined as a Level 1 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each particular output code to the true straight line. The error is then expressed as a percentage of the 2 V ADC full-scale signal. The input signal is always appropriately gained up to fill the ADC's full-scale range.

EQUIVALENT INPUT CIRCUITS

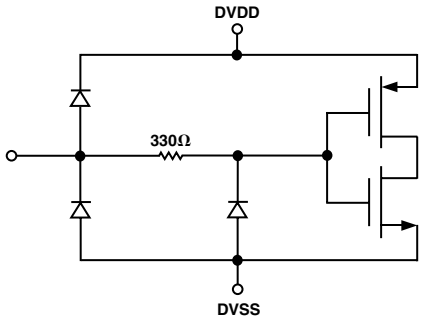


Figure 1. Digital Inputs—SHP, SHD, DATACLK, CLPOB, PBLK, SCK, SL

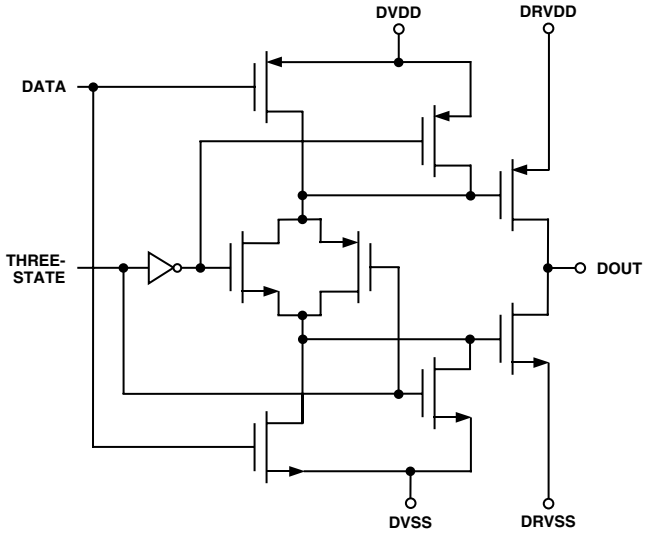


Figure 2. Data Outputs—D0–D9

Total Output Noise
The rms output noise is measured using histogram techniques. The standard deviation of the ADC output codes is calculated in LSB, and represents the rms noise level of the total signal chain at the specified gain setting. The output noise can be converted to an equivalent voltage, using the relationship 1 LSB = (ADC Full Scale/2^N codes) where N is the bit resolution of the ADC. For the AD9943, 1 LSB is 1.95 mV.

Power Supply Rejection (PSR)
The PSR is measured with a step change applied to the supply pins. This represents a very high frequency disturbance on the AD9943's power supply. The PSR specification is calculated from the change in the data outputs for a given step change in the supply voltage.

Internal Delay for SHP/SHD
The internal delay (also called aperture delay) is the time delay that occurs from when a sampling edge is applied to the AD9943 until the actual sample of the input signal is held. Both SHP and SHD sample the input signal during the transition from low to high, so the internal delay is measured from each clock's rising edge to the instant the actual internal sample is taken.

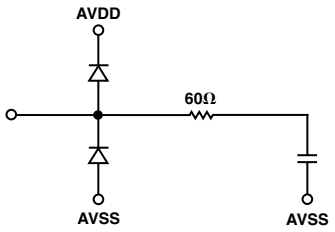
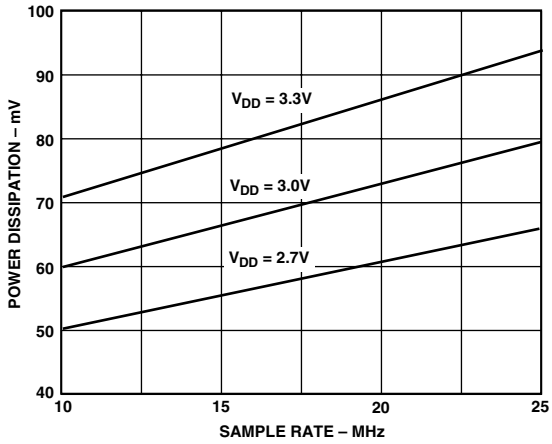
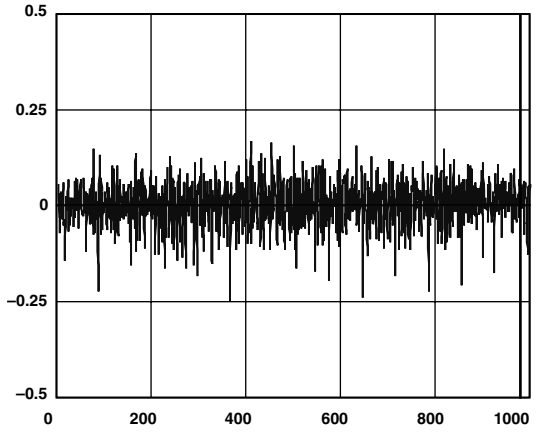


Figure 3. CCDIN (Pin 22)



TPC 1. Power vs. Sample Rate



TPC 2. Typical DNL Performance

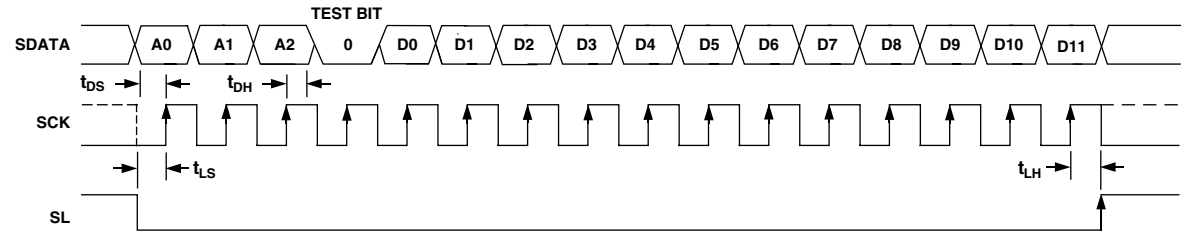
INTERNAL REGISTER DESCRIPTION

Table I. Internal Register Map

Register Name	Address Bits A2	A1	A0	Data Bits	Function
Operation	0	0	0	D0	Software Reset (0 = Normal Operation, 1 = Reset all registers to default)
				D2, D1	Power-Down Modes (00 = Normal Power, 01 = Standby, 10 = Total Shutdown)
				D3	OB Clamp Disable (0 = Clamp ON, 1 = Clamp OFF)
				D5, D4	Test Mode. Should always be set to 00.
				D6	PBLK Blanking Level (0 = Blank Output to Zero, 1 = Blank to OB Clamp Level)
				D8, D7	Test Mode 1. Should always be set to 00.
				D11–D9	Test Mode 2. Should always be set to 000.
Control	0	0	1	D0	SHP/SHD Input Polarity (0 = Active Low, 1 = Active High)
				D1	DATACLK Input Polarity (0 = Active Low, 1 = Active High)
				D2	CLPOB Input Polarity (0 = Active Low, 1 = Active High)
				D3	PBLK Input Polarity (0 = Active Low, 1 = Active High)
				D4	Three-State Data Outputs (0 = Outputs Active, 1 = Outputs Three-Stated)
				D5	Data Output Latching (0 = Latched by DATACLK, 1 = Latch is Transparent)
				D6	Data Output Coding (0 = Binary Output, 1 = Gray Code Output)
				D11–D7	Test Mode. Should always be set to 00000.
Clamp Level	0	1	0	D7–D0	OB Clamp Level (0 = 0 LSB, 255 = 63.75 LSB)
VGA Gain	0	1	1	D9–D0	VGA Gain (0 = 6 dB, 1023 = 40 dB)

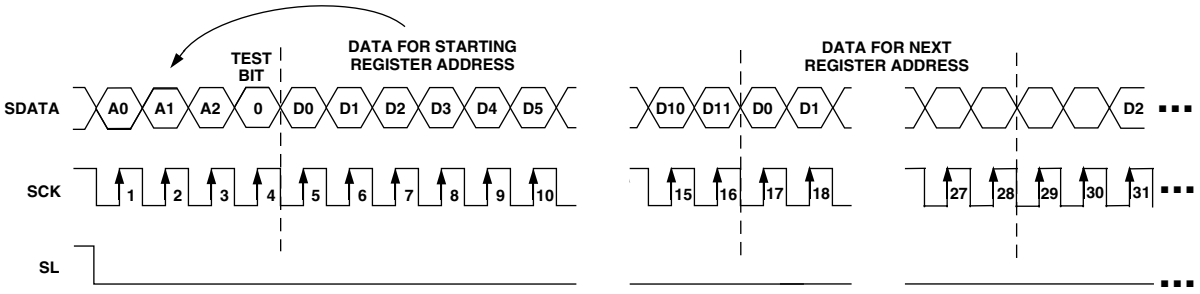
All register values default to x000 at power-up except Clamp Level, which defaults to 128 decimal (32 LSB clamp level).

SERIAL INTERFACE



NOTES
1. SDATA BITS ARE INTERNALLY LATCHED ON THE RISING EDGES OF SCK.
2. SYSTEM UPDATE OF LOADED REGISTERS OCCURS ON SL RISING EDGE.
3. ALL 12 DATA BITS D0–D11 MUST BE WRITTEN. IF THE REGISTER CONTAINS FEWER THAN 12 BITS, ZEROS SHOULD BE USED FOR THE UNDEFINED BITS.
4. TEST BIT IS FOR INTERNAL USE ONLY. MUST BE SET LOW.

Figure 4. Serial Write Operation



NOTES
1. MULTIPLE SEQUENTIAL REGISTERS MAY BE LOADED CONTINUOUSLY.
2. THE FIRST (LOWEST ADDRESS) REGISTER ADDRESS IS WRITTEN, FOLLOWED BY MULTIPLE 12-BIT DATA-WORDS.
3. THE ADDRESS WILL AUTOMATICALLY INCREMENT WITH EACH 12-BIT DATA-WORD (ALL 12 BITS MUST BE WRITTEN).
4. SL IS HELD LOW UNTIL THE LAST DESIRED REGISTER HAS BEEN LOADED.
5. NEW DATA IS UPDATED AT THE NEXT SL RISING EDGE.

Figure 5. Continuous Serial Write Operation to All Registers

CIRCUIT DESCRIPTION AND OPERATION

The AD9943 signal processing chain is shown in Figure 6. Each processing step is essential in achieving a high quality image from the raw CCD pixel data.

DC Restore

To reduce the large dc offset of the CCD output signal, a dc-restore circuit is used with an external 0.1 µF series coupling capacitor. This restores the dc level of the CCD signal to approximately 1.5 V to be compatible with the 3 V single supply of the AD9943.

Correlated Double Sampler

The CDS circuit samples each CCD pixel twice to extract the video information and reject low frequency noise. The timing shown in Figure 8 illustrates how the two CDS clocks, SHP and SHD, are used to sample the reference level and data level of the CCD signal, respectively. The CCD signal is sampled on the rising edges of SHP and SHD. Placement of these two clock signals is critical in achieving the best performance from the CCD. An internal SHP/SHD delay (t_{ID}) of 3 ns is caused by internal propagation delays.

Optical Black Clamp

The optical black clamp loop is used to remove residual offsets in the signal chain and to track low frequency variations in the CCD's black level. During the optical black (shielded) pixel interval on each line, the ADC output is compared with the fixed black level reference, selected by the user in the clamp level register. Any value between 0 LSB and 255 LSB may be programmed with 8-bit resolution. The resulting error signal is filtered to reduce noise, and the correction value is applied to the ADC input through a D/A converter. Normally, the optical black clamp loop is turned on once per horizontal line, but this loop can be updated more slowly to suit a particular application. If external digital clamping is used during the post processing, the AD9943 optical black clamping may be disabled using Bit D3 in the operation register (see the Serial Interface Timing and Internal Register Description section).

When the loop is disabled, the clamp level register may still be used to provide programmable offset adjustment.

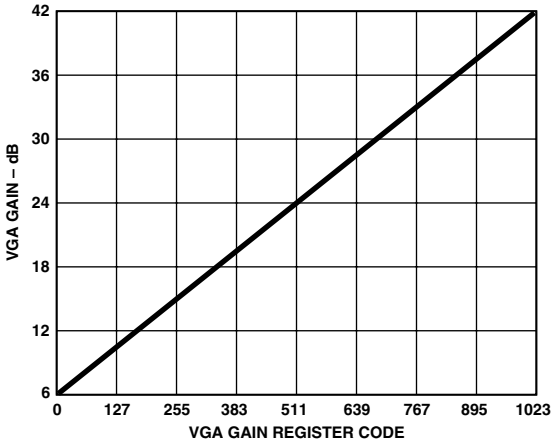


Figure 7. VGA *Gain Curve*

Horizontal timing is shown in Figure 9. The CLPOB pulse should be placed during the CCD's optical black pixels. It is recommended that the CLPOB pulse be used during valid CCD dark pixels. The CLPOB pulse should be a minimum of 20 pixels wide to minimize clamp noise. Shorter pulsewidths may be used, but clamp noise may increase and the loop's ability to track low frequency variations in the black level will be reduced.

A/D Converter

The ADC uses a 2 V input range. Better noise performance results from using a larger ADC full-scale range. The ADC uses a pipelined architecture with a 2 V full-scale input for low noise performance.

Variable Gain Amplifier

The VGA stage provides a gain range of 6 dB to 40 dB, programmable with 10-bit resolution through the serial digital interface. The minimum gain of 6 dB is needed to match a 1 V input signal with the ADC full-scale range of 2 V. A plot of the VGA gain curve is shown in Figure 7.

$$VGA\ Gain\ (dB) = (VGA\ Code \times 0.035\ dB) + 5.3\ dB$$

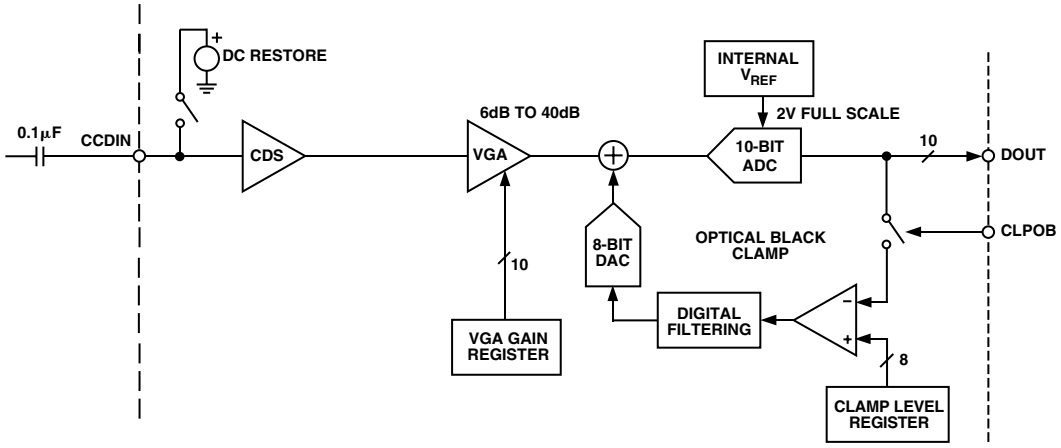
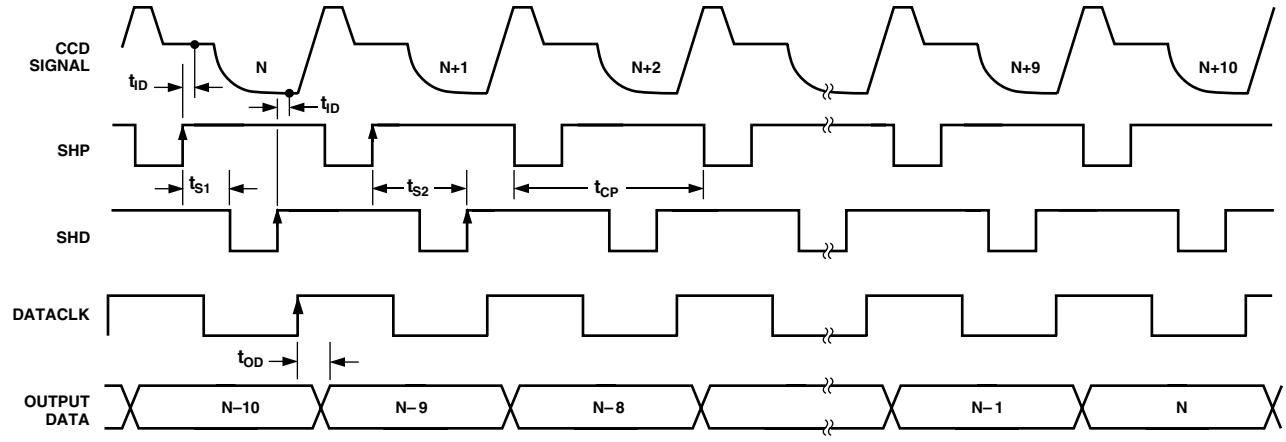


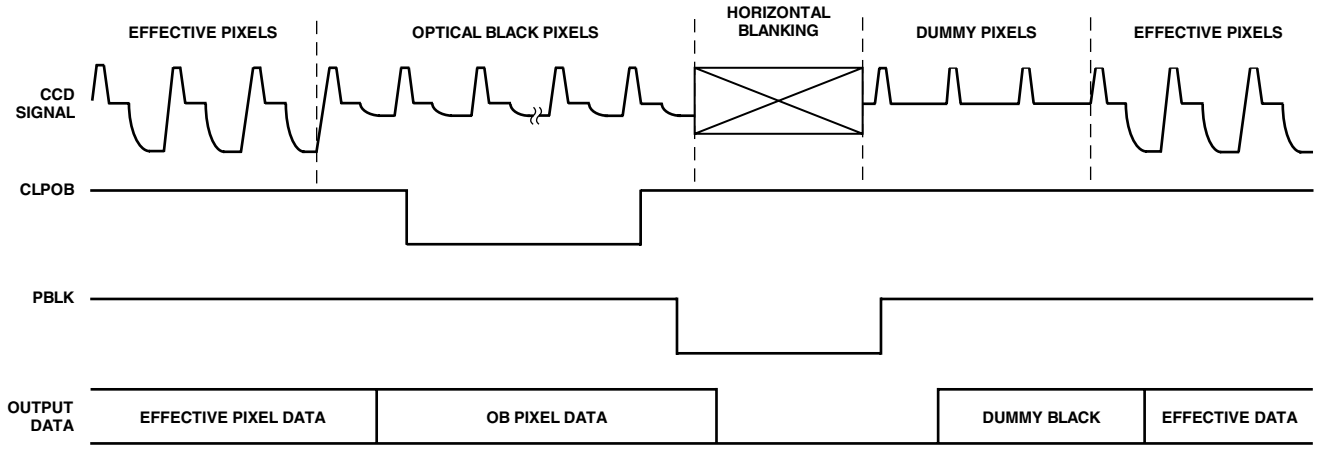
Figure 6. CCD Mode Block Diagram

CCD-MODE AND AUX MODE TIMING



NOTES
1. RECOMMENDED PLACEMENT FOR DATACLK RISING EDGE IS BETWEEN THE SHD RISING EDGE AND NEXT SHP FALLING EDGE.
2. CCD SIGNAL IS SAMPLED AT SHP AND SHD RISING EDGES.

Figure 8. CCD Mode Timing



NOTES
1. CLPOB WILL OVERWRITE PBLK. PBLK WILL NOT AFFECT CLAMP OPERATION IF OVERLAPPING WITH CLPOB.
2. PBLK SIGNAL IS OPTIONAL.
3. DIGITAL OUTPUT DATA WILL BE ALL ZEROS DURING PBLK. OUTPUT DATA LATENCY IS NINE DATACLK CYCLES.

Figure 9. Typical CCD Mode Line Clamp Timing

APPLICATIONS INFORMATION

The AD9943 is a complete analog front end (AFE) product for digital still camera and camcorder applications. As shown in Figure 6, the CCD image (pixel) data is buffered and sent to the AD9943 analog input through a series input capacitor. The AD9943 performs the dc restoration, CDS, gain adjustment, black level correction, and analog-to-digital conversion.

The AD9943's digital output data is then processed by the image processing ASIC. The internal registers of the AD9943—used to control gain, offset level, and other functions—are programmed by the ASIC or microprocessor through a 3-wire serial digital interface. A system timing generator provides the clock signals for both the CCD and the AFE.

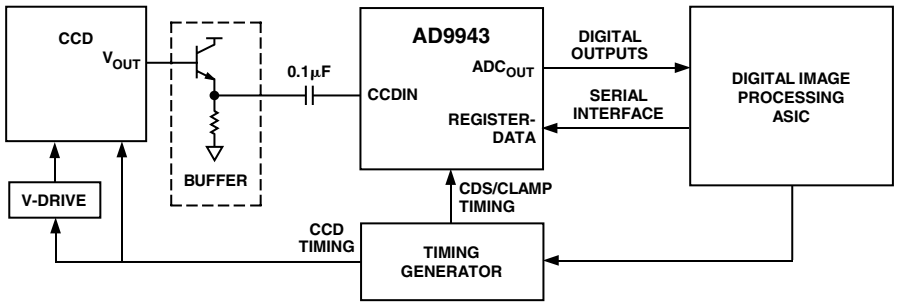


Figure 10. System Applications Diagram

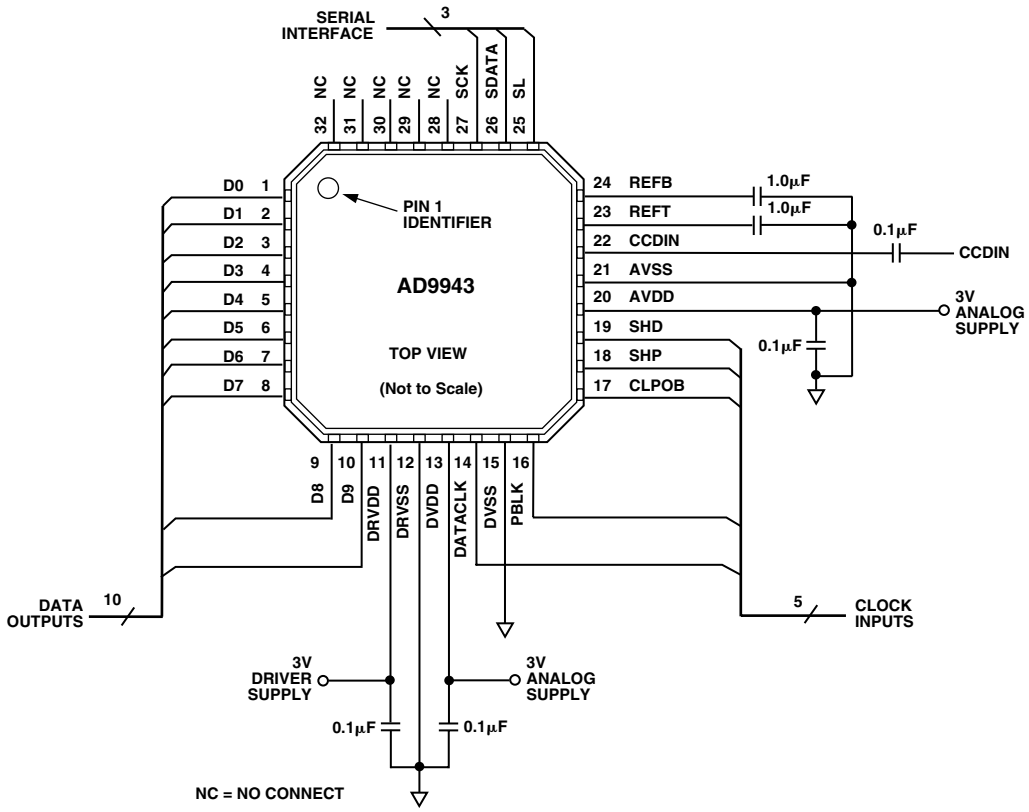


Figure 11. Recommended Circuit Configuration for CCD Mode

Internal Power-On Reset Circuitry

After power-on, the AD9943 will automatically reset all internal registers and perform internal calibration procedures. This takes approximately 1 ms to complete. During this time, normal clock signals and serial write operations may occur. However, serial register writes will be ignored until the internal reset operation is completed.

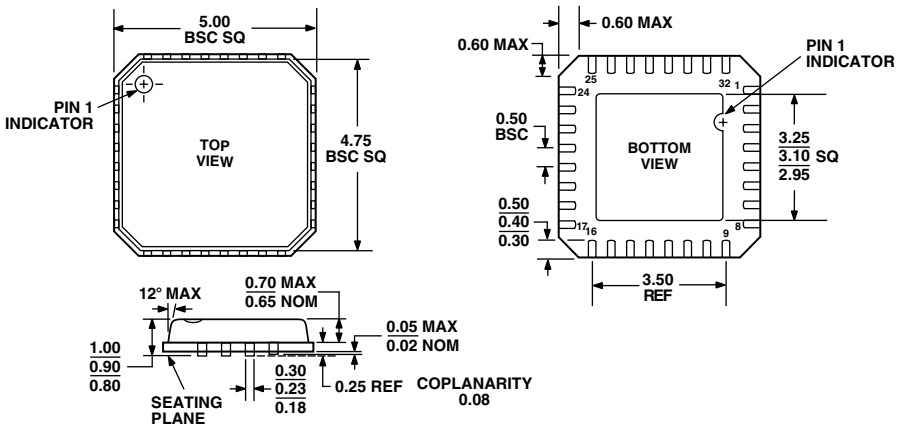
Grounding and Decoupling Recommendations

As shown in Figure 11, a single ground plane is recommended for the AD9943. This ground plane should be as continuous as possible. This will ensure that all analog decoupling capacitors provide the lowest possible impedance path between the power and bypass pins and their respective ground pins. All decoupling capacitors should be located as close as possible to the package pins. A single clean power supply is recommended for the AD9943, but a separate digital driver supply may be used for DRVDD (Pin 11). DRVDD should always be decoupled to DRVSS (Pin 12), which should be connected to the analog ground plane. Advantages of using a separate digital driver supply include using a lower voltage (2.7 V) to match levels with a 2.7 V ASIC, reducing digital power dissipation and reducing potential noise coupling. If the digital outputs (Pins 1–10) must drive a load larger than 20 pF, buffering is recommended to reduce digital code transition noise. Alternatively, placing series resistors close to the digital output pins may also help reduce noise.

NOTE: The exposed pad on the bottom of the AD9943 should be soldered to the GND plane of the printed circuit board.

OUTLINE DIMENSIONS

32-Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm Body
(CP-32)
Dimensions shown in millimeters



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