High Performance 12-Bit, 6-Channel Output, Decimating LCD DecDriver®

AD8382

PRODUCT FEATURES

High accuracy, high resolution voltage outputs
- **12-bit input resolution**
- **Laser trimmed outputs**

Fast settling, high voltage drive
- **33 ns settling time to 0.25% into 200 pF load**
- **Slew rate 390 V/µs**
- **Outputs to within 1.3 V of supply**

High update rates
- **Fast, 120 Ms/s data update rate**

Voltage controlled video reference (brightness) and full-scale (contrast) output levels

Flexible logic
- **STSQ/XFR allow parallel AD8382 operation**
- **INV bit reverses polarity of video signal**

Output overload protection

Low static power dissipation: 743 mW
- **Includes STBY function**

3.3 V logic, 9 V to 18 V analog supplies

Available in 48-lead 7 mm × 7 mm LFCSP

APPLICATIONS

LCD analog column driver

PRODUCT DESCRIPTION

The AD8382 DecDriver provides a fast, 12-bit latched decimating digital input that drives six high voltage outputs.12-bit input words are sequentially loaded into six separate, high speed, bipolar DACs. A flexible digital input format allows several AD8382s to be used in parallel for higher resolution displays.

STSQ synchronizes sequential input loading, XFR controls synchronous output updating, and R/L controls the direction of loading as either left-to-right or right-to-left. Six channels of high voltage output drivers drive to within 1.3 V of the rail. The output signal can be adjusted for dc reference, signal inversion, and contrast for maximum flexibility.

The AD8382 is fabricated on Analog Devices' XFHV, fast bipolar 26 V process, providing fast input logic bipolar DACs with trimmed accuracy and fast settling, high voltage, precision drive amplifiers on the same chip. The AD8382 dissipates 743 mW nominal static power. The STBY pin reduces power to a minimum, with fast recovery.

FUNCTIONAL BLOCK DIAGRAM

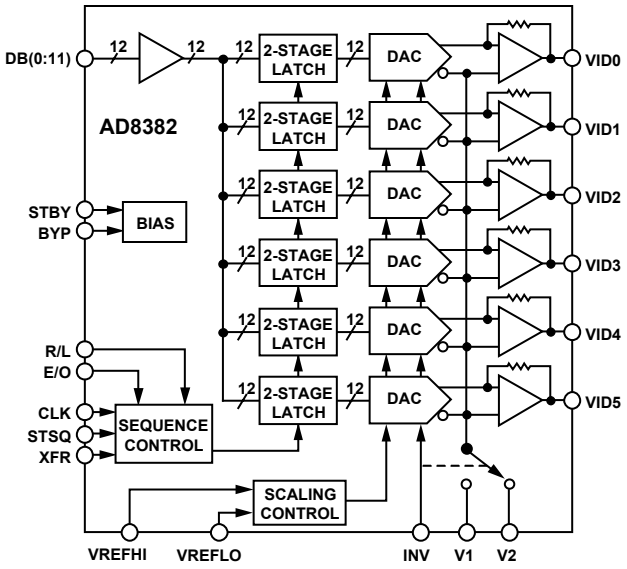

Figure 1. Functional Block Diagram

Rev. 0

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REVISION HISTORY

Revision 0: Initial Version

SPECIFICATIONS

Table 1. @ 25°C, AVCC = 15.5 V, DVCC = 3.3 V, T_{MIN} = 0°C, T_{MAX} = 85°C, VREFHI = 9.5 V, VREFLO = V1 = V2 = 7 V, unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Unit
VIDEO DC PERFORMANCE[1]	T_{MIN} to T_{MAX}				
VDE	DAC Code 1500 to 3200	−5		+5	mV
VCME	DAC Code 1500 to 3200	−3.5	+0.5	+3.5	mV
ΔV	DAC Code 2048		2.5	7.5	mV
ΔV	DAC Code 0 to 4095		4	15	mV
VIDEO OUTPUT DYNAMIC PERFORMANCE	$T_{C, MIN}$ to $T_{C, MAX}$, V_O = 5 V Step, C_L = 200 pF				
Data Switching Slew Rate	20% to 80%		390		V/μs
Invert Switching Slew Rate	20% to 80%		530		V/μs
Data Switching Settling Time to 1%			22	27	ns
Data Switching Settling Time to 0.25%			33	50	ns
Invert Switching Settling Time to 1%			34	100	ns
Invert Switching Settling Time to 0.25%			130	300	ns
Invert Switch Overshoot			100	200	mV
CLK and Data Feedthrough[2]			10		mV p-p
All-Hostile Crosstalk[3]					
Amplitude			40		mV p-p
Duration			30		ns
DAC Transition Glitch Energy	Code 2047 to Code 2048		0.3		nV-s
VIDEO OUTPUT CHARACTERISTICS					
Output Voltage Swing	AVCC – VOH, VOL– AGND		1.1	1.3	V
CLK to VID Delay: t_9[4]	50% of VIDx	10	12	14	ns
INV to VID Delay: t_{10}	50% of VIDx	10.4	12.4	14.4	ns
Output Current			100		mA
Output Resistance			22		Ω
RESOLUTION					
Coding	Binary	12			Bits
DIGITAL INPUT CHARACTERISTICS	Input t_r, t_f = 2 ns (10% to 90%)				
Max. Input Data Update Rate		120			Ms/s
Data Setup Time: t_1		0			ns
STSQ Setup Time: t_3		1			ns
XFR Setup Time: t_5		1			ns
Data Hold Time: t_2		3			ns
STSQ Hold Time: t_4		3			ns
XFR Hold Time: t_6		3			ns
CLK High Time: t_7		3			ns
CLK Low Time: t_8		2.5			ns
C_{IN}				3	pF
I_{IH}			0.05		μA
I_{IL}—All Inputs except CLK			0.6		μA
I_{IL}—CLK			1.2		μA
V_{IH}		2			V
V_{IL}				0.8	V
V_{TH}			1.6		V

Parameter	Conditions	Min	Typ	Max	Unit
REFERENCE INPUTS[1]					
V1 Range	V2 ≥ (V1 – 0.25 V)	5		AVCC – 4	V
V2 Range	V2 ≥ (V1 – 0.25 V)	5		AVCC – 4	V
V1 Input Current			0.2		μA
V2 Input Current			–7.5		μA
VREFLO Range	VREFHI ≤ (VREFLO + 2.75 V)	V1 – 0.5		AVCC – 1.3	V
VREFHI Range	VREFHI ≤ (VREFLO + 2.75 V)	VREFLO		AVCC	V
(VREFHI – VREFLO) Range		0		2.75	V
VREFHI Input Resistance			20		kΩ
VREFLO Bias Current			–0.2		μA
VREFHI Input Current			125		μA
VFS Range	VFS = 2 × (VREFHI – VREFLO)			5.5	V
POWER SUPPLY					
DVCC, Operating Range		3	3.3	3.6	V
DVCC, Quiescent Current			23	31	mA
AVCC, Operating Range		9		18	V
Total AVCC Quiescent Current			43	52	mA
STBY AVCC Current	STBY = HIGH		0.15	0.45	mA
STBY DVCC Current	STBY = HIGH		3.5	5	mA
OPERATING TEMPERATURE RANGE					
Ambient Temperature Range, T_A	Still Air	0		75	°C
Ambient Temperature Range, T_A[5]		0		85	°C
Junction Temperature Range, T_J	100% Tested	25		125	°C

[1] VDE = differential error voltage. VCME = common-mode error voltage. ΔV = maximum deviation between outputs. Full-scale output voltage = VFS = 2 × (VREFHI – VREFLO). See the Accuracy section on page 14.
[2] Measured on two outputs differentially as CLK and DB(0:11) are driven and STSQ and XFR are held LOW.
[3] Measured on two outputs differentially as the other four are transitioning by 5 V. Measured for both states of INV.
[4] Measured from 50% of falling CLK edge to 50% of output change. Measurement is made for both states of INV.
[5] Operation at 85°C ambient temperature requires a thermally optimized PCB layout (see Applications section), minimum airflow of 200 lfm, input clock rate not exceeding 120 MHz, black-to-white transition ≤ 4 V, and C_L ≤ 200 pF.

ABSOLUTE MAXIMUM RATINGS

Table 2. Absolute Maximum Ratings[1]

Parameter	Rating
Supply Voltages	
AVCCx to AGNDx	18 V
DVCC to DGND	4.5 V
Input Voltages	
Maximum Digital Input Voltage	DVCC + 0.5 V
Minimum Digital Input Voltage	DGND – 0.5 V
Maximum Analog Input Voltage	AVCC + 0.5 V
Minimum Analog Input Voltage	AGND – 0.5 V
Internal Power Dissipation[2]	
LFCSP Package @ 25°C Ambient	3.84 W
Operating Temperature Range	0°C to 85°C
Storage Temperature Range	–65°C to +125°C
Lead Temperature Range (Soldering 10 sec)	300°C

[1]Stresses above those listed under the Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum ratings for extended periods may reduce device reliability.

[2] 48-lead LFCSP Package:
θ_{JA} = 26°C/W (JEDEC STD, 4-layer PCB in still air)
θ_{JC} = 20°C/W.
Ψ_{JB} = 11°C/W in Still Air

OVERLOAD PROTECTION

The AD8382 employs a two-stage overload protection circuit that consists of an output current limiter and a thermal shutdown. The maximum current at any output of the AD8382 is internally limited to 100 mA average. In the event of a momentary short circuit between a video output and a power supply rail (VCC or AGND), the output current limit is sufficiently low to provide temporary protection.

The thermal shutdown "debiases" the output amplifier when the junction temperature reaches the internally set trip point. In the event of an extended short circuit between a video output and power supply rail, the output amplifier current continues to switch between 0 mA and 100 mA typ. with a period set by the thermal time constant and hysteresis of the thermal trip point. The thermal shutdown provides long-term protection by limiting average junction temperature to a safe level.

EXPOSED PADDLE

To ensure a high degree of reliability, the exposed paddle must be electrically connected to AVCC.

To ensure optimized thermal performance, the exposed paddle must be thermally connected to the AVCC plane as described in the Applications section.

MAXIMUM POWER DISSIPATION

The maximum power that the AD8382 can safely dissipate is limited by its junction temperature. The maximum safe junction temperature for plastic encapsulated devices, as determined by the plastic's glass transition temperature, is approximately 150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for extended periods can result in device failure.

OPERATING TEMPERATURE RANGE

Although the maximum safe operating junction temperature is higher, the AD8382 is 100% tested at a junction temperature of 125°C. Consequently, the maximum guaranteed operating junction temperature is 125°C. To ensure operation within the specified operating temperature range, it is necessary to limit the maximum power dissipation to:

$$P_{DMAX} \approx \frac{(T_{JMAX} - T_A)}{(\theta_{JA} - 0.9 \times \sqrt[3]{Airflow\ in\ lfm})}$$

where T_{JMAX} = 125°C

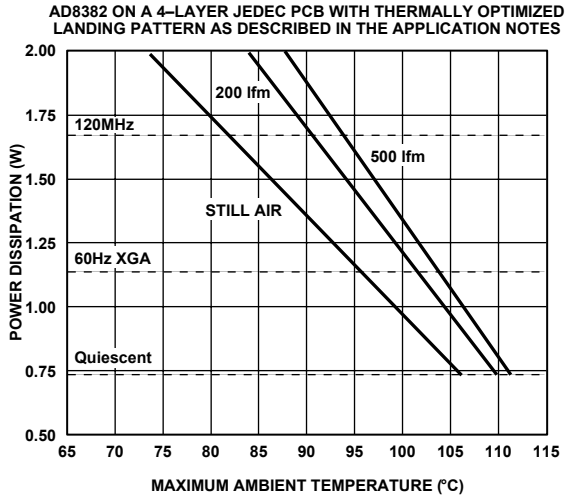

Figure 2. Maximum Power Dissipation vs. Temperature.

Note: Quiescent power dissipation is 0.74 W when operating under the conditions specified in this data sheet.

When driving a 6-channel XGA panel with an input capacitance of 200 pF, the AD8382 dissipates a total of 1.14 W when displaying 1 pixel wide alternating white and black vertical lines generated by a standard 60 Hz XGA input video.

The total power dissipation of the AD8382 is 1.67 W when operating at the maximum specified frequency of 120 MHz, under the conditions specified in this data sheet (Figure 2).

TIMING CHARACTERISTICS

Table 3. Timing Parameters and Conditions

Parameter	Conditions	Min	Typ	Max	Unit
t_1, Data Setup Time	tr, tf = 2 ns (10% to 90%)	0			ns
t_2, Data Hold Time		3			ns
t_3, STSQ Setup Time		1			ns
t_4, STSQ Hold Time		3			ns
t_5, XFR Setup Time		1			ns
t_6, XFR Hold Time		3			ns
t_7, CLK High Time		3			ns
t_8, CLK Low Time		2.5			ns
t_9, CLK to VIDx Delay	To 50% of VIDx	10	12	14	ns
t_{10}, INV to VIDx Delay	To 50% of VIDx	10.4	12.4	14.4	ns

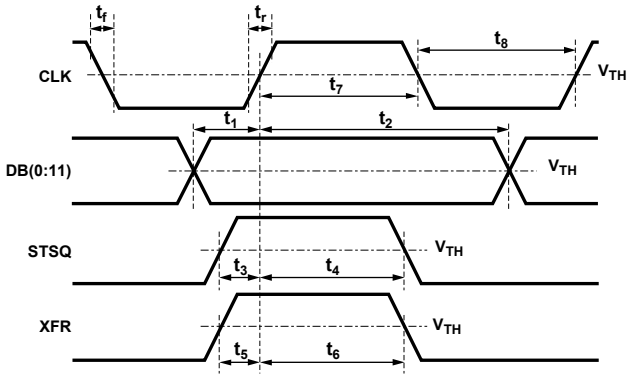

Figure 3. Timing Requirement E/O = HIGH

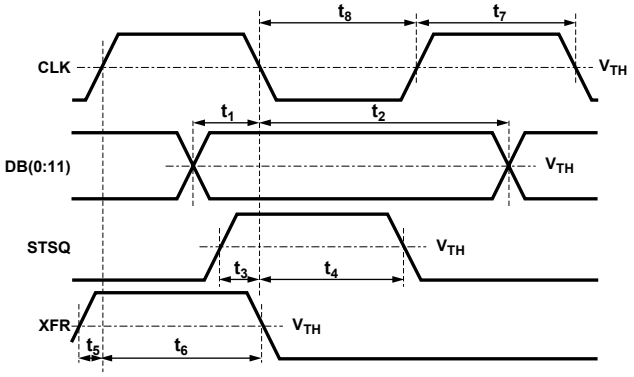

Figure 4. Timing Requirement E/O = LOW

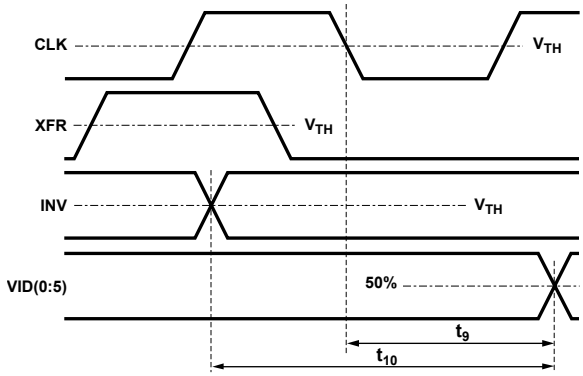

Figure 5. Output Timing

PIN CONFIGURATION AND FUNCTIONAL DESCRIPTIONS

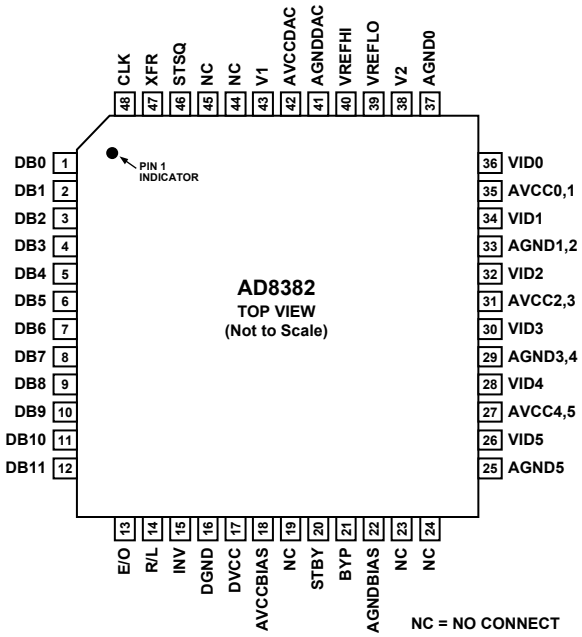

Figure 6. 48-Lead LFCSP, 7 mm × 7 mm Package

Table 4. Pin Function Descriptions

Mnemonic	Function	Description
DB(0:11)	Data Input	12-Bit Data Input. MSB = DB(11).
CLK	Clock	Clock Input.
STSQ	Start Sequence	A new data loading sequence begins on the rising edge of CLK when this input was HIGH on the preceding rising edge of CLK and the E/O input is held HIGH. A new data loading sequence begins on the falling edge of CLK when this input was HIGH on the preceding falling edge of CLK and the E/O input is held LOW.
R/L	Right/Left Select	A new data loading sequence begins on the left, with Channel 0, when this input is LOW, and on the right, with Channel 5, when this input is HIGH.
E/O	Even/Odd Select	The active CLK edge is the rising edge when this input is held HIGH and the falling edge when this input is held LOW. Data is loaded sequentially on the rising edges of CLK when this input is HIGH and on the falling edges when this input is LOW.
XFR	Data Transfer	Data is transferred to the outputs on the immediately following falling edge of CLK when this input is HIGH on the rising edge of CLK.
VID0–VID5	Analog Outputs	These pins are directly connected to the analog inputs of the LCD panel.
V1,V2	Reference Voltages	The voltages applied between these pins and AGND set the reference levels of the analog outputs.
VREFHI, VREFLO	Full-Scale References	The voltage applied between these pins sets the full-scale output voltage.
INV	Invert	When this pin is HIGH, the analog output voltages are at or above V2. When this pin is LOW, the analog output voltages are at or below V1.
DVCC	Digital Power Supply	Digital Power Supply.
DGND	Digital Supply Return	This pin is normally connected to the analog ground plane.
AVCCx	Analog Power Supplies	Analog Power Supplies.
AGNDx	Analog Supply Returns	Analog Supply Returns.
BYP	Bypass	A 0.1 µF capacitor connected between this pin and AGND ensures optimum settling time.
STBY	Standby	When HIGH, the internal circuits are debiased and the power dissipation drops to a minimum.

TYPICAL PERFORMANCE CHARACTERISTICS

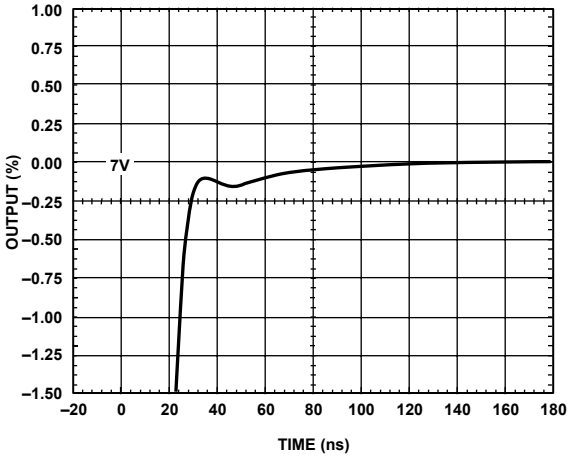

Figure 7. Output Settling Time (Rising Edge), C_L = 200 pF, 5 V Step, INV = LOW

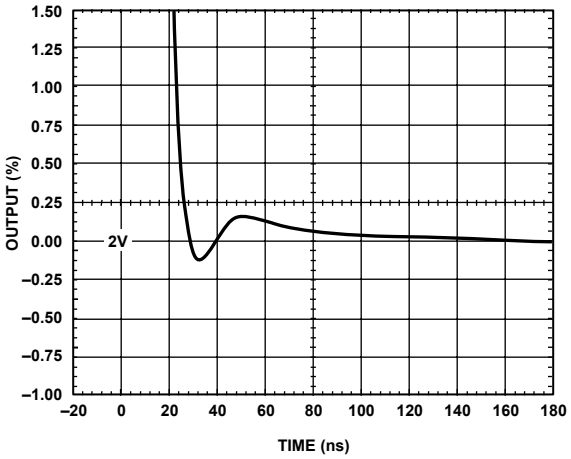

Figure 10. Output Settling Time (Falling Edge), C_L = 200 pF, 5 V Step, INV = LOW

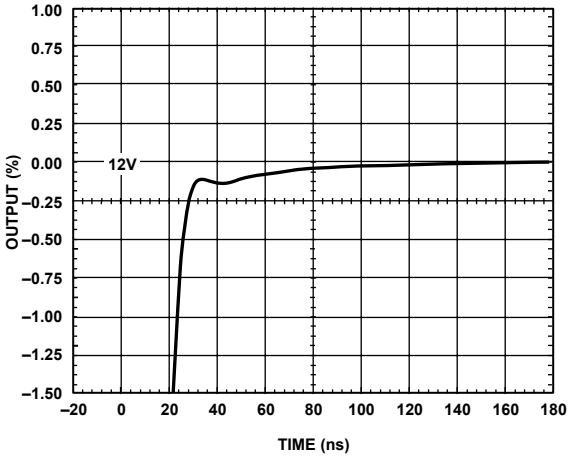

Figure 8. Output Settling Time (Rising Edge), C_L = 200 pF, 5 V Step, INV = HIGH

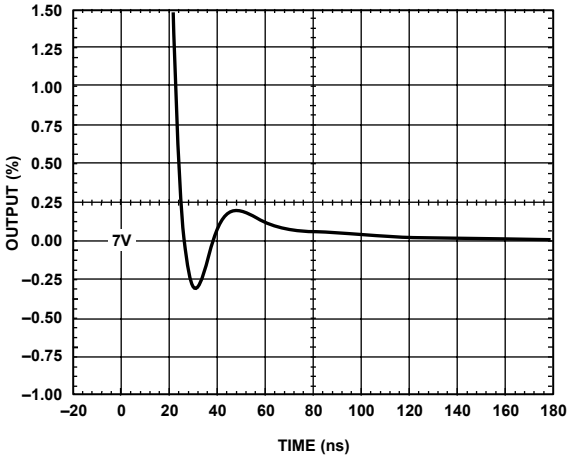

Figure 11. Output Settling Time (Falling Edge), C_L = 200 pF, 5 V Step, INV = HIGH

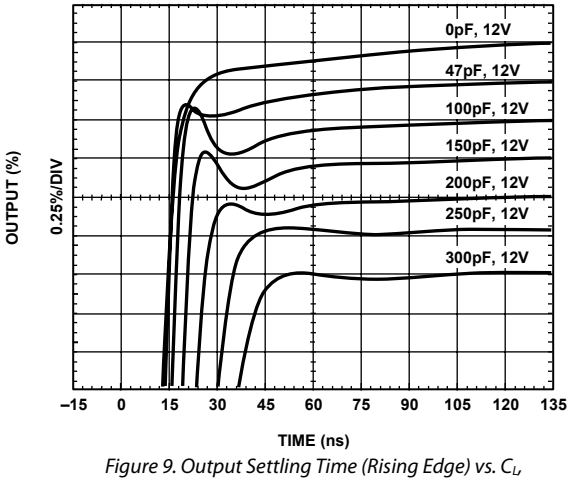

Figure 9. Output Settling Time (Rising Edge) vs. C_L, 5 V Step, INV = HIGH

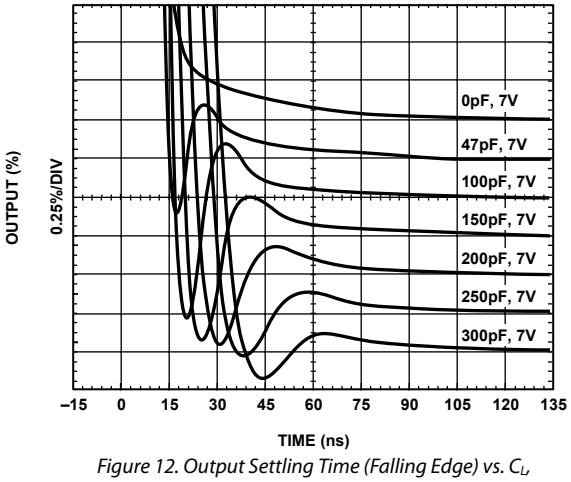

Figure 12. Output Settling Time (Falling Edge) vs. C_L, 5 V Step, INV = HIGH

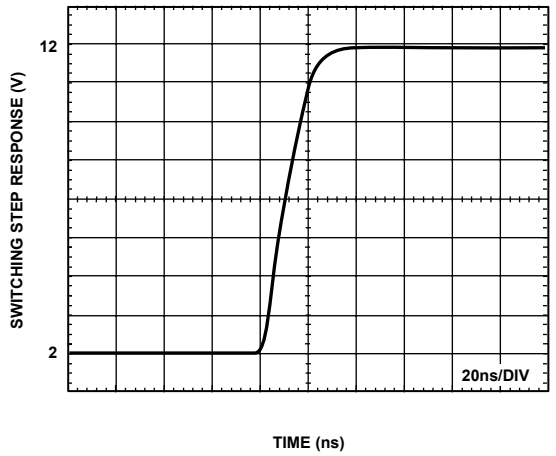

Figure 13. Invert Switching Step Response (Rising Edge), 10 V Step, C_L = 200 pF

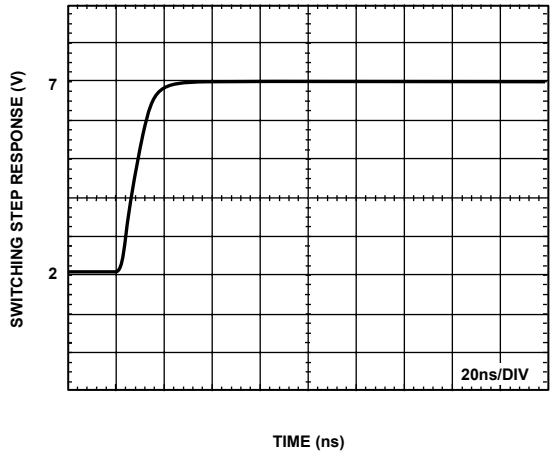

Figure 14. Data Switching Step Response (Rising Edge), 5 V Step, C_L=200 pF, INV = LOW

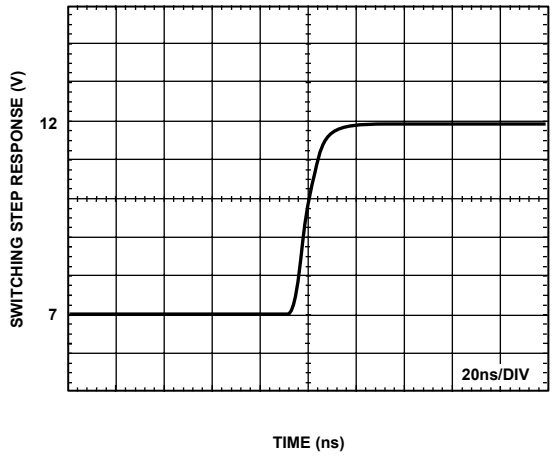

Figure 15. Data Switching Step Response (Rising Edge), 5 V Step, C_L = 200 pF, INV = HIGH

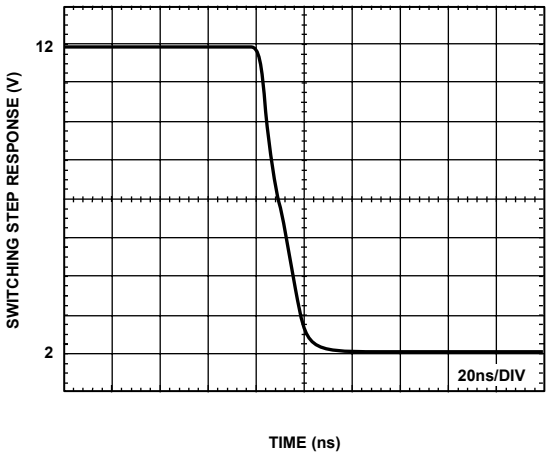

Figure 16. Invert Switching Step Response (Falling Edge), 10 V Step, C_L = 200 pF

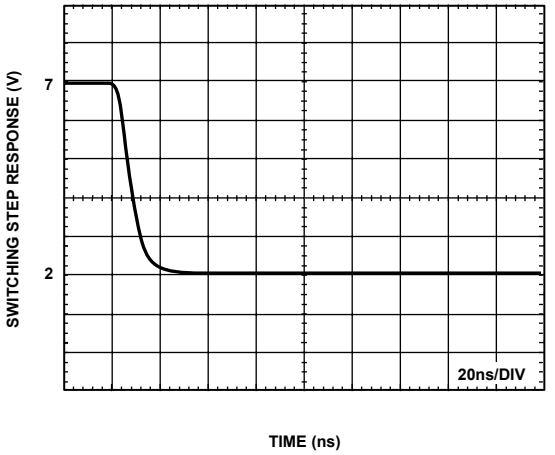

Figure 17. Data Switching Step Response (Falling Edge), 5 V Step, C_L = 200 pF, INV = LOW

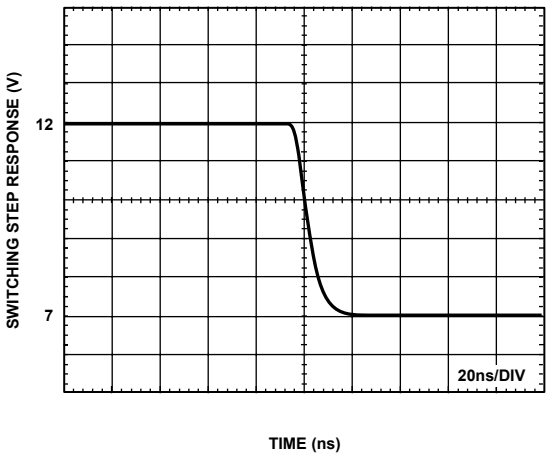

Figure 18. Data Switching Step Response (Falling Edge), 5 V Step, C_L = 200 pF, INV = HIGH

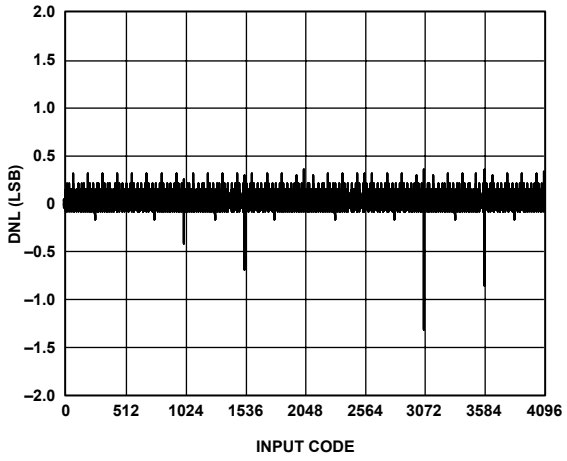

Figure 19. Differential Nonlinearity (DNL) vs. Code, INV = LOW

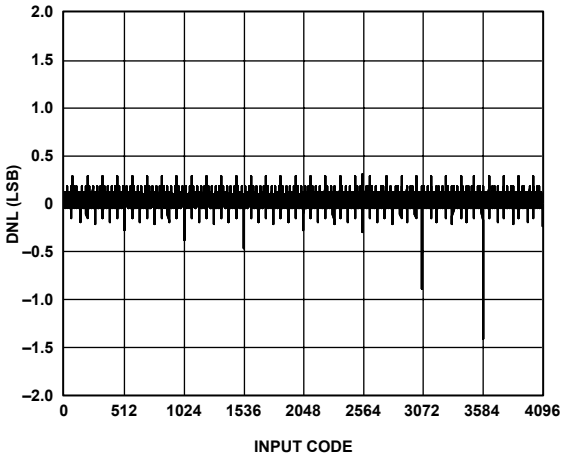

Figure 22. Differential Nonlinearity (DNL) vs. Code, INV = HIGH

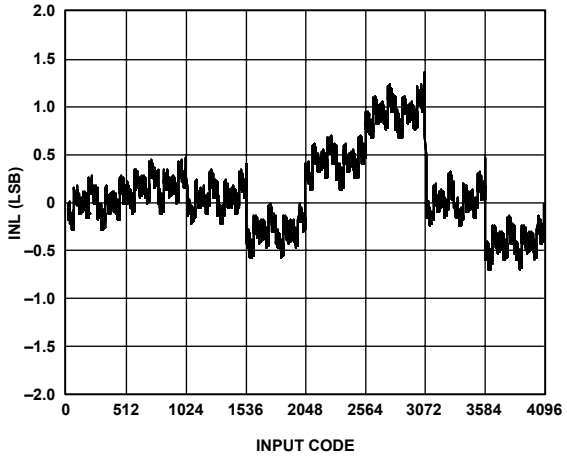

Figure 20. Integral Nonlinearity (INL) vs. Code, INV = LOW

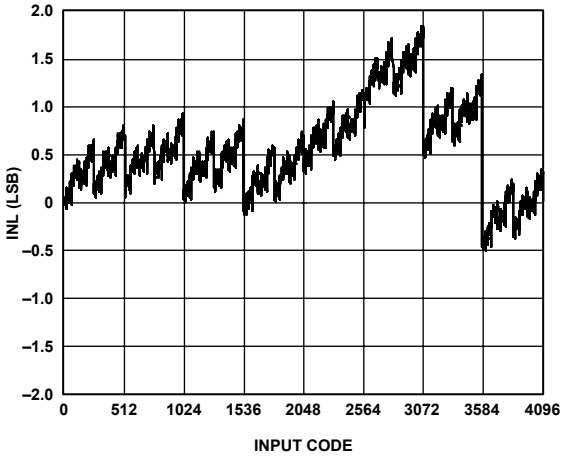

Figure 23. Integral Nonlinearity (INL) vs. Code, INV = HIGH

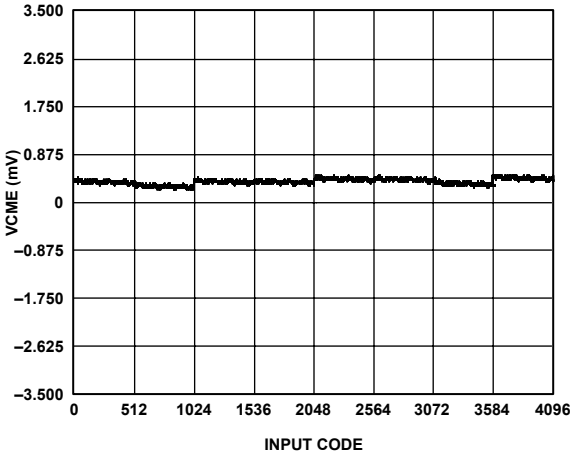

Figure 21. Common-Mode Error Voltage (VCME) vs. Code

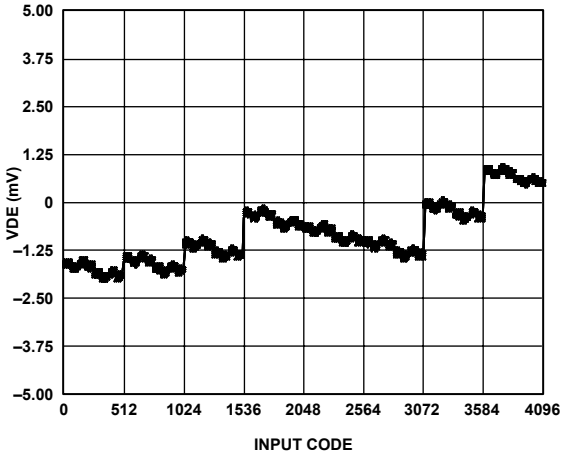

Figure 24. Differential Error Voltage (VDE) vs. Code

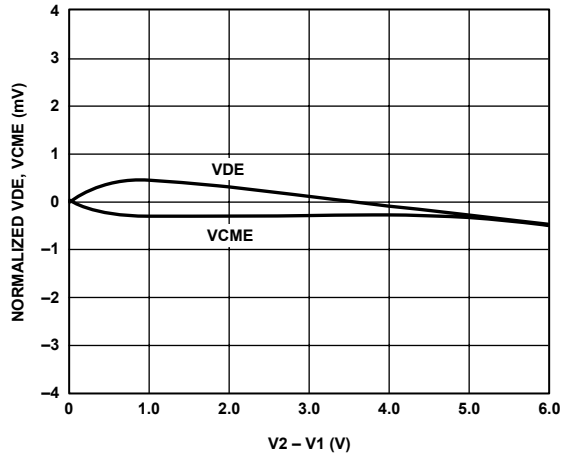

Figure 25. Normalized VDE, VCME vs. (V2 – V1) at Code 2048

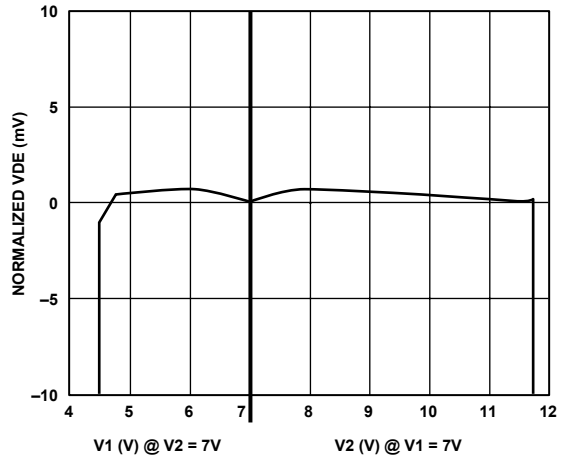

Figure 26. Normalized VDE vs. V1 and V2 at Code 2048

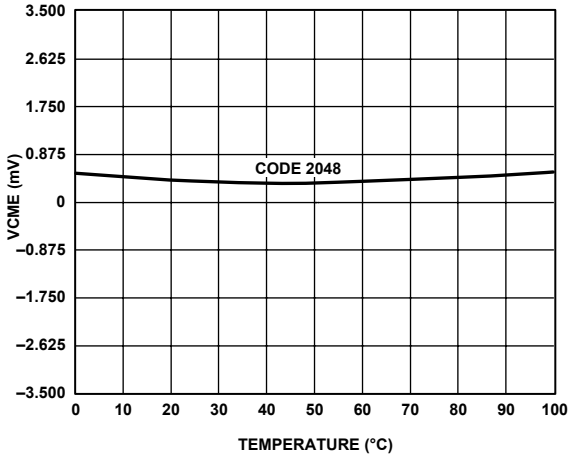

Figure 27. Common-Mode Error Voltage (VCME) vs. Temperature

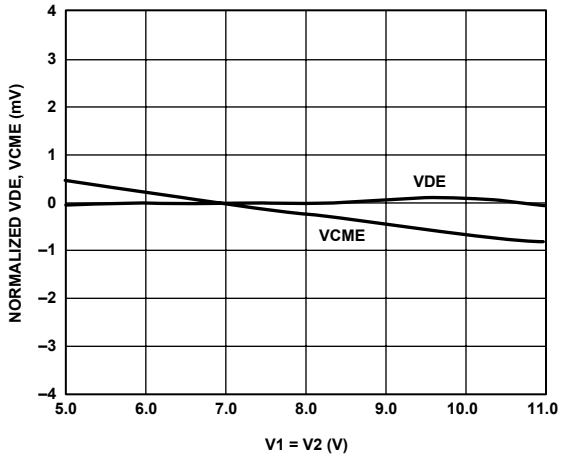

Figure 28. Normalized VDE, VCME vs. V1 = V2 at Code 2048

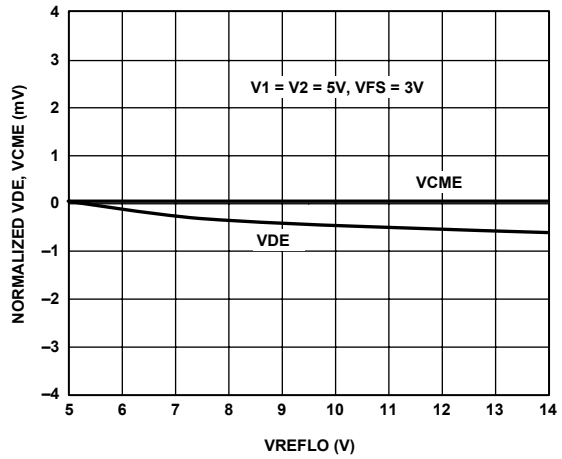

Figure 29. Normalized VDE, VCME vs. VREFLO at Code 2048

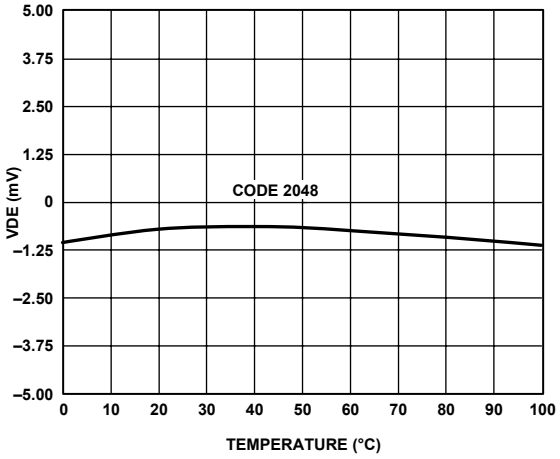

Figure 30. Differential Error Voltage (VDE) vs. Temperature

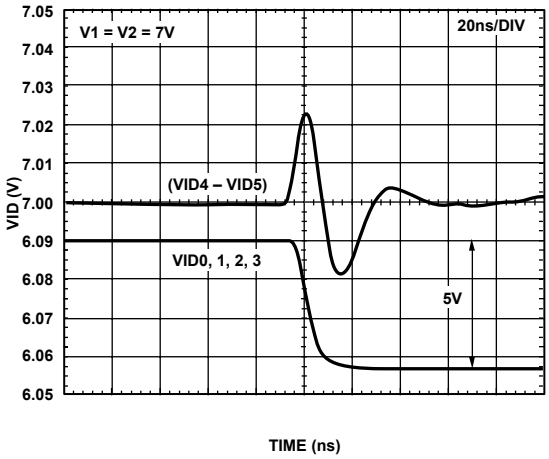

Figure 31. All-Hostile Crosstalk at C_L = 200 pF

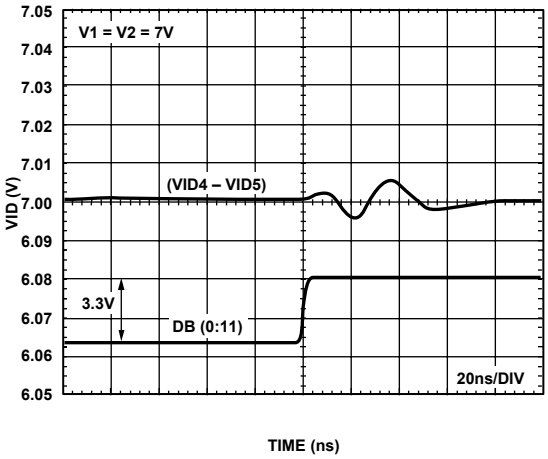

Figure 34. Data Switching Transient (Feedthrough) at C_L = 200 pF

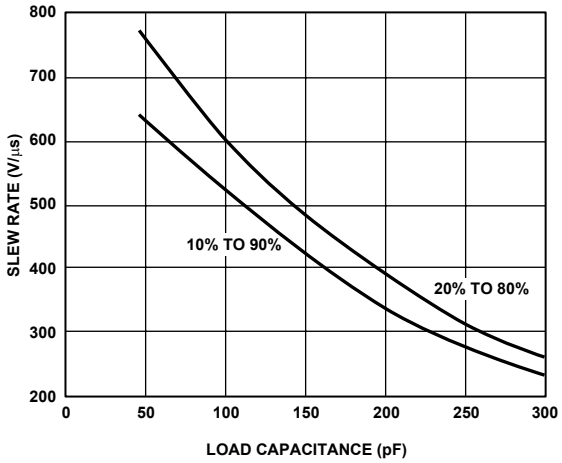

Figure 32. Slew Rate vs. C_L (Falling Edge)

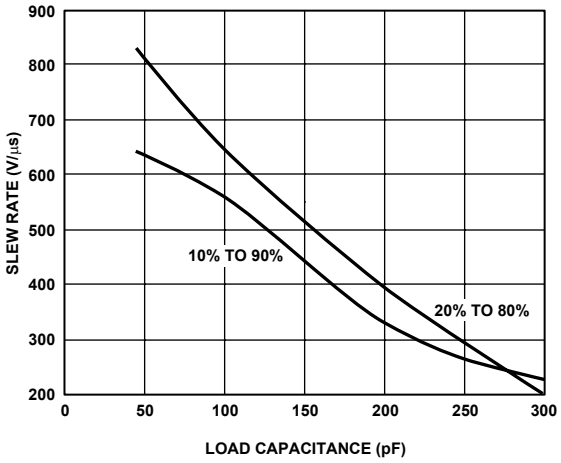

Figure 35. Slew Rate vs. C_L (Rising Edge)

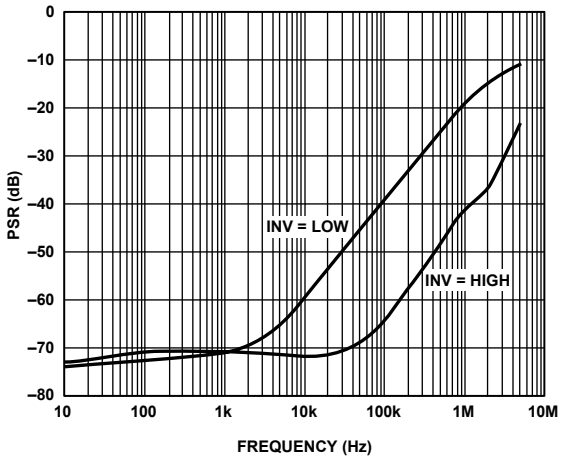

Figure 33. AVCC Power Supply Rejection vs. Frequency

FUNCTIONAL DESCRIPTION

The AD8382 is a system building block designed to directly drive the columns of LCD microdisplays of the type popularized for use in projection systems. It comprises six channels of precision, 12-bit digital-to-analog converters loaded from a single, high speed, 12-bit wide input. Precision current feedback amplifiers, providing well-damped pulse response and fast voltage settling into large capacitive loads, buffer the six outputs. Laser trimming at the wafer level ensures low absolute output errors and tight channel-to-channel matching. Tight part-to-part matching in high resolution systems is guaranteed by the use of external voltage references.

START SEQUENCE CONTROL—INPUT DATA LOADING

A valid STSQ control input initiates a new 6-clock loading cycle, during which six input data-words are loaded sequentially into six internal channels. A new loading sequence begins on the current active CLK edge only when STSQ was held HIGH at the preceding active CLK edge. Active CLK edge is defined by the E/O Control.

EVEN/ODD CONTROL—INPUT DATA LOADING

To facilitate 12-channel, single data bus systems, the active CLK edge, at which input data is loaded, is selected with the E/O control input. Input data is loaded on the rising CLK edges while the E/O input is held HIGH; input data is loaded on the falling CLK edges while the E/O input is held LOW.

RIGHT/LEFT CONTROL—INPUT DATA LOADING

To facilitate image mirroring, the direction of the loading sequence is set by the R/L control. A new loading sequence begins at channel 0 and proceeds to Channel 5 when the R/L control is held LOW. It begins at Channel 5 and proceeds to channel 0 when the R/L control is held HIGH.

XFR CONTROL—DATA TRANSFER TO OUTPUTS

Data transfer to the outputs is initiated by the XFR control. While XFR is held HIGH during a rising CLK edge, data is simultaneously transferred to all outputs on the immediately following falling CLK edge.

STBY CONTROL—STANDBY MODE

A HIGH applied to the STBY input debiases the internal circuitry, dropping the quiescent power dissipation to a few milliwatts. Upon returning STBY to LOW, normal operation is restored. Since both analog and digital circuitry is debiased, all stored data will be lost in standby mode.

V1, V2 INPUTS—VOLTAGE REFERENCE INPUTS

Two external analog voltage references set the levels of the outputs. V1 sets the output voltage at Code 4095 while the INV input is LOW, and V2 sets the output voltage at Code 4095 while the INV input is held HIGH.

VREFHI, VREFLO INPUTS—FULL-SCALE REFERENCE INPUTS

Twice the difference between these analog input voltages sets the full-scale output voltage *VFS*.

$$VFS = 2 \times (VREFHI - VREFLO)$$

INV CONTROL—ANALOG OUTPUT INVERSION

The analog voltage equivalent of the input code is subtracted from (V2 + VFS) while INV is held HIGH and added to (V1 – VFS) while INV is held LOW.

Transfer Function

The AD8382 has two regions of operation, where the video output voltages are either above reference voltage V2 or below reference voltage V1. The transfer function defines the video output voltage as the function of the digital input code as follows:

$$VIDx(n) = V2 + VFS \times (1 - n/4095), \textit{ for INV = HIGH}$$

$$VIDx(n) = V1 - VFS \times (1 - n/4095), \textit{ for INV = LOW}$$

where n = input code

$$VFS = 2 \times (VREFHI - VREFLO)$$

A number of internal limits define the usable range of the video output voltages, VIDx, as shown in Figure 36

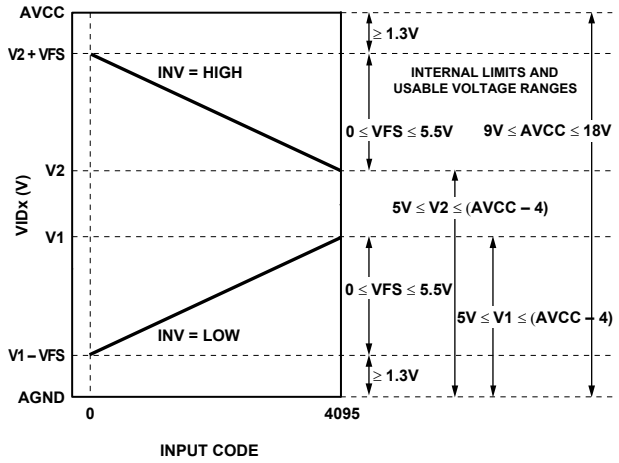

Figure 36. Transfer Function and Usable Voltage Ranges

Accuracy

To best correlate transfer function errors to image artifacts, the overall accuracy of the AD8382 is defined by three parameters: VDE, VCME, and ΔV.

VDE, the differential error voltage, measures the difference between the rms value of the output and the rms value of the ideal. The defining expression is:

$$VDE(n) = \frac{[VOUTN(n) - V2] - [VOUTP(n) - V1]}{2} - \left(1 - \frac{n}{4095}\right) \times VFS$$

VCME, the common-mode error voltage, measures one-half the dc bias of the output. The defining expression is:

$$VCME(n) = \frac{1}{2}\left[\frac{VOUTN(n) + VOUTP(n)}{2} - \frac{(V2 + V1)}{2}\right]$$

ΔV measures the maximum deviation between the output voltages. The defining expression is:

$$\Delta V\,(n) = max\{\Delta VN(n), \Delta VP(n)\}$$

where $\Delta VN(n) = max\{VOUTN(n)_{(0-5)}\} - min\{VOUTN(n)_{(0-5)}\}$

and $\Delta VP(n) = max\{VOUTP(n)_{(0-5)}\} - min\{VOUTP(n)_{(0-5)}\}$

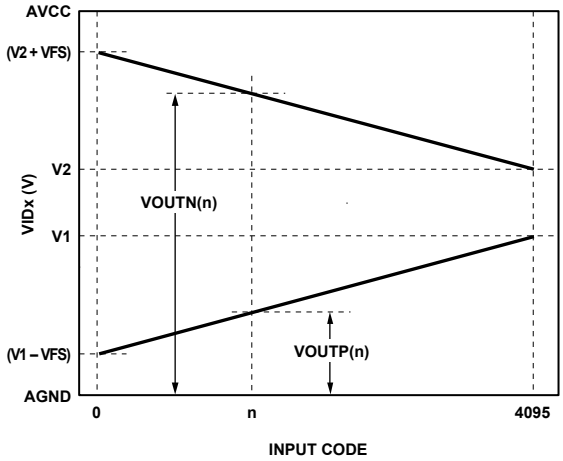

Figure 37. AD8382 Transfer Function

APPLICATIONS

OPERATING MODES—6-CHANNEL SYSTEMS

Depending on the speed of the LCD microdisplay, 6-channel systems are compatible with up to XGA resolutions and require one AD8382 per color. The input/output timing diagram of the AD8382 in such systems is shown in Figure 38.

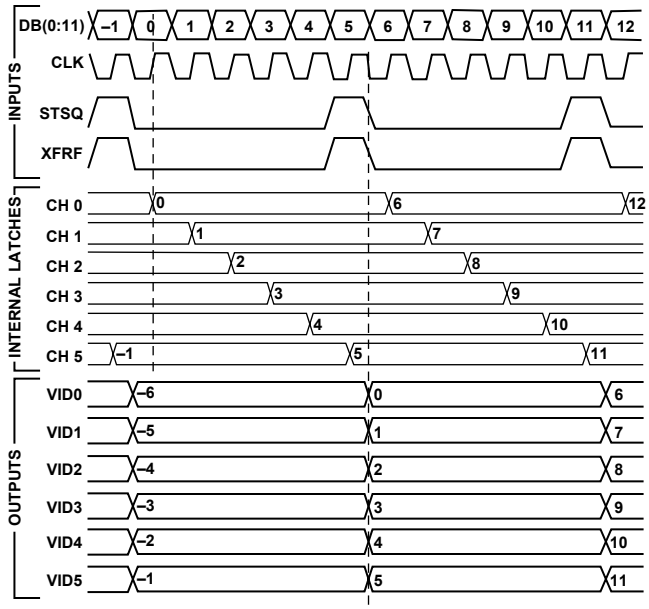

Figure 38. Timing Diagram in a Typical 6-Channel System, E/O=HIGH, R/L=LOW

OPERATING MODES—12-CHANNEL SYSTEMS

12-channel systems are usually those requiring video line doubling or compatibility with SXGA and higher resolutions. Depending on the input data rates, two types of 12-channel systems are in common use.

12-Channel, Even/Odd Systems

Single data bus systems are characterized by an image processor with a single data bus output. They require two AD8382s per color.

One AD8382 is set to operate in EVEN mode, while the other is set to operate in ODD mode. Both AD8382s share the same data bus and CLK. The timing diagram of such a system is shown in Figure 39.

12-Channel Parallel Systems

Dual data bus systems are characterized by an image processor with two data bus outputs. They require two AD8382s per color. Both AD8382s in dual data bus systems can be set independently. The timing diagram of each AD8382 in such systems is identical to that of a 6-channel system.

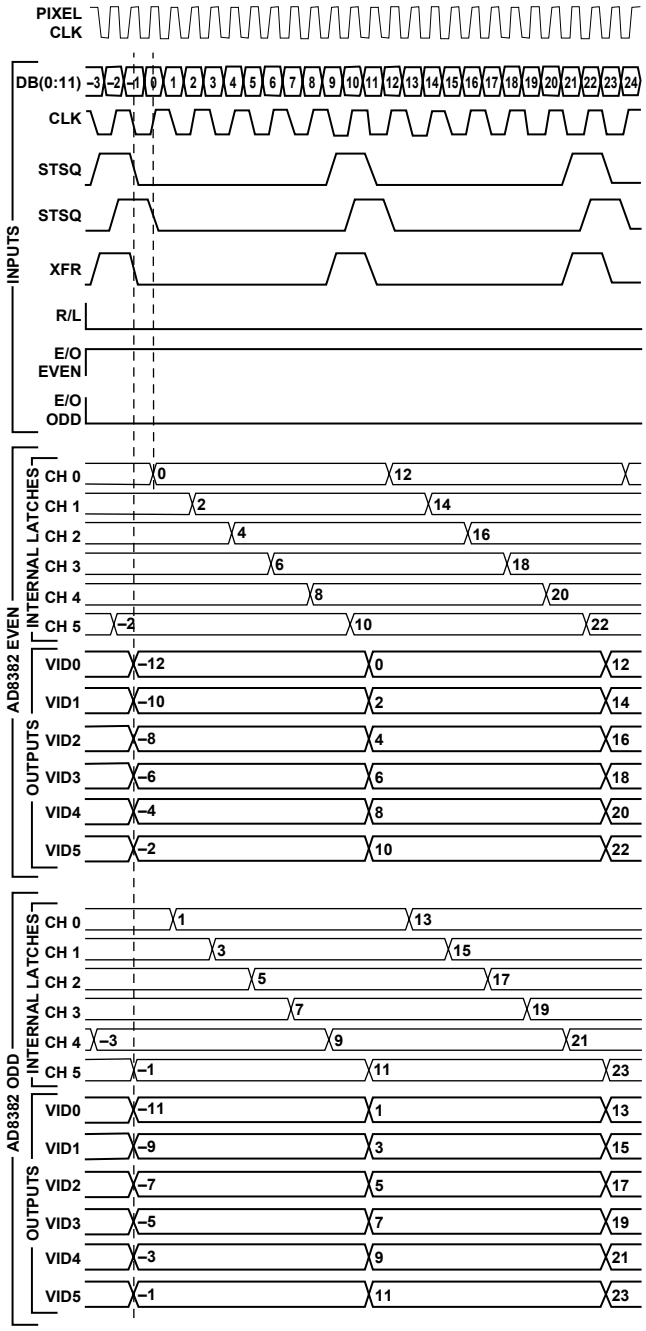

Figure 39. 12-Channel Even/Odd System Timing Diagram

OPERATING MODES—BEYOND 12 CHANNELS

Any number of AD8382s may be cascaded in even/odd pairs or in parallel to facilitate very high resolution systems.

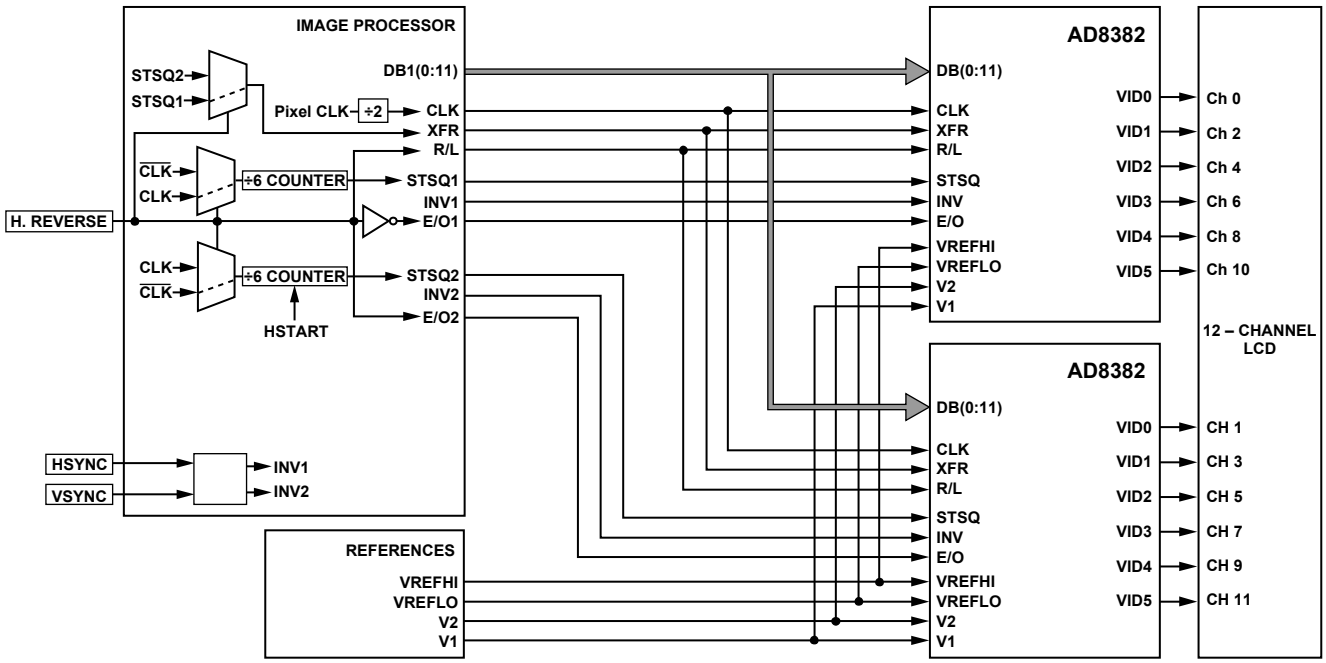

Figure 40. Single Data Bus 12-Channel Even/Odd System Block Diagram

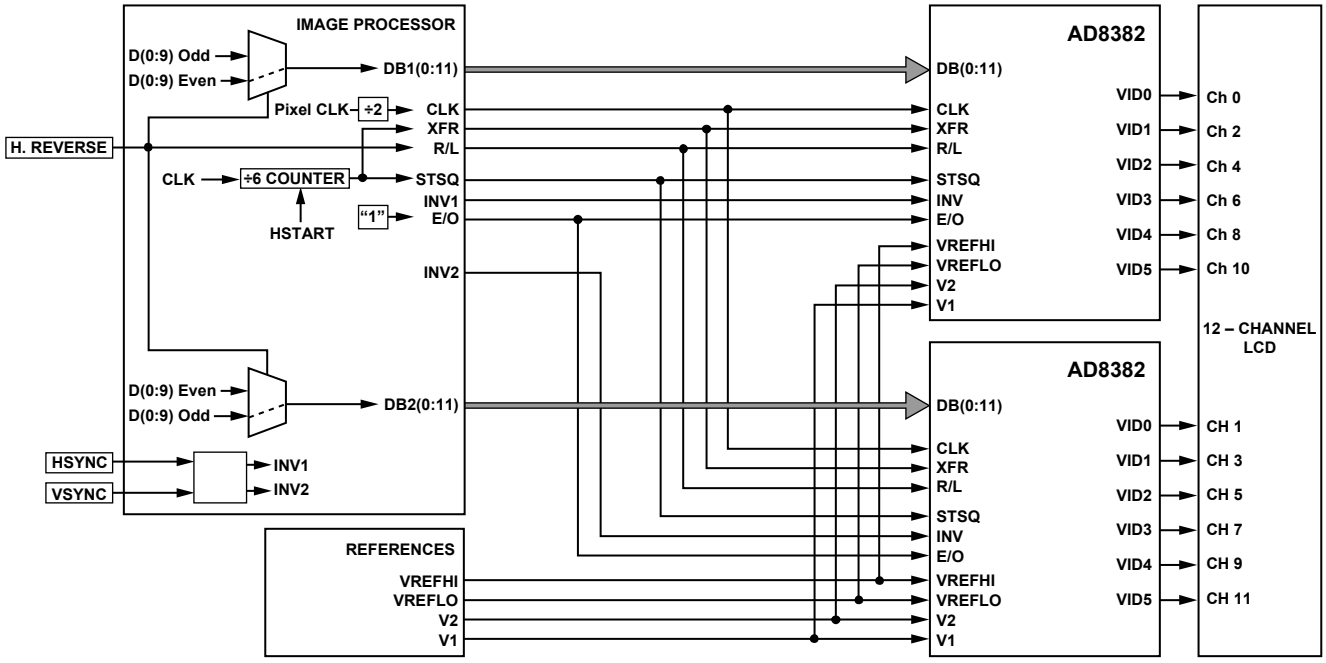

Figure 41. Dual Data Bus 12-Channel Even/Odd System Block Diagram

VBIAS Generation—V1, V2 Input Pin Functionality

In order to avoid image flicker, a symmetrical ac voltage is required and a bias voltage of approximately 1 V minimum must be maintained across the pixels of HTPS LCDs. The AD8382 provides two methods of maintaining this bias voltage.

INTERNAL BIAS VOLTAGE GENERATION

Standard systems that internally generate the bias voltage reserve the uppermost code range for the bias voltage and use the remaining code range to encode the video for gamma correction. A high degree of ac symmetry is guaranteed by the AD8382 in these systems.

The V1 and V2 inputs in these systems are tied together and are normally connected to VCOM, as shown in Figure 42.

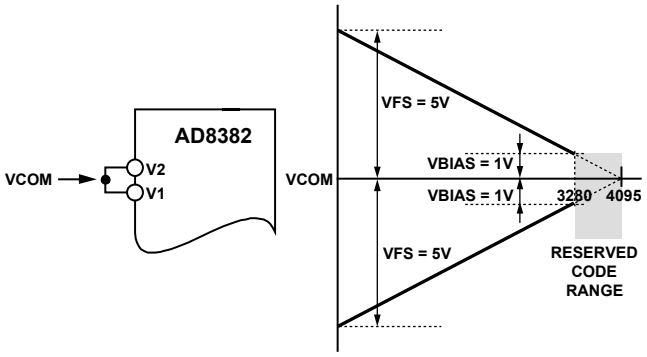

Figure 42. V1, V2 Connection and Transfer Function in a Typical Standard System

EXTERNAL BIAS VOLTAGE GENERATION

In systems that require improved brightness resolution and higher accuracy, the V1 and V2 inputs, connected to external voltage references, provide necessary bias voltage, VBIAS, while allowing the full code range to be used for gamma correction.

To ensure a symmetrical ac voltage at the AD8382's outputs, *VBIAS* must remain constant for both states of INV. Thus, *V*1 and *V*2 are defined as:

$$V1 = VCOM - VBIAS$$
$$V2 = VCOM + VBIAS$$

APPLICATIONS CIRCUIT

The circuit in Figure 41 ensures VBIAS symmetry to within 1 mV with a minimum component count. Bypass capacitors are omitted for clarity.

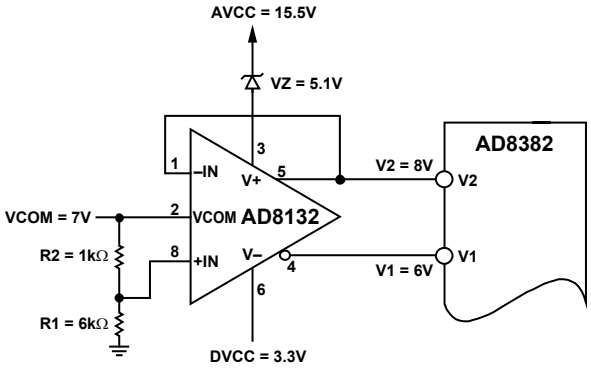

Figure 43. External VBIAS Generator with the AD8132

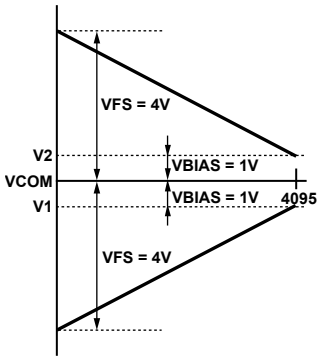

Figure 44. The AD8382 Transfer Function in a Typical High Accuracy System

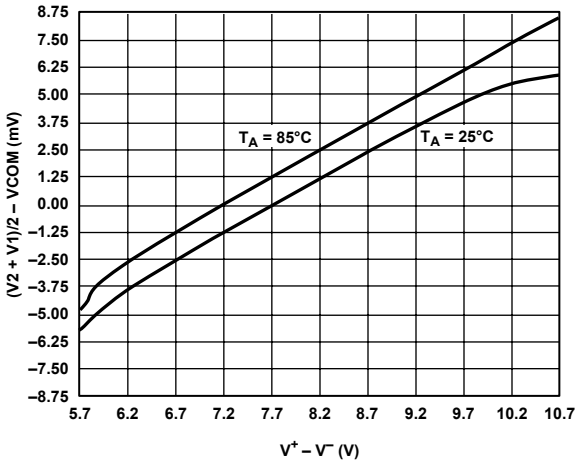

Figure 45. Typical Asymmetry at the Outputs of the AD8132 vs. Power Supply for the Application Circuit

The AD8132 typically produces a symmetrical output at 85°C when its supply, (V+) – (V–), is 7.2 V (Figure 45).

Power Supply Sequencing

As indicated in the Absolute Maximum Ratings, voltage at any input pin cannot exceed its supply voltage by more than 0.5 V. To ensure compliance with these ratings, the following power-up and power-down sequencing is recommended.

During power-up, initial application of nonzero voltages to any input pin must be delayed until supply voltage ramps up to at least the highest maximum operational input voltage. During power-down, the voltage at any input pin must reach zero during a period not exceeding the power supply's hold-up time.

Failure to comply with the Absolute Maximum Ratings may result in functional failure or damage to the internal ESD diodes. Damaged ESD diodes may cause temporary parametric failures, which may result in image artifacts. Damaged ESD diodes cannot provide full ESD protection, reducing reliability.

Power ON	Power OFF
1. Apply power to supplies.	1. Remove power from I/Os.
2. Apply power to other I/Os.	2. Remove power from supplies.

PCB Design for Optimized Thermal Performance

The total maximum power dissipation of the AD8382 is partly load dependent. In a 6-channel, 65 MHz, 60 Hz XGA system, the total maximum power dissipation is 1.14 W at an LCD input capacitance of 200 pF.

At a clock rate of 120 Ms/s, the total maximum power dissipation can exceed 2 W, as shown below for a black-to-white video output voltage swing of 4 V and 5 V.

Although the maximum safe operating junction temperature is higher, the AD8382 is 100% tested at a junction temperature of 125°C. Consequently, the maximum guaranteed operating junction temperature is 125°C. To limit the maximum junction temperature at or below the guaranteed maximum, the package, in conjunction with the PCB, must effectively conduct heat away from the junction.

The AD8382 package is designed to provide superior thermal characteristics, partly through the exposed die paddle on the bottom surface of the package. In order to take full advantage of this feature, the exposed paddle must be in direct thermal contact with the PCB, which then serves as a heat sink.

Table 5. AD8382 Power Dissipation

C_{LOAD} (pF)	$P_{QUIESCENT}$ (W)	V_{SWING} = 5 V		V_{SWING} = 4 V	
		$P_{DYNAMIC}$ (W)	P_{TOTAL} (W)	$P_{DYNAMIC}$ (W)	P_{TOTAL} (W)
200	0.74	0.93	1.67	0.74	1.48
250	0.74	1.16	1.90	0.93	1.67
300	0.74	1.39	2.13	1.11	1.85

A thermally effective PCB must incorporate a thermal pad and a thermal via structure. The thermal pad provides a solderable contact surface on the top surface of the PCB. The thermal via structure provides a thermal path to the inner and bottom layers of the PCB to remove heat.

THERMAL PAD DESIGN

Thermal performance of the AD8382 varies logarithmically with the contact area between the exposed thermal paddle and the thermal pad on the top layer of the PCB.

In order to minimize thermal performance degradation of production PCBs, the contact area between the thermal pad and the PCB should be maximized. Therefore, the size of the thermal pad should match the exposed paddle size of 5.25 mm × 5.25 mm. In addition, a second thermal pad of the same size should be placed on the bottom side of the PCB. At least one thermal pad should be in direct thermal (and electrical) contact with the AVCC plane.

THERMAL VIA STRUCTURE DESIGN

Effective heat transfer from the top to the inner and bottom layers of the PCB requires thermal vias incorporated into the thermal pad design. Thermal performance increases logarithmically with the number of vias. θ_{JA} reaches its specified value at approximately 16 vias, provided the AD8382 is on a standard JEDEC PCB. θ_{JA} approaches its optimum value as the slope of such a curve approaches zero, at above 36 vias. Near optimum thermal performance of production PCBs is attained when the number of thermal vias is at least 36.

AD8382 PCB DESIGN RECOMMENDATIONS

Land pattern Dimensions

Pad Size:

0.5 mm × 0.25 mm

Pad Pitch:

0.5 mm

Thermal Pad Size:

5.25 mm × 5.25 mm

Thermal via structure:

0.25 mm diameter.
Vias on 0.5mm grid.

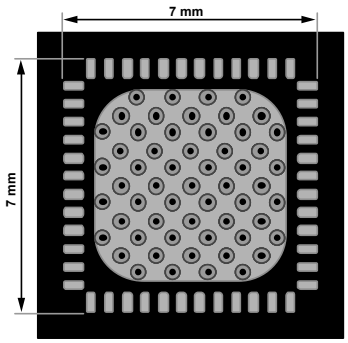

Figure 46. Land Pattern—Top Layer

THERMAL PAD AND VIA CONNECTIONS

Thermal Pads are connected to AVCC.

For PCBs with the AVCC plane located on one of the outer layers, direct connection of at least one thermal pad to the AVCC plane is recommended. For PCBs with the AVCC plane located on one of the internal layers, direct connection of all thermal vias to the AVCC plane is recommended.

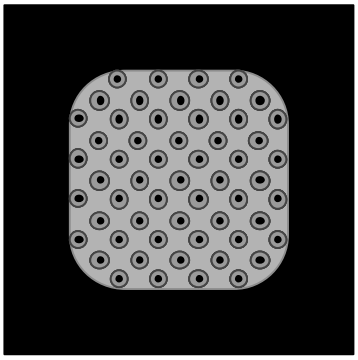

Figure 47. Land Pattern—Bottom Layer

The use of thermal spokes is not recommended when connecting the thermal pads or via structure to the AVCC plane.

SOLDER MASKING

To minimize the formation of solder voids due to solder flowing into the via holes (solder wicking), via diameter should be small. Solder masking of the via holes on the top layer of the PCB plugs the via holes, inhibiting solder flow into the holes. To optimize the thermal pad coverage, the solder mask diameter should be no more than 0.1 mm larger than the via diameter.

Solder Mask—Top Layer

Pads: Set by customer's PCB Design Rules

Thermal Vias: 0.25 mm dia. circular mask, centered on the vias.

Solder Mask—Bottom Layer

Set by customer's PCB Design Rules.

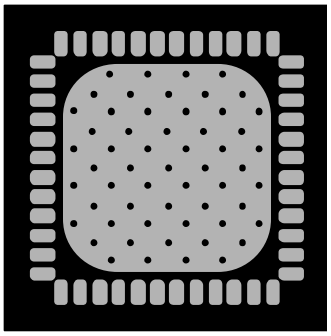

Figure 48. Solder Mask—Top Layer

Layout Considerations

The AD8382 is a mixed-signal, high speed, high accuracy device. In order to fully realize its specifications, it is essential to use a properly designed printed circuit board.

LAYOUT AND GROUNDING

The analog outputs and the digital inputs of the AD8382 are on opposite sides of the package. Keep these sections separated to minimize crosstalk and coupling of digital inputs into the analog outputs.

All signal trace lengths should be made as short and direct as possible to prevent signal degradation due to parasitic effects. Note that digital signals should not cross and should not be routed near analog signals.

It is imperative to provide a solid analog ground plane under and around the AD8382. All ground pins of the part should be connected directly to this ground plane with no extra signal path length. This includes DGND, AGNDBIAS, AGND5, AGND3,4, AGND1,2, AGND0, and AGNDDAC. The return traces for any of the signals should be routed close to the ground pin for that section to prevent stray signals from coupling into other ground pins.

POWER SUPPLY BYPASSING

All power supply and reference pins of the AD8382 must be properly bypassed to the analog ground plane for optimum performance.

All analog supply pins may be connected directly to an analog supply plane located as close to the part as possible. A 0.1 μF chip capacitor should be placed as close to each analog supply pin as possible and connected directly between each analog supply pin and the analog ground plane.

A minimum 47 μF tantalum capacitor should be placed near the analog supply plane and connected directly between the supply and analog ground planes.

A minimum 10 μF tantalum capacitor should be placed near the digital supply pin and connected directly to the analog ground plane. A 0.1 μF chip capacitor should be connected between the digital supply pin and the analog ground.

VREFHI, VREFLO, V2, V1 REFERENCE DISTRIBUTION

To ensure well-matched video outputs, all AD8382s must operate from equal reference voltages.

Each reference voltage should be distributed to each AD8382 directly from the source of the reference voltage with approximately equal trace lengths.

A 0.1 μF chip capacitor should be placed as close to each reference input pin as possible and directly connected between the reference input pin and the analog ground plane.

OUTLINE DIMENSIONS

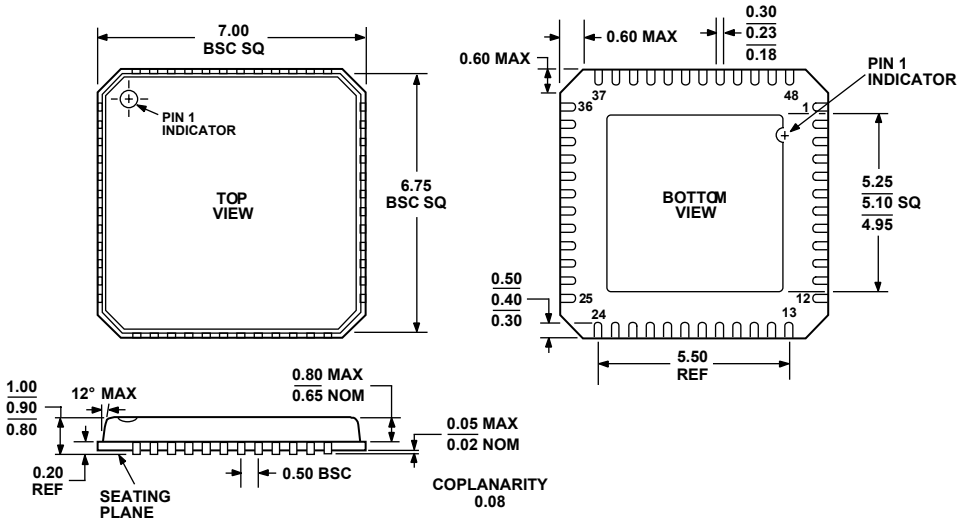

Figure 49. 48-Lead Frame Chip Scale Package [LFCSP] (CP-48)—Dimensions shown in millimeters

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8382 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Ordering Guide

Table 6.

Model	Temperature Range	Package Description	Package Option
AD8382ACP	0°C to 85°C	48-Lead LFCSP	CP-48

C03371-0-2/03(0)

www.analog.com