Broadband Modem Mixed Signal Front End

Preliminary Technical Data — AD9865/AD9866

FEATURES

Low Cost 3.3V-CMOS MxFE™ for Broadband Modems
10 or 12-Bit D/A Converter
- **2x / 4x Interpolating LPF or BPF Transmit Filter**
- **200 MSPS DAC Update Rate**
- **Wide (34 MHz) Transmit Bandwidth**
- **0 to -7.5 dBFS TxPGA**
- **Integrated 23 dBm (Peak) Line Driver w/PGA**

10 or 12-Bit, 80 MSPS A/D Converter
- **-12dB to 48dB Programmable Gain Amplifier**

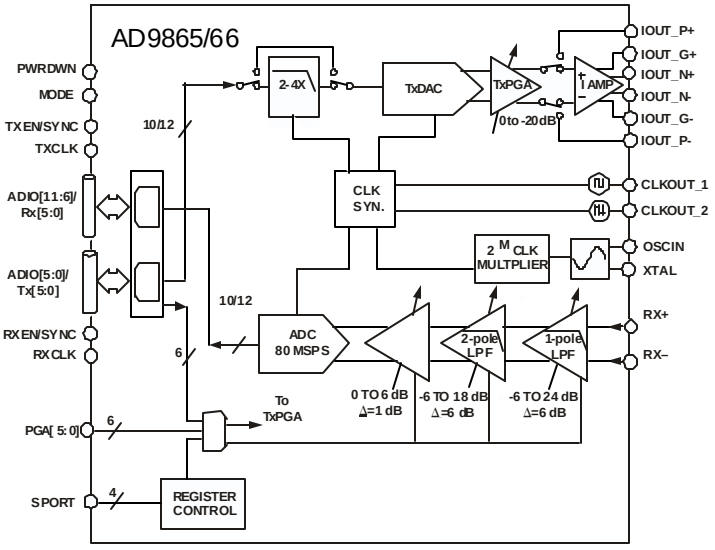
Flexible Digital Datapath Interface
- **Half and Full Duplex Operation**

Power Down Modes
Internal Clock Multiplier (PLL)
Auxiliary Clock Outputs
64-pin Chip-Scale Package

APPLICATIONS

Powerline Networking
Home Phone Networking
xDSL
Broadband Wireless
Home RF

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD9865 and AD9866 are single supply, broadband modem mixed-signal front-ends (MxFE™) IC's providing 10- and 12-bit converter resolution respectively. The transmit signal path contains an interpolation filter, a TxDAC, a PGA, and a line driver. The receive signal path provides a PGA, LPF and ADC that supports a variety of broadband modem applications. Also, an on-chip PLL clock multiplier and synthesizer provide all the required internal clocks and two external clocks from a single crystal or clock input.

The TxDAC+™ uses a by-passable digital 2X or 4X interpolation low pass or band pass filter to further oversample the transmit data and ease the complexity of analog reconstruction filtering. The transmit path bandwidth can be as high as 34 MHz at an input data rate of 80 MSPS. The 10/12-bit DAC provides differential current outputs whose full-scale current can be set over a 2-20 mA range.

These current outputs can be steered directly to an external load or to an internal low distortion current amplifier that can be configured as a current or voltage mode line driver. In the current mode, the amplified current ouputs are directed to a center-tap transformer referenced to a 3.0 V to +5.5 V supply. In the voltage mode, the amplifiers' current mirrors can be configured with an external pair of low cost npn transistors to provide a voltage output driver. Either mode of operation can deliver in excess of 22 dBm peak signal power.

The receive path consists of a PGA, LPF and ADC. The two-stage PGA has a gain range of -12dB to +48dB, and is programmable in 1 dB steps. This adds 60 dB of dynamic range to the receive path. The receive path LPF cutoff frequency can be either set over a 20-30 MHz range or simply bypassed. The 10/12-bit ADC achieves excellent dynamic performance with scalable power consumption allowing power/performance optimization.

The digital transmit and receive ports are extremely flexible allowing simple interfaces to digital backends that are configured as either master or slave to the MxFE. The 10/12-bit interface can be configured for full-duplex (i.e. nibble data transfer at $2*f_{DATA}$) or half-duplex operation (i.e. parallel data transfer at f_{DATA}). Power down modes also include the ability to reduce peak IC power consumption in half-duplex operation.

The AD9865/66 provides a highly integrated solution for many broadband modems. It is available in a space-saving 64-pin Chip-Scale package and is specified over the industrial (-40°C to +85°C) temperature range.

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REV PrA

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AD9865/66–SPECIFICATIONS

(V_S = +3.3V ± 10%, F_{OSCIN} = 25 MHz, f_{DAC} = 200 MHz, Gain = -6 dB, R_{SET} = 4.02 kΩ, 100 Ω DAC Load)

PARAMETER	Temp	Test Level	AD9865/6 Min	Typ	Max	Units
OSC IN CHARACTERISTICS						
Frequency Range	FULL	II	10		50	MHz
Duty Cycle	FULL	II	40	50	60	%
Input Capacitance	+25°C	III		3		pF
Input Impedance	+25°C	III		100		MΩ
CLOCK OUTPUT CHARACTERISTICS						
CLKOUT1 Jitter	+25°C	III		TBD		ps rms
CLKOUT1 Duty cycle	+25°C	III		±5		%
CLKOUT2 Jitter	+25°C	III		TBD		ps rms
CLKOUT2 Duty cycle	+25°C	III		+/-5		%
TX-CHARACTERISTICS						
TX-Path Latency, 4x Interpolation	FULL	II		96		F_{DAC} Cycles
Interpolation Filter Bandwidth (-0.2dB)						
4x Interpolation, LPF	FULL	II		21.9		MHz
2x Interpolation, LPF with f_{DAC}=100 MSPS	FULL	II		21.9		MHz
TX-DAC						
Resolution	FULL	II		10/12		Bits
Conversion Rate	FULL	II	0		200	MHz
Full-Scale Output Current	FULL	II	2	10	20	mA
Voltage Compliance Range	FULL	II	-0.5		1.5	V
Gain Error	FULL	II	-5	±2	+5	%FS
Output Offset	FULL	II	0	2	5	µA
Differential Nonlinearity	+25°C	III		+/-1.0		LSB
Integral Nonlinearity	+25°C	III		+/-2.0		LSB
Output Capacitance	+25°C	III		5		pF
Phase Noise @ 1kHz Offset, 10 MHz Signal	+25°C	III		-100		dBc/Hz
Signal-to-Noise and Distortion (SINAD)						
5 MHz Analog Out (28MHz BW)	FULL	I		61/70		dB
Wideband SFDR (to Nyquist, 64MHz max.)	+25°C	III				
5 MHZ Analog Out	+25°C	III		TBD		dBc
10 MHz Analog Out	+25°C	III		TBD		dBc
Narrowband SFDR (3MHz Window):						
10 MHz Analog Out	+25°C	III		TBD		dBc
IMD (f1 = 6.5MHz, f2 = 7.7MHz)	+25°C	III		TBD		dBFS
TX_IAMP CHARACTERISTICS						
ADC CHARACTERISTICS						
Resolution	n.a.	n.a.		10/12		Bits
Conversion Rate	FULL	II	7.5		80	MHz
Pipeline Delay, ADC Clock Cycles	n.a.	n.a.		TBD		Cycles
DC Accuracy						
Differential Nonlinearity	FULL	II	-1.0	±0.25	1.0	LSB
Integral Nonlinearity	FULL	II	-4.5	±1.0	3.5	LSB
Dynamic Performance (Ain=-0.5dB FS, f=5 MHz)						
@ F_{oscin}=50 MHz						
Signal-to-Noise and Distortion Ratio (SINAD)	FULL	I		61/68		dB
Effective Number of Bits (ENOB)	FULL	I		9.8/11		Bit
Signal-to-Noise Ratio (SNR)	+25°C	III		59		dB
Total Harmonic Distortion (THD)	+25°C	III		TBD		dB
Spurious Free Dynamic Range (SFDR)	+25°C	III		TBD		dB
Total Harmonic Distortion (THD)	+25°C	III		-67		dB
Spurious Free Dynamic Range (SFDR)	+25°C	III		68		dB
RX PATH GAIN/OFFSET						
Minimum Gain	+25°C	III		-12		dB
Maximum Gain (12 MHz Filter)	+25°C	III			36	dB
Gain Step Size	+25°C	III		1		dB

(V_S = +3.3V ± 10%, F_{OSCIN}=25 MHz, F_{DAC} = 200 MHz, Gain = -6dB, R_{SET} = 4.02 kΩ, 100Ω DAC Load)

PARAMETER	Temp	Test Level	AD9865/6 Min	Typ	Max	Units
Gain Step Accuracy	+25°C	III		+/-0.25		dB
Gain Range Error	+25°C	III		+/-1.0		dB
Offset Error, PGA Gain = 0dB	+25°C	III		TBD		LSBs
Absolute Gain Error, PGA Gain = 0dB	+25°C	III		+/-0.5		dB
RX PATH INPUT CHARACTERISTICS						
Input Voltage Range	FULL	III		4		Vppd
Input Capacitance	+25°C	III		4		pF
Differential Input Resistance	+25°C	III		400		Ohm
Input Bandwidth (-3dB)	+25°C	III		TBD		MHz
Input referred Noise (at 36 dB gain with filter)	+25°C	III		21		µV rms
Input referred Noise (at -6 dB gain with filter)	+25°C	III		TBD		µV rms
Common Mode Rejection	+25°C	III		40		dB
RX PATH LPF (Low Cutoff Frequency)						
Cut-off Frequency ($f_{CUT-OFF}$)	+25°C	III	20		30	MHz
Cut-off Frequency Variation	+25°C	III		±5		%
Attenuation @ 55.2 MHz w/ f_{CUT_OFF} =23 MHz	+25°C	III		20		dB
Passband Ripple	+25°C	III		±1.0		dB
Group Delay Variation	+25°C	III		TBD		ns
Settling Time (to 1% FS, Min to Max Gain Change)	+25°C	III		TBD		ns
Total Harmonic Distortion at Max Gain (THD)	+25°C	III		TBD		dBc
RX PATH DISTORTION PERFORMANCE						
IMD: f1 = 14 MHz, f2 = 15 MHz						
23 MHz Filter: 0 dB	+25°C	III		-65		dB_C
POWER DOWN/DISABLE TIMING						
Power Down Delay (Active-to-Power Down)						
DAC	FULL	II			TBD	ns
Interpolator	FULL	II			TBD	µs
Power Up Delay (Power Down-to-Active)						
DAC	FULL	II			TBD	µs
PLL	FULL	II			TBD	µs
ADC	FULL	II			TBD	µs
PGA	FULL	II			TBD	µs
LPF	FULL	II			TBD	µs
Interpolator	FULL	II			TBD	µs
Minimum RESET Pulsewidth Low (t_{RL})	FULL	II			5	F_{OSCIN} Cyc
TX Path Interface						
Maximum Input Nibble Rate, 2x Interp.	+25°C	I	160			MHz
TX-Set up time (t_{su})	+25°C	II	TBD			ns
TX-Hold time (t_{hd})	+25°C	II	TBD			ns
RX Path Interface						
Maximum Output Nibble rate	+25°C	I	160			MHz
RX-Data valid time(t_{vt})	+25°C	II			TBD	ns
RX-Data hold time (t_{ht})	+25°C	II	TBD			ns
Serial Control Bus						
Maximum SCLK Frequency (F_{SCLK})	FULL	II	32			MHz
Clock Pulsewidth High (t_{PWH})	FULL	II	18			ns
Clock Pulsewidth Low (t_{PWL})	FULL	II	18			ns
Clock Rise/Fall Time	FULL	II			1	ms
Data/Chip-Select Setup Time (t_{DS})	FULL	II	25			ns
Data Hold Time (t_{DH})	FULL	II	0			ns
Data Valid Time (t_{DV})	FULL	II			20	ns
CMOS LOGIC INPUTS						
Logic "1" Voltage	+25°C	II	V_{DRVDD}-0.7			V
Logic "0" Voltage	+25°C	II			0.4	V

AD9865/66–SPECIFICATIONS

(V_S = +3.3V ± 10%, F_{OSCIN} = 25 MHz, f_{DAC} = 200 MHz, Gain = -6 dB, R_{SET} = 4.02 kΩ, 100 Ω DAC Load)

PARAMETER	Temp	Test Level	AD9865/6 Min	Typ	Max	Units
Logic "1" Current	+25°C	II			10	µA
Logic "0" Current	+25°C	II			10	µA
Input Capacitance	+25°C	III		3		pF
CMOS LOGIC OUTPUTS[1]						
Logic "1" Voltage	FULL	II	V_{DRVDD}-0.6			V
Logic "0" Voltage	+25°C	II			0.3	V
Digital Output Rise-/Fall Time	FULL	II	1.5		2.5	ns
POWER SUPPLY						
All Blocks Powered Up						
I_{S_TOTAL} (Total Supply Current)	FULL	II		320		mA
Digital Supply Current (I_{DRVDD}+I_{DVDD})	+25°C	III		50		mA
Analog Supply Current (I_{AVDD})	+25°C	III		270		mA
Power Consumption of Functional Blocks:						
Rx PGA & LPF	+25°C	III		70		mA
ADC	+25°C	III		80		mA
Rx Reference	+25°C	III		5		mA
Interpolator	+25°C	III		40		mA
DAC&IAMP	+25°C	III		110		mA
PLL	+25°C	III		15		
All Blocks Powered Down						
Supply Current I_S, Foscin = 50 MHz	FULL	II		TBD		mA
Supply Current I_S, Foscin Idle	FULL	II		TBD		mA
Power Supply Rejection						
Tx Path (ΔV_S = +/-10%)	+25°C	III		62		dB
Rx Path (ΔV_S = +/-10%)	+25°C	III		54		dB
RECEIVE-TO-TRANSMIT ISOLATION (10MHz, Full-Scale Sinewave Output/Output)						
Isolation: Tx Path to Rx Path, Gain = 36dB	+25°C	III		-75		dB
Isolation: Rx Path to Tx Path, Gain = -6dB	+25°C	III		-70		dB

NOTES
Specifications subject to change without notice.
[1] 1mA Load and 10 pFcapacitor load

ABSOLUTE MAXIMUM RATINGS*

Power Supply (V_S) ..... + 3.9 V
Digital Output Current ..... 5 mA
Digital Inputs ..... -0.3 V to DRVDD + 0.3V
Analog Inputs ..... -0.3V to AVDD +0.3V
Operating Temperature ..... -40°C to+85 °C
Maximum Junction Temperature ..... +150 °C
Storage Temperature..... -65 °C to 150 °C
Lead Temperature (Solderring 10 sec) ..... +260 °C

*Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure of absolute maximum rating conditions for extended periods of time may affect device reliability.

ORDERING GUIDE

EXPLANATION OF TEST LEVELS

I - Devices are 100% production tested at +25°C and guaranteed by design and characterization testing for commercial operating temperature range (-40°C to 85°C).

II - Parameter is guaranteed by design and /or characterization testing.

III- Parameter is a typical value only.

THERMAL CHARACTERISTICS

Thermal Resistance

64-Lead CSP
θ_{JA} = °C/W
θ_{JC} = °C/W

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9865/6 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

DEFINITIONS OF SPECIFICATIONS

CLOCK JITTER

The clock jitter is a measure of the*intrinsic* jitter of the PLL generated clocks. It is a measure of the jitter from one rising and of the clock with respect to another edge of the clock 9 cycles later.

DIFFERENTIAL NONLINEARITY ERROR (DNL, NO MISSING CODES)

An ideal converter exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Guaranteed no missing codes to 10-bit resolution indicates that all 1024 codes respectively, must be present over all operating ranges.

INTEGRAL NONLINEARITY ERROR (INL)

Linearity error refers to the deviation of each individual code from a line drawn from "negative full scale" through "positive full scale." The point used as "negative full scale" occurs 1/2 LSB before the first code transition. "Positive full scale" is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

PHASE NOISE

Single-sideband phase noise power density is specified relativ to the carrier (dBc/Hz) at a given frequency offset (1kHz) from the carrier. Phase noise can be measured directly on a generated single tone with a spectrum analyzer that supports noise marker measurements. It detects the relative power between the carrier and the offset (1kHz) sideband noise and takes the resolution bandwidth (rbw) into account by subtracting 10log(rbw). It also adds a correction factor that compensates for the implementation of the resolution bandwidth, log display and detector characteristic.

OUTPUT COMPLIANCE RANGE

The range of allowable voltage at the output of a current-output DAC. Operation beyond the maximum compliance limits may cause either output stage saturation, resulting in nonlinear performance or breakdown.

SPURIOUS-FREE DYNAMIC RANGE (SFDR)

The difference, in dB, between the rms amplitude of the DACs output signal (or ADC's input signal) and the peak spurious signal over the specified bandwidth (Nyquist bandwidth unless otherwise noted).

PIPELINE DELAY (LATENCY)

The number of clock cycles between conversion initiation and the associated output data being made available.

OFFSET ERROR

First transition should occur for an analog value 1/2 LSB above negative full scale. Offset error is defined as the deviation of the actual transition from that point.

GAIN ERROR

The first code transition should occur at an analog value 1/2 LSB above negative full scale. The last transition should occur for an analog value 1 1/2 LSB below the nominal full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

INPUT REFERED NOISE

The RMS output nosie is measured using histogram techniques. The ADC output codes' standard deviation is calculated in LSB, and converted to an equivalent voltage. This results in a noise figure that can directly be referred to the Rx input of the AD9865.

SIGNAL-TO-NOISE AND DISTORTION RATIO (SINAD)

SINAD is the ratio of the RMS value of the measured input signal to theRMS sum of all other spectral components below the Nyquist frequency, including harmonics but excluding DC. The value for SINAD is expressed in decibels.

EFFECTIVE NUMBER OF BITS (ENOB)

For a sine wave, SINAD can be expressed in terms of the number of bits. Using the following formula,

$$N = (SINAD - 1.76)\text{dB}/6.02$$

it is possible to get a measure of performance expressed as$N$, the effective number of bits.

SIGNAL-TO-NOISE RATIO (SNR)

SNR is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

TOTAL HARMONIC DISTORTION (THD)

THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

POWER SUPPLY REJECTION

Power Supply Rejection specifies the converters maximum full-scale change when the supplies are varied from nominal to minimum and maximum specified voltages.

PIN #	Pin Name	Pin Function
	RXEN/RxSYNC	ADIO Buffer Control Input-Half DuplexMode Rx Data Synchronization Output-Full Duplex Mode
	RXCLK	ADIO Request Clock Input-Half DuplexMode Rx and Tx Clock Output at $2xf_{ADC}$-Full Duplex Mode
	ADIO9/Rx[5]	MSB of ADIO Buffer-Half Duplex Mode MSB of Rx Nibble Output-Full Duplex Mode
	ADIO8-5/Rx[4-1]	Bits 8-5 of ADIO Buffer-Half Duplex Mode Bits 4-1 of Rx Nibble Output-Full Duplex Mode
	ADIO4/Rx[0]	Bit 4 of ADIO Buffer-Half Duplex Mode LSB of Rx Nibble Output-Full Duplex Mode
	ADIO3/Tx[5]	Bit 3 of ADIO Buffer-Half Duplex Mode MSB of Tx Nibble Input-Full Duplex Mode
	ADIO2-1/Tx[4-3]	Bits 2-1 of ADIO Buffer-Half Duplex Mode Bits 4-3 of Tx Nibble Input-Full Duplex Mode
	ADIO0/Tx[2]	LSB of ADIO Buffer-Half Duplex Mode Bit 2 of Tx Nibble Input-Full Duplex Mode
	NC/Tx[1]	No Connect-Half Duplex Mode Bit 1 of Tx Nibble Input-Full Duplex Mode
	NC/Tx[0]	No Connect-Half Duplex Mode LSB of Tx Nibble Input-Full Duplex Mode
	TXEN/TxSYNC	Tx Path Enable Input-Half DuplexMode Tx Data Synchronization Output-Full Duplex Mode
	TXCLK/PGA_EN	Tx Clock Input-Half Duplex Mode

AD9865/AD9866

PIN #	Pin Name	Pin Function
	DRVDD	Digital Output Driver Supply Input
	DRVSS	Digital Output Driver Supply Return
	CLKOUT1	f_{DAC}/N Clock Output (L=1, 2, 4, or 8)
	GAIN/PGA[5]	Tx Data Port (Tx{4:0]) Mode Select-Full Duplex Mode MSB of Rx PGA Gain Setting Input-Half Duplex Mode
	PGA[4-0]	Rx PGA Gain Setting Input
	SEN	Serial Port Enable Input
	SCLK	Serial Port Clock Input
	SDIO	Serial Port Data Input/Output
	SDO	Serial Port Data Output
	RESET	Reset Input(Active Low)
	AVSS	Analog Ground
	REFB, REFT	ADC Reference Decoupling Nodes
	AVDD	Analog Power Supply Input
	RX+, RX-	Receive Path + and - Inputs
	REFADJ	TxDAC Full-Scale Current Adjust
	REFIO	TxDAC Reference Input/Output
	IOUT_G-	- Tx Amp Current Output_Sink
	IOUT_P-	- TxDAC Current Output_Source
	IOUT_N-	- Tx Mirror Current Output_Sink
	OUT_G+	+ Tx Amp Current Output_Sink
	OUT_P+	+ TxDAC Current Output_Source
	IOUT_N+	+ Tx Mirror Current Output_Sink
	VCC	+5 V Supply for Tx Amp in Voltage Output Mode
	CLKVSS	Clock Oscillator/Synthesizer Supply Return
	XTAL	Crystal Oscillator Inverter Output
	OSCIN	Crystal Oscillator Inverter Input
	CLKVDD	Clock Oscillator/Synthesizer Supply
	DVSS	Digital Supply Return
	MODE	Full-Duplex (HIGH) or Half Duplex(LOW) Select
	DVDD	Digital Supply Input
	CLKOUT2	f_{OSCIN}/L Clock Output (L=1, 2, or 4)
	PWR_DWN	Power Down Input (Full-Duplex mode is SPORT programable while Half-Duplex is ACTIVE HIGH places AD9865 into Stand-BY.

TRANSMIT PATH

The AD9865/66 transmit path consists of a selectable digital 2x/4x interpolation filter, a 10-bit TxDAC, a TxPGA, and a current-output amplifier as shown in figure 1a. The digital interpolation filter relaxes the Tx analog filtering requirements by simultaneously reducing the images from the DAC reconstruction process while increasing the analog filters transition band. The digital interpolation filter can also be bypassed resulting in lower digital current consumption.

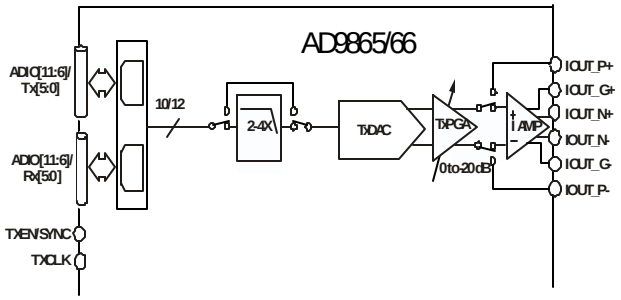

Figure 1a. AD9865/66 Tx Signal Path

Digital Interpolation Filters

The input data from the Tx port can be fed directly into the TxDAC or into a selectable 2X/4X interpolation filter. The interpolation filter configuration is controllable via the SPORT. The maximum input word rate into the interpolation filter is 80 MSPS while the maximum DAC update rate is 200 MSPS. Hence, applications with input word rates at or below 50 MSPS can benefit with 4X interpolation while applications with input word rates between 50-80 MSPS can benefit with 2X interpolation. Note, the default setting will be for 4X interpolation.

The interpolation filter consists of two cascaded half-band filter stages with each stage providing 2X interpolation. The 1st stage filter consists of 43 taps while the 2nd stage filter operating at the higher data rate consists of 11 taps. An alternative 2nd stage filter consisting of 43 taps is also included to provide a bandpass response that is backward compatible with the AD9875. Note, use of this filter limits the input word to only 32 MSPS thus this filter is only recommended if a *bandpass* response is desired.

The wideband and pass band filter responses for the 2X and 4X low pass interpolation filter (excluding the sinc response of the TxDAC) are shown in figure 1b and 1c respectively for an input data rate, f_{DATA}, of 50 MSPS. Both responses provide less than -0.1 dB passband ripple out to 21.5 MHz. The pipeline delay of the 2X and 4X filter response is 43 and 96 clock cycles relative to f_{DAC}. Note, relative to f_{DATA}, the 4X filter response has an additional 2.5 clock cycle delay than the 2X filter response. This filter delay is also taken into consideration for applications powering down the TxDAC and IAMP after a Tx bursts by adding an equal delay to their internal power-down control signal. This feature powers done the TxDAC and IAMP only after the last Tx input sample has propagated through the digital filter.

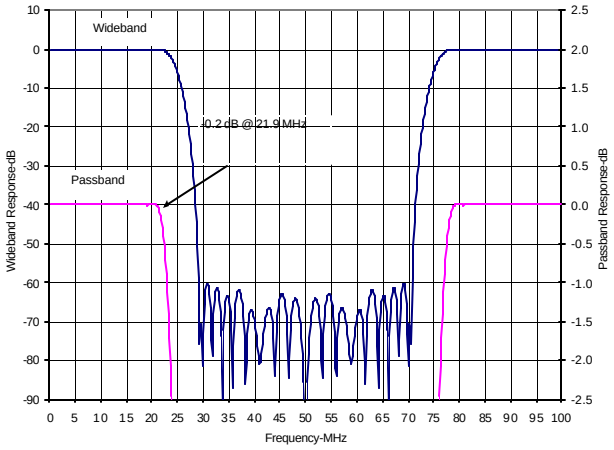

Figure 1b. Frequency Response of 2X Interpolation filter with f_{DATA}=50 MSPS and f_{DAC}=100 MSPS

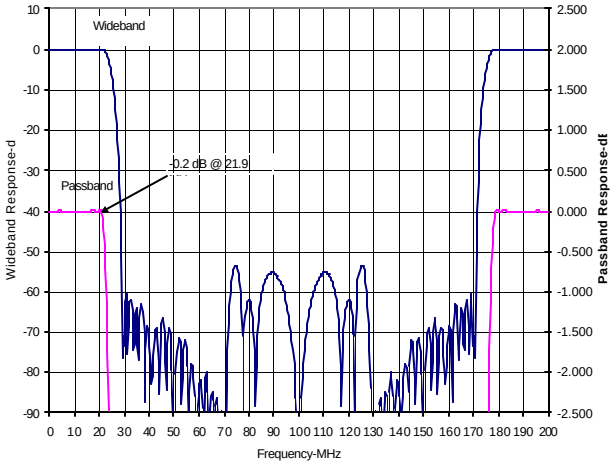

Figure 1c. Frequency Response of 4X Interpolation filter with f_{DATA}=50 MSPS and f_{DAC}=200 MSPS

TxDAC and TxPGA

The TxDAC provides a differential current output whose full-scale output, IOUTFS, can be set between 2-20 mA (i.e. 20 dB span). The IOUTFS is set by an external resistor, R_{SET}, and can also be digitally adjusted over a 20 dB range via the TxPGA. The gain of the TxPGA can be controlled via the PGA port (PGA[5:0]) for fast updates (i.e. during transmit bursts) or set via a SPORT register. A SPORT register bit must be set to enable Tx gain con-

trol via the PGA port for half-duplex applications. When this feature is enabled, data appearing at the PGA port during Tx burst updates the Tx gain after a slight delay through the decode logic. Applications configured for a half-duplex digital data interface can use the RXEN control signal to mux the PGA port between Tx and Rx gain. The Tx gain register is 6-bits wide allowing Tx gain adjustments over a 19.5 dB span with 0.5 dB resolution. Note, this gain range is distributed such that the TxDAC has 7.5 dB range and the IAMP has 12 dB of range. Tx PGA's default setting is *full-scale* (0 dBFS) with the PGA port *disabled* for Tx gain control.

The differential current output of the TxPGA can be either directed to an external ground referenced load or the current output amplifier. Applications not requiring additional Tx drive capabilities, demanding the highest spectral performance, and/or lower power consumption may benefit from using the TxPGA output directly as shown in figure 2. Optimum distortion performance is achieved with a common-mode voltage of 0.5 V or less and a differential output voltage swing of 1 Vp.p. Note, the Tx gain range is limited to 7.5 dB since the IAMP is not used.

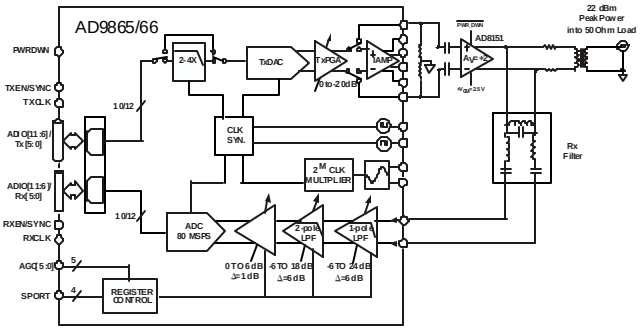

Figure 2. TxPGA current output sourcing current into load with external amplifier.

IAMP

Applications demanding higher output voltage swings and power drive capabilities will benefit from using the current output amplifier. The differential current output amplifier consists of two sets of NMOS current mirrors providing a gain range of 12 dB with ? dB resolution. The current output of the TxPGA is amplified by this gain with its signal reference to the positive supply. The standing current into these mirrors is programmable (independent of TxPGA) such that the signal-to-standing current ratio can be optimized for distortion performance.

The 1st set of mirrors is optimized for performance, replicating the TxPGA's current output with a selectable gain with minimal distortion. The maximum current through this mirror should be set to less than 25 mA. The outputs of this 1st mirror are IOUTN+ and IOUTN- and any loads should be sized and referenced to a positive supply such that the voltage appearing at either pin is always greater than +1 V and less than +7.0 V ????. The 2nd set is optimized for maximum current handling capability (i.e. 180 mA peak current per output) at the expense of degraded distortion performance. The outputs of this 2nd mirror are IOUTG+ and IOUTG-.

The IAMP can be configured for current or voltage mode operation. The current mode configuration shown in figure 3a is suited for well defined loads (i.e. 50 or 75Ω) that are referenced to a positive supply. Since the mirrors exhibit a high output impedance, it can be easily backward terminated. Maximum output drive capability is achieved using a center-tap transformer with each output swinging over a 1 to 7 V span . Note, the distortion performance of this configuration will be limited by the 2nd set of current amplification mirrors.

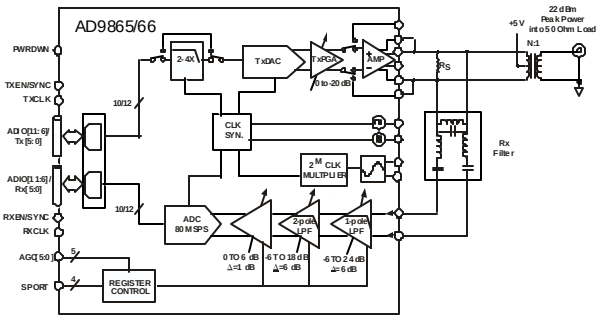

Figure 3a. Current Mode Operation.

The voltage mode configuration is shown in figure 3b. This configuration is suited for applications having a poorly defined load that can vary over a considerable range (i.e. powerline). A low impedance voltage driver can be realized with the addition of two external transistors (i.e. 2N3904) and resistors. In this configuration, the 1st set of current mirrors is used to generate a low distortion differential input signal for the npn transistors configured as source followers. The 2nd set of mirrors provides both the signal-dependent bias current for these transistors.

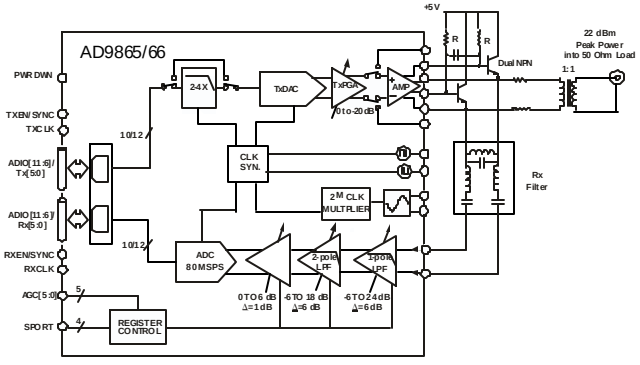

Figure 3b. Voltage Mode Operation.

The signal current is routed to the external resistors to develop a differential voltage as high as 3.3 V peak across the base of the npn transistors while operating off of a +5 V supply. The amount of standing and signal dependent current used to bias the npn transistors is SPI programmable allowing optimization of linearity vs power efficiency. Lastly, the voltage output driver will exhibit high output impedance if the bias currents for the npn transistors are removed.

RECEIVE PATH DESCRIPTION

The receive path block diagram is shown in figure xx. The receive path consists of a two stage PGA, a continuous time, 4-pole LPF, an ADC, and a digital data multiplexer. Also working in conjunction with the receive path is an offset correction circuit and a digital phase lock loop. Each of these blocks will be discussed in detail in the following sections.

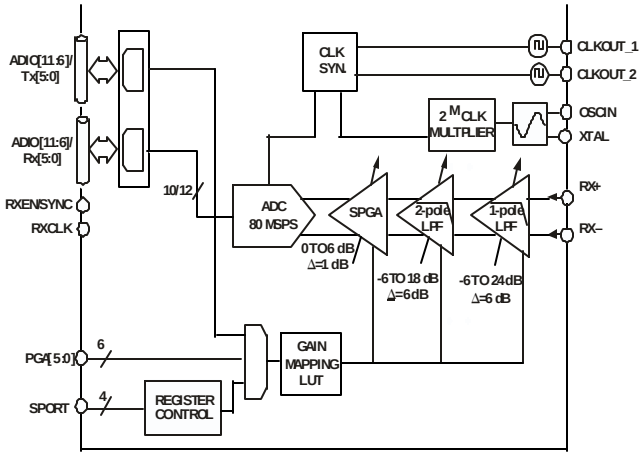

Figure 4. AD9865 Rx Path

RX PROGRAMMABLE GAIN AMPLIFIER

The Rx PGA has a programmable gain range from -12 to 48 dB with 1 dB resolution. The PGA is comprised of two sections, a Continuous Time PGA (CPGA) for course gain and a Switched Capacitor PGA (SPGA) for fine gain resolution. The CPGA consists of two cascaded gain stages providing a gain range from -12 to 42 dB with 6 dB resolution. The SPGA provides a gain range from 0 to 6 dB with 1 dB resolution.

Since the gain is distributed over 3 stages, all of the possible Rx PGA gain settings (excluding -12 dB and 48 dB) have 2 or more possible gain distribution settings that result in the desired PGA gain setting. As a result, a selectable gain mapping look-up table (LUT) is included that optimizes the PGA for either noise or distortion performance. Figure 5 provides the project SNR and spectral voltage noise density (Vn_rtHz) performance for optimum noise setting of the AD9865 over the full-range of gain settings. Note, the equivalent Vn_rtHz at 36 dB gain is 5.1 nV/rtHz thus the equivalent integrated noise over a 17 MHz bandwidth (i.e. HomePlug 1.0 passband) is 21 uVrms.

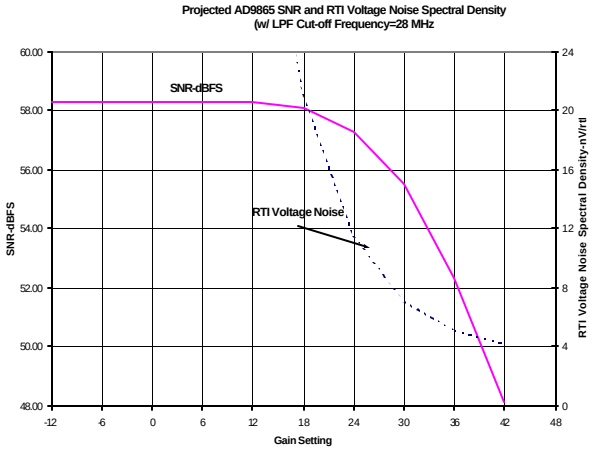

Figure 5. Projected SNR and input referred voltage noise of the AD9865 at different gain settings.

The maximum peak-to-peak differential voltage that will not result in clipping of the ADC is shown in Table I for various gain settings. While the table suggests that maximum input signal for a gain setting of -12 dB is 8.0 Vp.p., the maximum input voltage into the PGA should be limited to 6 Vp.p. to prevent turning on ESD protection diodes. Applications having higher maximum input signals should consider adding an external attenuator. Note, the input sensitivity of the Rx path will be degraded by amount of attenuation on a dB-to-dB basis.

Total Gain	Vpk-to-pk(Max)
-12	7.9621
-6	3.9905
0	2
6	1.0024
12	0.5024
18	0.2518
24	0.1262
30	0.0632
36	0.0317
42	0.0159

Table I. Max peak-to-peak PGAinput voltage per gain setting will not result in ADC clipping.

The nominal differential input impedance of the Rx PGA input appearing at the device RX+ and RX- input pins is 400 ohms//4 pF (+/-20%) that is relatively indpendent of gain. The PGA input is biased at a 1.3 V common-mode

level allowing a maximum input voltage swings of +/-1.5 V at RX+ and RX-. AC coupling the input signal to this stage is *recommended* to ensure that the AD9865/66 maintains high dynamic range for high gain settings since any dc offset appearing at the Rx PGA input will be amplified by the PGA gain, presenting a large dc offset to the ADC. To limit the PGA's self-induced input offset, an offset cancellation loop is included to servo this offset to a negligible low level. Note, the offset cancellation circuitry is only intended to reduce the voltage offset attributed to the PGA's input stage... not any dc offsets attributed by an external preamplifier.

The Rx PGA gain register is 6 bits wide to accommodate a 60 dB range with 1 dB resolution. For maximum flexiblity as well as backward compatibility with existing MxFE's (i.e. AD9875, AD9876 and AD9975), the PGA's gain can be updated via the following ports: PGA[5:0], PGA[5:3], Tx[5:0], and SPORT. The SPORT port should be used for slow updates since it is limited by the speed of the serial SPORT interface.

Applications requiring fast updates of the PGA gain setting (i.e. under AGC control) should use either the PGA[5:0] or Tx[5:0] port. Full-duplex applications requiring simultaneous Tx and Rx operation *must* use the PGA[5:0] for fast updates. Half-duplex applications demanding fast updates or AD9975 backward compatiblility should use the PGA[5:0] port. Half-duplex applications that require backward compatibility with the AD9875/76 can use the Tx[5:0] port along with the GAIN and TxSYNC pins. Refer to the Full Duplex Mode section of the datasheet for timing information.

PGA[5:0] is a dedicated port allowing direct update of the Rx (or Tx) PGA register via a mux. Updating of the TxPGA register via the PGA port requires proper setting of a SPORT register. This feature can be enabled for half-duplex digital interfaces in which RXEN can be used to control the mux.

Data appearing at PGA[5:0] automatically updates the Rx PGA gain setting after a slight propagation delay (due to LUT). This port can also be configured to be backwared compatible with the AD9975 with the MODE selection pin. In this case, pins PGA[5:3] can be driven by a 3-bit AGC word with the gain mapping shown in Table I. Note, the gain mapping provides only 7 gain steps with 8 dB resolution.

PGA[5:3]	PGA Gain	Vpk-to-pk(Max)
0x0	-10	6.3246
0x1	-10	6.3246
0x2	-2	2.5179
0x3	6	1.0024
0x4	14	0.3991
0x5	22	0.1589
0x6	30	0.0632
0x7	38	0.0252

Table I. Gain Mapping for AD9975 backward compatible mode

LOW PASS FILTER

The low pass filter (LPF) is a 3rd order low pass filter with a 20 to 30 MHz programmable cut-off frequency. The cut-off frequency remains relativley independent for most PGA gain setting and is programmable via a SPORT register (with a default setting of 23 MHz for f_{OSCIN}=50 MHz). The LPF may also be disabled providing a 3dB bandwidth of approximately ?? MHz.

Calibration of the LPF automatically occurs upon device power-up to compensate for process variations. After calibration, the cut-off frequency will have a 10% tolerance over the AD9865/66's full specified operation range Applications requiring tighter tolerance can also intiate a calibration via a SPORT register to compensate for temperature drift or supply variations.

Figure 4 shows that the first real pole is implemented within the 1st PGA gain stage while the complex pole pair is implemented in the 2nd PGA gain stage. The normalized wideband gain response is shown in Figure 9a while the normalized passband gain and group delay response is shown in figure 9b. Note, the normalized cut-off frequency, fo, results in -0.63 attenuation. Also, the actual group delay (GDT) response can be calculated given a programmed cut-off frequency using the following equation:

Actual GDT=Normalized GDT/(2.418*fo).

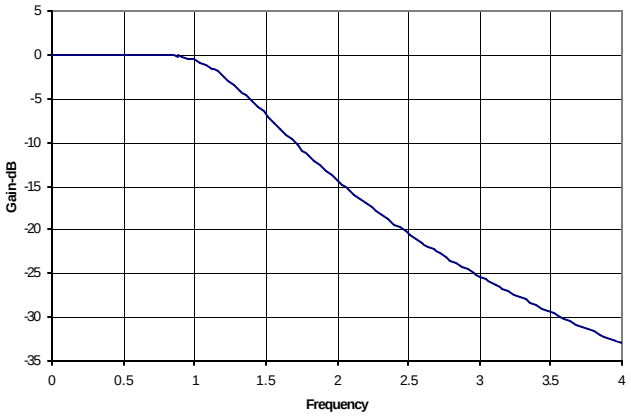

Figure 9a. LPF's Normalized Wideband Gain Response

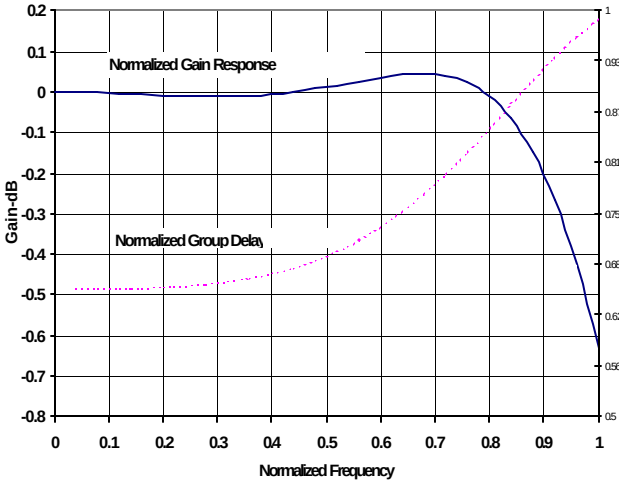

Figure 9b. LPF's Normaized Passband Gain and Group Delay Response

ADC

The AD9865 features a 10-bit analog-to-digital converter (ADC) capable of up to 80 MSPS. Refering to figure 4, the ADC is driven by the SPGA stage that performs both the sample-and-hold as well as fine gain adjust function. A buffer amplifier (not) shown isolates the last CPGA gain stage from the dynamic load presented by the SPGA stage. The full-scale input span of the ADC is 2 Vp.p. with the full-scale input span into the SPGA being adjustable from 1 to 2 V in 1 dB increments depending on the PGA gain setting.

A pipelined multistage ADC architecture is used to achieve high sample rates while consuming low power. The ADC distributes the conversion over several smaller A/D subblocks, refining the conversion with progressively higher accuracy as it passes the results from stage to stage. Its power consumption is programmable via a SPORT register allowing the user to optimize its power consumption vs. linearity performance for lower sample rates. Also, the ADC can be completely power-down for half-duplex operation further reducing the AD9865's peak power consumption.

The *default* power-up digital output data format is dependent on the mode selected and is as follows:

Half Duplex Mode-Straight Binary

Full Duplex Mode-2's Complement

Note, a SPORT register allows the the data format to be configured for Straight Binary or 2's Complement for either mode.

CLOCK AND OSCILLATOR CIRCUITRY

The AD9865's internal oscillator generates all sampling clocks from a fundamental frequency quartz crystal. Figure xx shows how the quartz crystal is connected between OSC IN) and XTAL with parallel resonant load capacitors as specified by the crystal manufacturer. It also supports overtone crystals. The internal oscillator circuitry can also be overdriven by a TTL level clock applied to OSC IN with XTAL left unconnected.

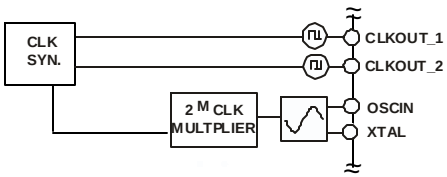

Figure 10. Clock Oscillator and Synthesizer

The 2 M CLK Multiplier contains a PLL and VCOcapable of generating an output frequency that is a multiple of 1,2,3 or 4 of the input reference frequency appearing at OSCIN. The CLK multiplier has an input frequency range between 10MHz and 50 MHz and its VCO can operate over a ?? and 200 MHz span. The TxDAC update rate, f_{DAC}, is always set to the same frequency as the VCO and the the loop filter is integrated into the PLL circuitry.

The CLK synthesizer block generates all of the internal clocks for the AD9865/66 as well as provides two user programmable clock outputs appearing at CLKOUT_1 and CLKOUT_2. Both outputs can be inverted or disabled. The CLKOUT_1 frequency can be set via a SPORT register to be a submultiple integer of f_{DAC}, (i.e. f_{DAC}/N where N=1, 2, 4, or 8) while the CLKOUT_2 frequency can be set to be a submultiple integer of the

oscillator's input frequency f_{OSCIN} (i.e. f_{OSCIN}/L where L=1, 2, or 4).

When the MODE pin is tied LOW (i.e. AD9975 backward compatible), the default setting for these clock outputs are N=2 and L=2 such that for an f_{OSCIN} =50 MHz (with 4X interpolation), the clock frequencies appearing at CLKOUT_1 and CLKOUT_2 are 100 and 25 MHz. When the MODE pin is tied HIGH (i.e. AD9875/76 backward compatible), the default setting for these clock outputs are N=2 and L=2. Note, the voltage levels appearing at these outputs are relative to DRVDD and *remain active* during a hardware or software reset.

DIGITAL INTERFACE

The digital interface port shown in figure x.x can be configured for a half-duplex mode (i.e. AD9975 backward compatible) or full-duplex mode (i.e. AD9875/76 backward compatible) of operation by pin-strapping the MODE pin LOW or HIGH respectively. The PGA port is automatically configured to support either backward compatible mode of operation. Hence, applications desiring to use all 6-bits of the PGA port Rx (and Tx) gain control must configure a SPORT register.

In the half-duplex mode, the AD9865/66 interface acts as a slave to the digital ASIC while in the full-duplex mode it acts as the master. In the half-duplex mode, the digital interface port becomes a 10/12-bit bidirectional ADIO bus (i.e. AD9865 or AD9866). In the full-duplex mode, the port is divided into two 6-bit ports called Tx[5:0] and Rx[5:0] for simultaneous Rx and Tx operations. In this mode, data is transferred between the ASIC and AD9865 in 6-bit nibbles. Also, the Rx PGA gain can be set via Tx[5:0] during transmit bursts (i.e. AD9875/76 backward compatible) with pin GAIN/PGA[5].

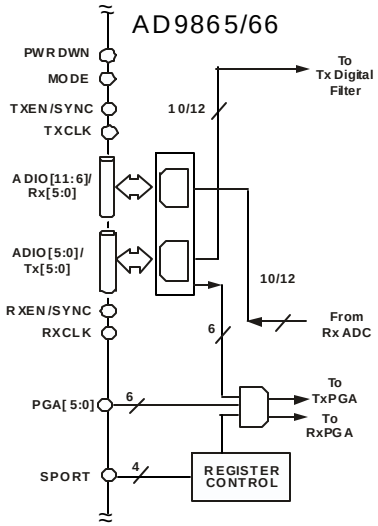

Figure x.x Digital Interface functional block diagram

HALF-DUPLEX MODE

The half-duplex mode functions as follows when the MODE pin is tied LOW. The bidirectional ADIO bus is shared in burst fashion between the transmit path and receive path. The AD9865/66 MxFE acts as a slave to the digital ASIC, accepting two input enable signals, TXEN and RXEN, as well as two input clock signals, TXCLK and RXCLK. Because the sampling clocks for the DAC and ADC are derived internally from the OSCIN signal, it is required that the TXCLK and RXCLK signals are exactly the same frequency as the OSCIN signal. The phase relationships between the TXCLK, RXCLK, and OSCIN signal are arbitrary.

In order to add flexibility to the digital interface port, there are several programming options available. The data input format is *straight binary* by default but can be changed to two's complement via a SPORT register. It is possible to independently change the data format of the transmit path and receive path to two's complement. Also, the clock timing can be independently changed on the transmit and receive paths by selecting either the rising or falling clock edge as the validating/sampling edge of the clock. The digital interface port can also be programmed into a three-state output mode allowing it to be connected onto
a shared bus.

The ADIO Bus accepts input data-words into the transmit path when the TXEN Pin is high, the RXEN Pin is low, and a clock is present on the TXCLK Pin. Figure x.x illustrates the transmit path input timing.

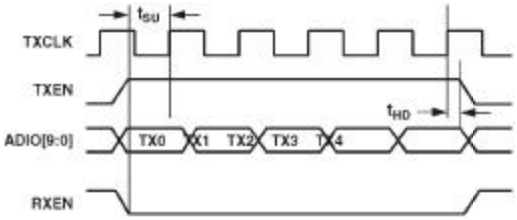

Figure x.x. Transmit Data Input Timing Diagram

It should be noted that to clear the transmit path input buffers, an additional six clock cycles on the TXCLK input are required after TXEN goes low. The interpolation filters will be "flushed" with zeros if the clock signal into the TXCLK Pin is present for 43/96 clock cycles for 2X/4X interpolation after TXEN goes low (the data on the ADIObus being irrelevant over this interval). ?????

The output from the receive path will be driven onto the ADIO Bus when the RXEN Pin is high, and a clock is present on the RXCLK Pin. When both TXEN and RXEN are low, the ADIO Bus is three-stated. Figure x.x illustrates the receive path output timing.

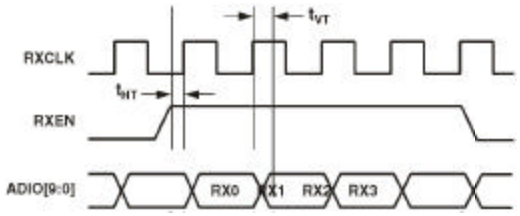

Figure x.x. Receive Data Output Timing Diagram

In the half-duplex mode interface, Rx and Tx PGA data can be loaded into the PGA port for fast updates. The default setting is for the PGA port to be backward compatible with the AD9975 such that pins PGA[5:3] correspond to the AD9975's AGC[2:0] pins with the gain mapping described in Table 2. In this default state, only the RxPGA can be updated. Applications desiring higher Rx PGA gain range/resolution and/or fast Tx PGA update, must configure the PGA port for this alternative option via the SPORT.

FULL-DUPLEX MODE

The full-duplex interface mode is selected by pin-strapping the MODE pin HIGH. The full-duplex mode is meant to be backward compatible with the AD9875/76 in the default state. The Tx data input and Rx output format is *two's complement* by default but can be changed to *straight binary* via a SPORT register. The RXCLK provides a clock that is twice the ADC sample rate (i.e. 2 x f_{ADC})

The transmit Digital Interface Port has several modes of operation. In its default configuration, the Tx Port accepts six bit nibbles through the TX[5:0] and TXSYNC pins and demultiplexes the data into 12 (or 10) bit words before passing it to the interpolation filter. Also, 6-bits of Rx PGA gain control data can be placed on the Tx Port and directed towards the RX PGA register using the GAIN pin to mux the data. Additional programming options for the Tx Port allow; sampling the input data on the falling edge of RXCLK inversion or disabling of RXCLK, and reversing the order of the nibbles. All of these modes are fully described in the "REGISTER PROGRAMMING DEFINITIONS" section of this datasheet.

Transmit Port Timing

The AD9865 transmit port consists of a 6 bit data bus TX[5:0], a clock and a TX SYNC signal. Two consecutive nibbles of the TX data are multiplexed together to form a 10/12 bit data word. The clock appearing on the RXCLK pin is a buffered version of the internal TX data sampling clock. Data from the TX port is read on the rising edge of this sampling clock. The TX SYNC signal is used to indicate to which word a nibble belongs. The first nibble of every word is read while TX SYNC is low, the second nibble of that same word is read on the following TX SYNC high level. When the TX SYNC is low, the sampled nibble is read as the most significant nibble. When the TX SYNC is high, the sampled nibble is read as the least significant nibble. The timing is illustrated in figure x.x. below.

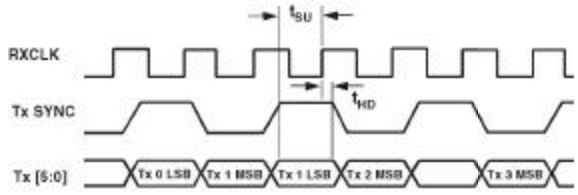

Figure x.x Tx Port Timing

The TX port is highly configurable and offers the following options:

Negative edge sampling can be chosen by two different methods; either by setting the *Tx Port Negative Edge Sampling* bit (register ?, bit ?) or the *Invert RXCLK* bit (register ?, bit ?). The main difference between the two methods is that setting register ?, bit ? inverts the internal sampling clock and will effect only the transmit path, even if RXCLK is used to clock the Rx data. Inverting RXCLK would effect both the Rx and Tx paths since they both use RXCLK.

The first nibble of each word can be read in as the least significant nibble by setting the *Tx LS nibble First* bit (register ?, bit ?).

For the AD9865, the most significant nibble defaults to 6 bits and the least significant nibble defaults to 4 bits. This can be changed so that the least significant nibble and most significant nibble have 5 bits each. This is done by setting the *Tx Port Width 5-bits* bit (register ?, bit ?). In all cases, the nibbles are justified toward bit 5.

If TX SYNC is low for more than one clock cycle, the last transmit data will read continuously until TX SYNC is brought high for the second nibble of a new transmit word. This feature can be used to "flush" the interpolator filters with zeros.

Receive Port Timing

The AD9865 receives port consists of a 6 bit data bus RX[5:0], a clock and an RX SYNC signal. Two consecutive nibbles of the RX data are multiplexed together to form a10/12 bit data word. The RX data is valid on the rising edge of CLK-A when the *ADC Clock Source PLL-B/2* bit (register 3, bit 6) is set to 0. The RX SYNC signal is used to indicate to which word a nibble belongs. The first nibble of every word is transmitted while RX SYNC is low, the second nibble of that same word is transmitted on the following RX SYNC high level. When RX SYNC is low, the sampled nibble is read as the most significant nibble. When the RX SYNC is high, the sampled nibble is read as the least significant nibble. The timing is illustrated in the diagram below.

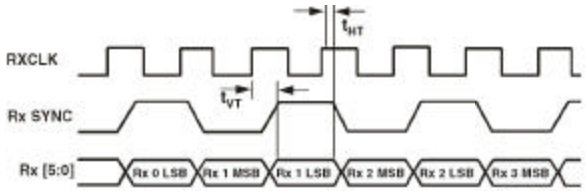

Figure x.x Full- Duplex Rx Port Timing

The RX port is highly configurable and offers the following options:

Negative edge sampling can be chosen by setting the *Invert RXCLK* bit (register 8, bit 6). Inverting RXCLK would effect both the Rx and Tx paths since they both use RXCLK

The first nibble of each word can be read in as the least significant nibble by setting the *Rx LS nibble First* bit (register 8, bit 2). For the AD9865, the most significant nibble defaults to 6 bits and the least significant nibble defaults to 4 bits. This can be changed so that the least significant nibble and most significant nibble have 5 bits each. This is done by setting the *Rx Port Width 5-bits* bit (register 8, bit 1). In all cases, the nibbles are justified toward bit 5. The RX[5:0] pins can be put into a high impedance state by setting the *Tristate Rx Port* bit (register 8, bit 3).

PGA Gain Setting

In addition to the serial port, the Rx PGA gain setting can be set via the Tx[5:0] or PGA[5:0] data port. These two methods provide fast updates to the Rx PGA gain register. The *default setting* is for the Rx PGA to be set via the Tx data port (i.e. AD9875/76 backward compatible) .

In this case, a high level on the GAIN pin with Tx SYNC low programs the PGA setting on either the rising edge (or falling edge) of RXCLK as shown in figure xx. The GAIN pin must be held high, Tx SYNC must be held low, and GAIN data must be stable for three clock cycles to successfully update the PGA gain setting. A low level on the GAIN pin enables data to be fed to the interpolator and DAC. This interface should be considered when upgrading existing designs from the AD9875/76 or half-duplex applications trying to minimize on a ASIC's pin-count.

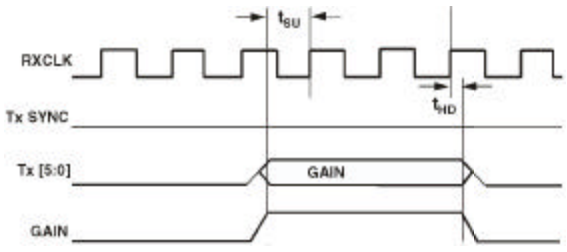

Figure x.x. PGA timing for AD9875/76 backward compatible mode

The PGA[5:0] port is recommended for full-duplex applications. This method is enabled by setting a SPORT register. A high level on the PGA_EN pin enables data appearing at PGA[5:0] to automatically updates the Rx PGA gain setting after a slight propagation delay (due to LUT). Figure x.x. shows the timing for this method.

Figure xx. PGA timing for Full-duplex operation

SYSTEM VERIFICATION/DEBUG FEATURES

The AD9865/66 will have several features that will assist in system verification and debut. For a full-duplex digital interface, the following features can be enabled via a SPORT register:

-Digital Loopback

- Ability to float the RX[5:0] and RXSYNC pins

POWER SAVINGS FEATURE

Half-Duplex Mode Interface

Power sensitive applications that use the half-duplex mode interface will have the ability to turnoff the Rx or Tx signal path when not in use. During a Tx burst, the RxPGA and ADC can be turned-off while in a Rx burst, the TxDAC and IAMP can be turned-off. Peak current consumption for the IC will be less than 160 mA in either state. **Note, the default state for the half duplex interface mode (i.e. MODE=0) has this feature enabled! To disable this feature, a SPORT register must be set.**

The TXEN and RXEN signal will be used to generate an internal delayed power-down signal for the Tx and Rx circuitry. For a Tx burst, the *falling edge* of TXEN will be used to trigger a power down signal whose delay is dependent on the interpolation filter factor. This delay is meant to match the pipeline delay of the last Tx burst sample such that power-down of the TxDAC and IAMP does not impact its transmission. Upon receipt of this signal, power-down should occur with 1usec. The *rising edge* of TXEN will be used to power-up the TxDAC and IAMP with no intentional delay inserted. These blocks will be powered up within 0.5 usec upon receipt of this signal. For a Rx burst, the *falling edge* of RXEN will be used to power-down the Rx PGA and ADC within 2usec and the *rising edge* of RXEN will be used power-up these blocks with 2 usec. **ANY PROBLEMS ???**

The PWR DWN pin for the half-duplex mode interface mode is active HIGH and places the AD9865/66 in stand-by.

In stand-by, all functional blocks that have power on and off times of less than 1 msec are power-down.

Full-Duplex Mode Interface

The combination of the PWR DWN pin and SPORT registers x and y allow for the configuration of two separate pin selectable power settings. This power down mode is intended to be backward compatible with the AD9875/76. In this mode, the PWR DWN pin selects between two sets of indiviually programmed operation modes. When the PWR DWN is low, the functional blocks corresponding to the bits in register x will be powered down. When the PWR DWN is high, the functional blocks corresponding to the bits in register y will be powered down. The default setting for the full-duplex mode interface (MODE=1) is as follows:.

Bit	Fuctional Block	Register x	Register y
0	Rx PGA	0	1
1	Rx ADC	0	1
2	Rx Ref	0	1
3	TxDAC	0	1
4	Tx Interp.	0	1
5	Tx Ref	0	1
6	CLK Syn	0	1
7	Not Used	x	x

1 is ON, 0 is OFF

Note, these default settings DO NOT support power savings for half-duplex applications using this interface. Users would have to reprogram these registers via the SPORT to turn off the Rx_PGA+ADC or TxDAC/IAMP. Also, the PWR DWN signal immediately affects the designated functional blocks without any "added" delays to compensate for the digital filter delay.

MODE SELECT UPON POWER-UP

The AD9865/66' power-up state will be determined by the logic level appearing at the MODE pin. A HIGH level will enable a full-duplex duplex mode that is backward compatible with the AD9875/76. A LOW level enables a half-duplex mode that is backward compatible with the AD9975.

Besides the digital interface mode, other device set-up parameters will also be set to a default state as outlined in the table below. The intent of these particular default settings is allow some applications to avoid using the SPORT interface (disabled by tying SENABLE LOW). Other applications will be required to use the SPORT to configure the device.

Functional Block	MODE=0	MODE=1
Digital Interface	Half Duplex	Full-Duplex
Rx_PGA Interface	3-bit using PGA[5:3]	6-bit using TX{5:0]
Tx_PGA	OFF	OFF
Rx_LPF1	23 MHz	23 MHz
Tx PGA	0 dBFS	0 dBFS
Tx Interpolation	4x	4x
IAMP Gain	36	36
CLKOUT1_N	2	?
CLKOUT2_L	2	?
PLL Multiplier	4x	4x
Tx/Rx Power Savings	YES	NO

1 f_{OSC_IN}=50 MHz

SERIAL INTERFACE FOR REGISTER CONTROL

The serial port is a three wire serial communications port consisting of a clock (SCLK), chip select (SENABLE), and a bidirectional data (SDATA) signal. The interface allows read/write access to all registers that configure the AD9865/6 internal parameters. Single or multiple byte transfers are supported as well as MSB first or LSB first transfer formats.

General Operation of the Serial Interface

Serial communication over the serial interface can be from 1 to 5 bytes in length. The first byte is always the instruction byte. The instruction byte establishes whether the communcation is going to be a read or write access, the number of data bytes to be transferred and the address of the first register to be accessed. The instruction byte transfer is complete immediately upon the eighth rising edge of SCLK after SENABLE is asserted. Likewise, the data registers change *immediately* upon writing to the eighth bit of each data byte.

Instruction Byte

The instruction byte contains the following information as shown below:

MSB LSB

I7	I6	I5	I4	I3	I2	I1	I0
R/W	N1	N0	A4	A3	A2	A1	A0

Bit I7 - R/W

This bit determines whether a read or a write data transfer will occur after the instruction byte write. Logic high

indicates read operation; logic zero indicates a write operation.

Bits I6:I5 - N1:N0
These two bits determine the number of bytes to be transferred during the data transfer cycle. The bit decodes are shown in the table below:

N1:N0	Description
0:0	Transfer **1** byte.
0:1	Transfer **2** bytes.
1:0	Transfer **3** bytes.
1:1	Transfer **4** bytes.

Bits I4:I0 - A4:A0
These bits determine which register is accessed during the data transfer portion of the communications cycle. For multibyte transfers, this address is the starting byte address. The remaining register addresses are generated by the AD9865/6.

Serial Interface Port Pin Description

SCLK—Serial Clock

The serial clock pin is used to synchronize data transfers to and from the AD9865 and to run the internal state machines. SCLK maximum frequency is 25 MHz. All data transmitted to the AD9865 is sampled on the rising edge of SCLK. All data read from the AD9865 is validated on the rising edge of SCLK and is updated on the falling edge.

SENABLE—Serial Interface Enable

The SENABLE pin is active low. It enables the serial communication to the device. SENABLE select should stay low during the entire communication cycle. All input on the serial port is ignored when SENABLE is inactive.

SDATA—Serial Data I/O

The signal on this line is sampled on the first eight rising edges of SCLK after SENABLE goes active. Data is then read from or written to the AD9865 depending on what was read.

The following diagrams show the timing relationships between the three SPI signals.

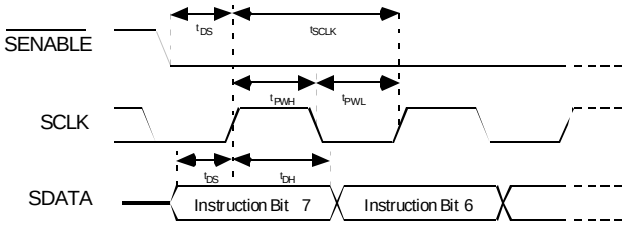

Figure x. Timing Diagram Register Write to AD9865/6

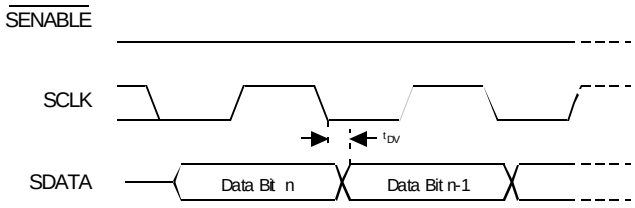

Figure x. Timing Diagram Register Read from AD9865/6

MSB/LSB Transfers

The AD9865 serial port can support both most significant bit (MSB) first or least significant bit (LSB) first data formats. The bit order is controlled by the *SPI LSB First* bit (Register 0, bit 6). The default is value is 0, MSB first. Multibyte data transfers in MSB format can be completed by writing an instruction byte that includes the register address of the last address to be accessed. The AD9865 will automatically decrement the address for each successive byte required for the multibyte communication cycle.

When the *SPI LSB First* bit (Register 0, bit 6) is set high, the serial port interprets both instruction and data bytes LSB first. Multibyte data transfers in LSB format can be completed by writing an instruction byte that includes the register address of the first address to be accessed. The AD9865 will automatically increment the address for each successive byte required for the multibyte communication cycle.

The diagrams that follow show how the serial port words are built for each of these modes.

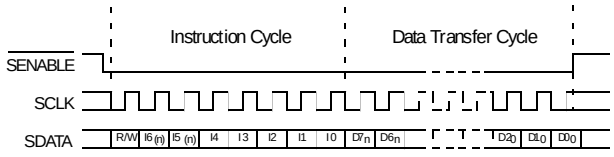

Figure x. Serial Register Interface Timing MSB-First

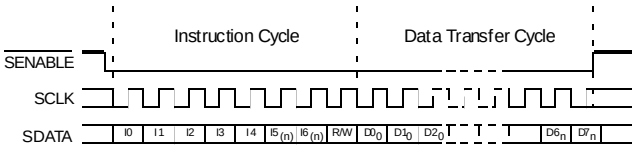

Figure x. Serial Register Interface Timing LSB-First

Notes on Serial Port Operation

The serial port is disabled and all registers are set to their default values during a hardware reset. During a software reset, all registers except register 0 are set to their default values. Register 0 will remain at the last value sent, with the exception that the *Software Reset* bit will be set to 0.

The serial port is operated by an internal state machine and is dependent on the number of SCLK cycles since the last time SENABLE went active. On every eighth rising edge of SCLK, a byte is transferred over the SPI. During a multibyte write cycle, this means the registers of the AD9865 are not simultaneously updated, but occur sequentially. For this reason, it is recommended that single byte transfers are used when changing the SPI configuration or performing a software reset.