



MAT-02/883

LOW-NOISE, MATCHED
DUAL MONOLITHIC TRANSISTOR

Precision Monolithics Inc.

1.0 SCOPE

This specification covers the detail requirements for a dual matched transistor.

It is highly recommended that this data sheet be used as a baseline for new military or aerospace spec control drawings.

1.2 Part Number. The complete part numbers per Table I of this specification follow:

<u>Device</u>	<u>Part Number</u>	<u>Package</u>
A	MAT-02AH/883	H
B	MAT-02BH/883	H
B	MAT-02BRC/883	RC

1.2.3 Case Outline.

<u>Letter</u>	<u>Case Outline (Lead finish per MIL-M-38510)</u>
H	6-lead metal can (TO-78)
RC	20-contact hermetic leadless chip carrier (LCC)

1.3 Absolute Maximum Ratings. ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Collector-Base Voltage (BV_{CBO})	40V
Collector-Emitter Voltage (BV_{CEO})	40V
Collector-Collector Voltage (BV_{CC})	40V
Emitter-Emitter Voltage (BV_{EE})	40V
Collector Current (I_C)	20mA
Emitter Current (I_E)	20mA
Total Power Dissipation	
Case Temperature $\leq 40^\circ\text{C}$ (Note 1)	1.8W
Ambient Temperature $\leq 70^\circ\text{C}$ (Note 2)	500mW
Operating Ambient Temperature Range	-55°C to $+125^\circ\text{C}$
Operating Junction Temperature Range	-55°C to $+125^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 60 sec)	$+300^\circ\text{C}$
DICE Junction Temperature Range (T_J)	-65°C to $+150^\circ\text{C}$

NOTES:

- Rating applies to applications using heat sinking to control case temperature. Derate linearly at $16.4\text{mW}/^\circ\text{C}$ for case temperatures above 40°C .
- Rating applies to applications not using heat sinking; device in free air only. Derate linearly at $6.3\text{mW}/^\circ\text{C}$ for ambient temperatures above 70°C .

January 1988

MAT-02/883 LOW-NOISE, MATCHED
DUAL MONOLITHIC TRANSISTOR



1.5 Thermal Characteristics:

Thermal Resistance, TO-78 (H) package:

Junction-to-Case (θ_{JC}) = 45°C/W MAX

Junction-to-Ambient (θ_{JA}) = 150°C/W MAX

Thermal Resistance, LCC (RC) package:

Junction-to-Case (θ_{JC}) = 35°C/W MAX

Junction-to-Ambient (θ_{JA}) = 110°C/W MAX

MAT-02/883 LOW-NOISE, MATCHED
DUAL MONOLITHIC TRANSISTORSpec. #D0171-01E
Rev. B

PMI

TABLE 1 $V_{CB} = 15V; I_C = 10\mu A; T_A = 25^\circ C$ unless otherwise specified.

Characteristics	Symbol	Special Conditions	MAT-02/883				Units
			LIMITS A		LIMITS B		
			Min	Max	Min	Max	
		$I_C = 1mA; V_{CB} = 0V, 40V$	500	—	400	—	
		$I_C = 100\mu A; V_{CB} = 0V, 40V$	500	—	400	—	
		$I_C = 10\mu A; V_{CB} = 0V, 40V$	400	—	300	—	
		$I_C = 1\mu A; V_{CB} = 0V, 40V$	300	—	200	—	
Current Gain	h_{FE}	$I_C = 1mA; V_{CB} = 0V, 40V$ $-55^\circ C \leq T_A \leq +125^\circ C$	275	—	250	—	
		$I_C = 100\mu A, V_{CB} = 15V$ $-55^\circ C \leq T_A \leq +125^\circ C$	225	—	200	—	
		$I_C = 10\mu A, V_{CB} = 15V$ $-55^\circ C \leq T_A \leq +125^\circ C$	175	—	150	—	
		$I_C = 1\mu A, V_{CB} = 15V$ $-55^\circ C \leq T_A \leq +125^\circ C$	150	—	100	—	
Current Gain Match (Note 1)	Δh_{FE}	$I_C = 10\mu A, 100\mu A, 1mA$ $V_{CB} = 0V$	—	2	—	4	%
Offset Voltage	V_{OS}	$V_{CB} = 0V$	—	50	—	150	μV
		$V_{CB} = 0V$ $-55^\circ C \leq T_A \leq +125^\circ C$	—	80	—	250	μV
Offset Voltage Change vs. V_{CB} (Note 2)	$\frac{\Delta V_{OS}}{\Delta V_{CB}}$	$V_{CB} = 0V, 40V$	—	25	—	50	μV
Offset Voltage Change vs. Collector Current (Note 3)	$\frac{\Delta V_{OS}}{\Delta I_C}$	$V_{CB} = 0V$ $I_C = 10\mu A, 1mA$	—	25	—	50	μV
Input Offset Current	I_{OS}	$V_{CB} = 0V, 40V$	—	0.6	—	1.3	nA
		$V_{CB} = 0V, 40V$ $-55^\circ C \leq T_A \leq +125^\circ C$	—	9.0	—	15.0	nA
Offset Current Change vs. V_{CB}	$\frac{\Delta I_{OS}}{\Delta V_{CB}}$	$V_{CB} = 0V, 40V$	—	70	—	70	pA/V

MAT-02/883 LOW-NOISE, MATCHED
DUAL MONOLITHIC TRANSISTORSpec. #D0171-01E
Rev. B

PMI

TABLE 1 (Continued) $V_{CB} = 15V; I_C = 10\mu A; T_A = 25^\circ C$ unless otherwise specified.

Characteristics	Symbol	Special Conditions	MAT-02/883				Units
			LIMITS A		LIMITS B		
			Min	Max	Min	Max	
Bulk Emitter Resistance	r_{BE}		—	0.5	—	0.5	Ω
Collector Base Leakage Current	I_{CBO}	$V_{CB} = 40V$	—	200	—	400	pA
Collector-Emitter Leakage Current (Note 4)	I_{CES}	$V_{CE} = 40V, V_{BE} = 0V$	—	200	—	400	pA
Collector-Collector Leakage Current (Note 4)	I_{CC}	$V_{CC} = 40V$	—	200	—	400	pA
Bias Current	I_B	$V_{CB} = 0V, 40V$	—	25	—	34	nA
		$V_{CB} = 0V, 40V$ $-55^\circ C \leq T_A \leq +125^\circ C$	—	60	—	70	nA
Collector Saturation Voltage	$V_{CE SAT}$	$I_C = 1mA, I_B = 100\mu A$	—	0.1	—	0.2	V
Breakdown Voltage	BV_{CEO}	$I_C = 100\mu A$	40	—	40	—	V
Change in Offset Voltage vs. Temperature (Note 5)	TCV_{OS}	$V_{CB} = 0V$	—	0.3	—	1.0	$\mu V/^\circ C$

9
MATCHED TRANSISTORS

MAT-02/883 LOW-NOISE, MATCHED
DUAL MONOLITHIC TRANSISTOR

Spec. #D0171-01E
Rev. B



TABLE 1 (Continued)

$V_{CB} = 15V; I_C = 10\mu A; T_A = 25^\circ C$ unless otherwise specified.

Characteristics	Symbol	Special Conditions	MAT-02/883				Units
			LIMITS A		LIMITS B		
			Min	Max	Min	Max	
Noise Voltage Density	e_n	$I_C = 1mA, V_{CB} = 0V$					
		$f_O = 10Hz$	-	2	-	-	3 nV/ \sqrt{Hz}
		$f_O = 100Hz$	-	1	-	-	2 nV/ \sqrt{Hz}
		$f_O = 1kHz$	-	1	-	-	2 nV/ \sqrt{Hz}
		$f_O = 10kHz$	-	1	-	-	1 nV/ \sqrt{Hz}

NOTES:

- Current gain match (Δh_{FE}) is defined as: $\Delta h_{FE} = \frac{100(\Delta I_B)h_{FEmin}}{I_C}$
- Measured at $I_C = 10\mu A$ and guaranteed by design over $10mA \leq I_C \leq 1mA$.
- This is the maximum change in V_{OS} measured at $I_C = 10\mu A$ with $V_{CB} = 0V$.
- I_{CC} and I_{CES} are verified by measurement of I_{CBO} .
- Guaranteed by V_{OS} test ($TCV_{OS} \approx \frac{V_{OS}}{T}$ for $V_{OS} \ll V_{BE}$) $T = 298^\circ K$ for $T_A = +25^\circ C$.

MAT-02/883 LOW-NOISE, MATCHED
DUAL MONOLITHIC TRANSISTOR

Spec. #D0171-01E
Rev. B



TABLE 2

MAT-02/883

**Electrical Test Requirements
For Class B Devices**

MIL-STD-883 Test Requirements	Subgroups (see Table 3)
Interim Electrical Parameters (pre Burn-In)	1
Final Electrical Test Parameters	1*, 2, 3
Group A Test Requirements	1, 2, 3, 7

* PDA applies to Subgroup 1 only.
No other Subgroups are included in PDA.

9

MATCHED TRANSISTORS

MAT-02/883 LOW-NOISE, MATCHED
DUAL MONOLITHIC TRANSISTORSpec. #D0171-01E
Rev. B

PMI

TABLE 3**Group A Inspection** $V_{CB} = 15V; I_C = 10\mu A$ unless otherwise specified.

Subgroup	Symbol	Special Conditions	MAT-02/883				Units
			LIMITS A		LIMITS B		
			Min	Max	Min	Max	
Subgroup 1 $T_A = +25^\circ C$	h_{FE}	$I_C = 1mA; V_{CB} = 0V, 40V$	500	—	400	—	
		$I_C = 100\mu A; V_{CB} = 0V, 40V$	500	—	400	—	
		$I_C = 10\mu A; V_{CB} = 0V, 40V$	400	—	300	—	
		$I_C = 1\mu A; V_{CB} = 0V, 40V$	300	—	200	—	
	Δh_{FE}	$I_C = 10\mu A, 100\mu A, 1mA$ $V_{CB} = 0V$ (Note 1)	—	2	—	4	%
	V_{OS}	$V_{CB} = 0V, I_C = 10\mu A$	—	50	—	150	μV
	$\frac{\Delta V_{OS}}{\Delta V_{CB}}$	$V_{CB} = 0V, 40V$ $I_C = 10\mu A$	—	25	—	50	μV
	$\frac{\Delta V_{OS}}{\Delta I_C}$	$V_{CB} = 0V$ $I_C = 10\mu A, 1mA$	—	25	—	50	μV
	I_{OS}	$V_{CB} = 0V, 40V$	—	0.6	—	1.3	nA
	$\frac{\Delta I_{OS}}{\Delta V_{CB}}$	$V_{CB} = 0V, 40V$	—	70	—	70	pA/V
	r_{BE}		—	0.5	—	0.5	Ω
	I_{CBO}	$V_{CB} = 40V$	—	200	—	400	pA
	I_{CES}	$V_{CE} = 40V, V_{BE} = 0V$ (Note 2)	—	200	—	400	pA
	I_{CC}	$V_{CC} = 40V$ (Note 2)	—	200	—	400	pA
	I_B	$V_{CB} = 0V, 40V$	—	25	—	34	nA
	V_{CE}^{SAT}	$I_C = 1mA, I_B = 100\mu A$	—	0.1	—	0.2	V
	BV_{CEO}	$I_C = 100\mu A$	40	—	40	—	V

MAT-02/883 LOW-NOISE, MATCHED
DUAL MONOLITHIC TRANSISTOR

Spec. #D0171-01E
Rev. B



TABLE 3

Group A Inspection (Continued)

$V_{CB} = 15V$; $I_C = 10\mu A$ unless otherwise specified.

Subgroup	Symbol	Special Conditions	MAT-02/883				Units
			LIMITS A		LIMITS B		
			Min	Max	Min	Max	
Subgroup 2 $T_A = +125^\circ C$		$I_C = 1mA$; $V_{CB} = 0V, 40V$	275	--	250	--	
		$I_C = 100\mu A$, $V_{CB} = 15V$	225	--	200	--	
	h_{FE}	$I_C = 10\mu A$, $V_{CB} = 15V$	175	--	150	--	
		$I_C = 1\mu A$, $V_{CB} = 15V$	150	--	100	--	
	V_{OS}	$V_{CB} = 0V$	--	80	--	250	μV
I_{OS}	$V_{CB} = 0V, 40V$	--	9	--	15	nA	
	I_B	$V_{CB} = 0V, 40V$	--	60	--	70	nA
Subgroup 3 $T_A = -55^\circ C$	All Tests, Limits and Conditions are the same as for Subgroup 2.						
Subgroup 7 $T_A = +25^\circ C$		$I_C = 1mA$, $V_{CB} = 0V$					
	e_n	$f_O = 10Hz$	--	2	--	3	nV/\sqrt{Hz}
		$f_O = 100Hz$	--	1	--	2	nV/\sqrt{Hz}
		$f_O = 1kHz$	--	1	--	2	nV/\sqrt{Hz}
		$f_O = 10kHz$	--	1	--	2	nV/\sqrt{Hz}

NOTES:

- Current gain match (Δh_{FE}) is defined as: $\Delta h_{FE} = \frac{100(\Delta I_B)h_{FEmin}}{I_C}$
- I_{CC} and I_{CES} are verified by measurement of I_{CBO} .

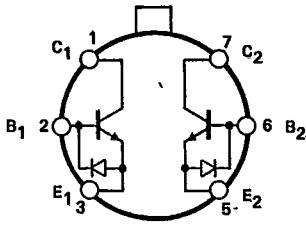
9
MATCHED TRANSISTORS

MAT-02/883 LOW-NOISE, MATCHED DUAL MONOLITHIC TRANSISTOR

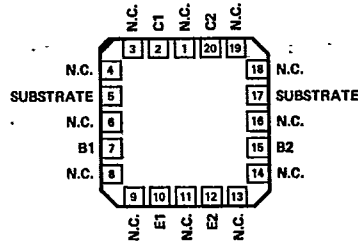
Spec. #D0171-01E
Rev. B



3.2.1 Pin Connections.



**TO-78
(H-Suffix)**



**MAT-02BRC/883
20-LEAD LCC
(RC-Suffix)**

NOTE: Substrate is connected to case on TO-78 package. Substrate is normally connected to the most negative circuit potential, but can be floated.

3.2.4 Microcircuit Group Assignment. This microcircuit is covered by microcircuit group 49.

4.2 Life Test/Burn-In Circuit.

