T-43-25

PMI

Audio Silicon Specialists™

SSM-2210

AUDIO DUAL MATCHED NPN TRANSISTOR

Precision Monolithics Inc.

FEATURES

- Very Low Voltage Noise .... @ 100Hz, 1nV/√Hz MAX
- Excellent Current Gain Match .... 0.5% TYP
- Tight V_{BE} Match (V_{OS}).. 200µV MAX
- Outstanding Offset Voltage Drift .... 0.03µV/°C TYP
- High Gain-Bandwidth Product .... 200MHz TYP
- Low Cost
- Direct Replacement For LM394BN/CN

ORDERING INFORMATION

PACKAGE PLASTIC 8-PIN	PACKAGE SO 8-PIN	OPERATING TEMPERATURE RANGE
SSM2210P	SSM2210S†	XIND*

* XIND = –40°C to +85°C
† For availability on SO package, contact your local sales office.

GENERAL DESCRIPTION

The SSM-2210 is a dual NPN matched transistor pair specificially designed to meet the requirements of ultra-low noise audio systems.

With its extremely low input base spreading resistance (rbb' is typically 28Ω), and high current gain (h_{FE} typically exceeds 600 @ I_C = 1mA), systems implementing the SSM-2210 can achieve outstanding signal-to-noise ratios. This will result in superior performance compared to systems incorporating commercially available monolithic amplifiers.

The equivalent input voltage noise of the SSM-2210 is typically only 0.8nV/√Hz over the entire audio bandwidth of 20Hz to 20KHz.

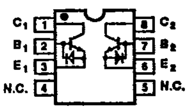
Excellent matching of the current gain (Δh_{FE}) to about 0.5% and low V_{OS} of less than 50µV (typical) make it ideal for symmetrically balanced designs which reduce high order amplifier harmonic distortion.

Stability of the matching parameters is guaranteed by protection diodes across the base-emitter junction. These diodes prevent degradation of Beta and matching characteristics due to reverse biasing of the base-emitter junction.

The SSM-2210 is also an ideal choice for accurate and reliable current biasing and mirroring circuits. Furthermore, since a current mirror's accuracy degrades exponentially with mismatches of V_{BE}'s between transistor pairs, the low V_{OS} of the SSM-2210 will preclude offset trimming in most circuit applications.

The SSM-2210 is offered in an 8-pin epoxy DIP and 8-pin SO, its performance and characteristics are guaranteed over the extended industrial temperature range of –40°C to +85°C.

PIN CONNECTIONS



8-PIN PLASTIC DIP (P-Suffix)

8-PIN SO (S-Suffix)

ABSOLUTE MAXIMUM RATINGS

Collector Current (I_C) 20mA
Emitter Current (I_E) 20mA
Collector-Collector Voltage (BV_{CC}) 40V
Collector-Base Voltage (BV_{CBO}) 40V
Collector-Emitter Voltage (BV_{CEO}) 40V
Emitter-Emitter Voltage (BV_{EE}) 40V
Operating Temperature Range....................... –40°C to +85°C
Storage Temperature .... –65°C to +125°C
Junction Temperature .... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) .... +300°C

PACKAGE TYPE	Θ_{jA} (NOTE 1)	Θ_{jC}	UNITS
8-Pin Plastic DIP (P)	110	50	°C/W
8-Pin SO (S)	160	44	°C/W

NOTE:
1. Θ_{jA} is specified for worst case mounting conditions, i.e., Θ_{jA} is specified for device in socket for P-DIP packages; Θ_{jA} is specified for device soldered to printed circuit board for SO packages.

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ELECTRICAL CHARACTERISTICS at V_{CB} = 15V, I_C = 10µA, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SSM-2210 MIN	TYP	MAX	UNITS
Current Gain	h_{FE}	I_C = 1mA (Note 1)	300	605	–	
		I_C = 10µA	200	550	–	
Current Gain Match	Δh_{FE}	10µA ≤ I_C ≤ 1mA (Note 2)	–	0.5	5	%
Noise Voltage Density	e_n	I_C = 1mA, V_{CB} = 0 (Note 3)				
		f_o = 10Hz	–	1.6	2	nV/√Hz
		f_o = 100Hz	–	0.9	1	
		f_o = 1kHz	–	0.85	1	
		f_o = 10kHz	–	0.85	1	
Offset Voltage	V_{OS}	V_{CB} = 0, I_C = 1mA	–	10	200	µV
Offset Voltage Change vs V_{CB}	$\Delta V_{OS}/\Delta V_{CB}$	0 ≤ V_{CB} ≤ V_{MAX} (Note 4), 1µA ≤ I_C ≤ 1mA (Note 5)	–	10	50	µV
Offset Voltage Change vs Collector Current	$\Delta V_{OS}/\Delta I_C$	V_{CB} = 0V, 1µA ≤ I_C ≤ 1mA (Note 5)	–	5	70	µV
Breakdown Voltage	BV_{CEO}		40	–	–	V
Gain-Bandwidth Product	f_T	I_C = 10mA, V_{CE} = 10V	–	200	–	MHz
Collector-Base Leakage Current	I_{CBO}	V_{CB} = V_{MAX}	–	25	500	pA
Collector-Collector Leakage Current	I_{CC}	V_{CC} = V_{MAX} (Notes 6, 7)	–	35	500	pA
Collector-Emitter Leakage Current	I_{CES}	V_{CE} = V_{MAX} (Notes 6, 7), V_{BE} = 0	–	35	500	pA
Input Bias Current	I_B	I_C = 10µA	–	–	50	nA
Input Offset Current	I_{OS}	I_C = 10µA	–	–	6.2	nA
Collector Saturation Voltage	$V_{CE(SAT)}$	I_C = 1mA, I_B = 100µA	–	0.05	0.2	V
Output Capacitance	C_{OB}	V_{CB} = 15V, I_E = 0	–	23	–	pF
Bulk Resistance	r_{BE}	10µA ≤ I_C ≤ 10mA (Note 6)	–	0.3	1.6	Ω
Collector-Collector Capacitance	C_{CC}	V_{CC} = 0	–	35	–	pF

NOTES:

1. Current gain is guaranteed with Collector-Base Voltage (V_{CB}) swept from 0 to V_{MAX} at the indicated collector currents.
2. Current Gain Match (Δh_{FE}) is defined as:

$$\Delta h_{FE} = \frac{100(\Delta I_B)(h_{FE}min)}{I_C}$$

3. Noise Voltage Density is guaranteed, but not 100% tested.
4. This is the maximum change in V_{OS} as V_{CB} is swept from 0V to 40V.
5. Measured at I_C = 10µA and guaranteed by design over the specified range of I_C.
6. Guaranteed by design.
7. I_{CC} and I_{CES} are verified by measurement of I_{CBO}.

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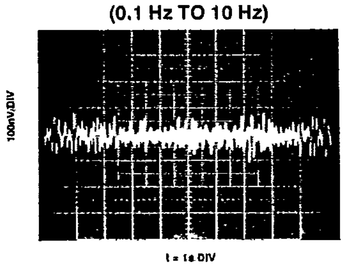
ELECTRICAL CHARACTERISTICS at V_{CB} = 15V, −40°C ≤ T_A ≤ +85°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SSM-2210 MIN	TYP	MAX	UNITS
Current Gain	h_{FE}	I_C = 1mA (Note 1) I_C = 10μA	300 200	– –	– –	
Offset Voltage	V_{OS}	V_{CB} = 0 I_C = 1mA	–	–	220	μV
Average Offset Voltage Drift	TCV_{OS}	10μA ≤ I_C ≤ 1mA, 0 ≤ V_{CB} ≤ V_{MAX} (Note 2) V_{OS} Trimmed to Zero (Note 3)	– –	0.08 0.03	1 0.3	μV/°C
Input Bias Current	I_B	I_C = 10μA	–	–	50	nA
Input Offset Current	I_{OS}	I_C = 10μA	–	–	13	nA
Input Offset Current Drift	TCI_{OS}	I_C = 10μA (Note 4)	–	40	150	pA/°C
Collector-Base Leakage Current	I_{CBO}	V_{CB} = V_{MAX}	–	3	–	nA
Collector-Emitter Leakage Current	I_{CES}	V_{CE} = V_{MAX}, V_{BE} = 0	–	4	–	nA
Collector-Collector Leakage Current	I_{CC}	V_{CC} = V_{MAX}	–	4	–	nA

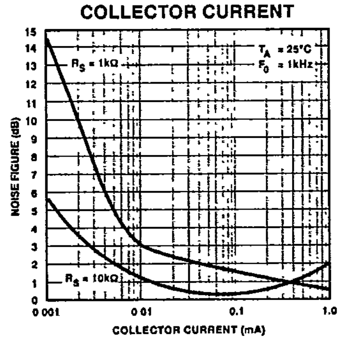
NOTES:
1. Current gain is guaranteed with Collector-Base Voltage (V_{CB}) swept from 0 to V_{MAX} at the indicated collector current.
2. Guaranteed by V_{OS} test ($TCV_{OS} \approx \frac{V_{OS}}{T}$ « V_{BE}), T = 298K for T_A = 25°C.
3. The initial zero offset voltage is established by adjusting the ratio of I_{C1} to I_{C2} at T_A = 25°C. This ratio must be held to 0.003% over the entire temperature range. Measurements are taken at the temperature extremes and 25°C.
4. Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

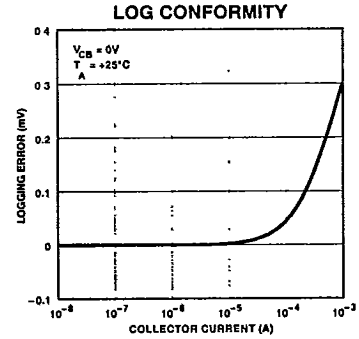
LOW FREQUENCY NOISE (0.1 Hz TO 10 Hz)



NOISE FIGURE vs COLLECTOR CURRENT



EMITTER-BASE LOG CONFORMITY



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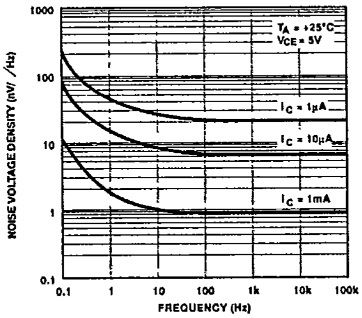
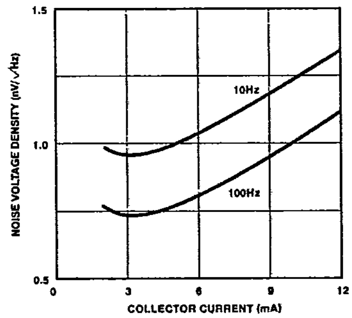
TYPICAL PERFORMANCE CHARACTERISTICS

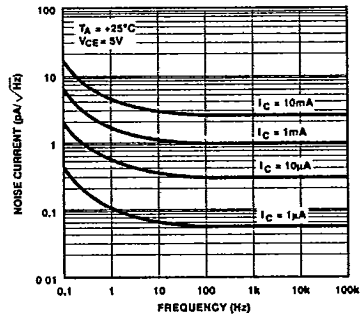
NOISE VOLTAGE DENSITY vs FREQUENCY



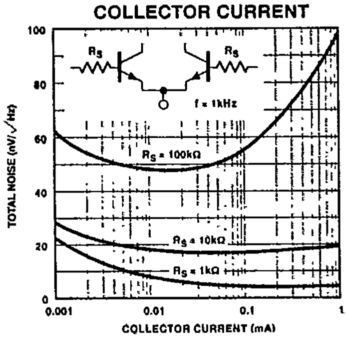
NOISE VOLTAGE DENSITY vs COLLECTOR CURRENT



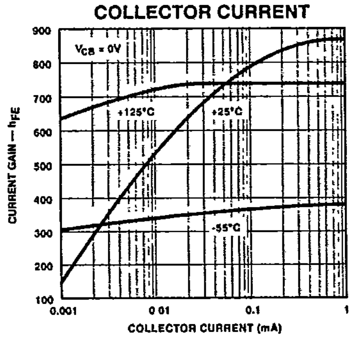
NOISE CURRENT DENSITY vs FREQUENCY



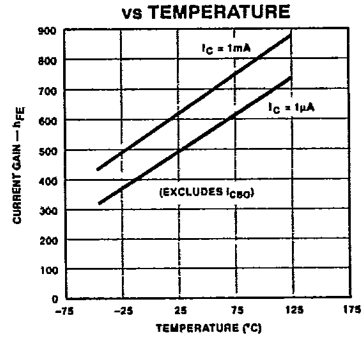
TOTAL NOISE vs COLLECTOR CURRENT



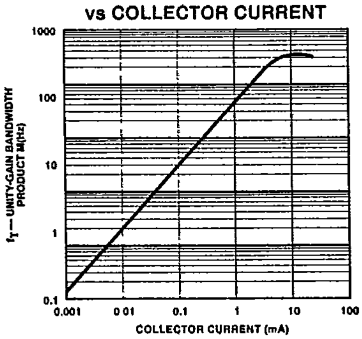
CURRENT GAIN vs COLLECTOR CURRENT



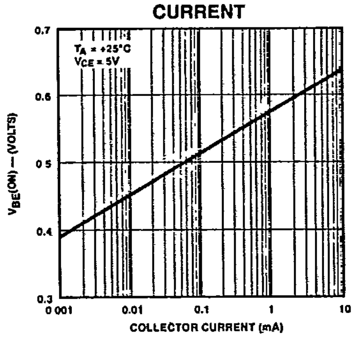
CURRENT GAIN vs TEMPERATURE



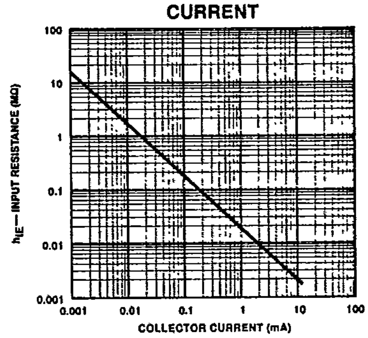
GAIN BANDWIDTH vs COLLECTOR CURRENT



BASE-EMITTER-ON-VOLTAGE vs COLLECTOR CURRENT



SMALL-SIGNAL INPUT RESISTANCE vs COLLECTOR CURRENT



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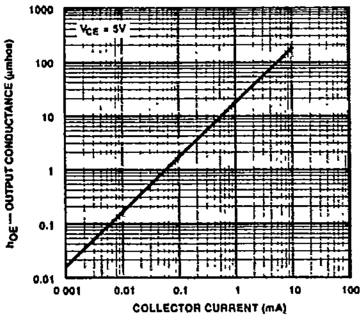
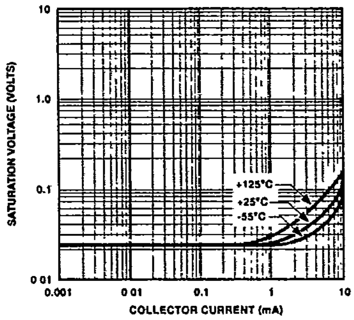
TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

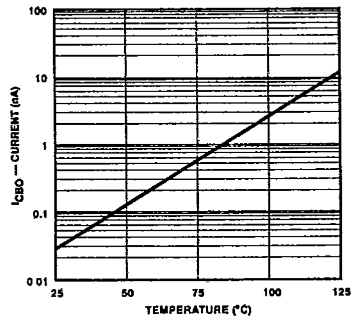
SMALL-SIGNAL OUTPUT CONDUCTANCE vs COLLECTOR CURRENT



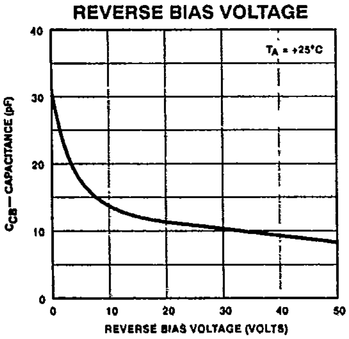
SATURATION VOLTAGE vs COLLECTOR CURRENT



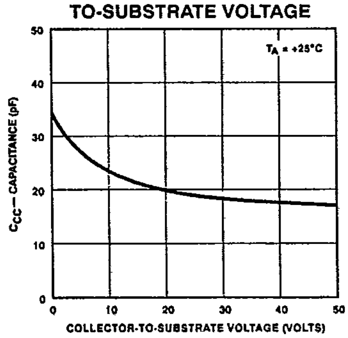
COLLECTOR-TO-BASE LEAKAGE vs TEMPERATURE



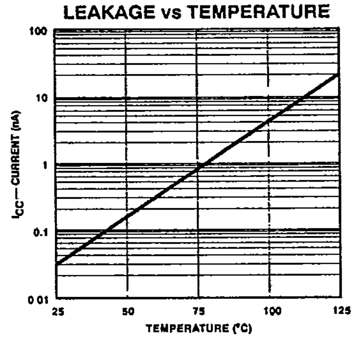
COLLECTOR-BASE CAPACITANCE vs REVERSE BIAS VOLTAGE



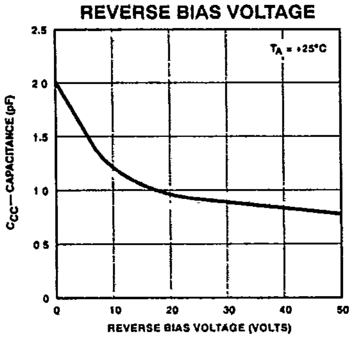
COLLECTOR-TO-COLLECTOR CAPACITANCE vs COLLECTOR-TO-SUBSTRATE VOLTAGE



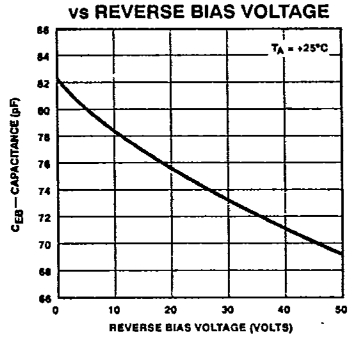
COLLECTOR-TO-COLLECTOR LEAKAGE vs TEMPERATURE



COLLECTOR-TO-COLLECTOR CAPACITANCE vs REVERSE BIAS VOLTAGE



EMITTER-BASE CAPACITANCE vs REVERSE BIAS VOLTAGE



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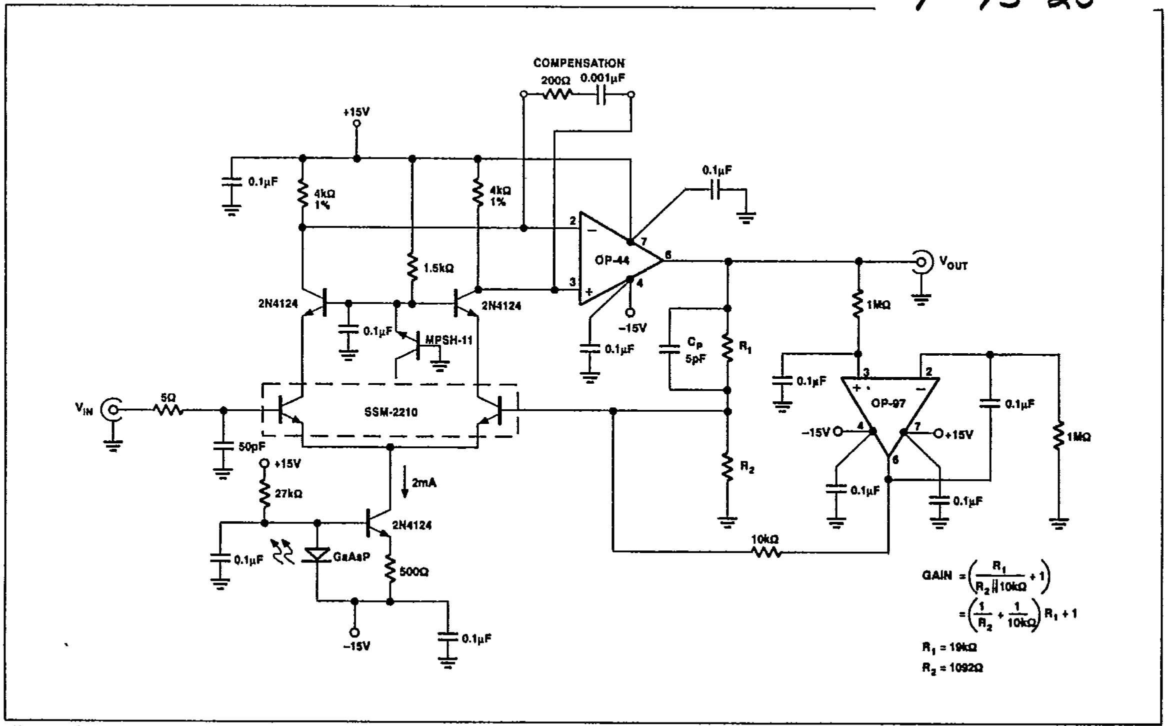

FIGURE 1: *A Low-Noise Wideband Amplifier*

A VERY LOW-NOISE, WIDEBAND AMPLIFIER

Figure 1 illustrates a low-noise, wide-band amplifier consisting of a high slew rate JFET amplifier, the OP-44, and a cascoded differential preamplifier using the SSM-2210 transistor pair. The SSM-2210 achieves extremely low input voltage noise performance ($e_n \approx 0.7nV/\sqrt{Hz}$) via a large geometry transistor design which minimizes the base-spreading resistance. This, however, results in relatively higher collector-to-base capacitance (C_{OB}) than ordinary small-signal transistors. For high gain stages, the Miller effect of C_{OB} will limit the voltage gain bandwidth; resorting to a cascode configuration reduces the Miller feedback capacitance, improving stability, bandwidth, and reducing distortion due to base-width modulation. Additionally, cascoding does not increase the noise figure of the overall amplifier system and reduces the high order harmonic distortion.

The circuit in Figure 1 balances the impedance symmetrically in the differential preamp. This serves to reject common-mode noise injected from the power supplies.

Although the SSM-2210's transistors are closely matched, an offset voltage error can still be created by imbalanced source impedances. Accordingly, a precision low-power amplifier (OP-97), configured as a noninverting integrator is implemented which servos-out the offset voltage to less than 100µV referred to the input of the amplifier.

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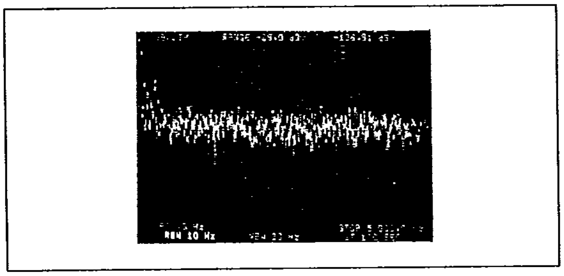

FIGURE 2: *Spectrum Analyzer Display of Wideband Amplifier Noise Spectral Density.* $e_n \approx 1.7nV/\sqrt{Hz}$

Figure 2 illustrates the composite amplifier's low voltage noise density of only 1.7nV/√Hz @ 1kHz. Figure 3 and Figure 4 show the excellent pulse response and an extremely low distortion of only 0.0015% over the audio bandwidth, respectively.

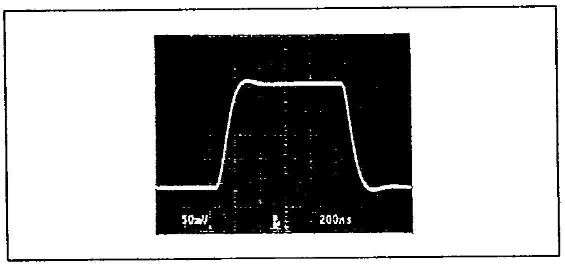

FIGURE 3: *Small-Signal Pulse Response*

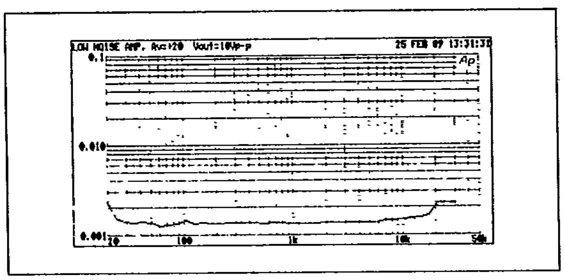

FIGURE 4: *Total Harmonic Distortion vs Frequency*

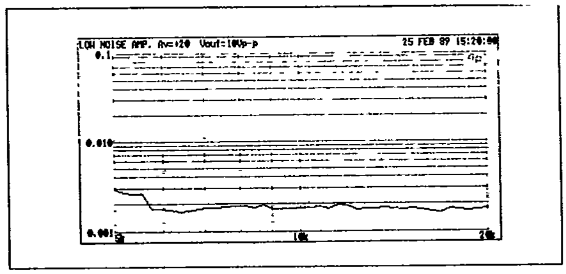

FIGURE 5: *D.I.M. vs Frequency*

A special test was performed to check for dynamic or transient intermodulation distortion. A square wave of 3.15kHz is mixed with a sine wave probe tone, and the resulting intermodulation distortion was found to be less than 0.002% (Figure 5). This is an impressively low value considering the amplifier's gain of 26dB. Interestingly, the GBW product of the composite amplifier was 63MHz which is much larger than that of the OP-44 by itself. This is made possible by the SSM-2210's cascoded preamplifier having a wide bandwidth and large signal gain.

The measured performance of this amplifier is summarized in Table 1.

TABLE 1: Measured Performance of the Low-Noise Wideband Amplifier

Slew-Rate	40V/µs
Gain-Bandwidth	63.6 MHz
Input Noise Voltage Density @ 1kHz	1.7nV/√Hz
Output Voltage Swing	±13V
Input Offset Voltage	10µV

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500pV/√Hz AMPLIFIER

In situations where low output, low-impedance transducers are used, amplifiers must have very low voltage noise to maintain a good signal-to-noise ratio. The design presented in this application is an operational amplifier with only 500pV/√Hz of broadband noise. The front end uses SSM-2210 low-noise dual transistors to achieve this exceptional performance. The op amp has superb DC specifications compatible with high-precision transducer requirements, and AC specifications suitable for professional audio work.

PRINCIPLE OF OPERATION

The design configuration in Figure 6 uses an OP-27 op amp (already a low-noise design) preceded by an amplifier consisting of three parallel-connected SSM-2210 dual transistors. Base spreading resistance (rbb) generates thermal noise which is reduced by a factor of √3 when the input transistors are parallel connected. Schottky noise, the other major noise-generating mechanism, is minimized by using a relatively high collector current (1mA per device). High current ensures a low dynamic emitter resistance, but does increase the base current and its associated current noise. Higher current noise is relatively unimportant when low-impedance transducers are used.

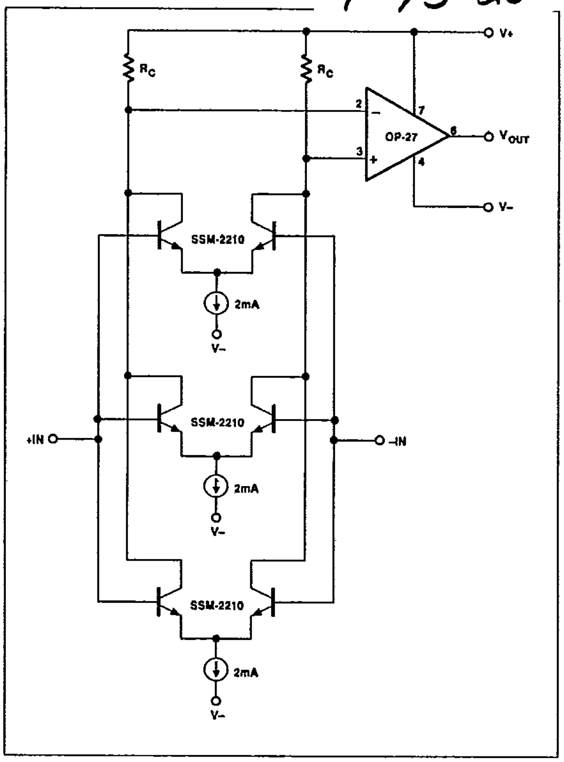

FIGURE 6: *Simplified Schematic*

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CIRCUIT DESCRIPTION

The detailed circuit is shown in Figure 7. A total input-stage emitter current of 6mA is provided by Q_4. The transistor acts as a true current source to provide the highest possible common-mode rejection. R_1, R_2, and R_3 ensure that this current splits equally among the three input pairs. The constant current in Q_4 is set by using the forward voltage of a GaAsP light-emitting diode as a reference. The difference between this voltage and the base-emitter voltage of a silicon transistor is predictable and constant (to within a few percent) over the military temperature range. The voltage difference, approximately 1V, is impressed across the emitter resistor R_{12} which produces a temperature-stable emitter current.

R_6 and C_1 provide phase compensation for the amplifier and are sufficient to ensure stability at gains of ten and above.

R_7 is an input offset trim that provides approximately ±300μV trim range. The very low drift characteristics of the SSM-2210 make it possible to obtain drifts of less than 0.1μV/°C when the offset is nulled close to zero. If this trim is not required, the R_4, R_7, and R_8 network should be omitted and R_5/R_9 connected directly to V+.

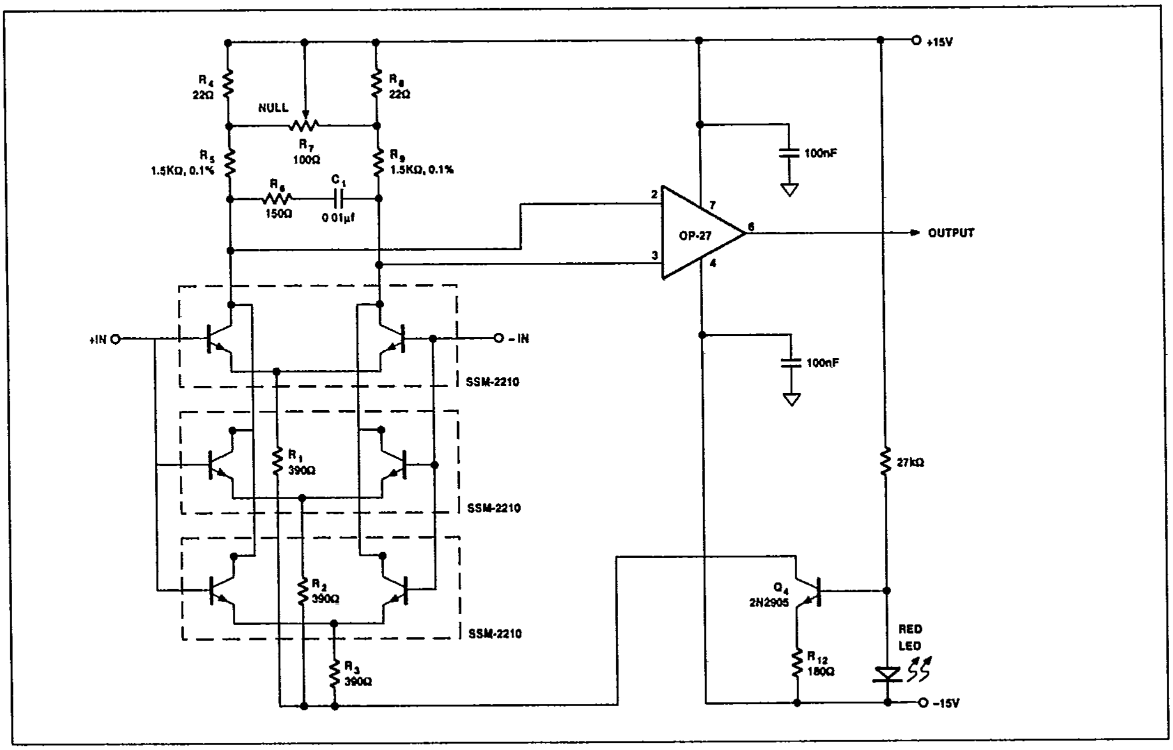

FIGURE 7: *Complete Amplifier Schematic*

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AMPLIFIER PERFORMANCE

The measured performance of the op amp is summarized in Table 2. Figure 8 shows the broadband noise spectrum which is flat at about 500pV/√Hz. Figure 9 shows the low-frequency spectrum which illustrates the low 1/f noise corner at 1.5Hz. The low-frequency characteristic in the time domain from 0.1Hz to 10Hz is shown in Figure 10; peak-to-peak amplitude is less than 40nV.

TABLE 2: Measured Performance of the Op Amp

Input Noise Voltage Density at 1kHz		500pV/√Hz
Input Noise Voltage from 0.1Hz to 10Hz		$40nV_{p-p}$
Input Noise Current at 1kHz		1.5pA/√Hz
Gain-Bandwidth	G = 10	3MHz
	G = 100	600kHz
	G = 1000	150kHz
Slew Rate		2V/µs
Open-Loop Gain		3×10^7
Common-Mode Rejection		130dB
Input Bias Current		3µA
Supply Current		10mA
Nulled TCV_{OS}		0.1µV/°C Max
T.H.D. at 1kHz	G = 1000	0.002%

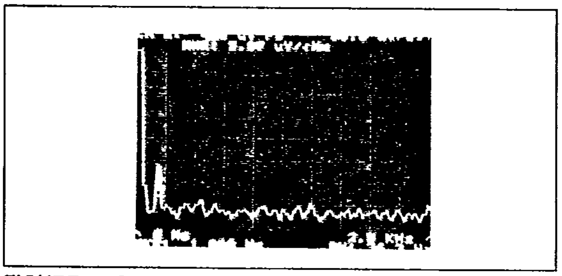

FIGURE 8: *Spectrum Analyzer Display – Broadband*

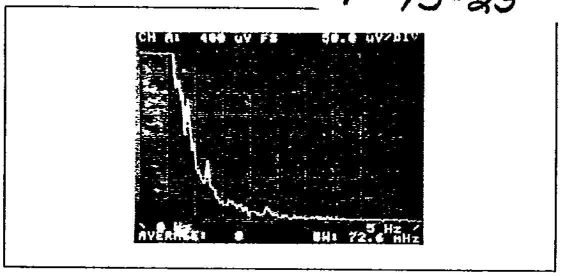

FIGURE 9: *Spectrum Analyzer Display – Low Frequency*

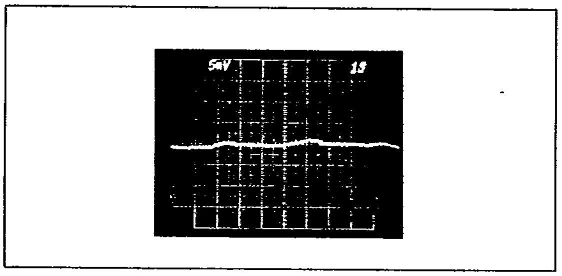

FIGURE 10: *Oscilloscope Display*

CONCLUSION

Using SSM-2210 matched transistor pairs operating at a high current level, it is possible to construct a high-performance, low-noise operational amplifier. The circuit uses a minimum of components and achieves performance levels exceeding monolithic amplifiers.

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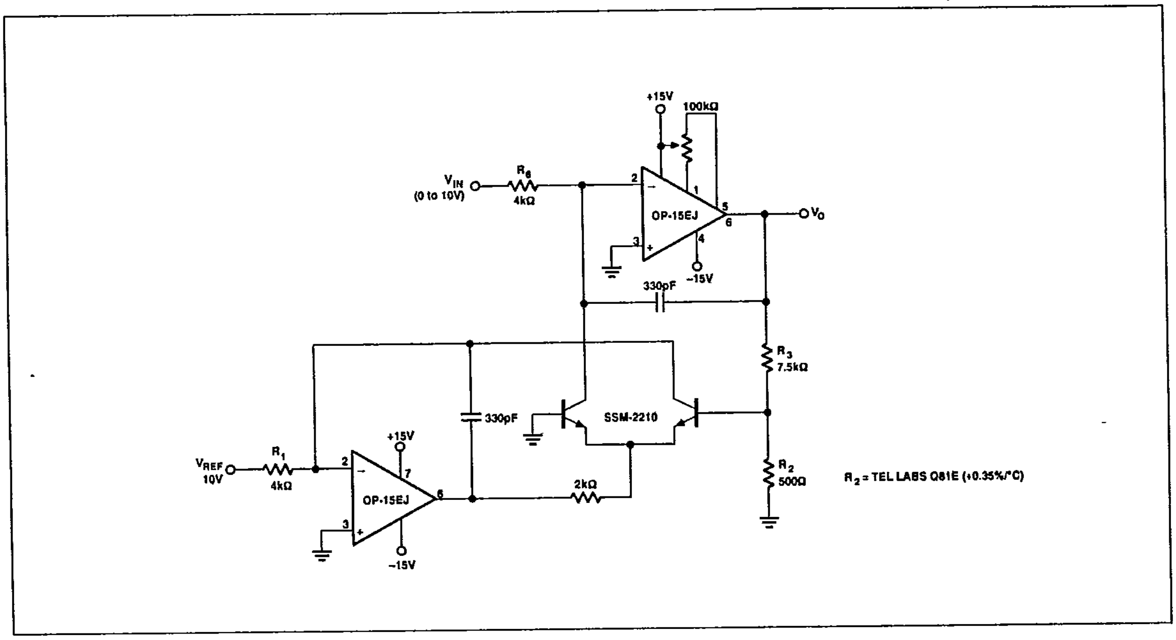

FIGURE 11: *Fast Logarithmic Amplifier*

FAST LOGARITHMIC AMPLIFIER

The circuit of Figure 11 is a modification of a standard logarithmic amplifier configuration. Running the SSM-2210 at 2.5mA per side (full-scale) allows a fast response with wide dynamic range. The circuit has a 7 decade current range, a 5 decade voltage range, and is capable of 2.5μs settling time to 1% with a 1 to 10V step.

The output follows the equation:

$$V_O = \frac{R_3 + R_2}{R_2} \frac{kT}{q} \ln \frac{V_{REF}}{V_{IN}}$$

To compensate for the temperature dependence of the kT/q term, a resistor with a positive 0.35%/°C temperature coefficient is chosen for R_2.

The output is inverted with respect to the input, and is nominally – 1V/decade using the component values indicated.

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