Multi-Channel ISM Band ASK/FSK/GFSK Transmitter

Preliminary Technical Data

ADF7012

FEATURES

Single Chip Low Power UHF Transmitter
50MHz - 1GHz Frequency Operation
Multi-Channel Operation using Frac-N PLL
2.3 – 3.6V Operation
On Board Regulator – Stable Performance
Programmable Output Power
-16dBm to +14dBm, 0.4dB steps
Data Rates – DC to 150kbits/s
Low Current Consumption

868MHz, 10dBm	**21mA**
433MHz, 10dBm	**17mA**
315MHz, 0dBm	**10mA**

Programmable Low Battery Voltage Readback
24-Lead TSSOP
Low Cost 0.25µm process

APPLICATIONS

Low Cost Wirelss Data Transfer
Security Systems
RF Remote Controls
Wireless Metering
Secure Keyless Entry

GENERAL DESCRIPTION

The ADF7012 is a low power ASK/FSK/GFSK UHF transmitter designed for use in Short Range Devices (SRD's). The output power, output channels, deviation frequency and modulation type are programmable by using four 32-bit registers.

The fractional-N and VCO with external inductor enable the user to select any frequency in the 50MHz to 1GHz band. The fast lock times of the fractional-N PLL make the ADF7012 suitable in fast frequency hopping systems. The fine frequency deviations available and PLL phase noise performance facilitates narrowband operation.

There are five different modulation schemes selectable: Binary or Gaussian On-Off Keying (OOK), Binary or Gaussian Frequency Shift Keying (FSK) and Amplitude Shift Keying (ASK). The compensation register allows the output to be moved in < 1ppm steps to allow indirect compensation for frequency error in the crystal reference.

Control of the registers is via a simple 3-wire interface. In power-down the part has a typical quiescent current of <0.1µA.

FUNCTIONAL BLOCK DIAGRAM

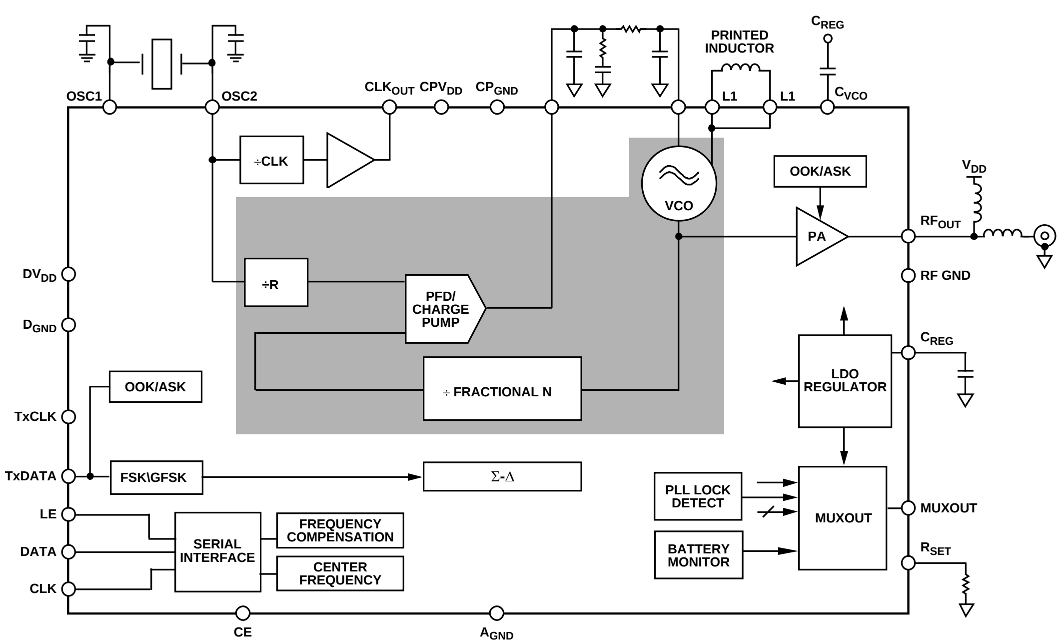

Figure 1.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.326.8703

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REVISION HISTORY

Revision PrE	Minor Typographical Edits
Revision PrD	Datasheet for final sampling silicon. Updated Register Maps. Functionality Description Added
Revision PrC	Measured Specifications for test silicon. Register Maps and pin descriptions of test silicon added
Revision PrB	Target specifications for test silicon
Revision PrA	Target Specifications for test silicon

SPECIFICATIONS[1]

Table 1. V_{DD} = 2.3V – 3.6V; AGND = DGND = 0 V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Parameter	B Version	Unit	Conditions/Comments
RF OUTPUT CHARACTERISTICS			
VCO Operating Frequency	50/1000	MHz min/max	VCO range adjustable using external inductor
Phase Frequency Detector	F_{RF} / 128	Hz min	
MODULATION PARAMETERS			
Datarate FSK/GFSK	179.2	kbits/s	Using 1MHz Loop BW
Datarate ASK/OOK	32	Kbits/s	Based on US FCC 15.247 Specfications for ACP
			Higher datarates are achievable depending on local regulations
Deviation FSK/GFSK	PFD/2^{14}	Hz min	e.g. 10MHz PFD – Deviation Min = +/- 610Hz
	511 * PFD/2^{14}	Hz max	e.g. 10MHz PFD – Deviation Max = +/- 311.7kHz
GFSK Bt	0.5	typ	
ASK Modulation depth	25	dB max	
OOK – PA Off – Feedthrough	-50	dBm typ	FRF = Fvco
	-80	dBm typ	FRF = Fvco / 2
POWER AMPLIFIER PARAMETERS			
Max Power Setting, Vdd = 3.6V	+14	dBm	FRF = 915MHz, PA is matched into 50Ω
Max Power Setting, Vdd = 3.0V	+13.5	dBm	FRF = 915MHz, PA is matched into 50Ω
Max Power Setting, Vdd = 2.3V	+12.5	dBm	FRF = 915MHz, PA is matched into 50Ω
Max Power Setting, Vdd = 3.6V	+14.5	dBm	FRF = 433MHz, PA is matched into 50Ω
Max Power Setting, Vdd = 3.0V	+14	dBm	FRF = 433MHz, PA is matched into 50Ω
Max Power Setting, Vdd = 2.3V	+13	dBm	FRF = 433MHz, PA is matched into 50Ω
PA Programmability	0.4	dB typ	
POWER SUPPLIES			
DV_{DD}	2.3/3.6	V min/V max	
Current Comsumption			
315MHz, 0dBm/5dBm	8/14	mA typ	Vdd = 3.0V, PA is matched into 50Ohms, IVCO = min
433MHz, 0dBm/10dBm	10/18	mA typ	
868MHz, 0dBm/10dBm/14dBm	14/21/32	mA typ	
915MHz, 0dBm/10dBm/14dBm	16/24/35	mA typ	
VCO Current Consumption	1/8	mA min/max	VCO current consumption is programmable
Crystal Oscillator Current Consumption	190	µA typ	
Regulator Current Consumption	280	µA typ	
Powerdown Current	0.1/1	µA typ	
REFERENCE INPUT			
Crystal Reference Frequency	3.4/26	MHz min/max	
Single Ended Reference Frequency	3.4/26	MHz min/max	
Crystal Power-on Time 3.4MHz/26MHz	1.8/2.2	ms typ	CE to Clock Enable Valid
Single Ended Input Level	TBD		Applied to OSC 2 – Oscillator Circuit Disabled

Parameter	B Version	Unit	Conditions/Comments
PHASE LOCKED LOOP PARAMETERS			
VCO Gain – 315MHz	10	MHz/V typ	
- 433MHz	15	MHz/V typ	
- 868MHz	30	MHz/V typ	
- 915MHz	40	MHz/V typ	
VCO Tuning Range	0.2/2.0	V min/max	
Spurious (IVCO Min/Max)	-65/-75	dBc	IVCO is programmable
Phase Noise (In band) – 315MHz	-94	dBc/Hz typ	PFD = 10MHz, 10kHz Offset, IVCO = 2mA
- 433MHz	-92	dBc/Hz typ	PFD = 10MHz, 10kHz Offset, IVCO = 2mA
- 868MHz	-91	dBc/Hz typ	PFD = 10MHz, 10kHz Offset, IVCO = 3mA
- 915MHz	-89	dBc/Hz typ	PFD = 10MHz, 10kHz Offset, IVCO = 3mA
Phase Noise (Out of Band) – 315MHz	TBD	dBc/Hz typ	PFD = 10MHz, 1MHz Offset, IVCO = 2mA
	TBD	dBc/Hz typ	PFD = 10MHz, 1MHz Offset, IVCO = 2mA
	TBD	dBc/Hz typ	PFD = 10MHz, 1MHz Offset, IVCO = 3mA
	TBD	dBc/Hz typ	PFD = 10MHz, 1MHz Offset, IVCO = 3mA
Harmonic Content (Second)	–27	dBc typ	FRF = FVCO
Harmonic Content (Third)	–21	dBc typ	
Harmonic Content (Others)	TBD	dBc max	.
Harmonic Content (Second)	–21	dBc typ	FRF = FVCO / N (Where N = 2,4,8)
Harmonic Content (Third)	–14	dBc typ	
Harmonic Content (Others)	TBD	dBc max	.
LOGIC INPUTS			
V_{INH},, Input High Voltage	0.7 x VDD	V min	
V_{INL}, Input Low Voltage	0.2 x VDD	V max	
I_{INH}/I_{INL}, Input Current	±1	µA max	
C_{IN}, Input Capacitance	3.0	pF max	
LOGIC OUTPUTS			
V_{OH}, Output High Voltage	DV_{DD} – 0.4	V min	CMOS output chosen.
I_{OH}, Output High Current	500	µA max	
V_{OL}, Output Low Voltage	0.4	V max	I_{OL} = 500 µA.

[1] Operating temperature range is: –40°C to +85°C.

TIMING CHARACTERISTICS

Table 2. $AV_{DD} = DV_{DD} = V_{VCO} = 3.3$ V ± 10%; AGND = DGND = 0 V; 1.8 V and 3 V logic levels used; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

Parameter	Limit at T_{MIN} to T_{MAX} (B Version)	Unit	Test Conditions/Comments
t_1	20	ns min	LE Setup Time
t_2	10	ns min	DATA to CLOCK Setup Time
t_3	10	ns min	DATA to CLOCK Hold Time
t_4	25	ns min	CLOCK High Duration
t_5	25	ns min	CLOCK Low Duration
t_6	10	ns min	CLOCK to LE Setup Time
t_7	20	ns min	LE Pulse Width

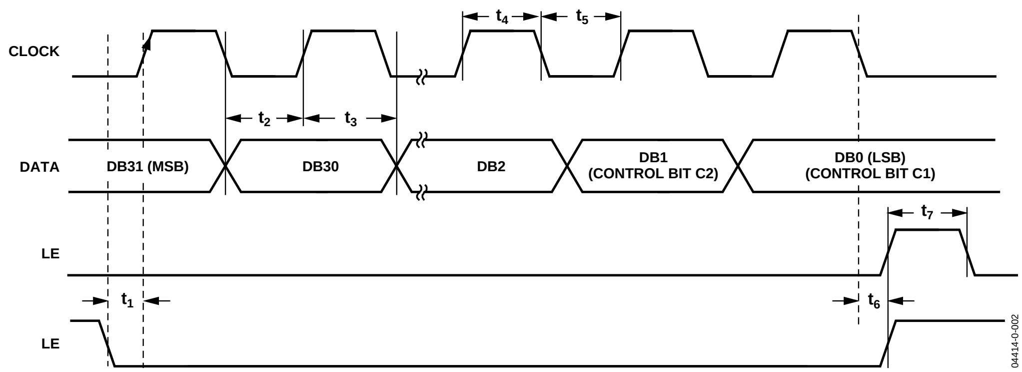


Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 3. $T_A = 25°C$, unless otherwise noted.

Parameter	Rating
AV_{DD} to GND*	–0.3 V to +3.9 V
AV_{DD} to DV_{DD}	–0.3 V to +0.3 V
Digital I/O Voltage to GND	–0.3 V to V_{DD} + 0.3 V
Analog I/O Voltage to GND	–0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Maximum Junction Temperature	150°C
TSSOP θ_{JA} Thermal Impedance	
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

*GND = AGND = DGND = 0 V.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device is a high performance RF integrated circuit with an ESD rating of 1 kV and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

TRANSISTOR COUNT

TBD (CMOS)

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTIONAL DESCRIPTIONS

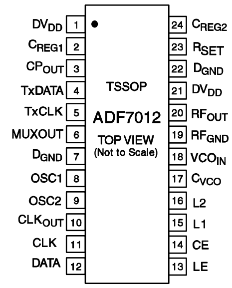


Figure 3. Pin Configuration

Table 4. Pin Functional Descriptions

Pin No.	Mnemonic	Function
1	DVDD	Positive Supply for the Digital Circuitry. This must be between 2.3 V and 3.6 V. Decoupling capacitors to the analog ground plane should be placed as close as possible to this pin.
2	Creg1	A 2.2 µF capacitor should be added at Creg to reduce regulator noise and improve stability. A reduced capacitor will improve regulator power-on time but may cause higher spurious.
3	CPout	Charge Pump Output. This output generates current pulses that are integrated in the loop filter. The integrated current changes the control voltage on the input to the VCO.
4	TxData	Digital data to be transmitted is inputted on this pin.
5	TxCLK	GFSK Only. This clock output is used to synchronize microcontroller data to the TxData Pin of the ADF7012. The clock is provided at the same frequency as the datarate.
6	MUXOUT	This pin provides the Lock_Detect signal, which is used to determine if the PLL is locked to the correct frequency, and a monitor of battery voltage. Other signals include Regulator_Ready which is an indicator of the status of the serial interface regulator.
7	DGND	Ground for digital section.
8	OSC1	The reference crystal should be connected between this pin and OSC2.
9	OSC2	The reference crystal should be connected between this pin and OSC1. A TCXO reference may be used, by driving this pin with CMOS levels, and powering down the crystal oscillator bit in software.
10	CLKout	A divided down version of the crystal reference with output driver. The digital clock output may be used to drive several other CMOS inputs, such as a microcontroller clock. The output has a 50:50 mark-space ratio.
11	CLK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the 24-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
12	DATA	Serial Data Input. The serial data is loaded MSB first with the two LSBs being the control bits. This is a high impedance CMOS input.
13	LE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift registers is loaded into one of the four latches, the latch being selected using the control bits..
14	CE	Chip Enable. Bringing CE low puts the ADF7012 into complete powerdown, drawing < 1uA. Register values are lost when CE is low and the part must be reprogrammed once CE is brought high.
15	L1	Connected to external printed or discrete inductor. See VCO description for values of L1,L2.
16	L2	Connected to external printed or discrete inductor.
17	Cvco	A 220nF capacitor should be tied between Cvco and Creg2 pin. This line should run under-neath the ADF7012. This capacitor isnecessary to ensure stable VCO operation.
18	VCOIN	The tuning voltage on this pin determines the output frequency of the Voltage Controlled Oscillator (VCO). The higher the tuning voltage the higher the output frequency.
19	RFGND	Ground for Output Stage of Transmitter
20	RFout	The modulated signal is available at this pin. Output power levels are from −16 dBm to +12 dBm. The output should be impedance matched using suitable components to the desired load. See Matching section (page 18).
21	DVDD	Voltage supply for VCO, and PA section. This should have the same supply as DVDD pin1, and should be between 2.3V and 3.6V. Decoupling capacitors to the analog ground plane should be placed as close as possible to this pin.
22	AGND	Ground Pin for the RF Analog Circuitry.
23	Rset	External resistor to set charge pump current and some internal bias currents. Use 3.6 kV as default:

24	Creg2	A 2.2 µF capacitor should be added at Creg to reduce regulator noise and improve stability. A reduced capacitor will improve regulator power-on time but may cause higher spurious.

TYPICAL PERFORMANCE CHARACTERISTICS

FSK Spectrum – 868MHz, Span 1MHz,F Deviation = 30kHz

OOK Spectrum, 9.6kbits/s

902MHz Output Spectrum, Span 50MHz

Harmonic levels (Start 800MHz, Stop 7.75GHz)

Phase Noise 868MHz (VCO Setting 7)

Lock Time, 902MHz to928Mhz(+/-1kHz)

Tuning Sensitivity of VCO vs Output Frequency

Spurious levels vs. Ibias for VCO

Phase Noise vs. Output Frequency

GFSK Spectrum- 2.4kbits/s 5kHz Deviation

Output Power Level vs. Idd, 915Mhz, 868MHz, 433MHz, 315MHz

Regulator Power-On Time (Over temp/Supply)

Crystal Power-On Time

OOK vs. GOOK Spectrum

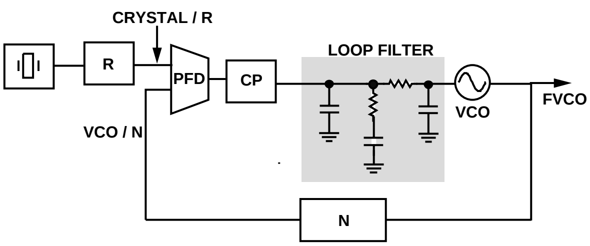
Clock Out Signal 4.8MHz in 20pF Load

FSK vs. GFSK Spectrum

CIRCUIT DESCRIPTION

PLL OPERATION

The fractional-N PLL allows mulitple output frequencies to be generated from a single reference oscillator (usually a crystal). simply by changing the programmable N-value found in the N-register. At the Phase Frequency Detector (PFD), the reference is compard to a divided-down version of the output frequency (VCO / N). If VCO/N is too low a frequency, this implies that the output frequency is lower than desired, and the PFD and charge pump combination will send additional current pulses to the loop filter. This increases the voltage applied to the input of the VCO. Since the VCO of the ADF7012 has a positive frequency vs. voltage characteristic, any increase in the Vtune voltage applied to the VCO input will increase the output frequency at a rate of Kv, the tuning sensitivity of the VCO (MHz/V). At each interval of 1/PFD seconds, a comparison is made at the PFD until eventually the PFD and charge pump force a state of equilibrium in the PLL where PFD frequency = VCO / N. At this point the PLL can be described as locked.



$$F_{OUT} = \frac{F_{CRYSTAL} \times N}{R}$$

$$= F_{PFD} \times N$$

For a Fractional N PLL

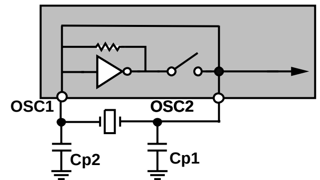
$$F_{OUT} = F_{PFD} \times \left(N_{INT} + \frac{N_{FRAC}}{2^{12}} \right)$$

Where N_{FRAC} are bits M1 – M12 in the fractional N register.

CRYSTAL OSCILLATOR

The on-board crystal oscillator circuitry (Figure 2), allows the use of an inexpensive quartz crystal as the PLL reference. The oscillator circuit is enabled by setting XOEB low. It is enabled by default on power-up and is disabled by bringing CE low. Errors in the crystal can be corrected using the Error Correction Register within the R-Register.

A single-ended reference (TCXO, CXO) may be used. By applying levels OSC2, with XOEB set high.



Two parallel resonant capacitors are required for oscillation at the correct frequency - the value of these are dependant on the crystal specification. They should be chosen so that the series value of capacitance added to the PCB track capitance adds to give the load capacitiance of the crystal, usually 20pF. Track capacitance values vary between 2-5pF dependant on board layout.

Where possible capacitors should be chosen so that they have a very low temperature coefficient and/or with opposite temperature coefficents to ensure stable frequency operation over all conditions.

CRYSTAL COMPENSATION REGISTER

The ADF7012 features a 15-bit fixed modulus, which allows the output frequency to be adjusted in steps of $F_{PFD} / 2^{15}$. This fine resolution can be used to easily compensate for initial error, and temperature drift in the reference crystal.

$$F_{ADJUST} = F_{STEP} \times FEC$$

where $F_{STEP} = F_{PFD} / 2^{15}$,

and FEC = Bits F1 to F11 in R-Register.

Note that notation is 2's compliment, so F11 represents the sign of the FEC number.

Example -

F_{PFD} = 10MHz

F_{ADJUST} = -11 kHz

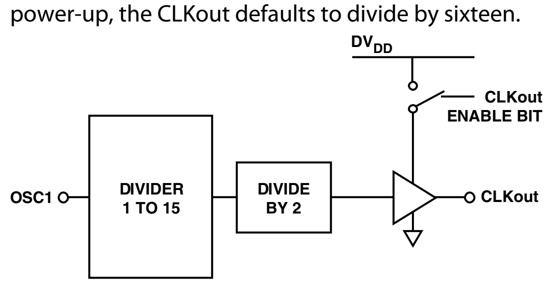
F_{STEP} = 10MHz / 2^{15} = 305.176 Hz

FEC = -11kHz / 305.176Hz

= -36 = -(00000100100) = 11111011100 = 0x7DC

CLOCK OUT CIRCUIT

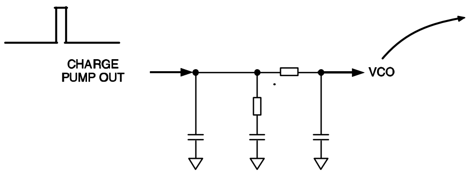
The CLKout circuit takes the reference clock signal from the oscillator section above and supplies a divided down 50:50 mark-space signal to the CLKout pin. An even divide from 2 to 30 is available. This divide is set by the TBD in the R-Register. On power-up, the CLKout defaults to divide by sixteen.



The output buffer to CLKout is enabled by setting Bit TBD in the function register high. On power-up, this bit is set high. The output buffer can drive up to a 20 pF load with a 10% rise time at 4.8 MHz. Faster edges can result in some spurious feedthrough to the output. A small series resistor (50Ω) can be used to slow the clock edges to reduce these spurs at F_{CLK}.

LOOP FILTER

The loop filter integrates the current pulses from the charge pump to form a voltage that tunes the output of the VCO to the desired frequency. It also attenuates spurious levels generated by the PLL. A typical loop filter design is shown below:



In FSK, the loop should be designed so that the loop bandwidth (LBW) is a minimum of 5 times the data-rate. Widening the LBW excessively reduces the time spent jumping between frequencies but will result in reduced spurious attenuation.

For OOK/ASK systems, a wider loop BW than for FSK systems is desirable. The sudden large transition between two power levels will result in VCO pulling (VCO will temporarily go to incorrect frequency) and can cause a wider output spectrum . By widening the loop BW a minimum of 10 x data rate, VCO pulling is minimised, since the loop will settle quickly back to the correct frequency. The free design tool ADIsimPLL can be used to design loop filters for the ADI family of transmitters.

VOLTAGE CONTROLLED OSCILLATOR (VCO)

The ADF7012 features an on-chip VCO, with an external tank inductor, which is used to set the frequency range. The centre frequency of oscillation is governed by the internal varactor capacitance and that of the external inductor combined with the bondwire inductance.

$$F_{VCO} = \frac{1}{2\pi\sqrt{(L_{INT} + L_{EXT}) \times (C_{VAR} + C_{FIXED})}}$$

where L_{INT} = 2.778nH, (C_{VAR} + C_{FIXED})= 6.5pF (min), 7.8pF(max).
The varactor capacitance can be adjusted in software to increase the effective VCO range by writing to bits VA1 and VA2 in the R-Register. Under typical conditions, setting VA1, and VA2 high will increase the centre frequency, by reducing the varactor capacitance by 1.3pF.

Figure TBD contains a plot of the VCO gain over temperature and frequency. VCO gain is impoortant in determining the loop filter design – Predictable changes in VCO gain resulting in a change in the loop filter BW can be offset by changing charge pump current in software.

VCO Bias Current

VCO bias current may be adjusted usinig bits VB1 to VB4 in the function register. Minimum bias currents under typical conditions to ensure VCO oscillation are shown in Table TBD. Additional bias current will reduce spurious levels as shown in figure TBD, but will increase overall current consumption in the part. A bias value of 0x7 should ensure oscillation at most frequencies and supplies. Settings 0x0, 0xE and 0xF are not recommended.

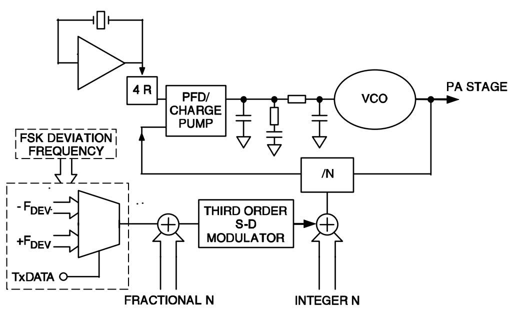
VOLTAGE REGULATORS

There are 2 bandgap voltage regulators on the ADF7012 providing a stable 2.2V internal supply. A 2.2µF capacitor (X5R, NP0) to ground at Creg1 and Creg2 should be used to ensure stability. The internal reference ensures consistent performance over all supplies and reduces the current consumption of each of the blocks.

The combination of regulator 1 and 2 consume TBDµA at 3.0V and can be powered down by bringing the CE line low. The serial interface is supplied by regulator 1, and so powering down the CE line will cause the contents of the registers to be lost. The CE line must be high, and the regulators must tbe fully powered on to write to the serial interface. Regulator power on time is a maximum of TBDµs and should be taken into account when writing to the ADF7012 after power up. Aternatively regulator status may be monitored at the MUXout pin once CE has been asserted, since MUXout will default to Reg_ready signal. Once Reg_ready is high, the regulator is powered up and the serial interface is active.

FSK MODULATION

FSK modulation is performed internally in the PLL loop by switching the value of the N-Register based on the status of the TxData line. The TxData line is sampled at each cycle of the PFD block (Every 1/ F_{PFD} seconds). When TxData makes a low to high transition, an N-value representing the deviation frequency will be added to the N-value representing the center frequency. Immediately the loop will begin to lock to the new frequency of $F_{CENTER} + F_{DEVIATION}$. Conversely, when TxData makes a high to low transition the N-Value representing the deviation will be subtracted from the PLL N-value representing the center frequency and the loop will transition to $F_{CENTER} - F_{DEVIATION}$.



The deviation from the center frequency is set using bits D1-D9 in the Modulation Register. The frequency deviation may be set in steps of :

$$F_{STEP}(Hz) = \frac{F_{PFD}}{2^{14}}$$

The deviation frequency is therefore

$$F_{DEVIATION}(Hz) = \frac{F_{PFD} \times ModulationNumber}{2^{14}}$$

where ModulationNumber is set by bits D1 to D9.

The maximum datarate is a function of the PLL lock time (and the requirement on FSK spectrum). Since PLL lock time is reduced by increasing the loop filter BW, highest data rates can be achieved for the wider loop filter BW's. The absolute maximum limit on loop filter BW to ensure stability for a fractional-N PLL is F_{PFD} / 7. For a 20MHz PFD frequency the loop BW could be as high as 2.85MHz.
FSK Modulation is selected by setting bits S1 and S2 in the Modulation Register low.

GFSK MODULATION

GFSK stands for Gaussian Frequency Shift Keying, and it represents a filtered form of frequency shift keying. The data to be modulated to RF is pre-filtered digitally using an Finite Impulse Response (FIR) filter. The filtered data is then used to modulate the sigma-delta fractional-N, to generate spectrally-efficient FSK.

FSK consists of a series of sharp transitions in frequency as the data is switched one level to the other. The sharp switching will generate higher frequency components at the output resulting in a wider output spectrum.

With GFSK the sharp transitions are replaced with up to 128 smaller steps. The result is a gradual change in frequency. As a result, the higher frequency components are reduced and the spectrum occupied is reduced significantly. GFSK does require some additional design work as the data is only sampled once per bit, and so the choice of crystal is important to allow for the correct sampling clock to be generated.

The number of steps per symbols is determined by the setting for the index counter.

The GFSK deviation is set up as follows :

$$GFSKdeviation(Hz) = \frac{F_{PFD} \times 2^{m}}{2^{12}}$$

where m is the mod control (Bits MC1 to MC3 in the Modulation Register).

The GFSK sampling clock will sample data at the datarate.

$$DataRate(bits/s) = \frac{F_{PFD}}{DividerFactor \times IndexCounter}$$

where DividerFactor are bits D1-D7, and IndexCounter are bits IC1 and IC2 in the Modulation Register.

POWER AMPLIFIER

The output stage is based on a Class E amplifier design, with an open drain output switched by the VCO signal. The output control consists of 6 current mirrors, operating as a programmable current source.

To achieve maximum voltage swing the RFout pin needs to be biased at Vdd. A single pull-up inductor to Vdd will ensure a current supply to the output stage, PA biased to Vdd volts, and with the correct choice of value will transform the impedance.
The output power can be adjusted by changing the value of bits P1-P6. Typically P1-P6 will output –35dBm at 0x0, and 13dBm at 0x7E at 868MHz with the optimum matching network.
The non-linear characteristic of the output stage will result in an output spectrum containing harmonics of the fundamental, especially the 3rd and 5th. A low pass filter will usually be required to filter these harmonics to meet local regulations.

The output stage can be powered down by setting bit PD2 in the Function Register low.

GASK MODULATION

Gaussian Amplitude Shift keying (GASK), represents a prefiltered form of ASK modulation. The usually sharp symbol transitions are replaced with smooth gaussian filtered transitions with the result being a reduction in frequency pulling of the VCO. Frequency pulling of the VCO in OOK mode can lead to a wider than desired BW, especially if it is not possible to increase the loop filter BW to > 300kHz.
The GASK sampling clock will sample data at the datarate.

$$DataRate(bits/s) = \frac{F_{PFD}}{DividerFactor \times IndexCounter}$$

Bits D1-D6 represent the output power for the system for a positive data bit. Divider Factor = 0x3F respresents the maximum possible deviation from PA at minimum to PA at maximum output.

OUTPUT DIVIDER

This is a programmable divider following the VCO in the PLL loop. This is useful in using the ADF7012 to generate frequencies of < 300MHz.
The output divider may be used to reduce feedthough of the VCO, by amplifying only the VCO/2 component, restricting the VCO feedthough to leakage.

Since the divider is in loop, the N-Register values should be setup according to the usual formula. However the VCO gain (Kv), should be scaled according to the divider setting.

e.g. Fout = 433MHz, Fvco = 866MHz, Kv @ 868MHz = 60MHz/V

-> Kv for loop filter design = 30MHz/V

The divider value is set in the R-Register.

OD1	OD2	Divider Status
0	0	Divider OFF
0	1	Divide by 2
1	0	Divide by 4
1	1	Divide by 8

MUXOUT MODES

The MUXout pin allows the user access to various internal signals in the transmitter, as well as providing information on the PLL lock status, the regulator and the battery voltage. The MUXout is accessed by programming bits M1-M4 in the function register, and observing the signal at the MUXout pin.

Battery Voltage Read back

By setting MUXout to settings 1010 to 1101, the battery voltage can be estimated. The battery measuring circuit features a voltage divider and a comparator, where the divided down supply voltage is compared to the regulator voltage.

MUXOUT	MUXout High	MUXout LOW
1010	Vdd > 3.25V	Vdd < 3.25V
1011	Vdd > 3.0V	Vdd < 3.0V
1100	Vdd > 2.75V	Vdd < 2.75V
1101	Vdd > 2.35	Vdd < 2.35

The acccuracy of the measurment is limited by the accuracy of the regulator voltage and also the internal resistor tolerances. Worst case accuracy is < TBD%

Regulator Ready

The regulator has a power-up time, dependant on process and the external capacitor. The regulator ready signal indicates that the regulator is fully powered, and that the serial interface is active. This is the default setting on power-up at MUXout.

Digital Lock Detect

Digital Lock Detect indicates that the status of the PLL loop. The PLL loop is will take time to settle on power-up, and when the frequency of the loop is changed by changing the N-value. When Lock Detect is high the PFD has counted a number of consequetive cycles where the phase error is < 15ns. The Lock Detect Precision Bit in the Function Register deteremines whether this is 3 (LDP = 0), or 5 (LDP=1) cycles. It is recommended that LDP be set to 1. The lock detect is not completely accurate and will go high before the output has settled to exactly the correct frequency. As a rule-of-thumb, add 50% to the indicated lock time to obtain locktime to within 1kHz. The lock detect signal can be used to decide when the Power Amplifer (PA) should be enabled .

R-Divider

MUXout will provide the output of the R-Divider. This is a narrow pulsed digital signal at F_{PFD}. This signal may be used to check the operation of the crystal circuit, and R-Divider. R-Divider / 2 is a buffered version of this signal at F_{PFD} / 2.

Table 2. R Register

					OUTPUT DIVIDER		VCO ADJUST		CLOCK OUT DIVIDER				XOEB	CRYSTAL DOUBLE R	4-BIT R-DIVIDER				11-BIT FREQUENCY ERROR CORRECTION											Address Bits	
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
					OD2	OD1	VA2	VA1	CL4	CL3	CL2	CL1	D1	X1	R4	R3	R2	R1	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	C2(0)	C1(0)

X1	XOEB
0	XTAL OSCILLATOR ON
1	XTAL OSCILLATOR OFF

D1	CRYSTAL DOUBLER
0	CRYSTAL DOUBLER OFF
1	CRYSTAL DOUBLER ON

F11		F3	F2	F1	F-COUNTER OFFSET
0	....	1	1	1	1023
0	....	1	1	0	1022
0	....	.	.	.	.
0	....	0	0	1	1
0	....	0	0	0	0
1	....	1	1	1	-1
1	....	1	1	0	-2
	....	.	.	.	.
1	....	0	0	1	-1023
1	....	0	0	0	-1024

e.g., F-COUNTER OFFSET = 1, FRACTIONAL OFFSET = $1/2^{15}$

OD2	OD1	Output Divider
0	0	Disabled
0	1	Divide by 2
1	0	Divide by 4
1	1	Divide by 8

VA2	VA1	VCO Adjust
0	0	No VCO Adjustment
0	1	(Fcenter - (1 x f))
1	0	(Fcenter - (2 x f))
1	1	(Fcenter - (3 x f))

CL4	CL3	CL2	CL1	CLK_{OUT} DIVIDE RATIO
0	0	0	1	2
0	0	1	0	4
0	0	1	1	6
0	1	0	0	8
	..	.	.	
	..	.	.	
1	1	1	0	28
1	1	1	1	30

R4	R3	R2	R1	RF R COUNTER DIVIDE RATIO
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

Table 3. N Counter Latch

									PRE-SCALER	8-BIT INTEGER-N								12-BIT FRACTIONAL-N												ADDRESS BITS	
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
									P1	N8	N7	N6	N5	N4	N3	N2	N1	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	C2 (0)	C1 (1)

M12	M11	M10		M3	M2	M1	MODULUS DIVIDE RATIO
0	0	0	....	0	0	0	0
0	0	0	....	0	0	1	1
0	0	0	....	0	1	0	2
.	.	.	....	.	.	.	.
.	.	.	....	.	.	.	.
.	.	.	....	.	.	.	.
1	1	1	....	1	0	0	4092
1	1	1	....	1	0	1	4093
1	1	1	....	1	1	0	4094
1	1	1	....	1	1	1	4095

N8	N7	N6	N5	N4	N3	N2	N1	N COUNTER DIVIDE RATIO
0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	1	1	3
	.	.	.	.	.	.	.	
	.	.	.	.	.	.	.	
	.	.	.	.	.	.	.	
1	1	1	1	1	1	1	0	254
1	1	1	1	1	1	1	1	255

The minimum N-Value is $P^2 + 3P + 3$ where P is the prescaler setting.

P1	PRESCALER
0	4/5
1	8/9

Table 4. Modulation Register

				PA_EX	GASK CONTROL		INDEX COUNTER		GFSK MOD CONTROL			MODULATION DEVIATION									POWER AMPLIFIER						GASK	MOD CONTROL		ADDRESS Bits	
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
					GC2	GC1	IC2	IC1	MC3	MC2	MC1	D9	D8	D7	D6	D5	D4	D3	D2	D1	P6	P5	P4	P3	P2	P1	G1	S2	S1	C2(1)	C1(0)

MUST BE LOW

G1	GAUSSIAN ASK
0	ON
1	OFF

S2	S1	MODULATION SCHEME
0	0	FSK
0	1	GFSK
1	0	ASK
1	1	OOK

If Amplitude Shift Keying Selected, TxData = 0

D6		.	D2	D1	
0	.	.	0	0	PA OFF
	.	.	0	1	-16.0dBm
0	.	.	1	0	-16 + 0.45dBm
0	.	.	1	1	-16 + 0.90dBm
.	.	.	.	.	.
.	.	.	.	.	.
1	1	1	1	1	13dBm

Power Amplifier Output Level

P6		.	P2	P1	
0	.	.	0	0	PA OFF
0	.	.	0	1	-16.0dBm
0	.	.	1	0	-16 + 0.45dBm
0	.	.	1	1	-16 + 0.90dBm
.	.	.	.	.	.
.	.	.	.	.	.
1	1	1	1	1	13dBm

IF FREQUENCY SHIFT KEYING SELECTED

D9. . . .	D3	D2	D1	F DEVIATION
0	0	0	0	PLL MODE
0	0	0	1	$1 \chi F_{STEP}$
0	0	1	0	$2 \chi F_{STEP}$
0	0	1	1	$3 \chi F_{STEP}$
.	.	.	.	....
1	1	1		$511x \; F_{STEP}$

$$F_{STEP} = F_{PFD}/2^{14}$$

IF GAUSSIAN FREQUENCY SHIFT KEYING SELECTED

IC2	IC1	INDEX COUNTER
0	0	16
0	1	32
1	0	64
1	1	128

D9	D3	D2	D1	DIVIDER FACTOR
0	0	0	0	
0	0	0	1	1
0	0	1	0	2
0	0	1	1	
.	.	.	.	......
1	1	1	1	511

MC3	MC2	MC1	GFSK MOD CONTROL
0	0	0	0
0	0	1	1
.	.	.	.
1	1	1	7

IF GAUSSIAN AMPLITUDE SHIFT KEYING SELECTED

IC2	IC1	INDEX COUNTER
0	0	16
0	1	32
1	0	64
1	1	128

MC3	MC2	MC1	GFSK MOD CONTROL
0	0	0	0
0	0	1	1
.	.	.	.
1	1	1	7

Power Amplifier Output Level

D6			D2	D1	
0			0	0	PA OFF
0			0	1	-16.0dBm
0			1	0	-16 + 0.45dBm
0			1	1	-16 + 0.90dBm
.	.	.	.	.	.
.	.	.	.	.	.
1	1	1	1	1	13dBm

Table 5. Function Register

SD TEST MODES				PLL TEST MODES					PA BIAS			VCO BIAS				LD PRECISION	MUXOUT				VCO DISABLE	BLEED CURRENT		CHARGE PUMP		DATA INVERT	CLKOUT ENABLE	PA ENABLE	PLL ENABLE	ADDRESS BITS	
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
ST4	ST3	ST2	ST1	PT5	PT4	PT3	PT2	PT1	PA3	PA2	PA1	VB4	VB3	VB2	VB1	LD1	M4	M3	M2	M1	VD1	CP4	CP3	CP2	CP1	I1	PD3	PD2	PD1	C2(1)	C2(1)

I1	DATA INVERT
0	DATA
1	DATA

CP4	BLEED DOWN
0	BLEED OFF
1	BLEED ON

PD1	PLL ENABLE
0	PLL OFF
1	PLL ON

PA3	PA2	PA1	PA Bias
0	0	0	5uA
0	0	1	6uA
0	1	0	7uA
.	.	.	
.	.	.	
1	1	1	12uA

CP3	BLEED UP
0	BLEED OFF
1	BLEED ON

PD2	PA ENABLE
0	PA OFF
1	PA ON

CP2	CP1	CHARGE PUMP CURRENT
0	0	1/7 * 2.5mA
0	1	3/7 * 2.5mA
1	0	5/7 * 2.5mA
1	1	2.5mA

VB4	VB3	VB2	VB1	VCO Bias Current
0	0	0	1	0.5mA
0	0	1	0	1mA
.	.	.	.	
1	1	1	1	8mA

VD1	VCO DISABLE
0	VCO ON
1	VCO OFF

PD3	CLK_{OUT}
0	CLK_{OUT} OFF
1	CLK_{OUT} ON

M4	M3	M2	M1	MUXOUT
0	0	0	0	LOGIC LOW
0	0	0	1	LOGIC HIGH
0	0	1	0	DO NOT USE
0	0	1	1	REGULATOR READY (DEFAULT)
0	1	0	0	DIGITAL LOCK DETECT
0	1	0	1	ANALOG LOCK DETECT
0	1	1	0	R DIVIDER / 2 OUTPUT
0	1	1	1	N DIVIDER / 2 OUTPUT
1	0	0	0	RF R DIVIDER OUTPUT
1	0	0	1	DATA RATE
1	0	1	0	BATTERY MEASURE IS > 3.25V ?
1	0	1	1	BATTERY MEASURE IS > 3V ?
1	1	0	0	BATTERY MEASURE IS > 2.75V ?
1	1	0	1	BATTERY MEASURE IS > 2.35V ?
1	1	1	0	NORMAL TEST MODES
1	1	1	1	SIGMA-DELTA TEST MODES

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

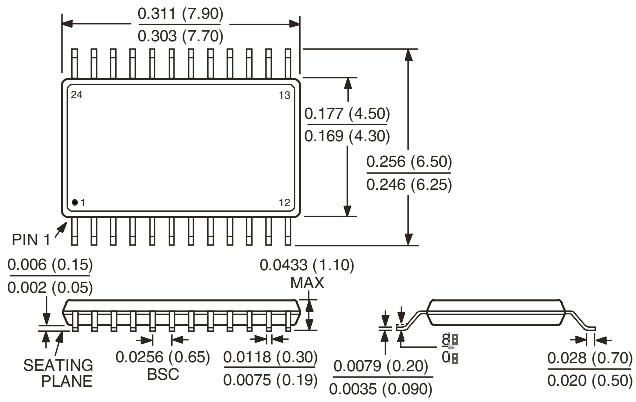


Figure TBD. 24-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-24)

ORDERING GUIDE

Model	Temperature Range	Frequency Range	Package Option
ADF7012BRU EVAL-ADF7012EB1	−40°C to +85°C	50 MHz to 1GHz 902-928 MHz	RU-24 Evaluation Board – Available Jan 2004
EVAL-ADF7012EB2		860-880 MHz	Evaluation Board – Available Jan 2004
EVAL-ADF7012EB3		418-435MHz	Evaluation Board – Available Jan 2004
EVAL-ADF7012EB4		310–330MHz	Evaluation Board – Available Jan 2004
EVAL-ADF7012EB5		50MHz – 1GHz	Evaluation Board – Available Dec 2003