128-Position I²C Compatible Digital Potentiometer

AD5247

FEATURES

128-position
End-to-end resistance 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ
Ultracompact SC70-6 (2 mm × 2.1 mm) package
I²C® compatible interface
Full read/write of wiper register
Power-on preset to midscale
Single supply 2.7 V to 5.5 V
Low temperature coefficient 45 ppm/°C
Low power, I_{DD} = 3 µA typical
Wide operating temperature –40°C to +125°C
Evaluation board available

APPLICATIONS

Mechanical potentiometer replacement in new designs
Transducer adjustment of pressure, temperature, position, chemical, and optical sensors
RF amplifier biasing
LCD brightness and contrast adjustment
Automotive electronics adjustment
Gain control and offset adjustment

GENERAL OVERVIEW

The AD5247 provides a compact 2 mm × 2.1 mm packaged solution for 128-position adjustment applications. This device performs the same electronic adjustment function as a mechanical potentiometer or a variable resistor. Available in four different end-to-end resistance values (5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ), these low temperature coefficient devices are ideal for high accuracy and stability variable resistance adjustments.

The wiper settings are controllable through the I²C compatible digital interface, which can also be used to read back the present wiper register control word. The resistance between the wiper and either end point of the fixed resistor varies linearly with respect to the digital code transferred into the RDAC[1] latch.

Operating from a 2.7 V to 5.5 V power supply and consuming 3 µA allows for usage in portable battery-operated applications.

FUNCTIONAL BLOCK DIAGRAM

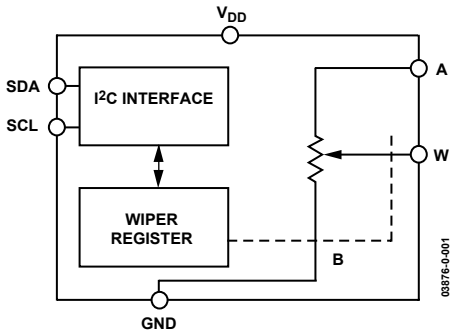

Figure 1.

[1] Note: The terms digital potentiometer, VR, and RDAC are used interchangeably in this document.

Rev. 0

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TABLE OF CONTENTS

REVISION HISTORY

Revision 0: Initial Version

ELECTRICAL CHARACTERISTICS—5 kΩ VERSION

Table 1. V_{DD} = 5 V ±10% or 3 V ± 10%; V_A = +V_{DD}; −40°C < T_A < +125°C; unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}, V_A = No Connect	−1.5	±0.1	+1.5	LSB
Resistor Integral Nonlinearity[2]	R-INL	R_{WB}, V_A = No Connect	−4	±0.75	+4	LSB
Nominal Resistor Tolerance[3]	ΔR_{AB}		−30		+30	%
Resistance Temperature Coefficient	$\Delta R_{AB}/\Delta T$	$V_A = V_{DD}$, Wiper = No Connect		45		ppm/°C
R_{WB}	R_{WB}	Code = 0x00		75	300	Ω
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE						
Differential Nonlinearity[4]	DNL		−1	±0.1	+1	LSB
Integral Nonlinearity[4]	INL		−1	±0.2	+1	LSB
Voltage Divider Temperature Coefficient	$\Delta V_W/\Delta T$	Code = 0x40		15		ppm/°C
Full-Scale Error	V_{WFSE}	Code = 0x7F	−3	−2	0	LSB
Zero-Scale Error	V_{WZSE}	Code = 0x00	0	+1	+2	LSB
RESISTOR TERMINALS						
Voltage Range[5]	$V_{B, W}$		GND		V_{DD}	V
Capacitance[6] A	C_A	f = 1 MHz, Measured to GND, Code = 0x40		45		pF
Capacitance[6] W	C_W	f = 1 MHz, Measured to GND, Code = 0x40		60		pF
Common-Mode Leakage	I_{CM}	$V_A = V_{DD}/2$		1		nA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}	V_{DD} = 5 V	2.4			V
Input Logic Low	V_{IL}	V_{DD} = 5 V			0.8	V
Input Logic High	V_{IH}	V_{DD} = 3 V	2.1			V
Input Logic Low	V_{IL}	V_{DD} = 3 V			0.6	V
Input Current	I_{IL}	V_{IN} = 0 V or 5 V			±1	µA
Input Capacitance[6]	C_{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	$V_{DD\ RANGE}$		2.7		5.5	V
Supply Current	I_{DD}	V_{IH} = 5 V or V_{IL} = 0 V		3	8	µA
Power Dissipation[7]	P_{DISS}	V_{IH} = 5 V or V_{IL} = 0 V, V_{DD} = 5 V			40	µW
Power Supply Sensitivity	PSSR	V_{DD} = +5 V ± 10%, Code = Midscale		±0.003	±0.05	%/%
DYNAMIC CHARACTERISTICS[6, 8]						
Bandwidth −3 dB	BW_5K	R_{AB} = 5 kΩ, Code = 0x40		1.2		MHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms, V_B = 0 V, f = 1 kHz		0.05		%
V_W Settling Time	t_S	V_A = 5 V, ±1 LSB Error Band		1		µs
Resistor Noise Voltage Density	e_{N_WB}	R_{WB} = 2.5 kΩ, R_S = 0 Ω		6		nV/√Hz

[1] Typical specifications represent average readings at 25°C and V_{DD} = 5 V.
[2] Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic.
[3] $V_A = V_{DD}$, Wiper (V_W) = no connect.
[4] INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. $V_A = V_{DD}$ and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
[5] Resistor terminals A and W have no limitations on polarity with respect to each other.
[6] Guaranteed by design and not subject to production test.
[7] P_{DISS} is calculated from ($I_{DD} \times V_{DD}$). CMOS logic level inputs result in minimum power dissipation.
[8] All dynamic characteristics use V_{DD} = 5 V.

ELECTRICAL CHARACTERISTICS—10 kΩ, 50 kΩ, 100 kΩ VERSIONS

Table 2. V_{DD} = 5 V ± 10% or 3 V ± 10%; $V_A = V_{DD}$; –40°C < T_A < +125°C; unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}, V_A = No Connect	–1	±0.1	+1	LSB
Resistor Integral Nonlinearity[2]	R-INL	R_{WB}, V_A = No Connect	–2	±0.25	+2	LSB
Nominal Resistor Tolerance[3]	ΔR_{AB}		–20		+20	%
Resistance Temperature Coefficient	$\Delta R_{AB}/\Delta T$	$V_A = V_{DD}$, Wiper = No Connect		45		ppm/°C
R_{WB}	R_{WB}	Code = 0x00		75	300	Ω
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE						
Differential Nonlinearity[4]	DNL		–1	±0.1	+1	LSB
Integral Nonlinearity[4]	INL		–1	±0.2	+1	LSB
Voltage Divider Temperature Coefficient	$\Delta V_W/\Delta T$	Code = 0x40		15		ppm/°C
Full-Scale Error (50 kΩ, 100 kΩ)	V_{WFSE}	Code = 0x7F	–1	–1	0	LSB
Zero-Scale Error (50 kΩ, 100 kΩ)	V_{WZSE}	Code = 0x00	0	+0.4	+1	LSB
Full-Scale Error (10 kΩ)	V_{WFSE}	Code = 0x7F	–2	–0.5	0	LSB
Zero-Scale Error (10 kΩ)	V_{WZSE}	Code = 0x00	0	+0.5	+1	LSB
RESISTOR TERMINALS						
Voltage Range[5]	$V_{A, W}$		GND		V_{DD}	V
Capacitance[6] A	C_A	f = 1 MHz, Measured to GND, Code = 0x40		45		pF
Capacitance[6] W	C_W	f = 1 MHz, Measured to GND, Code = 0x40		60		pF
Common-Mode Leakage	I_{CM}	$V_A = V_{DD}/2$		1		nA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}	V_{DD} = 5V	2.4			V
Input Logic Low	V_{IL}	V_{DD} = 5 V			0.8	V
Input Logic High	V_{IH}	V_{DD} = 3 V	2.1			V
Input Logic Low	V_{IL}	V_{DD} = 3 V			0.6	V
Input Current	I_{IL}	V_{IN} = 0 V or 5 V			±1	µA
Input Capacitance[6]	C_{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	$V_{DD\ RANGE}$		2.7		5.5	V
Supply Current	I_{DD}	V_{IH} = 5 V or V_{IL} = 0 V		3	8	µA
Power Dissipation[7]	P_{DISS}	V_{IH} = 5 V or V_{IL} = 0 V, V_{DD} = 5 V			40	µW
Power Supply Sensitivity	PSSR	V_{DD} = +5 V ± 10%, Code = Midscale		±0.01	±0.02	%/%
DYNAMIC CHARACTERISTICS[6, 8]						
Bandwidth –3 dB	BW	R_{AB} = 10 kΩ/50 kΩ/100 kΩ, Code = 0x40		600/100/40		kHz
Total Harmonic Distortion	THD_W	V_A =1 V rms, f = 1 kHz, R_{AB} = 10 kΩ		0.05		%
V_W Settling Time (10 kΩ/50 kΩ/100 kΩ)	t_S	V_A = 5 V ±1 LSB Error Band		2		µs
Resistor Noise Voltage Density	e_{N_WB}	R_{WB} = 5 kΩ, R_S = 0		9		nV/√Hz

[1] Typical specifications represent average readings at 25°C and V_{DD} = 5 V.
[2] Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic.
[3] $V_A = V_{DD}$, Wiper (V_W) = no connect.
[4] INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. $V_A = V_{DD}$ and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
[5] Resistor terminals A and W have no limitations on polarity with respect to each other.
[6] Guaranteed by design and not subject to production test.
[7] P_{DISS} is calculated from ($I_{DD} \times V_{DD}$). CMOS logic level inputs result in minimum power dissipation.
[8] All dynamic characteristics use V_{DD} = 5 V.

TIMING CHARACTERISTICS—5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ VERSIONS

Table 3. V_{DD} = 5 V ± 10% or 3 V ± 10%; $V_A = V_{DD}$; –40°C < T_A < +125°C; unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
I^2C INTERFACE TIMING CHARACTERISTICS[2, 3]						
(Specifications Apply to All Parts)						
SCL Clock Frequency	f_{SCL}				400	kHz
t_{BUF} Bus Free Time between STOP and START	t_1		1.3			µs
$t_{HD;STA}$ Hold Time (Repeated START)	t_2	After this period, the first clock pulse is generated.	0.6			µs
t_{LOW} Low Period of SCL Clock	t_3		1.3			µs
t_{HIGH} High Period of SCL Clock	t_4		0.6		50	µs
$t_{SU;STA}$ Setup Time for Repeated START Condition	t_5		0.6			µs
$t_{HD;DAT}$ Data Hold Time	t_6				0.9	µs
$t_{SU;DAT}$ Data Setup Time	t_7		100			ns
t_F Fall Time of Both SDA and SCL Signals	t_8				300	ns
t_R Rise Time of Both SDA and SCL Signals	t_9				300	ns
$t_{SU;STO}$ Setup Time for STOP Condition	t_{10}		0.6			µs

[1] Typical specifications represent average readings at 25°C and V_{DD} = 5 V.
[2] Guaranteed by design and not subject to production test.
[3] See timing diagrams (Figure 31, Figure 32, Figure 33) for locations of measured values.

ABSOLUTE MAXIMUM RATINGS

Table 4. T_A = 25°C, unless otherwise noted[1]

Parameter	Value
V_{DD} to GND	−0.3 V to +7 V
V_A, V_W to GND	V_{DD}
Terminal Current, Ax–Bx, Ax–Wx, Bx–Wx	
Pulsed[2]	±20 mA
Continuous	±5 mA
Digital Inputs and Output Voltage to GND	0 V to V_{DD} + 0.3 V
Operating Temperature Range	−40°C to +125°C
Maximum Junction Temperature (T_{JMAX})	150°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Thermal Resistance[3] θ_{JA}: SC70-6	340°C/W

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2] Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.

[3] Package power dissipation = $(T_{JMAX} - T_A)/\theta_{JA}$.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

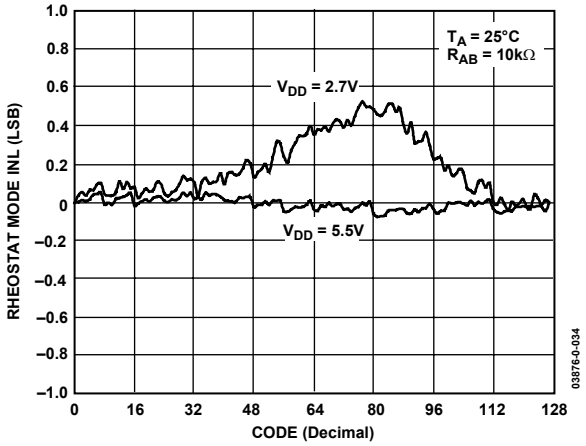

Figure 2. R-INL vs. Code vs. Supply Voltages

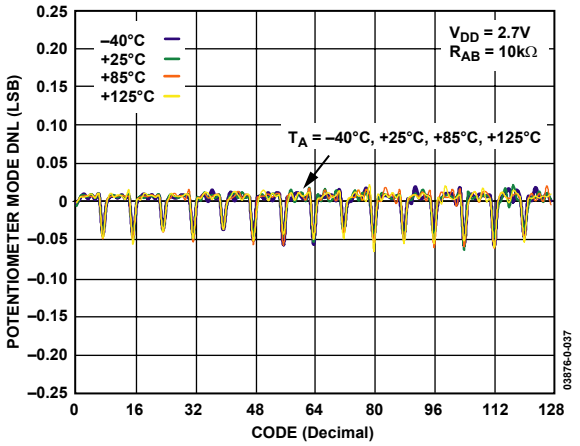

Figure 5. DNL vs. Code vs. Temperature

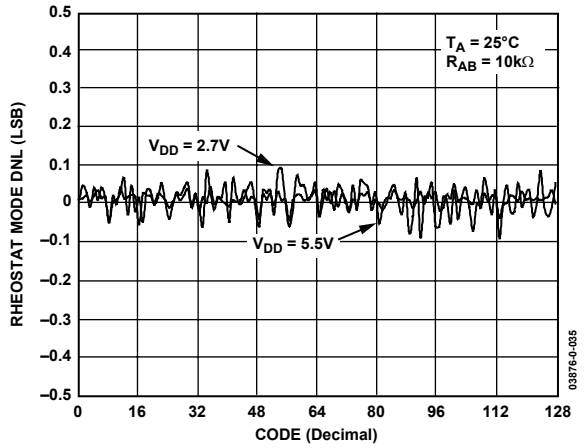

Figure 3. R-DNL vs. Code vs. Supply Voltages

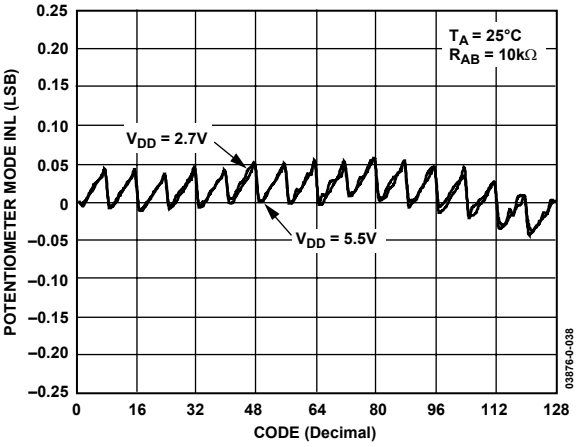

Figure 6. INL vs. Code vs. Supply Voltages

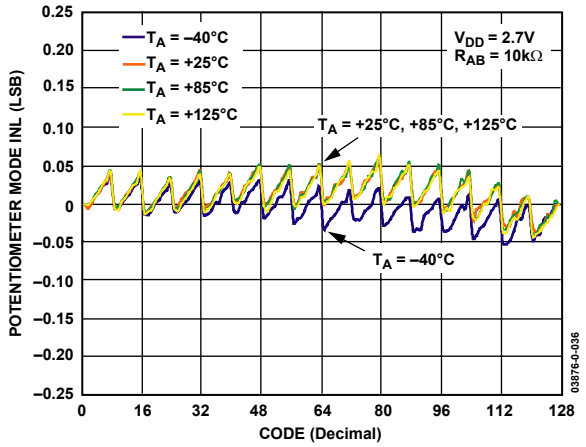

Figure 4. INL vs. Code vs. Temperature

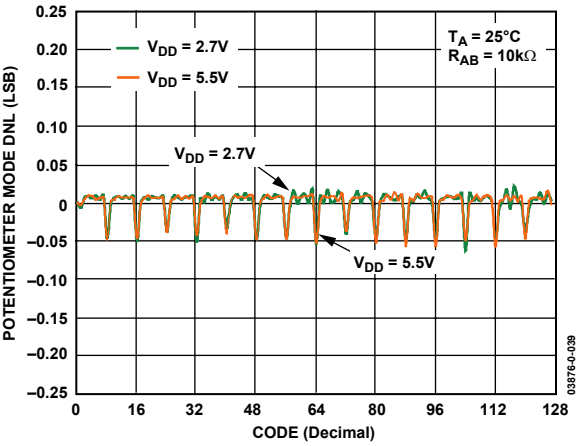

Figure 7. DNL vs. Code vs. Supply Voltages

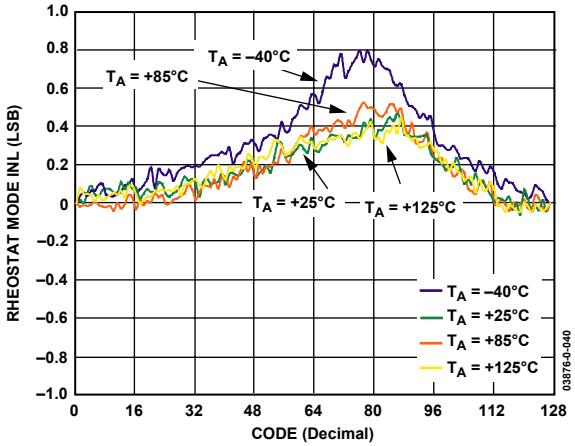

Figure 8. R-INL vs. Code vs. Temperature

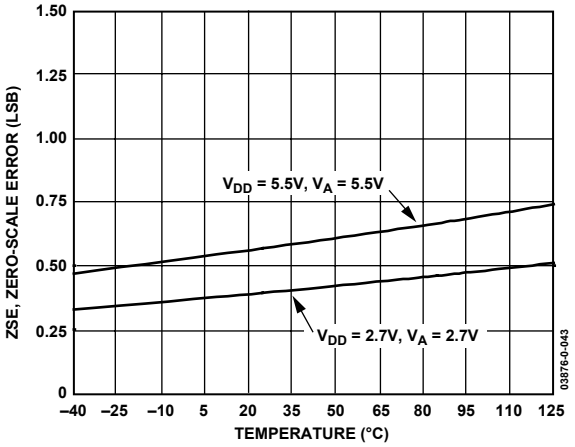

Figure 11. Zero-Scale Error vs. Temperature

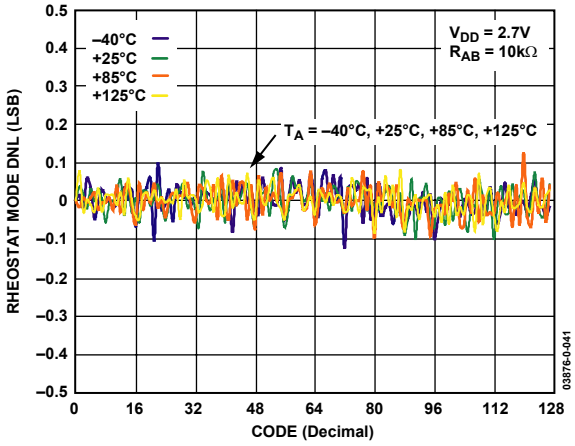

Figure 9. R-DNL vs. Code vs. Temperature

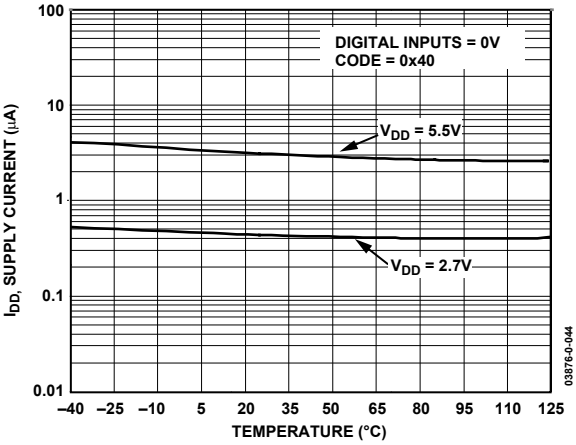

Figure 12. Supply Current vs. Temperature

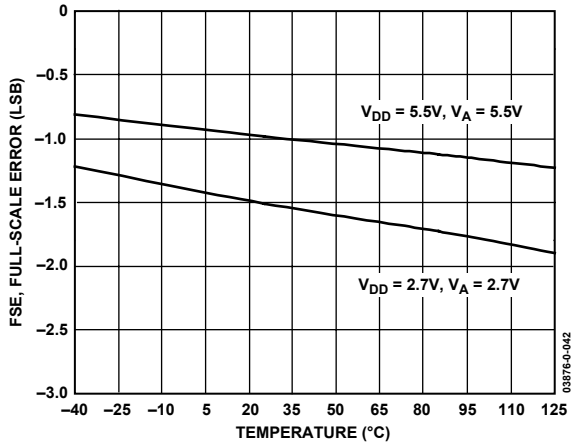

Figure 10. Full-Scale Error vs. Temperature

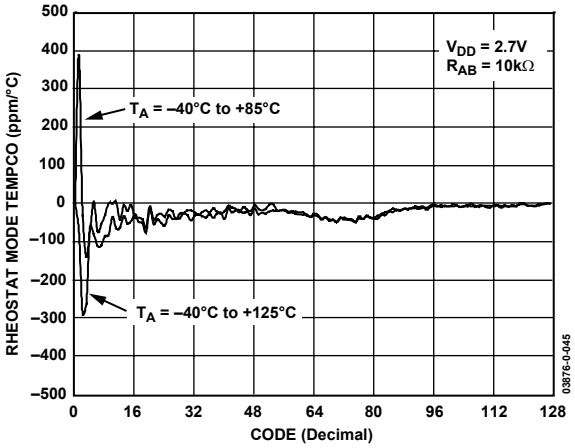

Figure 13. Rheostat Mode Tempco $\Delta R_{WB}/\Delta T$ vs. Code

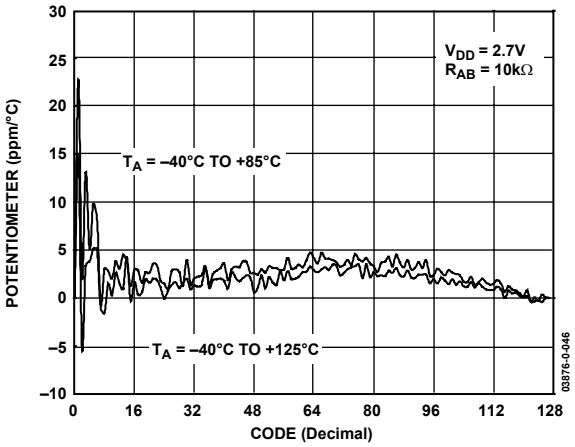

Figure 14. Potentiometer Mode Tempco $\Delta V_{WB}/\Delta T$ vs. Code

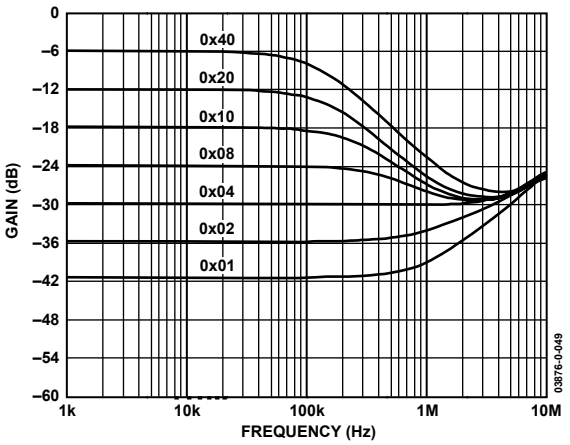

Figure 17. Gain vs. Frequency vs. Code, R_{AB} = 50 kΩ

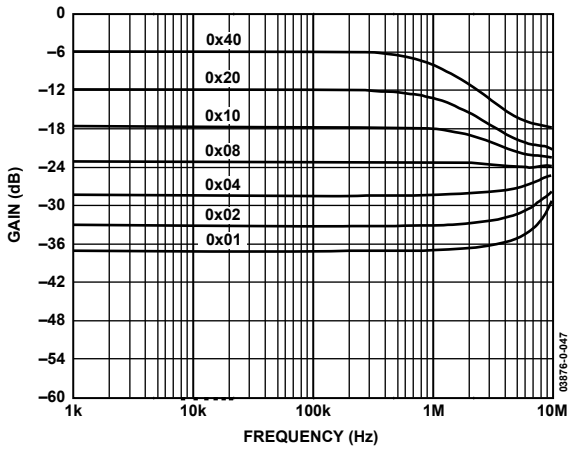

Figure 15. Gain vs. Frequency vs. Code, R_{AB} = 5 kΩ

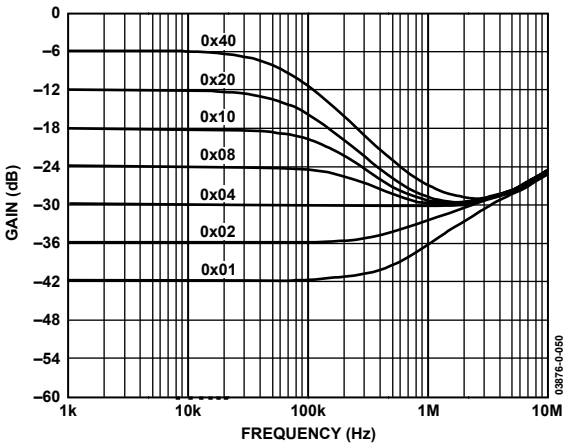

Figure 18. Gain vs. Frequency vs. Code, R_{AB} = 100 kΩ

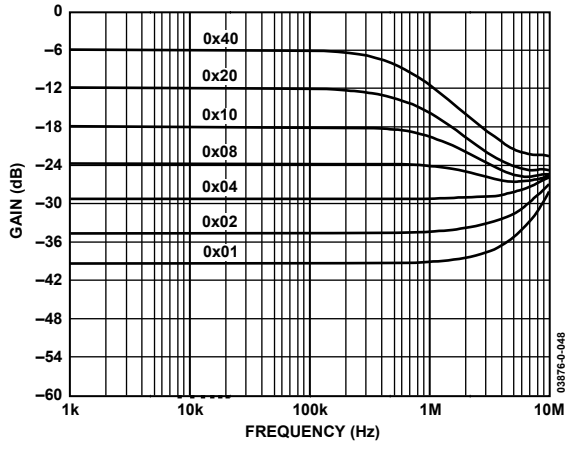

Figure 16. Gain vs. Frequency vs. Code, R_{AB} = 10 kΩ

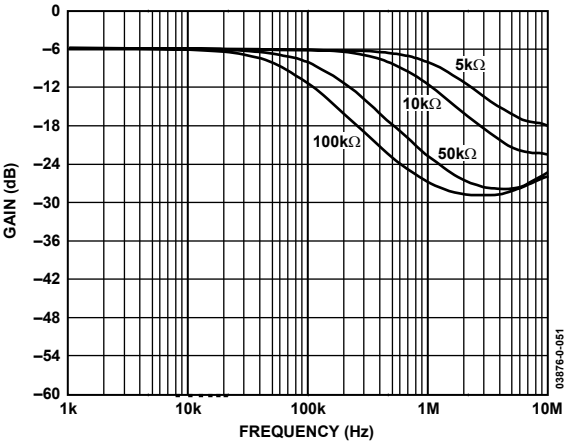

Figure 19. –3 dB Bandwidth @ Code = 0x80

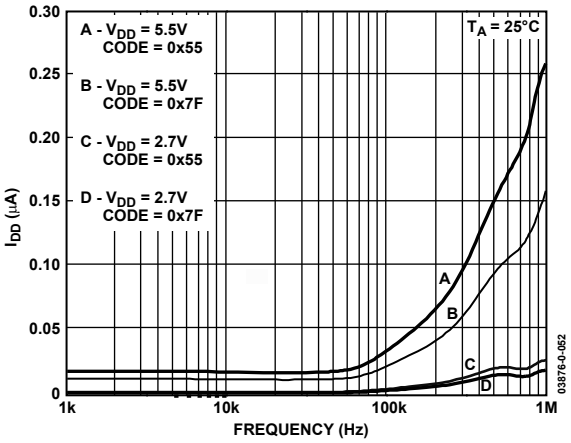

Figure 20. I_{DD} vs. Frequency

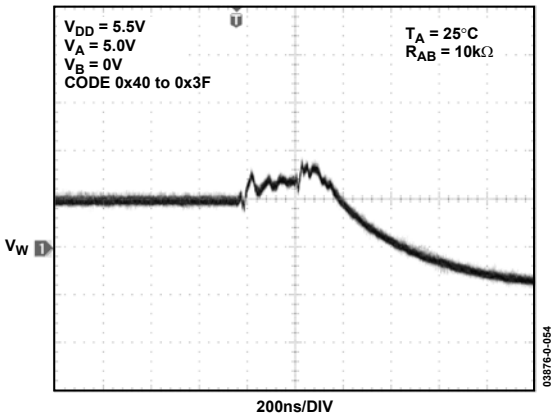

Figure 23. Midscale Glitch, Code 0x40 to 0x3F

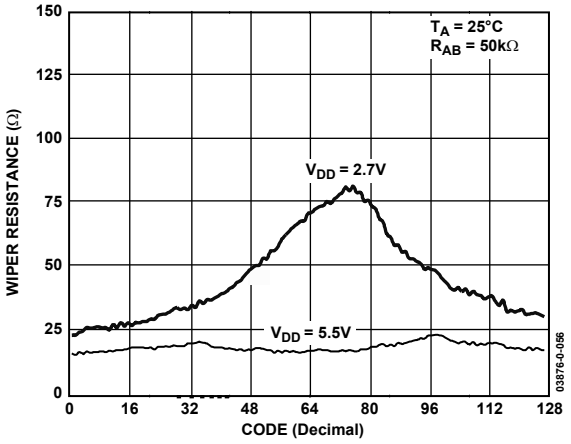

Figure 21. Wiper Resistance vs. Code vs. V_{DD}

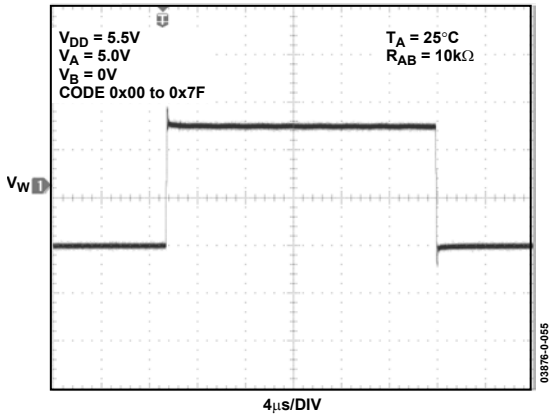

Figure 24. Large Signal Settling Time

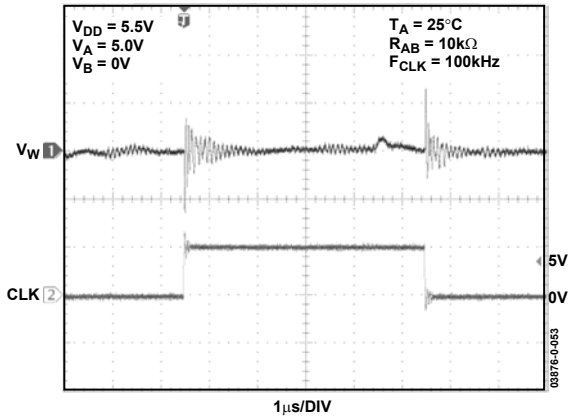

Figure 22. Digital Feedthrough

TEST CIRCUITS

Figure 25 to Figure 30 define the test conditions used in the product Specification tables.

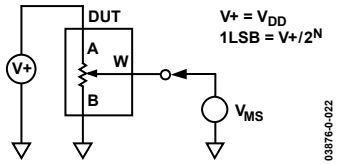

Figure 25. Test Circuit for Potentiometer Divider Nonlinearity Error (INL, DNL)

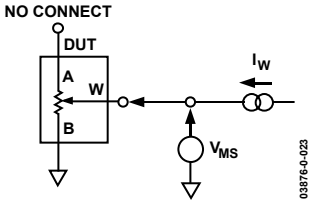

Figure 26. Test Circuit for Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)

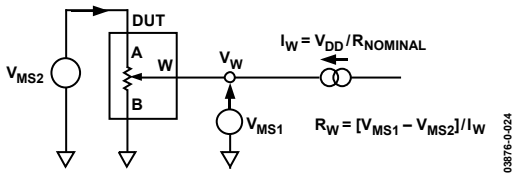

Figure 27. Test Circuit for Wiper Resistance

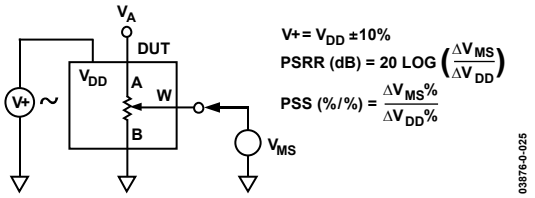

Figure 28. Test Circuit for Power Supply Sensitivity (PSS, PSSR)

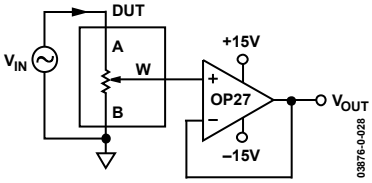

Figure 29. Test Circuit for Gain vs. Frequency

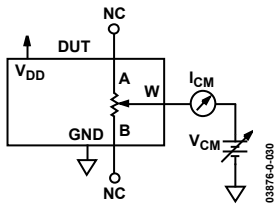

Figure 30. Test Circuit for Common-Mode Leakage Current

I²C INTERFACE

Table 5. Write Mode

S	0	1	0	1	1	1	0	$\overline{W}$	A	X	D6	D5	D4	D3	D2	D1	D0	A	P
	Slave Address Byte									Data Byte									

Table 6. Read Mode

S	0	1	0	1	1	1	0	R	A	0	D6	D5	D4	D3	D2	D1	D0	A	P
	Slave Address Byte									Data Byte									

S = Start Condition.

P = Stop Condition.

A = Acknowledge.

X = Don't Care.

$\overline{W}$ = Write.

R = Read.

D6, D5, D4, D3, D2, D1, D0 = Data Bits.

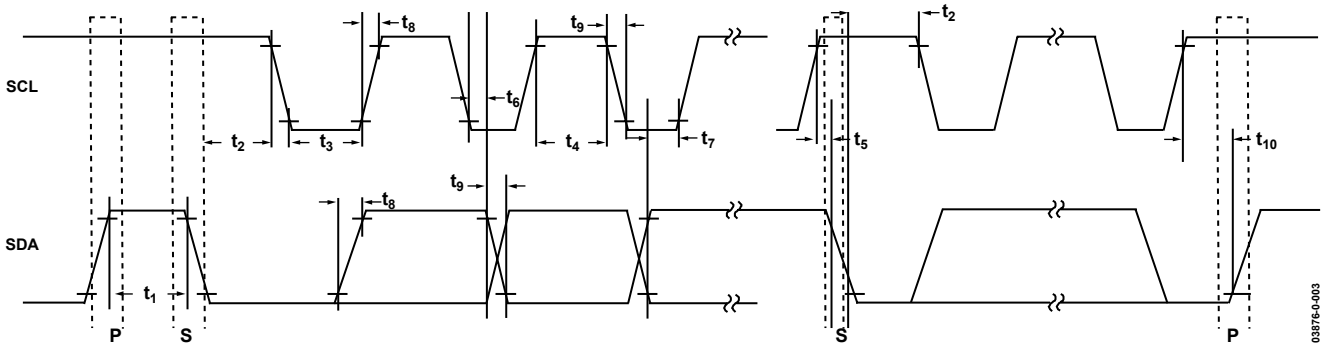

Figure 31. I²C Interface, Detailed Timing Diagram

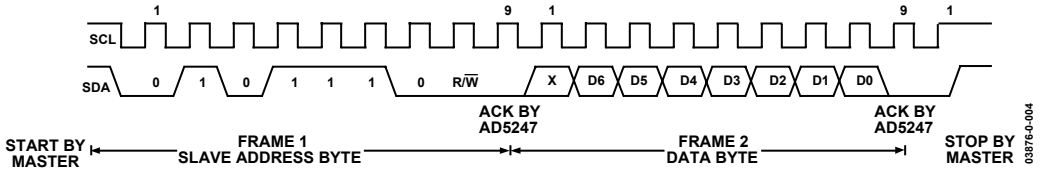

Figure 32. Writing to the RDAC Register

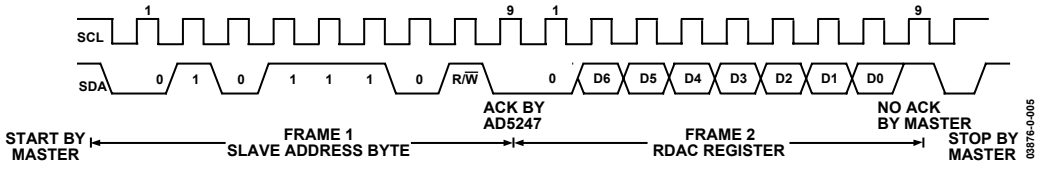

Figure 33. Reading from the RDAC Register

OPERATION

The AD5247 is a 128-position, digitally controlled variable resistor (VR) device. An internal power-on preset places the wiper at midscale during power-on, which simplifies the default condition recovery at power-up.

PROGRAMMING THE VARIABLE RESISTOR

Rheostat Operation

The nominal resistance of the RDAC between terminals A and B is available in 5 kΩ, 10 kΩ, 50 kΩ, and 100 kΩ. The final two or three digits of the part number determine the nominal resistance value, e.g., 10 kΩ = 10, 50 kΩ = 50. The nominal resistance (R_{AB}) of the VR has 128 contact points accessed by the wiper terminal, plus the B terminal contact. The 7-bit data in the RDAC latch is decoded to select one of the 128 possible settings.

Assuming a 10 kΩ part is used, the wiper's first connection starts at the B terminal for data 0x00. Since there is a 50 Ω wiper contact resistance, such a connection yields a minimum of 100 Ω (2 × 50 Ω) resistance between terminals W and B. The second connection is the first tap point, which corresponds to 178 Ω (R_{WB} = R_{AB}/128+ R_W = 78 Ω + 2 × 50 Ω) for data 0x01. The third connection is the next tap point, representing 256 Ω (2 × 78 Ω + 2 × 50 Ω) for data 0x02, and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at 10,100 Ω (R_{AB} + 2 × R_W).

Figure 34 shows a simplified diagram of the equivalent RDAC circuit where the last resistor string will not be accessed.

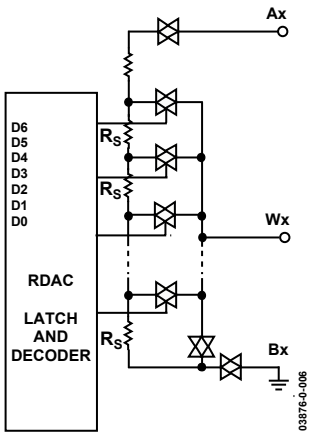

Figure 34. AD5247 Equivalent RDAC Circuit

The general equation determining the digitally programmed output resistance between W and B is

$$R_{WB}(D) = \frac{D}{128} \times R_{AB} + 2 \times R_W \quad (1)$$

where D is the decimal equivalent of the binary code loaded in the 7-bit RDAC register, R_{AB} is the end-to-end resistance, and R_W is the wiper resistance contributed by the on resistance of the internal switch. In summary, if R_{AB} = 10 kΩ and the A terminal is open-circuited, the output resistance R_{WB} shown in Table 7 will be set for the indicated RDAC latch codes.

Table 7. Codes and Corresponding R_{WB} Resistance

D (Dec.)	R_{WB} (Ω)	Output State
127	10,100	Full Scale (R_{AB} + 2 × R_W)
64	5,100	Midscale
1	178	1 LSB
0	100	Zero Scale (Wiper Contact Resistance)

Note that in the zero-scale condition, a finite resistance of 100 Ω between terminals W and B is present. Care should be taken to limit the current flow between W and B in this state to a maximum pulse current of no more than 20 mA. Otherwise, degradation or possible destruction of the internal switch contact can occur.

Similar to the mechanical potentiometer, the resistance of the RDAC between the wiper W and terminal A also produces a digitally controlled complementary resistance R_{WA}. When these terminals are used, the B terminal can be opened. Setting the resistance value for R_{WA} starts at a maximum value of resistance and decreases as the data loaded in the latch increases in value. The general equation for this operation is

$$R_{WA}(D) = \frac{128 - D}{128} \times R_{AB} + 2 \times R_W \quad (2)$$

For R_{AB} = 10 kΩ and the B terminal open circuited, the output resistance R_{WA} shown in Table 8 will be set for the indicated RDAC latch codes.

Table 8. Codes and Corresponding R_{WA} Resistance

D (Dec.)	R_{WA} (Ω)	Output State
127	178	Full Scale
64	5,100	Midscale
1	9,961	1 LSB
0	10,100	Zero Scale

Typical device-to-device matching is process lot dependent and may vary by up to ±30%. Since the resistance element is processed in thin film technology, the change in R_{AB} with temperature has a very low 45 ppm/°C temperature coefficient.

PROGRAMMING THE POTENTIOMETER DIVIDER

Voltage Output Operation

The digital potentiometer easily generates a voltage divider at wiper-to-B and wiper-to-A proportional to the input voltage at A-to-B. Unlike the polarity of V_{DD} to GND, which must be positive, voltage across A–B, W–A, and W–B can be at either polarity.

If ignoring the effect of the wiper resistance for approximation, connecting the A terminal to 5 V and the B terminal to ground produces an output voltage at the wiper-to-B starting at 0 V up to 1 LSB less than 5 V. Each LSB of voltage is equal to the voltage applied across terminal AB divided by the 128 positions of the potentiometer divider. The general equation defining the output voltage at V_W with respect to ground for any valid input voltage applied to terminals A and B is

$$V_W(D) = \frac{D}{128} V_A \quad (3)$$

For a more accurate calculation, which includes the effect of wiper resistance, V_W, can be found as

$$V_W(D) = \frac{R_{WB}(D)}{R_{AB}} V_A \quad (4)$$

Operation of the digital potentiometer in the divider mode results in a more accurate operation over temperature. Unlike in rheostat mode, the output voltage in divider mode is dependent mainly on the ratio of internal resistors R_{WA} and R_{WB} and not the absolute values. Therefore, the temperature drift reduces to 15 ppm/°C.

I²C COMPATIBLE 2-WIRE SERIAL BUS

The first byte of the AD5247 is a slave address byte (see Table 5 and Table 6). It has a 7-bit slave address and a R/$\overline{W}$ bit. The seven MSBs of the slave address are 0101110 followed by 0 for a write command or 1 to place the device in read mode.

The 2-wire I²C serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a START condition, which is when a high-to-low transition on the SDA line occurs while SCL is high (see Figure 32). The following byte is the slave address byte, which consists of the 7-bit slave address followed by an R/$\overline{W}$ bit (this bit determines whether data will be read from or written to the slave device).

   The slave whose address corresponds to the transmitted address responds by pulling the SDA line low during the ninth clock pulse (this is termed the acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to or read from its serial register. If the R/$\overline{W}$ bit is high, the master will read from the slave device. On the other hand, if the R/$\overline{W}$ bit is low, the master will write to the slave device.

2. In write mode, after acknowledgement of the slave address byte, the next byte is the data byte. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Table 5).

3. In read mode, after acknowledgment of the slave address byte, data is received over the serial bus in sequences of nine clock pulses (a slight difference from write mode, where eight data bits are followed by an acknowledge bit). Similarly, the transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Figure 33).

4. When all data bits have been read or written, a STOP condition is established by the master. A STOP condition is defined as a low-to-high transition on the SDA line while SCL is high. In write mode, the master will pull the SDA line high during the tenth clock pulse to establish a STOP condition (see Figure 32). In read mode, the master will issue a No Acknowledge for the ninth clock pulse (i.e., the SDA line remains high). The master will then bring the SDA line low before the tenth clock pulse, which goes high to establish a STOP condition (see Figure 33).

A repeated write function gives the user flexibility to update the RDAC output a number of times after addressing the part only once. For example, after the RDAC has acknowledged its slave address in the write mode, the RDAC output will update on each successive byte. If different instructions are needed, the write/read mode has to start again with a new slave address and data byte. Similarly, a repeated read function of the RDAC is also allowed.

LEVEL SHIFTING FOR BIDIRECTIONAL INTERFACE

While most legacy systems may be operated at one voltage, a new component may be optimized at another. When two systems operate the same signal at two different voltages, proper level shifting is needed. For instance, one can use a 3.3 V E²PROM to interface with a 5 V digital potentiometer. A level shifting scheme is needed to enable a bidirectional communication so that the setting of the digital potentiometer can be stored to and retrieved from the E²PROM. Figure 35 shows one of the implementations. M1 and M2 can be any N channel signal FETs, or if V_{DD} falls below 2.5 V, M1 and M2 can be low threshold FETs such as the FDV301N.

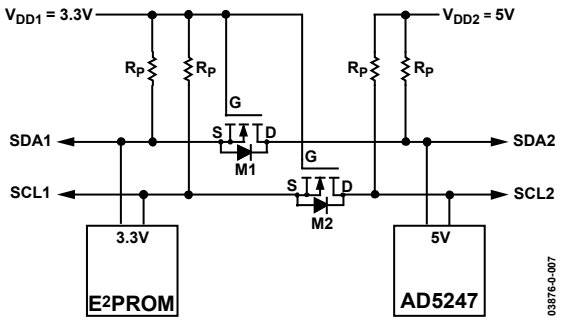

Figure 35. Level Shifting for Operation at Different Potentials

ESD PROTECTION

All digital inputs are protected with a series input resistor and parallel Zener ESD structures shown in Figure 36 and Figure 37. This applies to the digital input pins SDA and SCL.

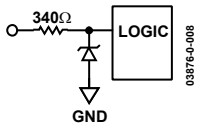

Figure 36. ESD Protection of Digital Pins

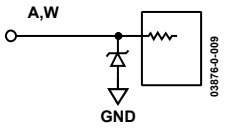

Figure 37. ESD Protection of Resistor Terminals

TERMINAL VOLTAGE OPERATING RANGE

The AD5247 V_{DD} and GND power supply defines the boundary conditions for proper 3-terminal digital potentiometer operation. Supply signals present on terminals A and W that exceed V_{DD} or GND will be clamped by the internal forward biased diodes (see Figure 38).

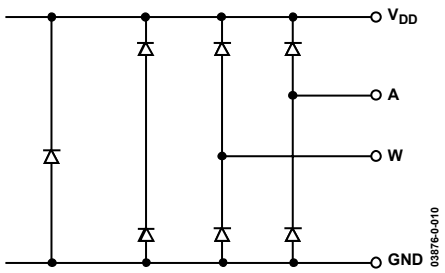

Figure 38. Maximum Terminal Voltages Set by V_{DD} and GND

MAXIMUM OPERATING CURRENT

At low code values, the user should be aware that due to low resistance values, the current through the RDAC may exceed the 5 mA limit. In Figure 39, a 5 V supply is placed on the wiper, and the current through terminals W and B is plotted with respect to code. A line is also drawn denoting the 5 mA current limit. Note that at low code values (particularly for the 5 kΩ and 10 kΩ options), the current level increases significantly. Care should be taken to limit the current flow between W and B in this state to a maximum continuous current of 5 mA and a maximum pulse current of no more than 20 mA. Otherwise, degradation or possible destruction of the internal switch contacts can occur.

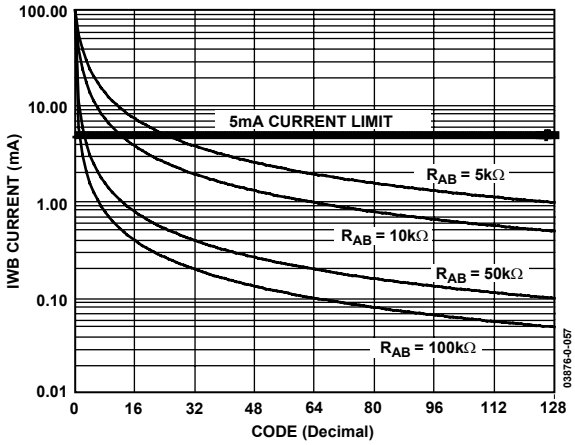

Figure 39. Maximum Operating Current

POWER-UP SEQUENCE

Since the ESD protection diodes limit the voltage compliance at terminals A and W (see Figure 38), it is important to power V_{DD}/GND before applying any voltage to terminals A and W; otherwise, the diode will be forward biased such that V_{DD} will be powered unintentionally and may affect the rest of the user's circuit. The ideal power-up sequence is in the following order: GND, V_{DD}, digital inputs, and then V_A/V_W. The relative order of powering V_A and V_W and the digital inputs is not important as long as they are powered after V_{DD}/GND.

LAYOUT AND POWER SUPPLY BYPASSING

It is a good practice to employ a compact, minimum lead-length layout design. The leads to the inputs should be as direct as possible with a minimum conductor length. Ground paths should have low resistance and low inductance.

Similarly, it is a good practice to bypass the power supplies with quality capacitors for optimum stability. Supply leads to the device should be bypassed with 0.01 µF to 0.1 µF disc or chip ceramic capacitors. Low ESR 1 µF to 10 µF tantalum or electrolytic capacitors should also be applied at the supplies to minimize any transient disturbance and low frequency ripple (see Figure 40). Note that the digital ground should also be joined remotely to the analog ground at one point to minimize the ground bounce.

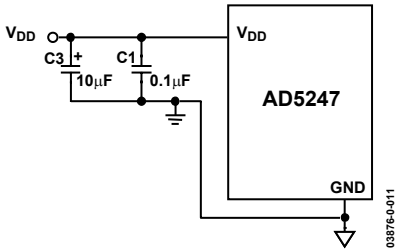

Figure 40. Power Supply Bypassing

CONSTANT BIAS TO RETAIN RESISTANCE SETTING

For users who desire nonvolatility but cannot justify the additional cost for the EEMEM, the AD5247 may be considered as a low cost alternative by maintaining a constant bias to retain the wiper setting. The AD5247 was designed specifically with low power in mind, which allows low power consumption even in battery-operated systems. The graph in Figure 41 demonstrates the power consumption from a 3.4 V 450 mAhr Li-ion cell phone battery, which is connected to the AD5247. The measurement over time shows that the device draws approximately 1.3 µA and consumes negligible power. Over a course of 30 days, the battery was depleted by less than 2%, the majority of which is due to the intrinsic leakage current of the battery itself.

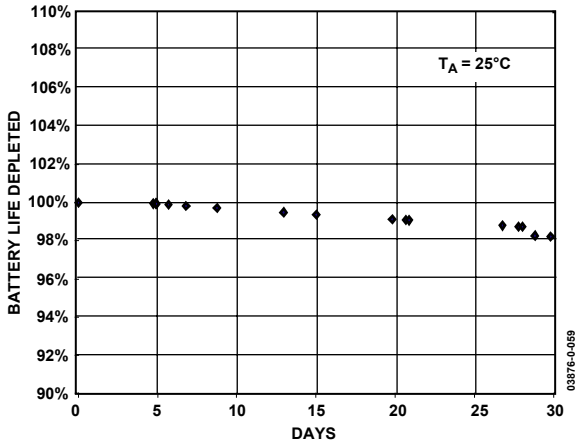

Figure 41. Battery Operating Life Depletion

This demonstrates that constantly biasing the pot is not an impractical approach. Most portable devices do not require the removal of batteries for the purpose of charging. Although the resistance setting of the AD5247 will be lost when the battery needs replacement, such events occur rather infrequently such that this inconvenience is justified by the lower cost and smaller size offered by the AD5247. If and when total power is lost, the user should be provided with a means to adjust the setting accordingly.

EVALUATION BOARD

An evaluation board, along with all necessary software, is available to program the AD5247 from any PC running Windows® 98, Windows 2000®, or Windows XP®. The graphical user interface, as shown in Figure 42, is straightforward and easy to use. More detailed information is available in the user manual, which comes with the board.

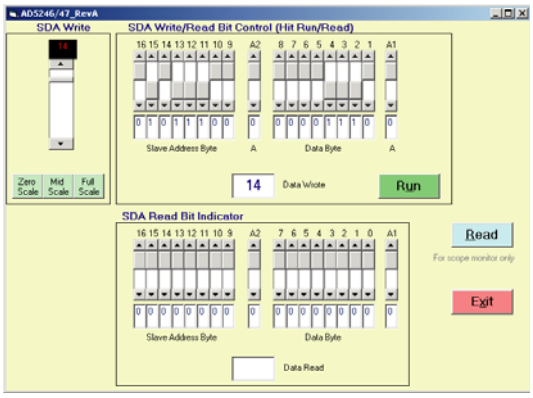

Figure 42. AD5247 Evaluation Board Software

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

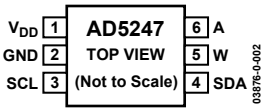

Figure 43. Pin Configuration (6-Lead SC70)

Table 9. AD5247 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD}	Positive Power Supply.
2	GND	Digital Ground and B Termination Voltage.
3	SCL	Serial Clock Input. Positive edge triggered.
4	SDA	Serial Data Input/Output.
5	W	W Terminal.
6	A	A Terminal.

OUTLINE DIMENSIONS

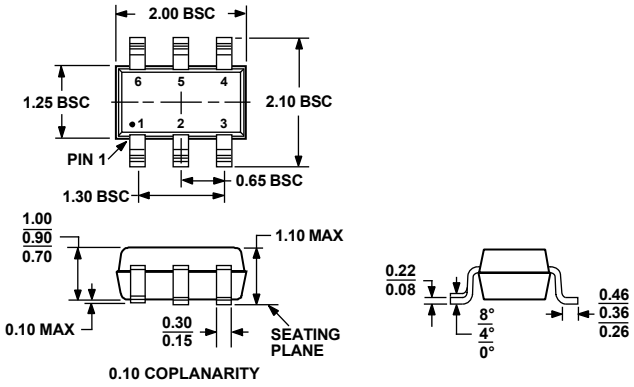

Figure 44. 6-Lead Thin Shrink Small Outline Transistor [SC70]
(KS-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model	R_{AB} (kΩ)	Temperature Range	Package Description	Package Option	Branding
AD5247BKS5-R2	5	–40°C to +125°C	6-lead SC70	KS-6	D1E
AD5247BKS5-RL7	5	–40°C to +125°C	6-lead SC70	KS-6	D1E
AD5247BKS10-R2	10	–40°C to +125°C	6-lead SC70	KS-6	D19
AD5247BKS10-RL7	10	–40°C to +125°C	6-lead SC70	KS-6	D19
AD5247BKS50-R2	50	–40°C to +125°C	6-lead SC70	KS-6	D18
AD5247BKS50-RL7	50	–40°C to +125°C	6-lead SC70	KS-6	D18
AD5247BKS100-R2	100	–40°C to +125°C	6-lead SC70	KS-6	D17
AD5247BKS100-RL7	100	–40°C to +125°C	6-lead SC70	KS-6	D17
AD5247EVAL	See Note 1		Evaluation Board		

[1] The evaluation board is shipped with the 10 kΩ R_{AB} resistor option; however, the board is compatible with all available resistor value options.

NOTES

NOTES

Purchase of licensed I²C components of Analog Devices or one of its sublicensed Associated Companies conveys a license for the purchaser under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

C03876–0–9/03(0)

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