CDMA Power Management System

ADP3502

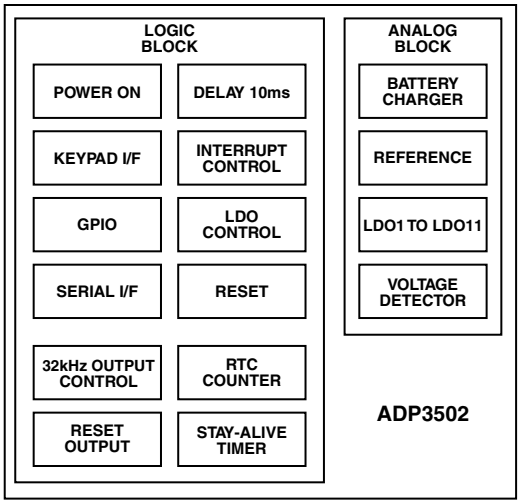
FEATURES

11 LDOs Optimized for Specific CDMA Subsystems
4 Backup LDOs for Standby Mode Operation
Ultra Low Standby Supply Current
High Accuracy Battery Charger (0.7%)
3 Li-Ion Battery Charge Modes
5 mA Precharge
Low Current Charge
Full Current Charge
Integrated RTC
Ambient Temperature: –30°C to +85°C
64-Lead 7 mm × 7 mm × 1 mm TQFP Package

APPLICATIONS

CDMA/CDMA2000/PCS Handsets

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADP3502 is a multifunction chip optimized for CDMA-1x cell phone power management. It offers a total power solution for the handset baseband and RF section, including LDOs to power 11 subsystems. Also integrated are a real-time clock (RTC), serial bus interface, and charging control for Li-Ion/Li-Polymer batteries. Sophisticated controls are available for power-up during battery charging, keypad interface, GPIO/INT function, and RTC function.

The ADP3502 is optimized for CDMA handsets powered by single-cell Li-Ion batteries. Its high level of integration significantly reduces the design effort, number of discrete components, and solution size/cost. The main-sub LDO structure reduces the standby current consumption, and as a result, greatly extends the standby time of the phone. System operation has been proven to be fully compatible with MSM51xx-based designs.

The ADP3502 comes in a 64-lead 7 mm × 7 mm × 1 mm TQFP package and is specified over a wide temperature range of –30°C to +85°C.

REV. 0

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ADP3502–SPECIFICATIONS

MAIN FUNCTIONS (T_A = –30°C to +85°C, C_{VBAT} = 1 μF MLCC, VBAT = 3.6 V, unless otherwise noted. See Table II for C_{OUT}.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SHUTDOWN GND CURRENT Power OFF	IGND	T_A = –20°C to +60°C LDO3b: ON, Connect to RTCV through Schottky Diode RTC/32K OSC: Active All Other LDOs: OFF All Logic Inputs: VBAT or GND MVBAT: OFF		25	45	μA
OPERATING GND CURRENT Standby Mode Operation (Light Load)	IGND	LDO1b, LDO2b, LDO3b, LDO6b: ON I_O = 1 mA for LDO3b and LDO6b I_O = 3 mA for LDO1b I_O = 300 μA for LDO2b All Other LDOs: OFF RTC/32K OSC: Active MVBAT: OFF All Logic Output: No Load		60	125	μA
Standby Mode Operation (Midload)		LDO1, LDO2, LDO3, LDO6, All Sub-LDOs: ON, I_O = 70% Load All Other LDOs: OFF RTC/32K OSC: Active MVBAT: ON All Logic Outputs: No Load		300		μA
Active Operation		LDO5: OFF All Other LDOs: ON, 70% Load RTC/32K OSC: Active All Logic Outputs: No Load MVBAT: ON		700		μA
THERMAL SHUTDOWN THRESHOLD				160		°C
THERMAL SHUTDOWN HYSTERESIS				35		°C
ADAPTER/ADPSUPPLY VOLTAGE RANGE	VADP		5		12	V
VBAT VOLTAGE RANGE	VBAT		3.3		5.5	V

LDO SPECIFICATIONS (T_A = 25°C, C_{VBAT} = 1 μF MLCC, VBAT = V_{OUT} + 1 V, NRCAP = 0.1 μF. See Table II for C_{OUT}.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
BASEBAND VDD MAIN-LDO (LDO1a)						
Output Voltage	V_{LDO1a}	I_O = 1 mA to 150 mA T_A = –30°C to +85°C	2.81	2.90	2.99	V
Output Capacitor Required for Stability	C_{LDO1a}		2.2			μF
Dropout Voltage	V_{DO}	I_O = 150 mA		200		mV
Start-Up Time from Shutdown				250		μs
BASEBAND VDD SUB-LDO (LDO1b)						
Output Voltage	V_{LDO1b}	I_O = 3 mA T_A = –30°C to +85°C	2.8	2.87	3.0	V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
BASEBAND AVDD MAIN-LDO (LDO2a)						
Output Voltage	V_{LDO2a}	16 Steps, 20 mV/Step, I_O = 50 mA				
		Code: 1000	2.30	2.36	2.43	V
		Code: 0111	2.60	2.66	2.74	V
		T_A = 25°C				
Output Default Voltage	V_{LDO2a}	I_O = 50 mA, T_A = 25°C	2.46	2.52	2.6	V
Output Voltage	V_{LDO2a}	16 Steps, 20 mV/Step, I_O = 50 mA				
		Code: 1000	2.29	2.36	2.47	V
		Code: 0111	2.57	2.66	2.81	V
		T_A = –30°C to +85°C				
Output Default Voltage	V_{LDO2a}	I_O = 50 mA, T_A = –30°C to +85°C	2.42	2.52	2.66	V
Output Capacitor Required for Stability	C_{LDO2a}		1			µF
Dropout Voltage	V_{DO}	I_O = 50 mA		210		mV
Ripple Rejection		f = 1 kHz		60		dB
Output Noise Voltage	V_{NOISE}	f = 100 Hz to 100 kHz		120		µV rms
Start-Up Time from Shutdown				250		µs
BASEBAND AVDD SUB-LDO (LDO2b)						
Output Voltage	V_{LDO2b}	I_O = 300 µA, $V_{LDO2MAIN}$ = 2.6 V T_A = –30°C to +85°C	2.50	2.57	2.70	V
REFO SWITCH						
On Resistance	R_{ON}	T_A = –30°C to +85°C, I_O = 500 µA		50	130	Ω
Off Leak	I_{LEAK}	LDO2: ON, Switch: OFF		0.01	1	µA
COIN CELL MAIN-LDO (LDO3a)						
Output Voltage	V_{LDO3a}	I_O = 1 mA to 50 mA T_A = –30°C to +85°C	2.90	3.0	3.09	V
Dropout Voltage	V_{DO}	I_O = 50 mA		140		mV
Output Capacitor Required for Stability	C_{LDO3a}		1			µF
Start-Up Time from Shutdown				250		µs
COIN CELL SUB-LDO (LDO3b)						
Output Voltage	V_{LDO3b}	I_O = 1 mA T_A = –30°C to +85°C	2.85	2.97	3.15	V
AUDIO LDO (LDO4)						
Output Voltage	V_{LDO4}	I_O = 1 mA to 180 mA T_A = –30°C to +85°C	2.81	2.9	2.99	V
Output Capacitor Required for Stability	C_{LDO4}		2.2			µF
Dropout Voltage	V_{DO}	I_O = 180 mA		200		mV
Ripple Rejection		f = 1 kHz		60		dB
Output Noise Voltage	V_{NOISE}	f = 100 Hz to 10 kHz		50		µV rms
Start-Up Time from Shutdown				250		µs
VIBRATOR LDO (LDO5)						
Output Voltage	V_{LDO5}	I_O = 1 mA to 150 mA T_A = –30°C to +85°C	2.75	2.9	3.05	V
Dropout Voltage	V_{DO}	I_O = 150 mA		200		mV
Output Capacitor Required for Stability	C_{LDO5}		2.2			µF
BASEBAND CORE MAIN-LDO (LDO6a)						
Output Voltage	V_{LDO6a}	I_O = 1 mA to 150 mA T_A = –30°C to +85°C	2.75	2.85	2.95	V
Output Capacitor Required for Stability	C_{LDO6a}		2.2			µF
Dropout Voltage	V_{DO}	I_O = 150 mA		200		mV
Start-Up Time from Shutdown				250		µs

LDO SPECIFICATIONS (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
BASEBAND CORE SUB-LDO (LDO6b)						
Output Voltage	V_{LDO6b}	I_O = 1 mA T_A = –30°C to +85°C	2.70	2.80	2.90	V
RF RX1 LDO (LDO7)						
Output Voltage	V_{LDO7}	I_O = 1 mA to 100 mA T_A = –30°C to +85°C	2.81	2.9	2.99	V
Output Capacitor Required for Stability	C_{LDO7}		1.5			µF
Dropout Voltage	V_{DO}	I_O = 100 mA		200		mV
Ripple Rejection		f = 1 kHz		60		dB
Output Noise Voltage	V_{NOISE}	f = 100 Hz to 100 kHz		40		µV rms
Start-Up Time from Shutdown				250		µs
RF TX LDO (LDO8)						
Output Voltage	V_{LDO8}	I_O = 1 mA to 150 mA T_A = –30°C to +85°C	2.81	2.9	2.99	V
Output Capacitor Required for Stability	C_{LDO8}		2.2			µF
Dropout Voltage	V_{DO}	I_O = 150 mA		200		mV
Ripple Rejection		f = 1 kHz		60		dB
Output Noise Voltage	V_{NOISE}	f = 100 Hz to 100 kHz		40		µV rms
Start-Up Time from Shutdown				250		µs
RF RX2 LDO (LDO9)						
Output Voltage	V_{LDO9}	I_O = 1 mA to 50 mA T_A = –30°C to +85°C	2.81	2.9	2.99	V
Output Capacitor Required for Stability	C_{LDO9}		1			µF
Dropout Voltage	V_{DO}	I_O = 50 mA		150		mV
Ripple Rejection		f = 1 kHz		60		dB
Output Noise Voltage	V_{NOISE}	f = 100 Hz to 100 kHz		40		µV rms
Start-Up Time from Shutdown				250		µs
RF OPTIONAL LDO (LDO10)						
Output Voltage	V_{LDO10}	I_O = 1 mA to 50 mA T_A = –30°C to +85°C	2.81	2.9	2.99	V
Output Capacitor Required for Stability	C_{LDO10}		1			µF
Dropout Voltage	V_{DO}	I_O = 50 mA		150		mV
Ripple Rejection		f = 1 kHz		60		dB
Output Noise Voltage	V_{NOISE}	f = 100 Hz to 100 kHz		40		µV rms
Start-Up Time from Shutdown				250		µs
OPTIONAL LDO (LDO11)						
Output Voltage	V_{LDO11}	I_O = 1 mA to 100 mA T_A = –30°C to +85°C	1.42	1.5	1.58	V
Output Capacitor Required for Stability	C_{LDO11}		2.2			µF
Ripple Rejection		f = 1 kHz		60		dB
Output Noise Voltage	V_{NOISE}	f = 100 Hz to 100 kHz		50		µV rms
Start-Up Time from Shutdown				250		µs
VOLTAGE DETECTOR FOR LDO1 AND LDO6						
LDO1 Detect Voltage	V_{DET1}	T_A = –30°C to +85°C	2.7	2.72		V
LDO1 Release Voltage	V_{DET1}	T_A = –30°C to +85°C		2.77	$V_{LDO1–NOM}$	V
LDO1 Hysteresis	V_{HYS1}	T_A = –30°C to +85°C	35	52		mV
LDO6 Detect Voltage	V_{DET6}	T_A = –30°C to +85°C	2.50	2.58		V
LDO6 Release Voltage	V_{DET6}	T_A = –30°C to +85°C		2.67	$V_{LDO6–NOM}$	V
LDO6 Hysteresis	V_{HYS6}	T_A = –30°C to +85°C	45	90		mV

BATTERY VOLTAGE DIVIDER: MVBAT

(T_A = –30°C to +85°C, C_{VBAT} = 10 μF MLCC, $C_{ADAPTER}$ = 1 μF MLCC, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
MVBAT OUTPUT VOLTAGE 5-Bit Programmable	V_{MVBAT}	VBAT = 4.35 V, MVEN = 1 T_A = 25°C Code: 10000 Code: 01111	 2.459 2.648	 2.508 2.697	 2.538 2.732	 V V
MVBAT OUTPUT VOLTAGE STEP	V_{STEP}	VBAT = 4.35 V, MVEN = 1		6		mV/LSB
OUTPUT DRIVE CURRENT CAPABILITY	I_{OUT}		1	2		mA
MVBAT LOAD REGULATION	ΔMVBAT	0 < I_{OUT} < 100 μA		3	5	mV
OPERATING BATTERY CURRENT		VBAT = 4.35 V, MVEN = 1		78	97	μA
SHUTDOWN CURRENT		VBAT = 4.35 V, MVEN = 0			1	μA

BATTERY CHARGER

(T_A = –30°C to +85°C, C_{VBAT} = 10 μF MLCC, $C_{ADAPTER}$ = 1 μF MLCC, 4.0 V ≤ ADAPTER ≤ 12 V, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
CHARGER CONTROL VOLTAGE RANGE 2-Bit Programmable	VBAT SENSE	T_A = 25°C V_{R_SENSE} = 30 mV, CHI = 1 4.8 V ≤ ADAPTER ≤ 12 V Code: 00 (Default) Code: 01 Code: 10 Code: 11	 3.440 4.175 4.195 4.215	 3.500 4.205 4.225 4.245	 3.560 4.235 4.255 4.275	 V V V V
CHARGER CONTROL VOLTAGE RANGE[1] 2-Bit Programmable	VBAT SENSE	T_A = –20°C to +55°C V_{R_SENSE} = 160 mV, CHI = 1 4.8 V ≤ ADAPTER ≤ 12 V (Note 1) Code: 00 (Default) Code: 01 Code: 10 Code: 11	 3.440 4.155 4.175 4.195	 3.500 4.205 4.225 4.245	 3.560 4.255 4.275 4.295	 V V V V
CHARGER VOLTAGE TEMPERATURE DRIFT[1]		+25°C to +55°C or +25°C to –20°C V_{R_SENSE} = 30 mV, Constant Adapter Voltage between 4.8 V and 12 V	–20		+20	mV
CHARGER DETECT ON THRESHOLD	ADAPTER-VBAT		110	165	225	mV
CHARGER DETECT OFF THRESHOLD	ADAPTER-VBAT		0	25	60	mV
CHARGER SUPPLY CURRENT	$I_{ADAPTER}$	ADAPTER = 5 V, VBAT = 4.3 V			2	mA
CURRENT LIMIT THRESHOLD High Current Limit (Full Charge Current Enabled) Low Current Limit (Full Charge Current Disabled)	ADAPTER-V_{ISNS}	ADAPTER = 5 V VBAT = 3.6 V VBAT = 3.0 V	 170 40	 210 60	 255 75	 mV mV
PRECHARGE CURRENT SOURCE		VBAT ≤ DDLO	3	5	7	mA
BASE PIN DRIVE CURRENT			20	35		mA
DEEP DISCHARGE LOCK-OUT (Releasing Voltage)	DDLO	VBAT< DDLO, T_A = 25°C, (5 mA Precharge), VBAT Ramping Up		2.650	2.80	V
DEEP DISCHARGE LOCK-OUT HYSTERESIS[2]			100	200		mV
ISENSE BIAS CURRENT	I_{ISNS}	V_{ISNS} = 5 V			1	μA

BATTERY CHARGER (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
CHARGE TRANSISTOR REVERSE LEAKAGE CURRENT[3]	$I_{CHG} - I_{LKG}$	No Adapter Present			1	µA
MINIMUM LOAD FOR STABILITY[1]	I_L	CBAT = 10 µF MLCC, No Battery			10	mA

NOTES
[1]Guaranteed but not tested.
[2]DDLO hysteresis is dependent on DDLO threshold value. If DDLO threshold is at maximum, DDLO hysteresis is at maximum at the same time.
[3]This includes the total reverse current from battery to BVS, BASE, ISENSE, and ADAPTER pins with no adapter present. No signal path between ADAPTER pin and ADPSUPPLY pin.

Specifications subject to change without notice.

LOGIC DC SPECIFICATIONS (T_A = 25°C, C_{VBAT} = 1 µF MLCC, VBAT = 3.6 V, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
CS, CLKIN, RESETIN–, TCXOON, SLEEP–						
Input Current H/L	I_{IL}/I_{IH}	V_{IN} = V_{LDO1} or 0 V	–1		+1	µA
Input High Voltage	V_{IH}		2.25			V
Input Low Voltage	V_{IL}				0.5	V
Hysteresis				520		mV
KEYPADROW (Internal 20 kΩ Pull-Up)						
Input High Voltage	V_{IH}		2.25			V
Input Low Voltage	V_{IL}				0.5	V
Hysteresis				470		mV
GPIO, DATA						
Input Current H/L	I_{IL}/I_{IH}	V_{IN} = V_{LDO1} or 0 V	–1		+1	µA
Input High Voltage	V_{IH}		2.25			V
Input Low Voltage	V_{IL}				0.5	V
Hysteresis				260		mV
Output High Voltage	V_{OH}	I_{OH} = 400 µA	2.69			V
Output Low Voltage	V_{OL}	I_{OL} = –1.8 mA			0.28	V
INT–						
Output High Voltage	V_{OH}	I_{OH} = 400 µA	2.69			V
Output Low Voltage	V_{OL}	I_{OL} = –1.8 mA			0.28	V
BLIGHT (Open-Drain Output)						
Output Low Voltage	V_{OL}	I_{OL} = –100 mA			0.4	V
KEYPADCOL (Open-Drain Output)						
Output Low Voltage	V_{OL}	I_{OL} = –1.8 mA			0.15	V
PWRONKEY–, OPT1 (Internal 140 kΩ Pull-Up)						
Input High Voltage	V_{IH}		0.8 × VBAT			V
Input Low Voltage	V_{IL}				0.2 × VBAT	V
Hysteresis	V_{HYS}			950		mV
OPT2– (Input/Open-Drain Output)						
Input Current H	I_{IH}	V_{IN} = VBAT			1	µA
Input High Voltage	V_{IH}		0.8 × VBAT			V
Input Low Voltage	V_{IL}				0.2 × VBAT	V
Hysteresis	V_{HYS}	I_{OL} = –1.8 mA		950		mV
Output Low Voltage	V_{OL}				0.1 × VBAT	V

LOGIC (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OPT3						
Input Current H/L	I_{IL}/I_{IH}	V_{IN} = VBAT or 0 V	–1		+1	µA
Input High Voltage	V_{IH}		0.7 × VBAT			V
Input Low Voltage	V_{IL}				0.2 × VBAT	V
Hysteresis	V_{HYS}			300		mV
32K OUT						
Output High Voltage	V_{OH}	I_{OH} = 400 mA	0.9 × RTCV			V
Output Low Voltage	V_{OL}	I_{OL} = –1.8 mA			0.1 × RTCV	V
RESET+ (Open-Drain Output)						
Output Low Voltage	V_{OL}	I_{OL} = –1.8 mA			0.28	V
OFF Leak	OFF_{LEAK}			0.005	1	µA
RSTDELAY–, RESETOUT– (Open-Drain Output)						
Output Low Voltage	V_{OL}	I_{OL} = –1.8 mA			0.28	V
SUPPLY CURRENT OR RTCV	I_{OSC}	RTCV = 3 V, VBAT = 2 V All Logic: No Load		1		µA

AC SPECIFICATIONS (All specifications include temperature, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OPERATIONAL SUPPLY RANGE	RTCV		2		3.1	V
OSCILLATOR FREQUENCY	F_{CLK}			32.768		kHz
START-UP TIME	t_{START}	RTCV = 0 V to 3 V		100	200	ms
FREQUENCY JITTER	f_{JITTER}/SEC	RTCV = 3 V, T_A = 25°C				
Cycle to Cycle				40		ns
>100 Cycles				50		ns
FREQUENCY DEVIATION		RTCV = 3 V, 3 Minutes		1000		ppm

SERIAL INTERFACE

Parameter	Min	Typ	Max	Unit	Test Condition/Comments
t_{CKS}	50			ns	CLK Setup Time
t_{CSS}	50			ns	CS Setup Time
t_{CKH}	100			ns	CLK High Duration
t_{CKL}	100			ns	CLK Low Duration
t_{CSH}	100			ns	CS Hold Time
t_{CSR}	62			µs	CS Recovery Time
t_{DS}	50			ns	Input Data Setup Time
t_{DH}	40			ns	Input Data Hold Time
t_{RD}			50	ns	Data Output Delay Time
t_{RZ}			50	ns	Data Output Floating Time
t_{CSZ}			50	ns	Data Output Floating Time after CS Goes Low

ABSOLUTE MAXIMUM RATINGS*

Voltage on ADAPTER, ADPSUPPLY Pin to GND ..... –0.3 V, 15 V
Voltage on VBAT Pin to GND ..... –0.3 V, +6.5 V
Voltage on Pins 6–13, 21–28 to GND ..... –0.3 V, V_{LDO1} + 0.3 V
Voltage on Pins 1, 62–64 ..... –0.3 V, VBAT + 0.3 V
Voltage on Pins 20, 32 ..... –0.3 V, V_{RTCV} + 0.3 V
Voltage on Pin 60 ..... –0.3 V, $V_{ADAPTER}$ + 0.3 V
Voltage on Pins 2–5, 14, 30, 31, 33 ..... –0.3 V, +6.5 V
Storage Temperature Range ..... –65°C to +150°C
Operating Temperature Range ..... –30°C to +85°C
Maximum Junction Temperature ..... 125°C
θ_{JA} Thermal Impedance (TQFP-64) (2-Layer Board) .....87.4°C/W
θ_{JA} Thermal Impedance (TQFP-64) (4-Layer Board) ..... 56.2°C/W
Lead Temperature Range (Soldering, 60 sec) ..... 300°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute maximum ratings apply individually only, not in combination. Unless otherwise specified all other voltages are referenced to GND.

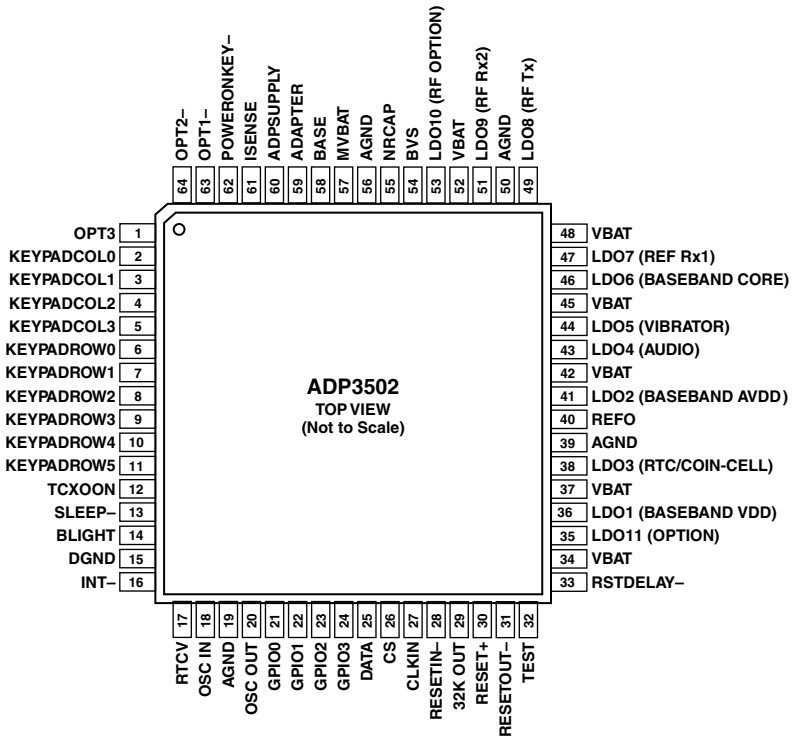
ORDERING GUIDE

Model	Temperature Range	Package
ADP3502ASU	–30°C to +85°C	64-Lead TQFP

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADP3502 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTION

Pin No.	Mnemonic	I/O	Supply	Function
1	OPT3	I	VBAT	Optional Power ON Input. ADP3502 will keep power ON when this pin goes high.
2	KEYPADCOL0	O	LDO1	Keypad Column Strobe 0 (Open-Drain, Pull Low)
3	KEYPADCOL1	O	LDO1	Keypad Column Strobe 1 (Open-Drain, Pull Low)
4	KEYPADCOL2	O	LDO1	Keypad Column Strobe 2 (Open-Drain, Pull Low)
5	KEYPADCOL3	O	LDO1	Keypad Column Strobe 3 (Open-Drain, Pull Low)
6	KEYPADROW0	I	LDO1	Keypad Row Input 0. Pulled up internally, 20 kΩ.
7	KEYPADROW1	I	LDO1	Keypad Row Input 1. Pulled up internally, 20 kΩ.
8	KEYPADROW2	I	LDO1	Keypad Row Input 2. Pulled up internally, 20 kΩ.
9	KEYPADROW3	I	LDO1	Keypad Row Input 3. Pulled up internally, 20 kΩ.
10	KEYPADROW4	I	LDO1	Keypad Row Input 4. Pulled up internally, 20 kΩ.
11	KEYPADROW5	I	LDO1	Keypad Row Input 5. Pulled up internally, 20 kΩ.
12	TCXOON	I	LDO1	Logic Input Pin for Main LDOs (LDO1, LDO2, LDO3, LDO6) Turning On Control. L: OFF, H: ON.
13	SLEEP–	I	LDO1	Logic Input Pin for LDO7 and LDO9. This input gates register data for these LDOs. LDO7 and LDO9 are turned OFF when SLEEP goes low even if the registers are set to ON. If register of SLEEP7 and SLEEP9 are set to "1," the SLEEP signal is ignored.
14	BLIGHT	O	VBAT	LED Drive. Open-drain output.
15	DGND			Digital Ground
16	INT–	O	LDO1	Interrupt Signal Output

PIN FUNCTION DESCRIPTION (continued)

Pin No.	Mnemonic	I/O	Supply	Function
17	RTCV			Supply input for RTC, 32 kHz OSC, and other logic. Connects to coin cell battery in typical operation.
18	OSC IN		RTCV	Connect to 32.768 kHz crystal
19	AGND			Analog Ground
20	OSC OUT		RTCV	Connect to 32.768 kHz crystal
21	GPIO0	I/O	LDO1	General-purpose input and output port. Integrated interrupt function. Interrupt occurs on both the falling and rising edges.
22	GPIO1	I/O	LDO1	General-purpose input and output port. Integrated interrupt function. Interrupt occurs on both the falling and rising edges.
23	GPIO2	I/O	LDO1	General-purpose input and output port. Integrated interrupt function. Interrupt occurs on both the falling and rising edges.
24	GPIO3	I/O	LDO1	General-purpose input and output port. Integrated interrupt function. Interrupt occurs on both the falling and rising edges.
25	DATA	I/O	LDO1	Serial interface data input and output
26	CS	I	LDO1	Serial interface chip select input. Active high input.
27	CLKIN	I	LDO1	Serial interface clock input
28	RESETIN–	I	LDO1	Reset input signal for internal reset signal; Starts stay-alive timer.
29	32K OUT	O	RTCV	32.768 kHz output. Output after 30 ms when reset is released.
30	RESET+	O	RTCV	Reset output. Invert signal of RESETOUT–. Open-drain and low leakage.
31	RESETOUT–	O	RTCV	Reset output. Follows voltage detector operation. Open-drain output.
32	TEST	I	RTCV	Test pin. Reserved for ADI use. Connect to GND for normal operation.
33	RSTDELAY–	O	RTCV	Reset output. 50 ms delayed. Connect to baseband's reset input in typical application. Open-drain output.
34	VBAT			Supply input. Connect to battery.
35	LDO11	O	VBAT	Regulator No. 11 output. General-purpose supply.
36	LDO1	O	VBAT	Regulator No. 1 output. Use for baseband I/O supply.
37	VBAT			Supply input. Connect to battery.
38	LDO3	O	VBAT	Regulator No. 3 output. If VBAT > 2.7 V, the output is always active. Use for coin cell supply.
39	AGND			Analog ground
40	REFO	O	VBAT	Output of LDO2 through FET switch
41	LDO2	O	VBAT	Regulator No. 2 output. Use for baseband analog supply.
42	VBAT			Supply input. Connect to battery.
43	LDO4	O	VBAT	Regulator No. 4 output. Use for general analog supplies, for example, speaker amp.
44	LDO5	O	VBAT	Regulator No. 5 output. Use for vibrator.
45	VBAT			Supply input. Connect to battery.
46	LDO6	O	VBAT	Regulator No. 6 output. Use for baseband core supply.
47	LDO7	O	VBAT	Regulator No. 7 output. Use for RF Rx IC supply. Gated with SLEEP– signal input.
48	VBAT			Supply input. Connect to battery.
49	LDO8	O	VBAT	Regulator No. 8 output. Use for RF Tx IC supply.
50	AGND			Analog Ground
51	LDO9	O	VBAT	Regulator No. 9 output. Use for RF Rx IC supply. Gated with SLEEP– input signal.
52	VBAT			Supply input. Connect to battery.
53	LDO10	O	VBAT	Regulator No. 10 output. General-purpose supply.

PIN FUNCTION DESCRIPTION (continued)

Pin No.	Mnemonic	I/O	Supply	Function
54	BVS			Battery voltage sense input for charger. Connect to battery with a separate low current trace
55	NRCAP	O	VBAT	Noise reduction capacitor, 0.1 µF MLCC
56	AGND			Analog Ground
57	MVBAT	O	VBAT	Battery voltage divider output. Buffered internally. Connect to baseband ADC.
58	BASE	O	ADAPTER	Base drive output for PNP pass transistor
59	ADAPTER			AC Adapter Input
60	ADPSUPPLY	I	ADAPTER	Supply bias current to charging related blocks
61	ISENSE	I	ADAPTER	Charge current sense input
62	PWRONKEY–	I	VBAT	Power ON/OFF key input. Pulled up internally with 140 kΩ.
63	OPT1–	I	VBAT	Optional power ON input. ADP3502 will keep power on when this pin goes low.
64	OPT2–	I/O	VBAT	Optional power ON input. ADP3502 will keep power on when this pin goes low. While the part is powered up, the input is pulled low (GND) internally. Do not connect to any supply or signal source.

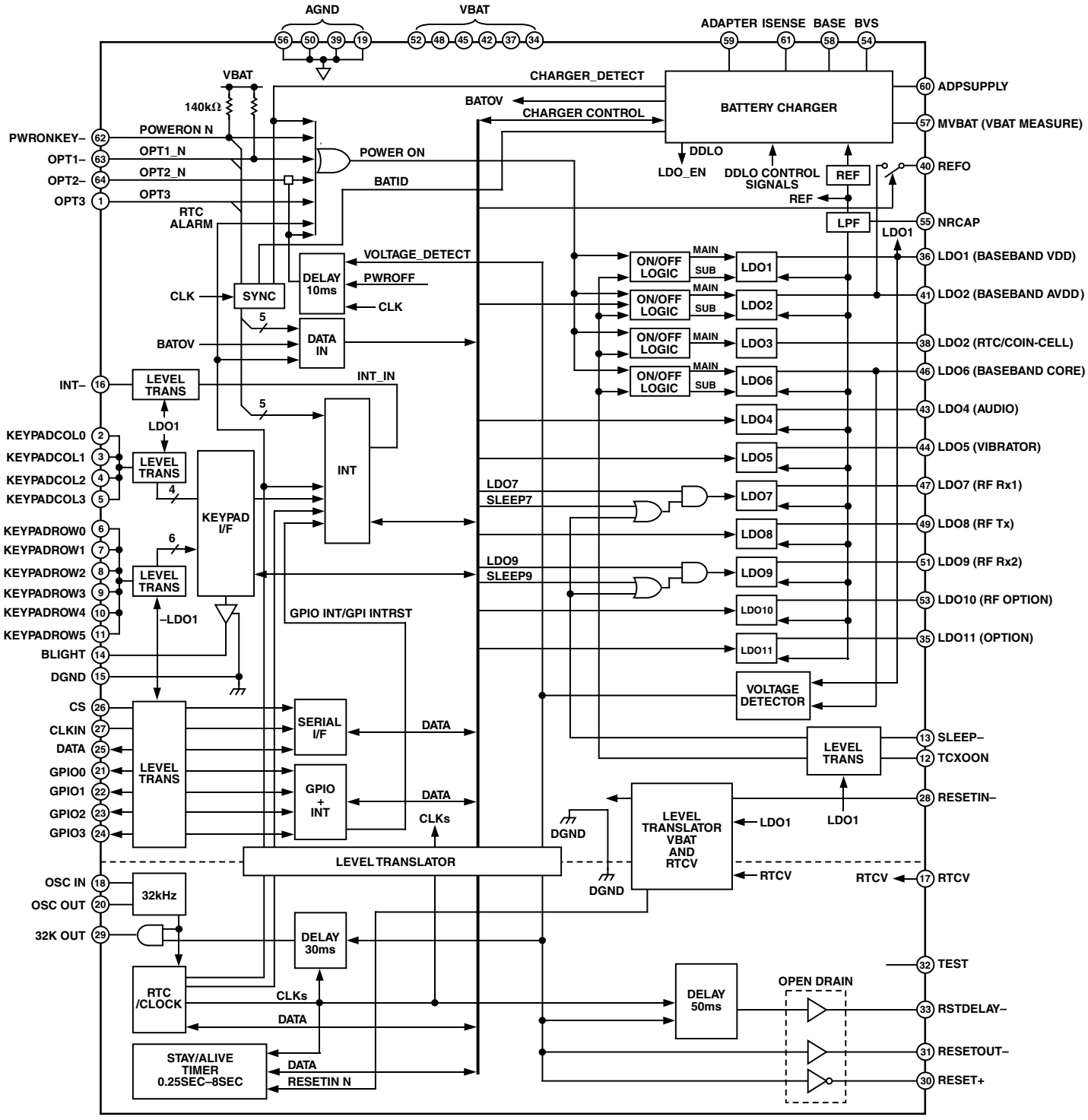
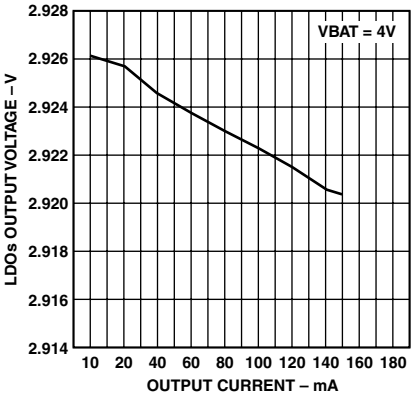
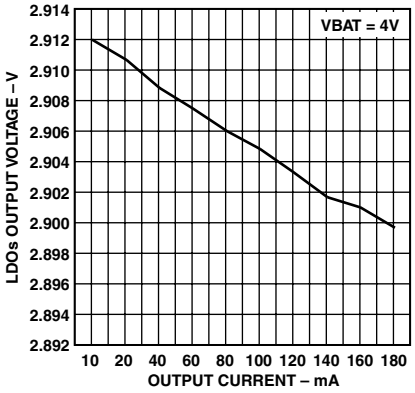


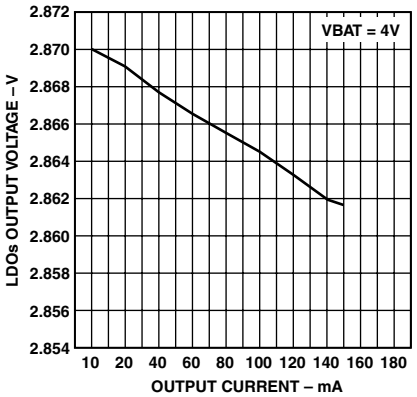
Figure 1. Overall Block Diagram



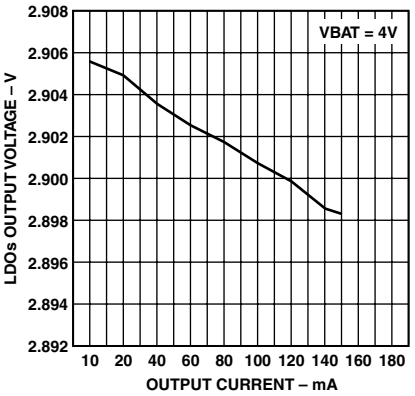
TPC 1. LDO1 Load Regulation



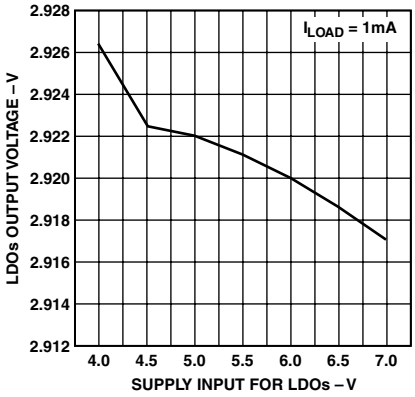
TPC 2. LDO4 Load Regulation



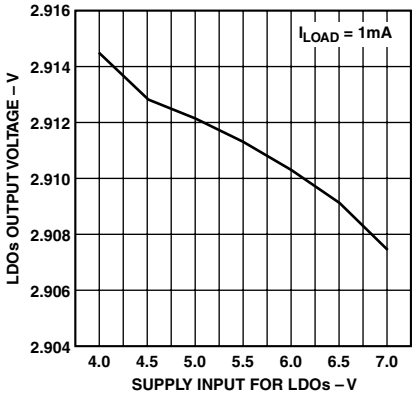
TPC 3. LDO6 Load Regulation



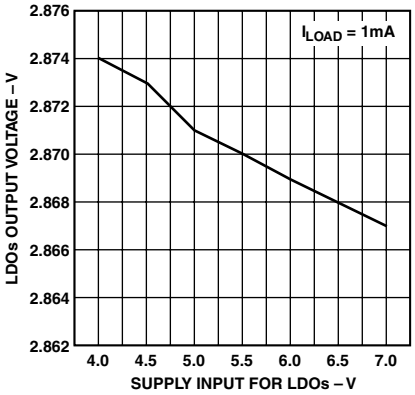
TPC 4. LDO8 Load Regulation



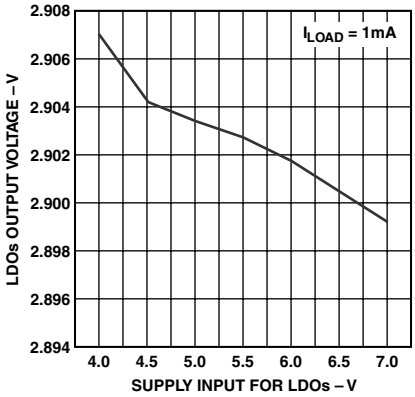
TPC 5. LDO1 Line Regulation



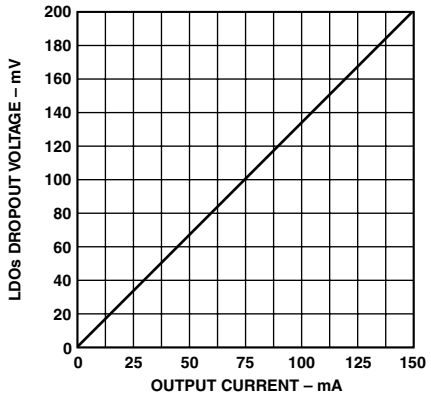
TPC 6. LDO4 Line Regulation



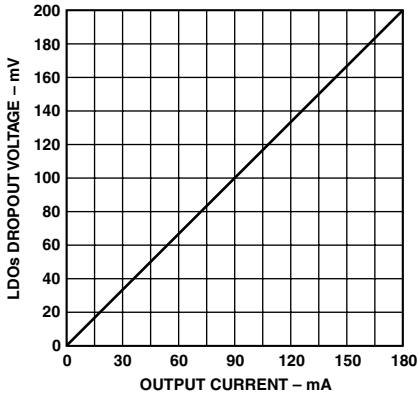
TPC 7. LDO6 Line Regulation



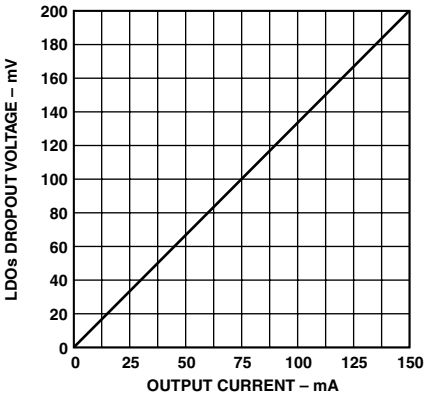
TPC 8. LDO8 Line Regulation



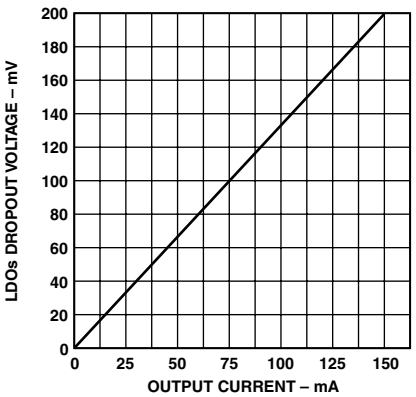
TPC 9. LDO1 Dropout Voltage



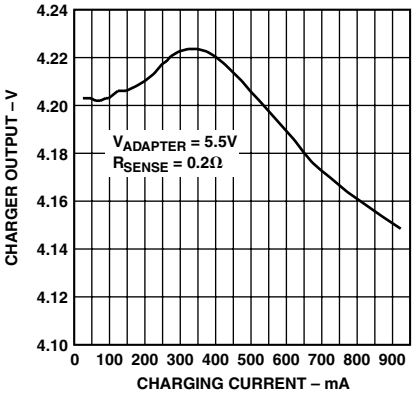
TPC 10. LDO4 Dropout Voltage



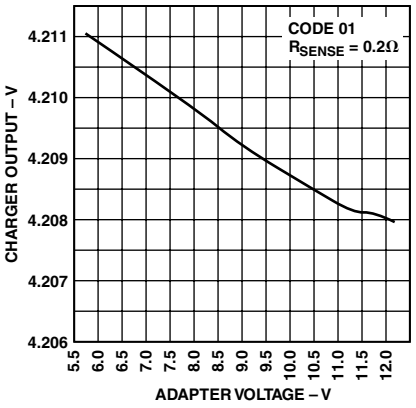
TPC 11. LDO6 Dropout Voltage



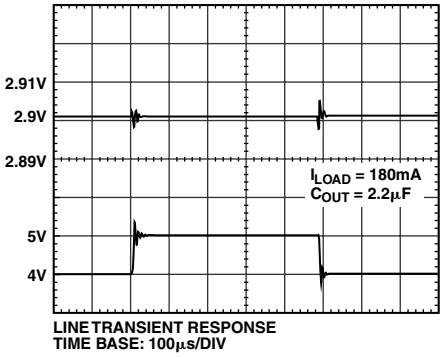
TPC 12. LDO8 Dropout Voltage



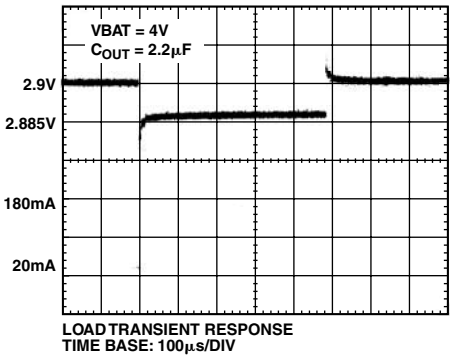
TPC 13. Charger Load Regulation



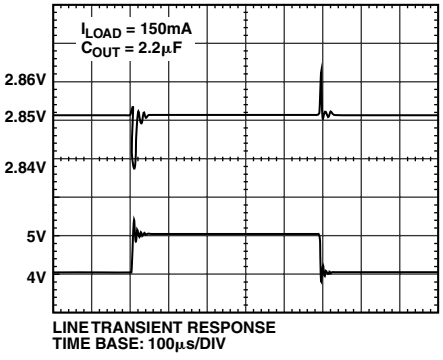
TPC 14. Charger Line Regulation



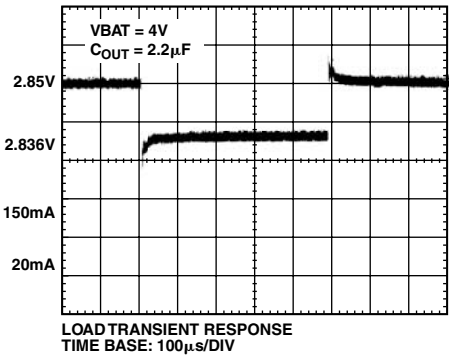
TPC 15. LDO4 Line Transient



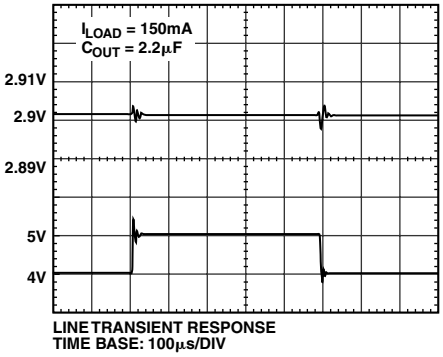
TPC 16. LDO4 Load Transient



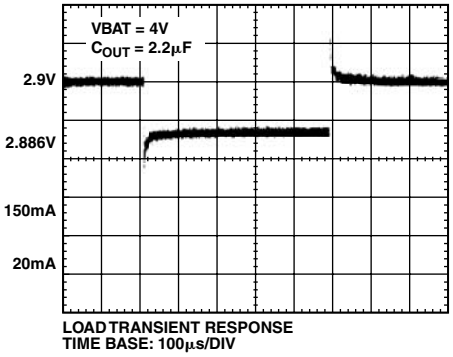
TPC 17. LDO6 Line Transient



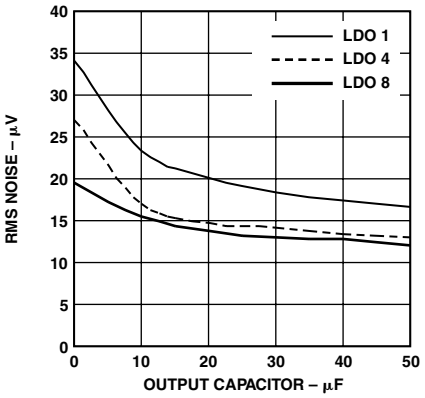
TPC 18. LDO6 Load Transient



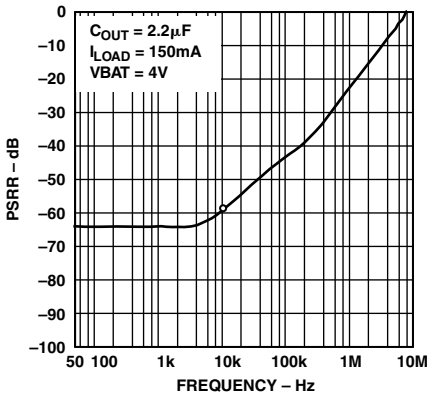
TPC 19. LDO8 Line Transient



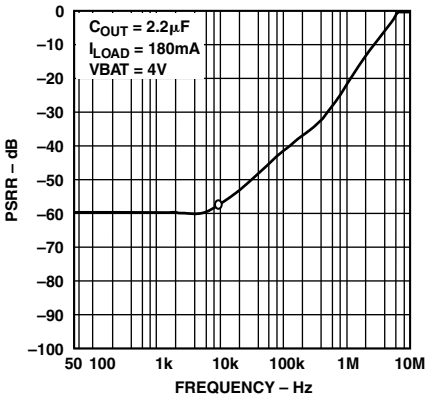
TPC 20. LDO8 Load Transient



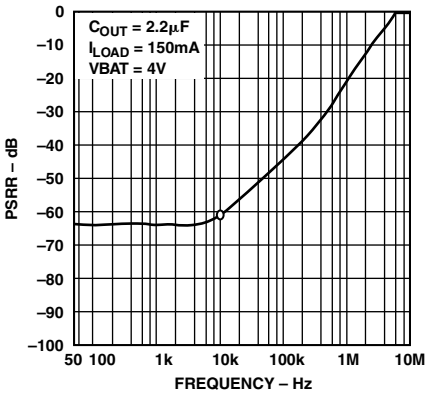
TPC 21. RMS Noise vs. C_{OUT}



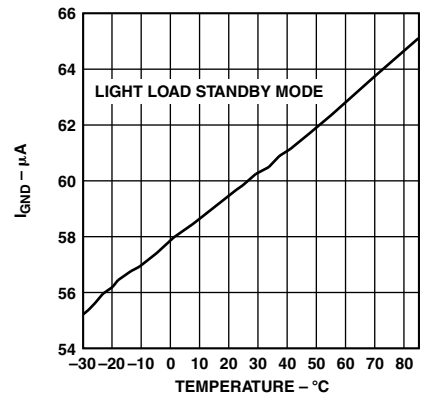
TPC 22. LDO1 PSRR



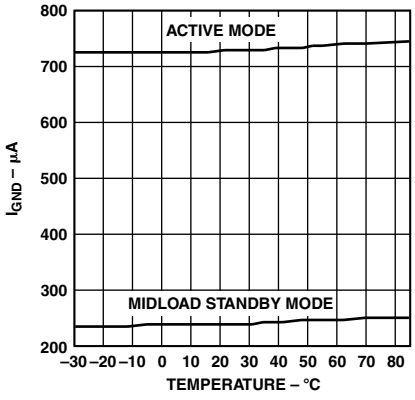
TPC 23. LDO4 PSRR



TPC 24. LDO8 PSRR



TPC 25. I_{GND} vs. Temperature



TPC 26. I_{GND} vs. Temperature

THEORY OF OPERATION

As illustrated in the Functional Block Diagram, the ADP3502 can be divided into two high level blocks—analog and logic. The analog block consists mainly of LDO regulators, a battery charger, reference voltage, and voltage detector subblocks, all of which are powered by the main battery or the charging adapter. On the other hand, VBAT powers all the logic subblocks except the RTC counter, 32 kHz output control, RESET output, and stay-alive timer. The RTCV pin powers these subblocks (see the shaded area of Figure 2).

ANALOG BLOCKS

Low Drop-Out (LDO) Regulators

There are four sub-LDOs for LDO1, LDO2, LDO3, and LDO6, in order to meet low power consumption at light load (standby operation). They are used at low load condition, but they are continuously on even if each of the main LDOs are on. LDO3 and LDO3b are used for the coin cell, and LDO3b is always on until the main battery (VBAT) is decreased to 2.5 V, the DDLO threshold. LDO7 and LDO9 are gated by a control signal from SLEEP or register setting of SLEEP7/SLEEP9. LDO4 and LDO11 are initially on. For details of LDO on/off control, refer to the LDO Control section.

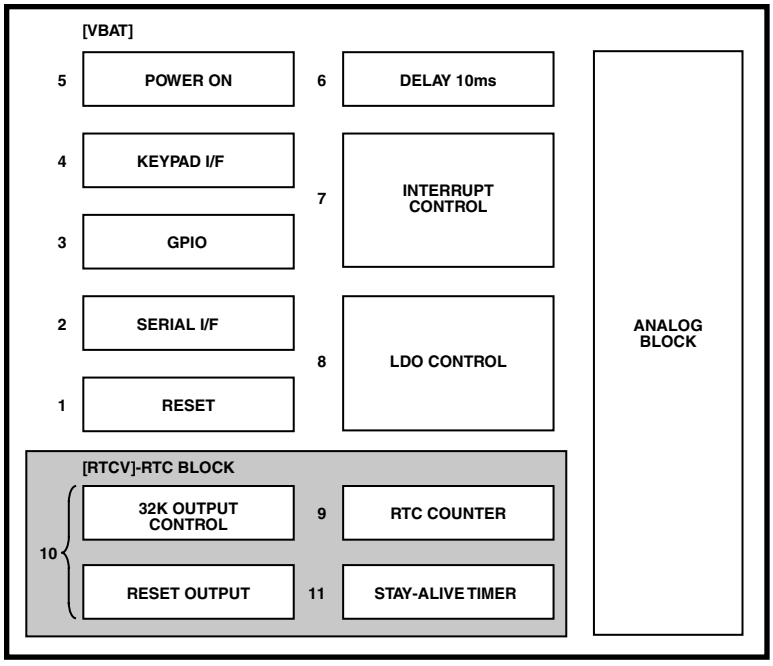


Figure 2. Power Partitioning of Subblocks

Table I. Ground Currents of LDOs with Each Handset Operation

LDO Names		Baseband VDD	Baseband Core	Coin Cell	Audio	Vibrator	Baseband AVDD	RF Rx1	RF Tx	RF Rx2	RF Option	Option	Main REF	Total LDO IGND
LDO Number		1	6	3	4	5	2	7	8	9	10	11		
Power OFF		OFF	OFF	10 µA	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	20 µA	30 µA
Standby Mode	Light Load	10 µA	5 µA	10 µA	OFF	OFF	5 µA	OFF	OFF	OFF	OFF	OFF	20 µA	50 µA
	Midload	60 µA	55 µA	60 µA	OFF	OFF	55 µA	OFF	OFF	OFF	OFF	OFF	20 µA	250 µA
	Active Load	60 µA	55 µA	60 µA	OFF	OFF	55 µA	80 µA	80 µA	80 µA	80 µA	OFF	20 µA	570 µA
Talk		60 µA	55 µA	60 µA	55 µA	OFF	55 µA	80 µA	80 µA	80 µA	80 µA	80 µA	20 µA	675 µA
Ring		60 µA	55 µA	60 µA	55 µA	69 mA	55 µA	80 µA	80 µA	80 µA	80 µA	80 µA	20 µA	744 µA

Table II. LDO Operation Overview

Regulator	Names	Current Rating (mA)	Voltage (Typ) or Range (V)	Program Steps	Step Size (mV)	Default	C_{OUT} (μF)
LDO1a	Baseband VDD	150	2.90	N/A	N/A		2.2
LDO1b	Baseband VDD Sub	3	2.87	N/A	N/A		2.2
LDO2a	Baseband AVDD	50	2.36 ~ 2.66	16	20	2.52 V	1
LDO2b	Baseband AVDD Sub	0.3	2.33 ~ 2.63	16	20	2.49 V	1
LDO3a	RTC/Coin Cell	50	3.0	N/A	N/A		1
LDO3b	RTC/Coin Cell Sub	1	2.97	N/A	N/A		1
LDO4	Audio	180	2.9	N/A	N/A		2.2
LDO5	Vibrator	150	2.9	N/A	N/A		2.2
LDO6a	Baseband Core	150	2.85	N/A	N/A		2.2
LDO6b	Baseband Core Sub	1	2.80	N/A	N/A		2.2
LDO7	RF Rx1	100	2.9	N/A	N/A		1.5
LDO8	RF Tx	150	2.9	N/A	N/A		2.2
LDO9	RF Rx2	50	2.9	N/A	N/A		1
LDO10	RF Option	50	2.9	N/A	N/A		1
LDO11	Option	100	1.5	N/A	N/A		2.2

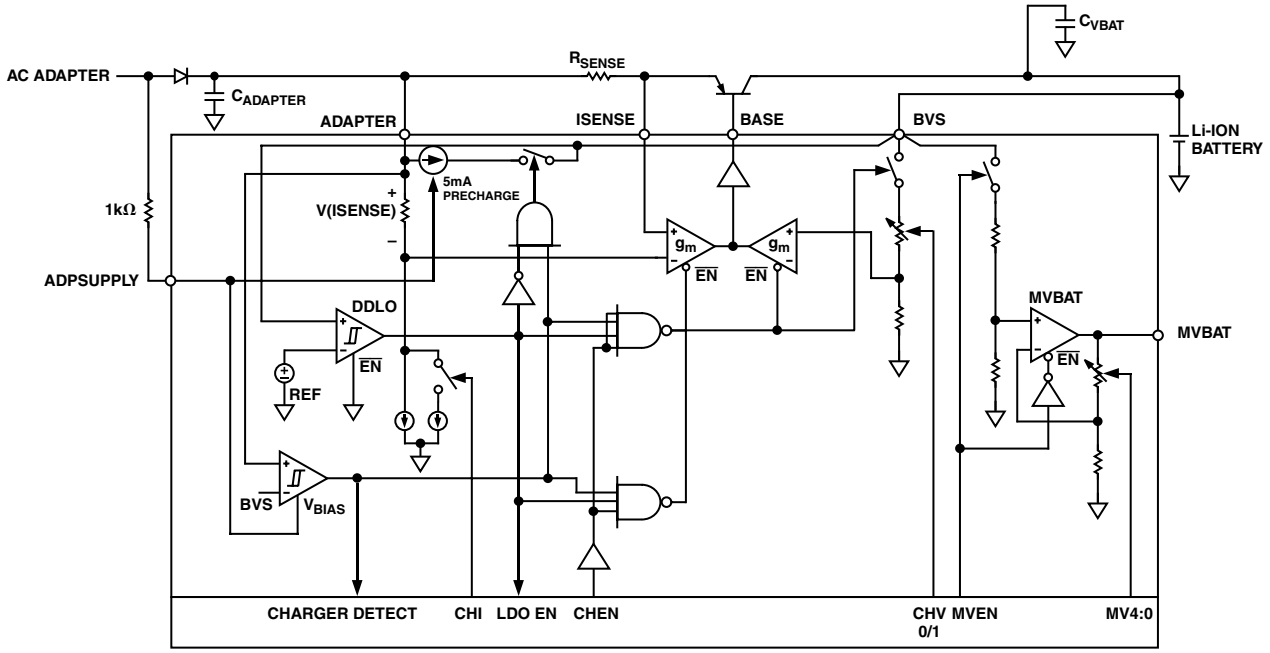


Figure 3. Battery Charger Block Diagram

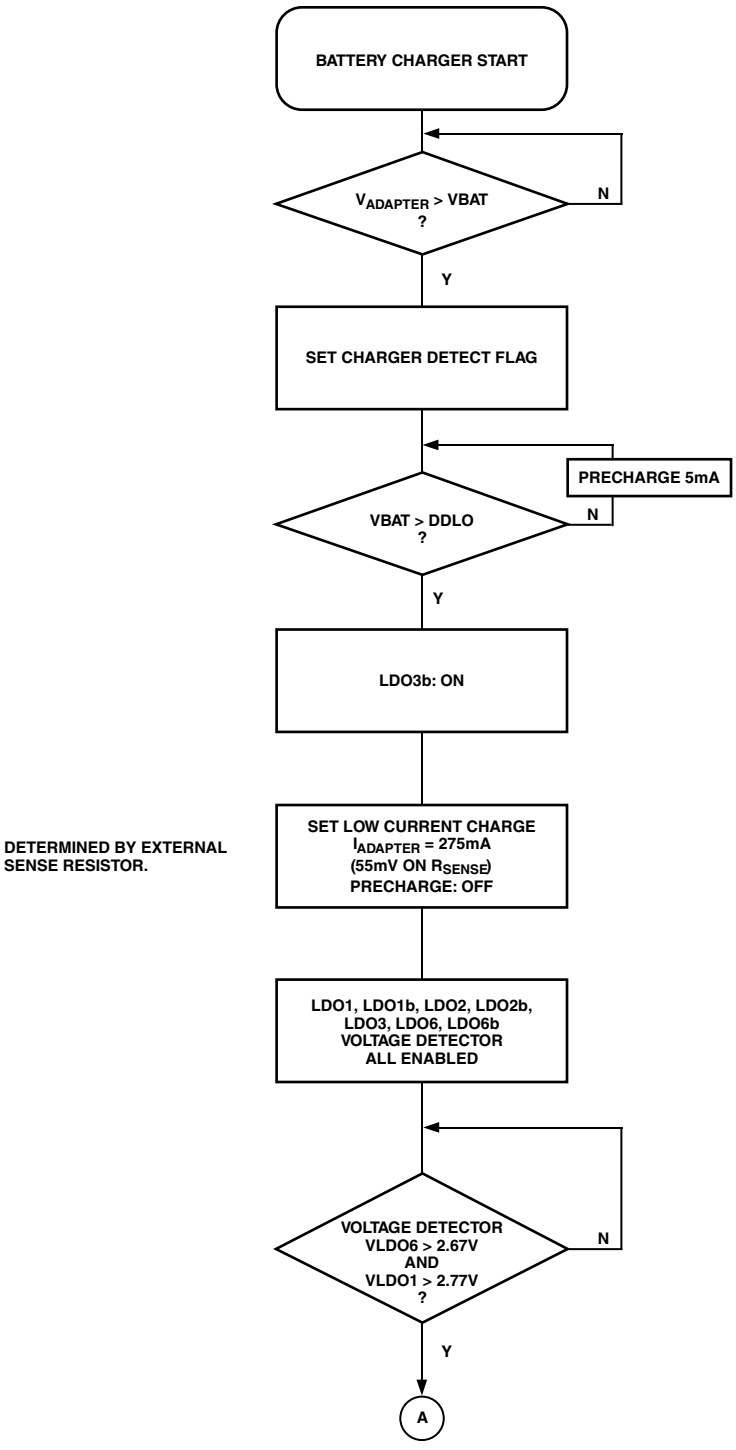


Figure 4. Charger Flow Chart A

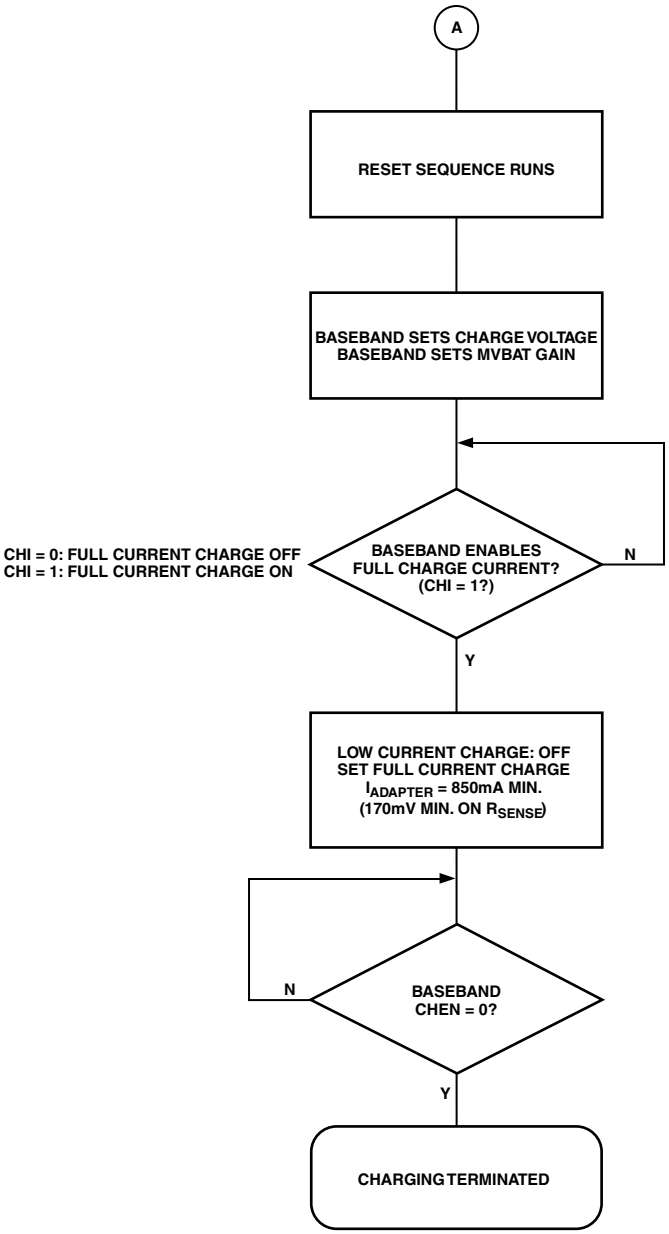


Figure 5. Charger Flow Chart B

Adapter Connection
There are two adapter connections on the ADP3502, Pins ADAPTER and ADPSUPPLY. The ADPSUPPLY pin only provides bias current to the charger detect comparator and precharge block. With a diode placed on the adapter side of the PNP transistor, as shown in Figure 3, the reverse battery current will be blocked.

Charger Detect Function
The ADP3502 will detect that a charging adapter has been applied when the voltage at the ADAPTER pin exceeds the voltage at BVS. The ADAPTER pin voltage must exceed the BVS voltage by a small positive offset. This offset has hysteresis to prevent jitter at the detection threshold. The charger detection comparator will set the charger detect flag in the 20h register and generate an interrupt to the system. If the ADAPTER input voltage drops below the detection threshold, charging will stop automatically, and the charger detect flag will be cleared and generate an interrupt also.

DDLO Function and Operation
The ADP3502 contains a comparator that will lock out system operation if the battery voltage drops to the point of deep discharge. When the battery voltage exceeds 2.675 V, the reference will start as will the sub-LDO3b. If the battery voltage drops below the hysteresis level, the reference and LDOs will be shut down if for some reason they are still active. Since LDO1 will be in deep drop-out and well below the voltage detector threshold at this point, the reset generator will have already shut down the rest of the system via RESET+, RESETOUT–, and RSTDELAY–.

If a charging adapter has been applied to the system, the DDLO comparator will force the charging current to trickle charge if the battery is below the DDLO threshold. During this time, the charging current is limited to 5 mA. When the battery voltage exceeds the upper threshold, the low current charging is enabled, which allows 55 mV (typical) across the external charge current sense resistor (see Figure 4).

MVBAT
The ADP3502 provides a scaled buffered output voltage for use in reading the battery voltage with an A/D converter. The battery voltage is divided down to be nominally 2.600 V at the full-scale battery of 4.35 V. To assist with calibrating out system errors in the ADP3502 and the external A/D converter, this full-scale voltage may be trimmed digitally with five bits stored in register 12h. At full-scale input voltage, the output voltage of MVBAT can be scaled in 6 mV steps, allowing a very fine calibration of the battery voltage measurement. The MVBAT buffer is enabled by the MVEN bit of register 11h and will consume less than 1 μA of leakage current when disabled.

Reference
The ADP3502 has an internal temperature compensated and trimmed band gap reference. The battery charger and LDOs all use this system reference. This reference is not available for use externally. However, to reduce thermal noise in the LDOs, the reference voltage is brought out to the NRCAP pin through a 50 kΩ internal resistor. A cap on the NRCAP pin will complete a low-pass filter that will reduce the noise on the reference voltage. All the LDOs, with the exception of LDO3, use the filtered reference.

Since the reference voltage appears at NRCAP through a 50 kΩ series internal impedance, it is very important to never place any load current on this pin. Even a voltmeter with 10 MΩ input impedance will affect the resulting reference voltage by about 6 mV or 7 mV, affecting the accuracy of the LDOs and charger. If for some reason the reference must be measured, be certain to use a high impedance range on the voltmeter or a discrete high impedance buffer prior to the measurement system.

LOGIC BLOCKS
ADP3502 includes the following functions:

- 3-wire serial interface (CS, CLK, DATA)
- RTC counter section has year, month, day, week, hour, minute, and second and controls leap year and days in month automatically.
- Detect alarms based on RTC counter
- Periodically constant interrupt feature (2 Hz, 1 Hz, 1/60 Hz, 1/3600 Hz, once a month)
- GPIO and INT ports control
- Keypad interface
- LED light control
- LDO functions
- Clock and reset output control
- Stay-alive timer

Figure 6 is a block diagram based on the logic circuit.

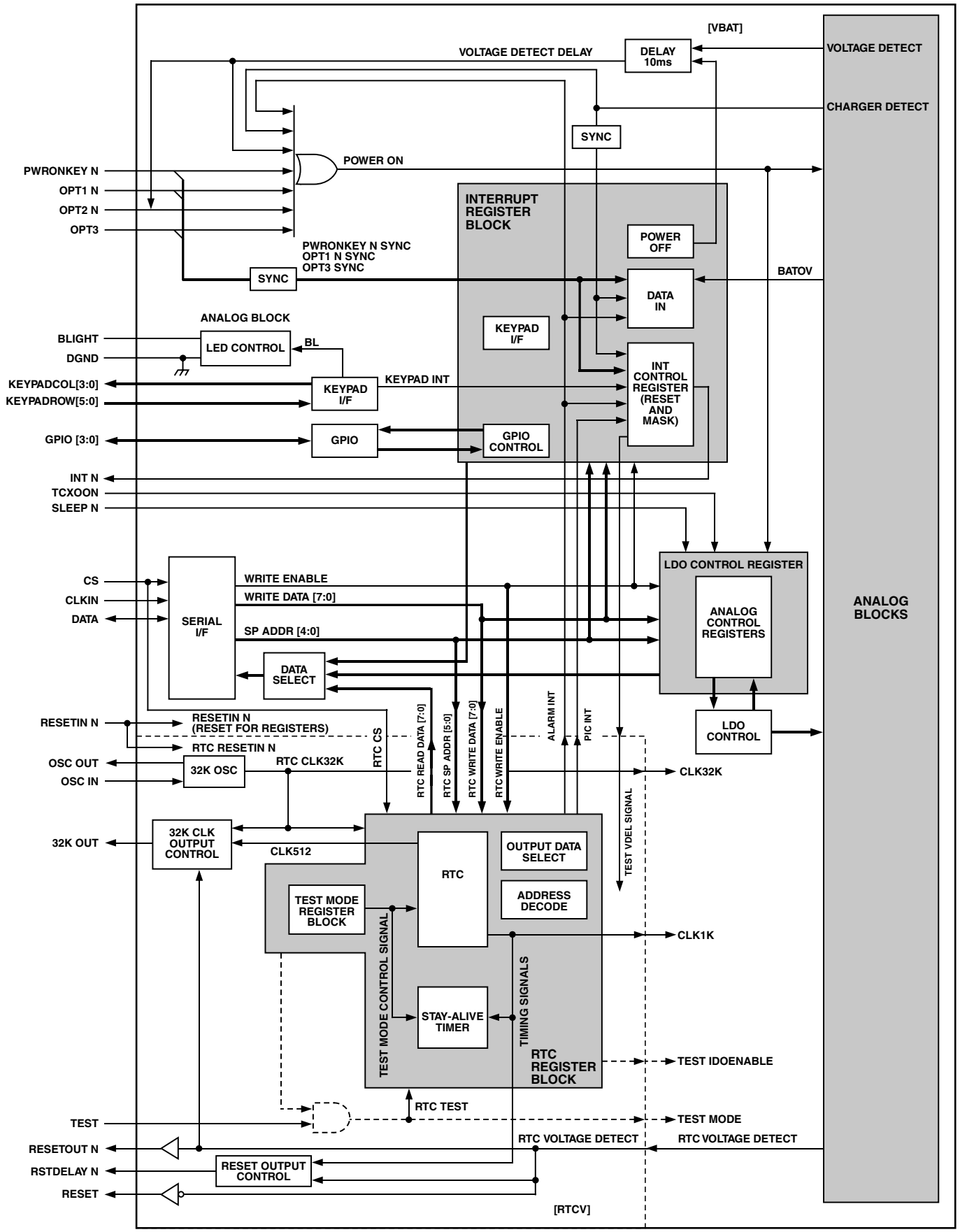


Figure 6. LOGIC Block Diagram

RESET

RESETIN– Signal

The internal reset function is activated by the external reset input, RESETIN–, and is an asynchronous signal. The internal reset signal is used in the following blocks:

- Serial I/F
- Interrupt control
- Stay-alive timer
- Registers (refer to the Register section for additional information).

LDOs, controlled by Serial I/F, are applied "RESET" by RESETIN–. LDO5, LDO7, LDO8, LDO9, LDO10, and REFO are set to "0," and LDO4 and LDO11 are set to "1." In case RESETIN– has noise, the internal circuit may be in reset and cause the system to have an unexpected result. Take care to avoid this situation. RESETIN– is level translated from LDO1 to both VBAT and RTCV supplies.

RESET Output Control and 32 kHz Output Control

Using a voltage detect signal, the device generates 32K OUT, RSTDELAY–, RESETOUT–, and RESET signals. About 32 ms after the RTC Voltage Detect (voltage detect signal in RTCV supply) signal goes from "0" to "1," the 32K OUT signal is generated from the internal RTC_CLK32K signal. RSTDELAY N (RSTDELAY–) goes to "0" when the RTC Voltage Detect is "0," and it goes to "1" at 50 ms after the "0" to "1" transition of the RTC Voltage Detect. RESETOUT N (RESETOUT–) and RESET toggle their states. Signal CLK512 is a 512 Hz, which is generated in USEC counter block.

SERIAL INTERFACE

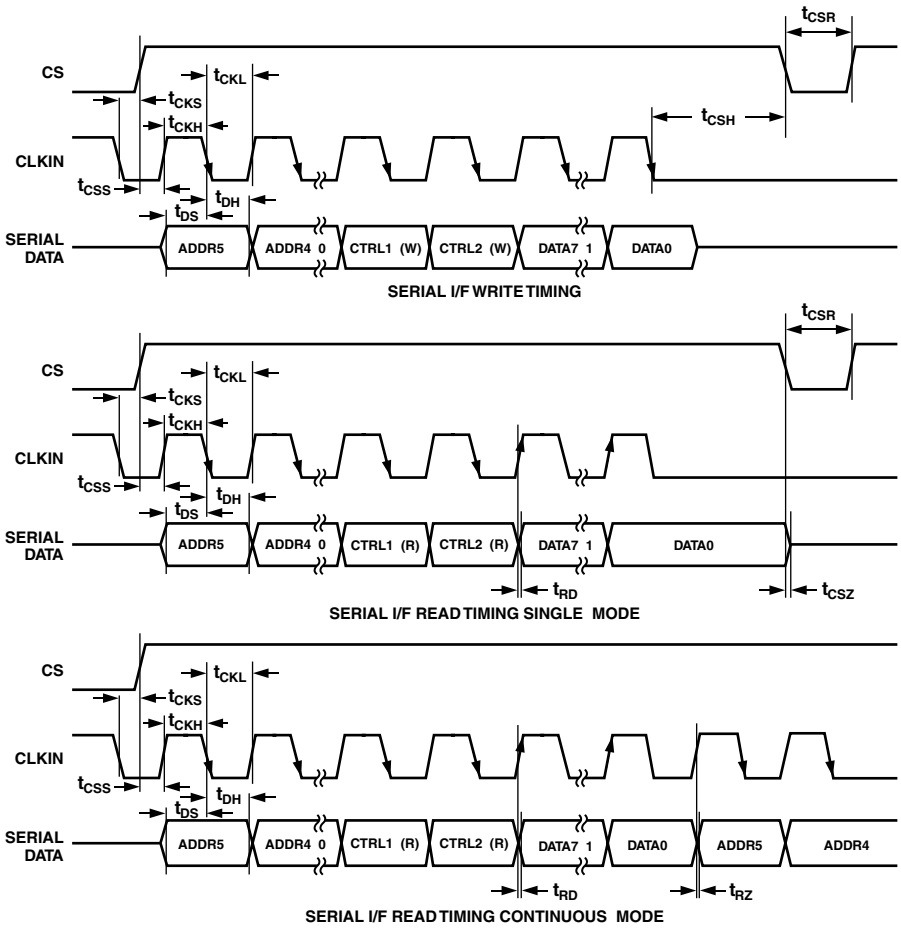


Figure 7. Serial Interface Signal

Table III. Setup and Hold Specifications

Parameter*	Min	Typ	Max	Unit	Test Condition/Comments
t_{CKS}	50			ns	CLK Setup Time
t_{CSS}	50			ns	CS Setup Time
t_{CKH}	100			ns	CLK High Duration
t_{CKL}	100			ns	CLK Low Duration
t_{CSH}	100			ns	CS Hold Time
t_{CSR}	62			µs	CS Recovery Time
t_{DS}	50			ns	Input Data Setup Time
t_{DH}	40			ns	Input Data Hold Time
t_{RD}			50	ns	Data Output Delay Time
t_{RZ}			50	ns	Data Output Floating Time
t_{CSZ}			50	ns	Data Output Floating Time after CS Goes Low

*These parameters are not tested.

Function Block

The ADP3502 integrates the serial bus interface for easy communication with the system. The data bus consists of three wires (CLK, CS, and DATA) and is capable of serial-to-parallel/parallel-to-serial conversion of data, as well as clock transfer.

Serial interface block works during the time period at CS signal enable. After the falling edge of CLKIN, signals right after the rising edge of the CS signal, address, transfer control signal, and write data are held in sequentially. In case of DATA READ, data will be prepared by the rising edge of CLKIN, and the baseband chip may want to read or latch the data at the falling edge of CLKIN. While CS is not asserted, CLKIN is ignored. If CS goes "L" while CLKIN is continuously applied or input DATA, all data is canceled, and the DATA line would be high impedance. In this case, users need to input the data again.

Note that CLKIN should stay "L" when CS goes "H." RTC counter registers should be accessed at a certain time (>62 µs) after CS assertion. Asserting RESETIN N (RESETIN–), signal resets the block.

Notes:

- CLKIN should be "L" when CS goes "H."
- In case of RTC counter access, the access should be approximately 62 µs (two clock cycles of CLK32K) after the CS signal is asserted to hold the RTC value.
- The CS should not be asserted for 62 µs (2 clock cycles of CLK32K) after the CS is released.
- CS signal should never be asserted for 1 sec or longer; otherwise the RTC counter makes an error.
- CLKIN should be chosen as a multiple of 16 if CS < 31 µs.

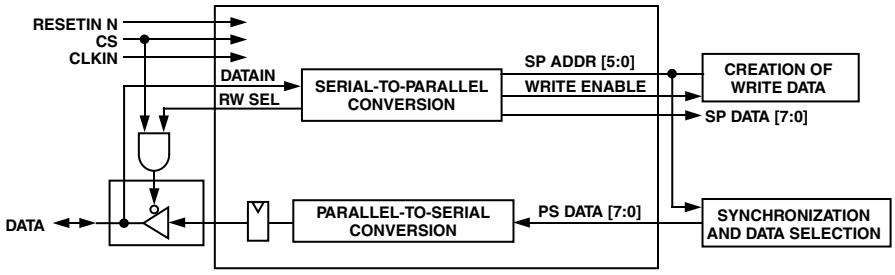


Figure 8. Serial Interface Block Diagram

DATA INPUT/OUTPUT TIMING

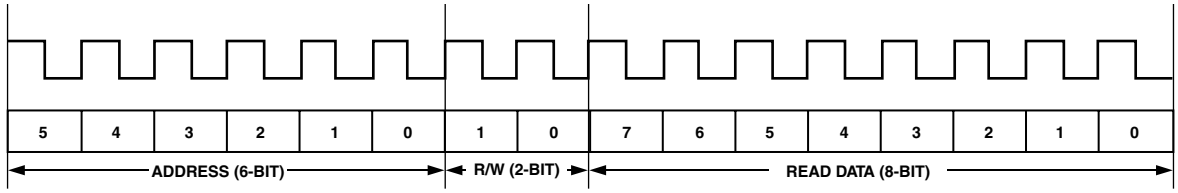


Figure 9. Serial I/F Data Read/Write Timing

In Figure 9:

- SP ADDR[5:0]: 6-Bit Address
- SP CTRL[1:0]: 2-Bit Read/Write Control (01: Write, 10: Read)
- SP DATA[7:0]: 8-Bit Input/Output Data

All transfers will be done MSB first.

GPIO + INT

The GPIO block has 4-channel I/O function and interrupt. With the GPIO CONTROL register (1Ah), it is possible to control the input or output setting of each channel individually. The output data is set in the GPIO register (1Ch). When the port is set in input mode, the input signal transitions from "1" to "0" and from "0" to "1" and then generates an interrupt signal with edge detection. The held interrupt signals are reset by the GPIO INT RESET register (1Dh). Setting the GPIO MASK register (1Bh) to "1" enables the interrupt of GPIO. (Not MASKED, "1" at default in reset.)

INT Register

If the interrupt event occurs, "1," the signal is held in this register. INT detect and reset are synchronized at the rising edge of CLK32K. If the interrupt event and reset signal occur at the same time, the interrupt event has priority. The RESETIN N signal resets the INT register (1Eh) to "0" (no INT detected), except alarm int and pic int. The INT MASK register (1Fh) goes to "1" (not masked). This block masks alarm int and pic int, which generated in RTCV block, but these signals are reset with the ALARM CONTROL register (0Dh) and PIC CONTROL register (0Eh). The interrupt signal, INT N, is an inverted OR signal of the value in the INT register and GPIO register.

The DATA-IN register is a port to read an interrupt status. The input data are through the SYNC block, except the alarm signal. Since this is for just readback purposes, the user cannot write any data.

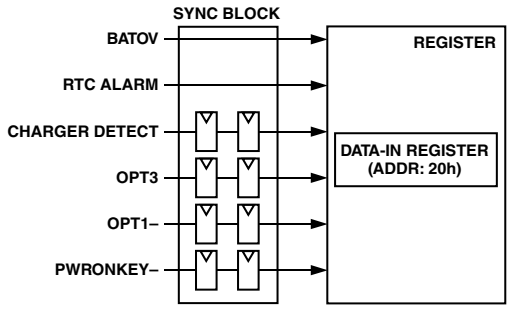


Figure 10. DATA-IN Block

Keypad Control and LED Drive

KEYPADCOL[3:0] are open-drain outputs. The KEYPADROW[5:0] are falling edge trigger inputs (input state transition from "1" to "0") and generate interrupt signal and are pulled up to LDO1. By providing four keypad-column outputs and six keypad-row inputs, the ADP3502 can monitor up to 24 keys with the baseband chip. Writing column outputs and reading row inputs are controlled through a serial interface. The address of the KEYPADROW is 19h, and KEYPADCOL is 18h. The initial register value is "1," which means the output of KEYPADCOL is low. Three-stage flip-flop synchronizes signals into interrupt circuit to 1 kHz clock.

The back-light drive is an open-drain output. The maximum current of the internal FET is 100 mA. The initial register value is "0," which means the output of BLIGHT is high impedance.

Power ON Input

PWRONKEY and OPT1 have pull-up resistors, and others do not. In addition to these inputs, other internal input signals, such as charger detect and alarm signal (alarm int) from RTC, enable the main and sub-LDOs of LDO1, LDO2, LDO3, LDO4, LDO6, and LDO11. The Power ON status is held by latch data in the delay circuit, called voltage detect delay (see 10 ms Delay section for more information). OPT3 has a lower voltage threshold. OPT2 has a different structure than the other inputs and is pulled down to zero by the internal signal when the phone is in Power ON status, in order to ensure Power ON status, even if short-term disconnection happens. Figure 11 is a block diagram of the Power ON sequence.

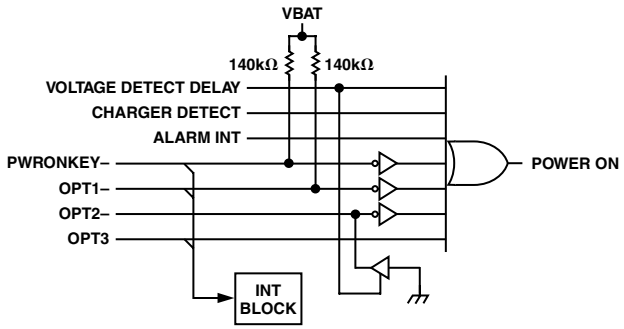


Figure 11. Power ON Input Block Diagram

In Figure 11:

- Voltage Detect Delay: Voltage Detect Signal (10 ms Delay) (1: Assert)
- Charger detect: Charger Detect Signal (1: Assert)
- Alarm INT: Alarm Detect Signal (Alarm 1 or Alarm 2) (1: Assert)
- PWRONKEY–: Power On Key Input (0: Assert)
- OPT1–: Power On Signal (0: Assert)
- OPT2–: Power On Signal (0: Assert)
- OPT3: Power On Signal (1: Assert)

10 ms Delay

This block generates a 10 ms delayed signal after the reset of the voltage detect signal is released. 10 ms (11 clocks of 1024 Hz) after the voltage detect signal is asserted, the voltage detect delay signal is asserted. If the duration of the voltage detect signal is less than 10 ms, the voltage detect delay signal will not be asserted. When the voltage detect signal is released, the voltage detect delay signal is released simultaneously. The voltage detect delay signal can be reset by writing "1" in the POWER OFF register (21h).

If users want to go back to a Power ON state, users should set "1" to address 22h within a time constant of the external R/C network, which is suppose to be connected to OPT2.

Note that users just need to write a "1" in the Power OFF register to reset the voltage detect delay and do not need to overwrite it with a "0."

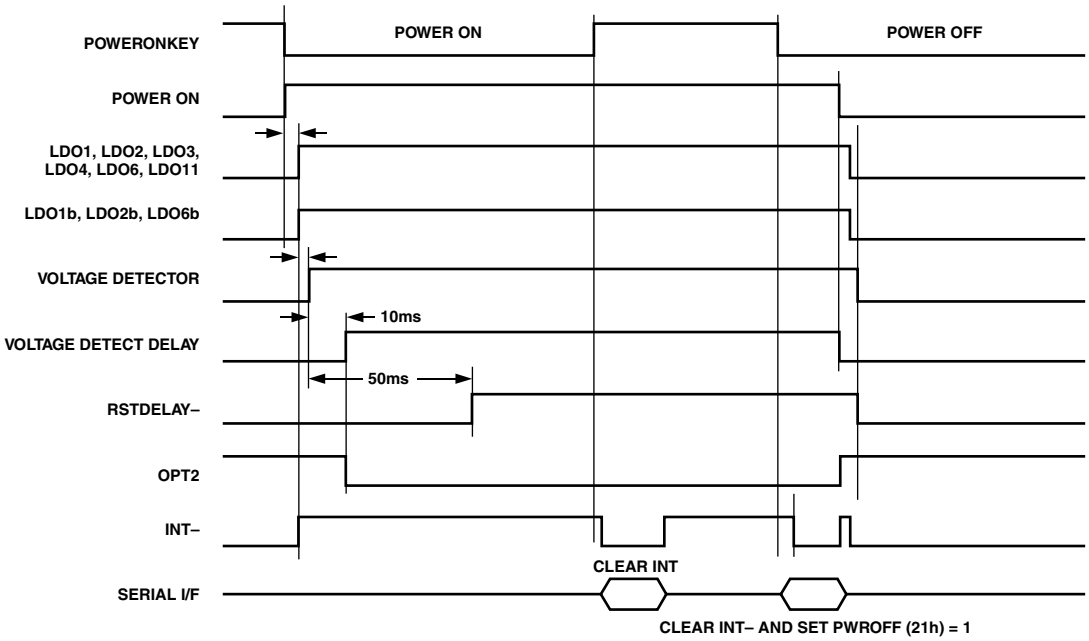


Figure 12. Power ON Sequence

LDO Control

The LDO control block controls Power ON/OFF of the LDO block. The function in this block has:

- Hardware control using external signals
- Software control using serial interface
- A mixture of the hardware and software above

LDO1, LDO2, LDO3, and LDO6 are structured with main and sub-LDOs. LDO4, LDO5, LDO7, LDO8, LDO9, LDO10, and LDO11 are set through the serial interface, but LDO7 and LDO9 are gated (AND gate) with SLEEP– signal in order to get into the SLEEP mode. If the SLEEP– signal is enabled (goes low), the outputs of LDO7 and LDO9 are turned OFF. The Power ON Logic controls the remainder of the LDOs, including LDO1, LDO2, and LDO6. A sub-LDO called LDO3b is independently controlled, and this LDO control block doesn't control LDO3b. Also, the main LDO3, called LDO3a, is turned on by the Power ON signal, but the sub-LDO3, called LDO3b, is always ON while the battery supplies, and only the DDLO controls LDO3b. A DDLO is the control signal from the battery charger block and is monitoring the battery voltage. When VBAT is under 2.5 V (200 mV hysteresis from VBAT = 2.7 V), DDLO minimizes (DDLO enable) the current flow from the Li-Ion battery.

Main LDOs: LDO1a, LDO2a, LDO3a, LDO6a
Sub-LDOs: LDO1b, LDO2b, LDO3b, LDO6b

Table IVa. DDLO Status Table

Status	LDO1a	LDO1b	LDO2a	LDO2b	LDO3a	LDO3b	LDO4	REFO	LDO5	LDO6a	LDO6b	LDO7	LDO8	LDO9	LDO10	LDO11
	Baseband VDD		Baseband AVDD		Coin Cell		Audio	REFO	Vibrator	Baseband Core		Rx1	Tx	Rx2	RF Option	Option
DDLO Enable	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
DDLO Disable	X	X	X	X	X	ON	X	X	X	X	X	X	X	X	X	X

X means a status of LDO depends on other conditions.

Table IVb. LDO Control Event Table[1]

Event	LDO1a	LDO1b	LDO2a	LDO2b	LDO3a	LDO3b	LDO4	REFO	LDO5	LDO6a	LDO6b	LDO7	LDO8	LDO9	LDO10	LDO11
	Baseband VDD		Baseband AVDD		Coin Cell		Audio	REFO	Vibrator	Baseband Core		Rx1	Tx	Rx2	RF Option	Option
Power ON[2]	ON	ON	ON	ON	ON		ON			ON	ON					ON
TCXOON[3]	ON/ OFF		ON/ OFF		ON/ OFF					ON/ OFF						
SLEEP–[4]												ON/ OFF		ON/ OFF		
RESETIN–							OFF	OFF	OFF			OFF	OFF	OFF	OFF	OFF
ALLOFF Bit Goes "H"							OFF	OFF	OFF			OFF	OFF	OFF	OFF	OFF
PWROFF Bit Goes "H"	OFF	OFF	OFF	OFF	OFF		OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

NOTES
[1]This table indicates only the status change caused by an event. Blank cells mean no change and keep previous status.
[2]Power-ON Event: Indicating a status just after the power-ON event. After the event, a status of LDO1a, LDO2a, LDO3a, and LDO6a are changed by the TCXOON signal.
[3]TCXOON: Hardware control, change all main LDOs' ON/OFF status.
[4]SLEEP–: The LDO7 and LDO9 can be controlled by software if SLEEP = "H" level. If SLEEP– goes "L," these LDOs are turned OFF immediately.

Table IVc. Software Controllability of LDOs

LDO	LDO1a	LDO1b	LDO2a	LDO2b	LDO3a	LDO3b	LDO4	REFO	LDO5	LDO6a	LDO6b	LDO7	LDO8	LDO9	LDO10	LDO11
Description	Baseband VDD		Baseband AVDD		Coin Cell		Audio	REFO	Vibrator	Baseband Core		Rx1	Tx	Rx2	RF Option	Option
Software Turn ON							√	√	√			√*	√	√*	√	√
Software Turn OFF	√	√	√	√	√		√	√	√	√	√	√	√	√	√	√

*LDO7 and LDO9 have a gate with SLEEP–. If SLEEP– is in "L" (active) status, users cannot control it and both LDOs are kept in an OFF status. Users may want to use this function as an immediate control to get OFF status by using SLEEP– hardware control when setting Register "1" to the LDO control register.

RTC Block

The calendar registers are set through the serial interface.

Function

- RTC counter using binary
- Reading out and writing settings of year, month, day, week, hour, minute, and second data
- Leap year controls, number of days in a month control
- Alarm function (week, hour, minute)
- Periodic interrupt function—2 Hz, 1 Hz, 1/60 Hz, 1/3600 Hz, each month (first day of each month)
- Protection of wrong data readout during RTC data update

Operation

Synchronizing with the RTC CLK32K clock, the USEC counter generates a 1 sec timing clock, which hits the RTC counter. Through the serial interface, the CPU can write the setting value and read the RTC counter value. In case the RTC counter toggles during the serial interface access to the RTC counter, the wrong data can be read/written between the RTC counter and the interface. The CS signal stops the clocking to the RTC counter until the CS signal is released. In case the CPU writes data into the SEC counter, the USEC counter is reset to zero.

Note the following:

- In case of RTC counter access, the access should wait approximately 62 μs, (two clock cycles of CLK32K) after the CS signal is asserted, to hold the RTC value.
- The CS signal should never be asserted 1 sec or longer since this effects counter operation.

USEC Counter Operation

The USEC counter counts up synchronizing with the RTC CLK32K clock. It generates a 1 sec timing signal and is used as an increment clocking of the RTC counter. In case the 1 sec signal is generated during the CS signal asserted, the increment clock is delayed until the CS signal is released.

RTC Counter Operation

The RTC counter uses the increment signal from the USEC counter to control the counting operation, including the leap year control and numbers of days in a month control.

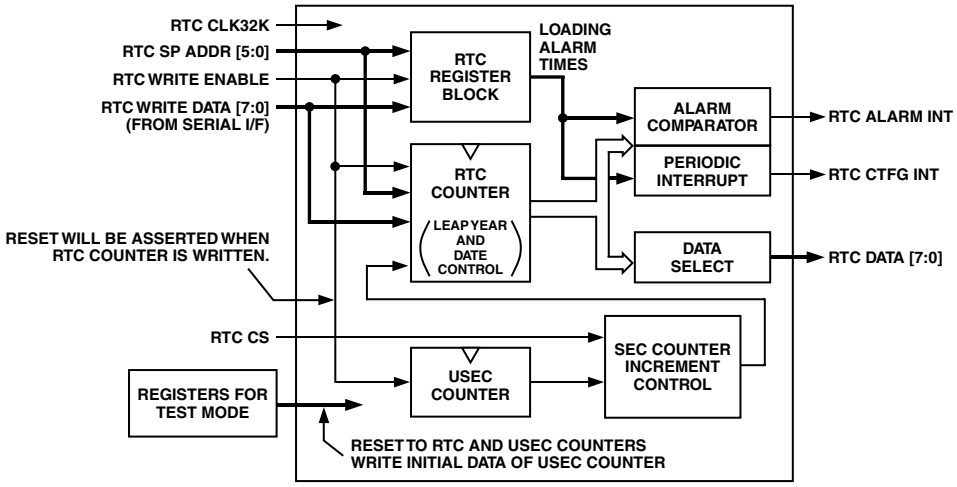


Figure 13. RTC Counter Block

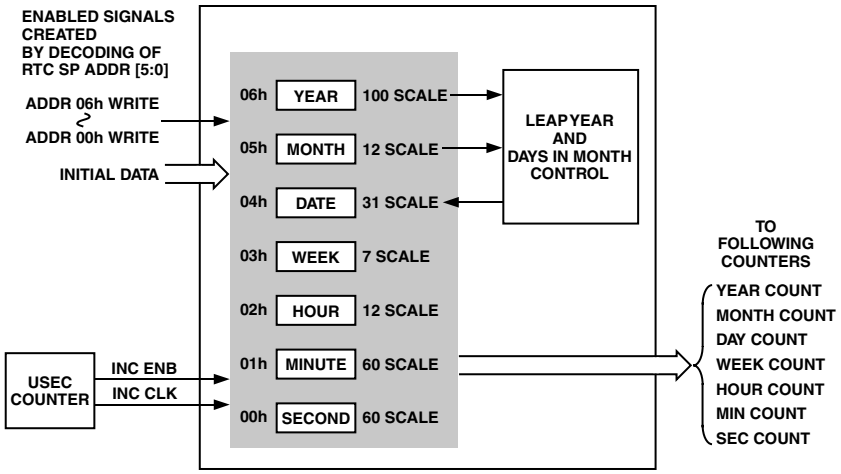


Figure 14. RTC Counter Block Diagram

Definition of Leap Year

For this device, the following definition of a leap year is used instead:

"A year that can be divided by 4."

Note:

- Year counter = "00" means year 2000 and is a leap year, because it can be divided by 400.
- Actual covered year period is from 1901 to 2099.

Number of Days of Month Control

- Months 1, 3, 5, 7, 8, 10, and 12 have 31 days.
- Months 4, 6, 9, and 11 have 30 days.
- Month 2 has 28 days but has 29 days in a leap year.

Alarm Function

Comparing the RTC counter value with the setting value in the alarm setting register (07h–09h), the alarm condition is detected. Setting of week uses seven bits for each day of the week and works with multiple day settings. There is a delay of 62 µs from alarm detection to setting up the AOUT/BOUT registers.

The ALA EN flag in the ALARM CONTROL register (0Dh) sets the enable/disable of the alarm detection. The INT register (1Eh) indicates the interrupt signals, ALARM INT of ALA or/and ALB. The INT MASK register (1Fh) does mask the alarm interrupt signal. The alarm detection state is indicated as AOUT of the ALARM CONTROL register (0Dh), and the alarm can be released by writing a "1" at the bit. Alarm B is controlled the same as Alarm A.

Note: Users just need to write a "1" to release the alarm and do not need to write a "0" after the "1." Users do not need to wait 62 µs from CS assertion.

Periodic Interrupt Function

This function generates interrupt periodically. The timing of the cycle can be selected from 2 Hz (0.5 sec clock pulse), 1 Hz (1 sec clock pulse), 1/60 Hz (minutes), 1/3600 Hz (hour), and month (first day of each month).

The cycle is set using the PI2–PI0 value in the periodic interrupt control, PIC register (0Eh). The state when interrupt is generated is indicated at the INTRA bit of PIC register (0Eh). The INT MASK register (1Fh) only masks the periodic interrupt signal. There are two periodic interrupt signal output patterns:

1. Hold the value when the interrupt occurs (level).
2. After the interrupt event happens, assert the interrupt signal in a certain time period and then release it (pulse).

In level case, interrupt occurs at each 0 min (1/60 Hz), 0 o'clock (1/3600 Hz), or the first day of the month. Because they happen in long cycles, the value is held at the register. After the CPU checks the state, it is released by writing a "1" to the PIC Bit of the PIC Register. If 2 Hz and 1 Hz, the interrupt is not held because the event happens in short cycles. These event signals output the pulse signal 2 Hz or 1 Hz in the RTC counter directly. The interrupt release operation doesn't affect the interrupt signal in this case.

Stay-Alive Timer

This is a counter that increments each 250 ms after RTC RESETIN N is asserted. It holds its value when the counter counts full up. Signal CLK4 is a 4 Hz (250 ms) clock that was generated in the USEC counter. The counter can be reset by writing a "1" at the CLR of the Stay-Alive TIMER CONTROL register (0Fh). The RTC RESETIN N signal is transferred from a logic input circuit that is supplied by VBAT of RESETIN N.

Note: Users just need to write a "1" to release the interrupt and do not need to write a "0" after the "1."

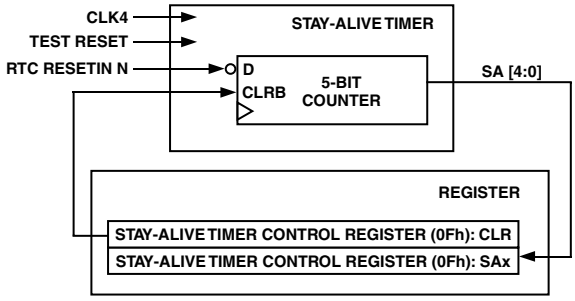


Figure 15. Stay-Alive Timer Block Diagram

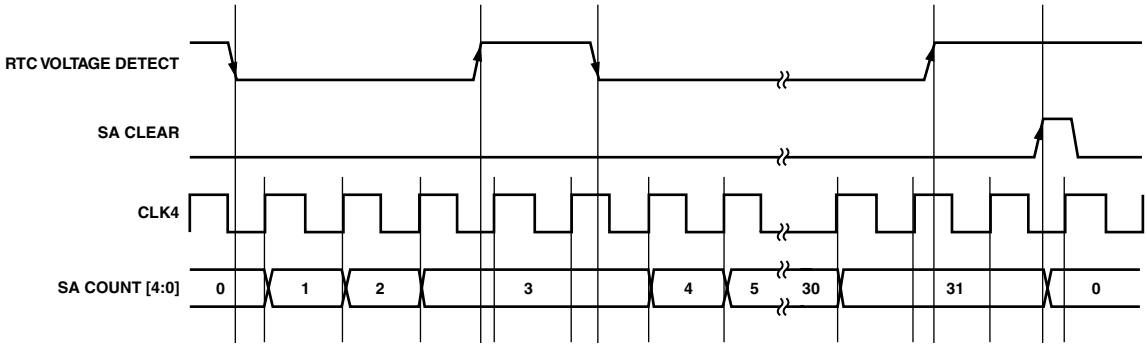


Figure 16. Stay-Alive Timer Operation Timing

Table V. Registers

ADDR	Description	D7	D6	D5	D4	D3	D2	D1	D0	Comments
00h	Second Counter			S5	S4	S3	S2	S1	S0	Note 1, 2
01h	Minute Counter			M5	M4	M3	M2	M1	M0	Note 1, 2
02h	Hour Counter				H4	H3	H2	H1	H0	Note 1, 2
03h	Week Counter						W2	W1	W0	Note 1, 2
04h	Day Counter				D4	D3	D2	D1	D0	Note 1, 2
05h	Month Counter					MO3	MO2	MO1	MO0	Note 1, 2
06h	Year Counter		Y6	Y5	Y4	Y3	Y2	Y1	Y0	Note 1, 2
07h	Alarm A Minute			AM5	AM4	AM3	AM2	AM1	AM0	Note 2
08h	Alarm A Hour				AH4	AH3	AH2	AH1	AH0	Note 2
09h	Alarm A Week		AW6	AW5	AW4	AW3	AW2	AW1	AW0	Note 2
0Ah	Alarm B Minute			BM5	BM4	BM3	BM2	BM1	BM0	Note 2
0Bh	Alarm B Hour				BH4	BH3	BH2	BH1	BH0	Note 2
0Ch	Alarm B Week		BW6	BW5	BW4	BW3	BW2	BW1	BW0	Note 2
0Dh	Alarm Control					ALA EN	AOUT	ALB EN	BOUT	Note 2
0Eh	Periodic Interrupt Control					PIC	PI2	PI1	PI0	Note 2
0Fh	Stay-Alive Timer Control			CLR	SA4	SA3	SA2	SA1	SA0	Note 2
10h	Charger Control							CHI	CHEN	Note 3
11h	Charger MVBAT Control							REF0	MVEN	Note 3
12h	Charger MVBAT		CHV1	CHV0	MV4	MV3	MV2	MV1	MV0	Note 3
13h	LDO Control 1						LDO11	LDO5	LDO4	Note 3
14h	Not Available									Note 4
15h	LDO Control 2			SLEEP9	SLEEP7	LDO10	LDO9	LDO8	LDO7	Note 3
16h	LDO Control 3								ALLOFF	Note 3
17h	LDO2 Gain					G23	G22	G21	G20	Note 3
18h	Keypad Column/LED				BL	KO3	KO2	KO1	KO0	Note 5
19h	Keypad Row Input			KI5	KI4	KI3	KI2	KI1	KI0	Note 5
1Ah	GPIO Control					GPC3	GPC2	GPC1	GPC0	Note 5
1Bh	GPIO MASK					GPMSK3	GPMSK2	GPMSK1	GPMSK0	Note 5
1Ch	GPIO					GPI3	GPI2	GPI1	GPIO	Note 5
						GPO3	GPO2	GPO1	GPO0	Note 5
1Dh	GPIO INT					GPINT3	GPINT2	GPINT1	GPINT0	Note 5, 6
						GPRST3	GPRST2	GPRST1	GPRST0	Note 5, 6
1Eh	INT		INT6	INT5	INT4	INT3	INT2	INT1	INT0	Note 5, 6
			IRST6	INT5	INT4	IRST3	IRST2	IRST1	IRST0	Note 5, 6
1Fh	INT MASK		MSK6	MSK5	MSK4	MSK3	MSK2	MSK1	MSK0	Note 5
20h	DATA IN			DI5	DI4	DI3	DI2	DI1	DI0	Note 5
21h	Power OFF								PWROFF	Note 5
22h	Power ON								PWRON	Note 5
3Fh	TEST Register (Option)						LDOENB	USENB	TEST	Note 2, 7

NOTES
1. For RTC counter data protection, access should wait for a certain time period (62 μs) after the CS signal assertion. (Refer to the RTC Counter Operation section for the wait time).
2. Registers regarding the RTC counter. They are powered by RTCV.
3. Analog block control registers. They control LDO and so on. They are powered by VBAT.
4. Not available.
5. These are the registers for INT, GPIO, KEYPAD I/F, and so on. They are powered by VBAT.
6. The INT reset operation will be valid at 62 μs or later after it's set.
7. This is a set register for an internal test and should not be accessed at normal operation.

APPLICATION INFORMATION

Input Voltage

The input voltage of the ADP3502 is 4.2 V and is optimized for a single Li-Ion cell. The thermal impedance of the ADP3502 is 56.2°C/W for 4-layer boards. Power dissipation should be calculated at the maximum ambient temperatures and battery voltage should not exceed the 125°C maximum allowable junction temperature. The junction and ambient temperature limits are selected to prevent both catastrophic package material deterioration and excessive device power output degradation. The ADP3502 can deliver the maximum power (0.71 W) up to 85°C ambient temperature. Figure 17 shows the maximum power dissipation as a function of ambient temperature.

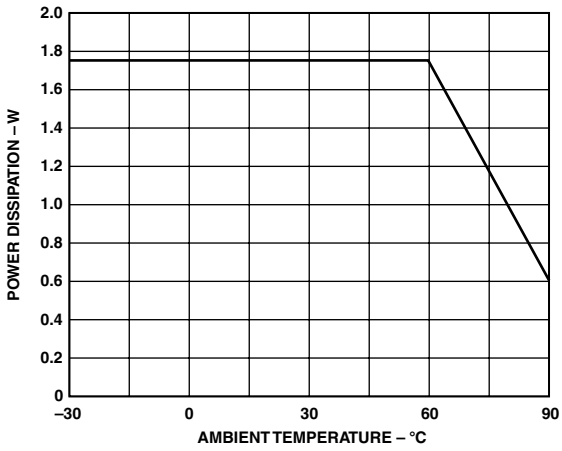


Figure 17. Power Dissipation vs. Temperature

Printed Circuit Board Layout Considerations

Use the following guidelines when designing printed circuit boards:

1. Connect the battery to the VBAT and BVS pins of the ADP3502. Kelvin-connect the BVS pin by running a separate trace to the VBAT pin. Locate the input capacitor, C13, in the Figure 18 as close as possible to these pins.
2. REFO, LDO2, LDO4, LDO8–LDO10, ADAPTER, and NRCAP capacitors should be returned to AGND.
3. LDO1, LDO3, LDO5–LDO7, LDO11, and VBAT capacitors should be returned to DGND.
4. Split the ground connections. Use separate traces or planes for the analog, digital, and power grounds and tie them together at a single point, preferably close to the battery return.
5. Kelvin-connect the charger's sense resistor by running separate traces to the ADAPTER and ISENSE pins. Make sure the traces are terminated as close to the resistor's body as possible.
6. Run a separate trace from the BVS pin to the battery to prevent a voltage drop error in the MVBAT measurement.
7. Use the best industry practice for thermal considerations during the layout of the ADP3502 and charger components. Careful use of the copper area, weight, and multilayer construction all contribute to improved thermal performance.

Input Capacitor Selection

For the input (ADAPTER and VBAT) of the ADP3502, a local bypass capacitor is recommended. Use a 10 µF, low ESR capacitor. Larger input capacitance and lower ESR provide better supply noise rejection and line-transient response. Multilayer ceramic chip (MLCC) capacitors provide the best combination of low ESR and small size but may not be cost effective. A lower cost alternative may be to use a 10 µF tantalum capacitor in parallel with a small (1 µF to 2 µF) ceramic capacitor (ceramic capacitors will produce the smallest supply ripple).

LDO Capacitor Selection

Low dropout regulators need capacitors on both their input and output. The input capacitor provides bypassing of the internal amplifier used in the voltage regulation loop. The output capacitor improves the regulator response to sudden load changes. The output capacitor determines the performance of any LDO. The LDO1, LDO4, LDO5, LDO7, LDO8, and LDO11 require a 2.2 µF capacitor, and the LDO2, LDO3, LDO6, LDO9, and LDO10 require a 1 µF capacitor. Transient response is a function of output capacitance. Larger values of output capacitance decrease peak deviations, providing improved transient response for large load current changes. Choose the capacitors by comparing their lead inductance, ESR, and dissipation factor. Output capacitor ESR affects stability. Note that the capacitance of some capacitor types show wide variations over temperature or with dc voltage. A good quality dielectric, X7R or better, capacitor is recommended.

The RTCV LDO can have a rechargeable coin cell or an electric double-layer capacitor as a load, but an additional 0.1 µF ceramic capacitor is recommended for stability and optimal performance.

RTCV LDO

The RTCV LDO charges a rechargeable coin cell to run the real-time clock module. It has been targeted to charge manganese lithium batteries, such as the ML series (ML621/ML1220) from Sanyo. With high energy density and relatively flat discharge characteristics, the lithium coin cell is widely used in mobile devices, such as cellular phones, digital cameras, and PDAs. The ML621 has a small physical size (6.8 mm diameter) and a nominal capacity of 2.5 mAh, which yields about 250 hours of backup time.

The nominal charging voltage is 3.0 V. This precise output voltage regulation charges the cell to more than 90% of its capacity. In addition, it features a very low quiescent of 50 µA typically. It requires an external low leakage diode for reverse current protection that is needed when the main battery is removed, and the coin cell supplies the RTCV pin.

Setting the Charge Current

The ADP3502 will control the charging operations when requested by the software. It includes a complete constant current/voltage single-cell lithium charge controller, as well as input current monitoring for the charger and voltage regulators. The ADP3502 will default to the lowest charge voltage of 3.50 V. To reach final charge on standard lithium batteries, the software must select one of the programmed values from this data sheet. The current comparator of the ADP3502 senses the voltage drop across an external sense resistor to control the average current for charging a battery. The voltage drop can be adjusted from 60 mV to 210 mV, giving a charging current limit from 300 mA to 1.05 A with a 0.2 Ω sense resistor. For lithium batteries, selecting the sense resistor, R_{SENSE}, programs the charge current. Use the following equation to select the current sense resistor, R_{SENSE}. The maximum battery charge current, I_{CHGR}, must be known.

$$R_{SENSE} = \frac{210\ mV}{I_{CHGR}}$$

Similarly, the end of charge current can be calculated from the low current limit threshold of 60 mV.

$$I_{LOW} = \frac{60\ mV}{R_{SENSE}}$$

CHARGER DIODE SELECTION

The diode, D3, shown in the Figure 18, is used to prevent the battery from discharging through the adapter supply. Choose a diode with a low leakage current but with a current rating high enough to handle the battery current and a voltage rating greater than VBAT. The blocking diode is required for lithium battery types.

External Pass Transistor Selection

The ADP3502 drives an external PNP pass transistor. The BASE pin drives the base of the transistor. The driver can draw up to 35 mA from the base of the pass device. The PNP pass transistor must meet specifications for:

- Current gain
- Power dissipation
- Collector current

The current gain, hfe, influences the maximum output current the circuit can deliver. The largest guaranteed output current is given by I_{CHGR} (max) = 35 mA × hfe (min). To ensure proper operation, the minimum V_{BE} the ADP3502 can provide must be enough to turn on the PNP. The available base drive voltage can be estimated using the following:

$$V_{BE} = V_{ADAPTER} - V_{DIODE} - V_{BASE}$$

where $V_{ADAPTER}$ (min) is the minimum adapter voltage, V_{BASE} is the base drive voltage, and V_{SENSE} is the maximum high current limit threshold voltage. The difference between the adapter voltage ($V_{ADAPTER}$) and the final battery voltage (V_{BAT}) must exceed the voltage drop due to the blocking diode, the sense resistor, and the saturation voltage of the PNP at the maximum charge current, where:

$$V_{CE(SAT)} = V_{ADAPTER} - V_{DIODE} - V_{SENSE} - V_{BAT}$$

The thermal characteristics of the PNP must be considered next. The transistor's rated power dissipation must exceed the actual power dissipated in the transistor. The worst-case dissipation can be determined using:

$$P_{DISS} = \left(V_{ADAPTER(MAX)} - V_{DIODE} - V_{BAT}\right) \times I_{CHGR}$$

It should be noted that the adapter voltage could be either preregulated or nonregulated. When preregulated, the difference between the maximum and minimum adapter voltage is probably not significant. When unregulated, the adapter voltage can have a wide range specified. However, the maximum voltage specified is usually with no load applied. Therefore, the worst-case power dissipation calculation will often lead to an overspecified pass device. In either case, it is best to determine the load characteristics of the adapter to optimize the charger design.

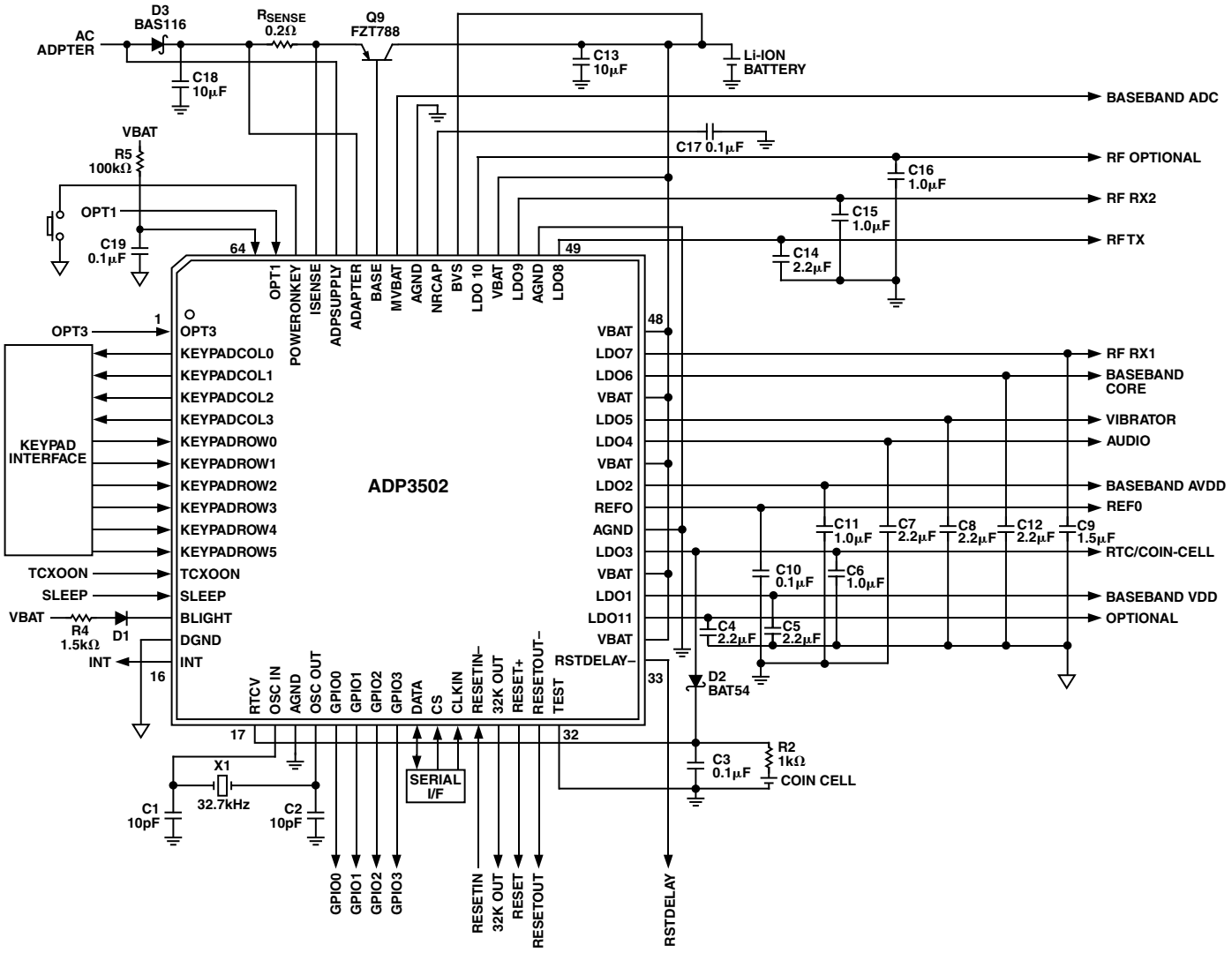
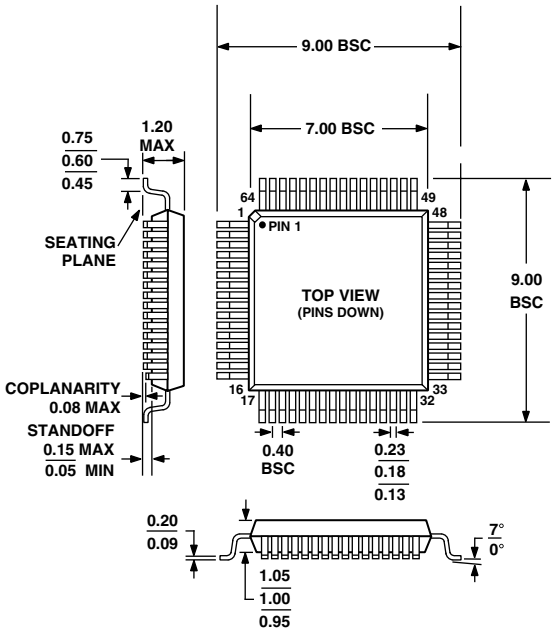


Figure 18. Typical Application Circuit

OUTLINE DIMENSIONS

64-Lead Thin Plastic Quad Flat Package [TQFP]
7 x 7 x 1.00 mm Body
(SU-64)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-026ABD

C03147–0–2/03(0)

PRINTED IN U.S.A.