


**ANALOG
DEVICES**

2 pF Off Capacitance, 1 pC Charge Injection, ±15 V/12 V 4:1 *i*CMOS™ Multiplexer

Preliminary Technical Data
ADG1204

FEATURES

2 pF off capacitance
 1 pC charge injection
 33 V supply range
 120 Ω on resistance
 Fully specified at +12 V, ± 15 V
 No V_L supply required
 3 V logic-compatible inputs
 Rail-to-rail operation
 14-lead TSSOP and 12-lead LFCSP
 Typical power consumption: <0.03 μ W

APPLICATIONS

Automatic test equipment
 Data acquisition systems
 Battery-powered systems
 Sample-and-hold systems
 Audio signal routing
 Communication systems

GENERAL DESCRIPTION

The ADG1204 is a CMOS analog multiplexer, comprising four single channels designed on an *i*CMOS process. *i*CMOS (industrial-CMOS) is a modular manufacturing process that combines high voltage CMOS (complementary metal-oxide semiconductor) and bipolar technologies. It enables the development of a wide range of high performance analog ICs capable of 30-V operation in a footprint that no other generation of high voltage parts has been able to achieve. Unlike analog ICs using conventional CMOS processes, *i*CMOS components can tolerate high supply voltages, while providing increased performance, dramatically lower power consumption, and reduced package size.

The ultralow capacitance and charge injection of these switches make them ideal solutions for data acquisition and sample-and-hold applications, where low glitch and fast settling are required. Fast switching speed coupled with high signal bandwidth make the parts suitable for video signal switching. *i*CMOS construction ensures ultralow power dissipation, making the parts ideally suited for portable and battery powered instruments.

FUNCTIONAL BLOCK DIAGRAM

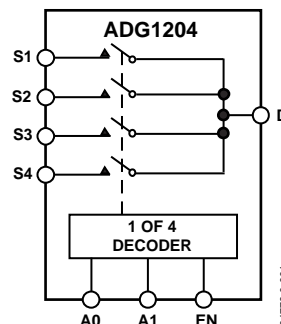


Figure 1.

The ADG1204 switches one of four inputs to a common output, D, as determined by the 3-bit binary address lines, A0, A1, and EN. Logic 0 on the EN pin disables the device. Each switch conducts equally well in both directions when on, and has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked. All switches exhibit break-before-make switching action. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

PRODUCT HIGHLIGHTS

1. 2 pF off capacitance (± 15 V supply).
2. 1 pC charge injection.
3. 3 V logic-compatible digital inputs:
 $V_{IH} = 2.0$ V, $V_{IL} = 0.8$ V
4. No V_L logic power supply required.
5. Ultralow power dissipation: <0.03 μ W.
6. 14-lead TSSOP and 12-lead 3 mm \times 3 mm LFCSP package.

Rev. PrD

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REVISION HISTORY

11/04—Revision PrD: Preliminary Version

SPECIFICATIONS

DUAL SUPPLY

$V_{DD} = 15\text{ V} \pm 10\%$, $V_{SS} = -15\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted.

Table 1.

Parameter	25°C	85°C	Y Version ¹	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance (R_{ON})	120	160	180	Ω typ Ω max	$V_S = \pm 10\text{ V}$, $I_S = -10\text{ mA}$; Figure 21
On Resistance Match between Channels (ΔR_{ON})	5			Ω typ	$V_S = \pm 10\text{ V}$, $I_S = -10\text{ mA}$
On Resistance Flatness ($R_{FLAT(ON)}$)	25		50	Ω max Ω typ Ω max	$V_S = -5\text{ V}, 0\text{ V}, +5\text{ V}$; $I_S = -10\text{ mA}$
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	± 0.01 ± 0.5	± 1	± 5	nA typ nA max	$V_{DD} = +10\text{ V}$, $V_{SS} = -10\text{ V}$ $V_S = 0\text{ V}/10\text{ V}$, $V_D = 10\text{ V}/0\text{ V}$; Figure 22
Drain Off Leakage, I_D (Off)	± 0.01 ± 0.5	± 1	± 5	nA typ nA max	$V_S = 0\text{ V}/10\text{ V}$, $V_D = 10\text{ V}/0\text{ V}$; Figure 22
Channel On Leakage, I_D , I_S (On)	± 0.04 ± 1	± 2	± 5	nA typ nA max	$V_S = V_D = 0\text{ V}$ or 10 V ; Figure 23
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005		± 0.5	μA typ μA max	$V_{IN} = V_{INL}$ or V_{INH}
Digital Input Capacitance, C_{IN}	5			pF typ	
DYNAMIC CHARACTERISTICS²					
Transition Time, t_{TRANS}	40			ns typ ns max	$R_L = 50\text{ }\Omega$, $C_L = 35\text{ pF}$ $V_S = \pm 10\text{ V}$; Figure 24
t_{ON} (EN)	40		90	ns typ ns max	$R_L = 50\text{ }\Omega$, $C_L = 35\text{ pF}$ $V_S = \pm 10\text{ V}$; Figure 24
t_{OFF} (EN)	20		40	ns typ ns max	$R_L = 50\text{ }\Omega$, $C_L = 35\text{ pF}$ $V_S = \pm 10\text{ V}$; Figure 24
Break-before-Make Time Delay, t_D	15		1	ns typ ns min	$R_L = 50\text{ }\Omega$, $C_L = 35\text{ pF}$ $V_{S1} = V_{S2} = 10\text{ V}$; Figure 25
Charge Injection	1			pC typ	$V_S = 0\text{ V}$, $R_S = 0\text{ }\Omega$, $C_L = 1\text{ nF}$; Figure 26
Off Isolation	75			dB typ	$R_L = 50\text{ }\Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; Figure 27
Channel-to-Channel Crosstalk	85			dB typ	$R_L = 50\text{ }\Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; Figure 28
Total Harmonic Distortion + Noise	0.002			% typ	$R_L = 600\text{ }\Omega$, 5 V rms , $f = 20\text{ Hz}$ to 20 kHz
-3 dB Bandwidth	700			MHz typ	$R_L = 50\text{ }\Omega$, $C_L = 5\text{ pF}$; Figure 29
C_S (Off)	2			pF typ	
C_D (Off)	7			pF typ	
C_D , C_S (On)	4			pF typ	
POWER REQUIREMENTS					
I_{DD}	0.001		5.0	μA typ μA max	$V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$ Digital Inputs = 0 V or V_{DD}
I_{DD}	150		300	μA typ μA max	Digital Inputs = 5 V
I_{SS}	0.001		5.0	μA typ μA max	Digital Inputs = 0 V or V_{DD}

Parameter	25°C	85°C	Y Version ¹	Unit	Test Conditions/Comments
I_{GND}	0.001			$\mu\text{A typ}$	Digital Inputs = 0 V or V_{DD}
I_{GND}	150		5.0	$\mu\text{A max}$	Digital Inputs = 5 V
			300	$\mu\text{A typ}$	
				$\mu\text{A max}$	

¹ Y Version temperature range is -40°C to $+125^{\circ}\text{C}$.

² Guaranteed by design, not subject to production test.

$V_{\text{DD}} = +5\text{ V} \pm 10\%$, $V_{\text{SS}} = -5\text{ V} \pm 10\%$, $\text{GND} = 0\text{ V}$, unless otherwise noted.

Table 2.

Parameter	25°C	85°C	Y Version ¹	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{SS} to V_{DD}	V	
On Resistance (R_{ON})	220			Ω typ Ω max	$V_{\text{S}} = \pm 3.3\text{ V}$, $I_{\text{S}} = -10\text{ mA}$; Figure 21
On Resistance Match between Channels (ΔR_{ON})	10			Ω typ	
On Resistance Flatness ($R_{\text{FLAT(ON)}}$)	30			Ω max Ω typ Ω max	$V_{\text{S}} = \pm 3.3\text{ V}$, $I_{\text{S}} = -10\text{ mA}$ $V_{\text{S}} = \pm 3.3\text{ V}$, $I_{\text{S}} = -10\text{ mA}$
LEAKAGE CURRENTS					
Source Off Leakage, I_{S} (Off)	± 0.01 ± 0.5	± 1	± 5	nA typ nA max	$V_{\text{DD}} = 5.5\text{ V}$, $V_{\text{SS}} = -5.5\text{ V}$ $V_{\text{D}} = \pm 4.5\text{ V}$, $V_{\text{S}} = \pm 4.5\text{ V}$; Figure 22
Drain Off Leakage, I_{D} (Off)	± 0.01 ± 0.5	± 1	± 5	nA typ nA max	$V_{\text{D}} = \pm 4.5\text{ V}$, $V_{\text{S}} = \pm 4.5\text{ V}$; Figure 22
Channel On Leakage, I_{D} , I_{S} (On)	± 0.04 ± 1	± 2	± 5	nA typ nA max	$V_{\text{D}} = V_{\text{S}} = \pm 4.5\text{ V}$; Figure 23
DIGITAL INPUTS					
Input High Voltage, V_{INH}		2.0		V min	
Input Low Voltage, V_{INL}		0.8		V max	
Input Current, I_{INL} or I_{INH}	0.005		± 0.5	$\mu\text{A typ}$ $\mu\text{A max}$	$V_{\text{IN}} = V_{\text{INL}}$ or V_{INH}
Digital Input Capacitance, C_{IN}	5			pF typ	
DYNAMIC CHARACTERISTICS²					
t_{ON}	160			ns typ ns max	$R_{\text{L}} = 300\ \Omega$, $C_{\text{L}} = 35\text{ pF}$ $V_{\text{S}} = 3\text{ V}$; Figure 24
t_{OFF}	60			ns typ ns max	$R_{\text{L}} = 300\ \Omega$, $C_{\text{L}} = 35\text{ pF}$ $V_{\text{S}} = 3\text{ V}$; Figure 24
Break-before-Make Time Delay, t_{D}	50			ns typ ns min	$R_{\text{L}} = 300\ \Omega$, $C_{\text{L}} = 35\text{ pF}$ $V_{\text{S1}} = V_{\text{S2}} = 3\text{ V}$; Figure 25
Charge Injection	20		1	pC typ pC max	$V_{\text{S}} = 0\text{ V}$, $R_{\text{S}} = 0\ \Omega$, $C_{\text{L}} = 1\text{ nF}$; Figure 26
Off Isolation	56			dB typ	$R_{\text{L}} = 50\ \Omega$, $C_{\text{L}} = 5\text{ pF}$, $f = 1\text{ MHz}$; Figure 27
Channel-to-Channel Crosstalk	60			dB typ	$R_{\text{L}} = 50\ \Omega$, $C_{\text{L}} = 5\text{ pF}$, $f = 1\text{ MHz}$; Figure 28
-3 dB Bandwidth	20			MHz typ	$R_{\text{L}} = 50\ \Omega$, $C_{\text{L}} = 5\text{ pF}$; Figure 29
C_{S} (Off)	15			pF typ	$f = 1\text{ MHz}$
C_{D} (Off)				pF typ	$f = 1\text{ MHz}$
C_{D} , C_{S} (On)	100			pF typ	$f = 1\text{ MHz}$

Parameter	25°C	85°C	Y Version ¹	Unit	Test Conditions/Comments
POWER REQUIREMENTS					$V_{DD} = +5.5\text{ V}$, $V_{SS} = -5.5\text{ V}$
I_{DD}	0.001		5.0	$\mu\text{A typ}$	Digital Inputs = 0 V or 5.5 V
I_{SS}	0.001		5.0	$\mu\text{A max}$ $\mu\text{A typ}$ $\mu\text{A max}$	Digital Inputs = 0 V or 5.5 V

¹ Y Version temperature range is -40°C to $+125^{\circ}\text{C}$.

² Guaranteed by design, not subject to production test.

SINGLE SUPPLY

$V_{DD} = 12\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $\text{GND} = 0\text{ V}$, unless otherwise noted.

Table 3.

Parameter	25°C	85°C	Y Version ¹	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance (R_{ON})	220			Ω typ Ω max	$V_S = 10\text{ V}$, $I_S = -10\text{ mA}$; Figure 21
On Resistance Match between Channels (ΔR_{ON})	1			Ω typ Ω max	$V_S = 10\text{ V}$, $I_S = -10\text{ mA}$
On Resistance Flatness ($R_{FLAT(ON)}$)	12			Ω typ	$V_S = 3\text{ V}, 6\text{ V}, 9\text{ V}$; $I_S = -10\text{ mA}$
LEAKAGE CURRENTS					$V_{DD} = 12\text{ V}$
Source Off Leakage, I_S (Off)	± 0.01 ± 0.5	± 1	± 5	nA typ nA max	$V_S = 1\text{ V}/10\text{ V}$, $V_D = 10\text{ V}/1\text{ V}$; Figure 22
Drain Off Leakage, I_D (Off)	± 0.01 ± 0.5	± 1	± 5	nA typ nA max	$V_S = 1\text{ V}/10\text{ V}$, $V_D = 10\text{ V}/1\text{ V}$; Figure 22
Channel On Leakage, I_D , I_S (On)	± 0.04 ± 1	± 2	± 5	nA typ nA max	$V_S = V_D = 1\text{ V}$ or 10 V ; Figure 23
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.001		± 0.5	$\mu\text{A typ}$ $\mu\text{A max}$	$V_{IN} = V_{INL}$ or V_{INH}
Digital Input Capacitance, C_{IN}	5			pF typ	
DYNAMIC CHARACTERISTICS ²					
Transition Time, t_{TRANS}	40			ns typ ns max	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$ $V_S = \pm 10\text{ V}$; Figure 24
t_{ON} (EN)	50			ns typ ns max	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 8\text{ V}$; Figure 24
t_{OFF} (EN)	15			ns typ ns max	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 8\text{ V}$; Figure 24
Break-before-Make Time Delay, t_D	15		1	ns typ ns min	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$ $V_{S1} = V_{S2} = 8\text{ V}$; Figure 25
Charge Injection	5			pC typ	$V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; Figure 26
Off Isolation	75			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; Figure 27
Channel-to-Channel Crosstalk	85			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; Figure 28
-3 dB Bandwidth	700			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; Figure 29
C_S (Off)	2			pF typ	
C_D (Off)	2			pF typ	
C_D , C_S (On)	4			pF typ	

Parameter	25°C	85°C	Y Version ¹	Unit	Test Conditions/Comments
POWER REQUIREMENTS					$V_{DD} = 13.2\text{ V}$
I_{DD}	0.001		5.0	$\mu\text{A typ}$	Digital inputs = 0 V or V_{DD}
I_{DD}	150		300	$\mu\text{A max}$	Digital inputs = 5 V
				$\mu\text{A typ}$	
				$\mu\text{A max}$	

¹ Y Version temperature range is -40°C to $+125^{\circ}\text{C}$.² Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 4.

Parameter	Rating
V_{DD} to V_{SS}	38 V
V_{DD} to GND	−0.3 V to +25 V
V_{SS} to GND	+0.3 V to −25 V
Analog Inputs ¹	$V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$
Digital Inputs	GND − 0.3 V to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Peak Current, S or D	100 mA (pulsed at 1 ms, 10% duty cycle max)
Continuous Current, S or D	30 mA
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Automotive (Y Version)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
14-Lead TSSOP, θ_{JA} Thermal Impedance	150.4°C/W
12-Lead LFCSP, θ_{JA} Thermal Impedance	30.4°C/W
Lead Temperature, Soldering	
Vapor Phase (60 s)	215°C
Infrared (15 s)	220°C

¹ Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

TRUTH TABLE

Table 5.

EN	A1	A0	S1	S2	S3	S4
0	X	X	Off	Off	Off	Off
1	0	0	On	Off	Off	Off
1	0	1	Off	On	Off	Off
1	1	0	Off	Off	On	Off
1	1	1	Off	Off	Off	On

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

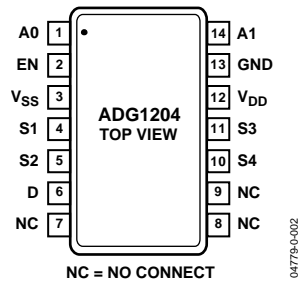


Figure 2. TSSOP Pin Configuration

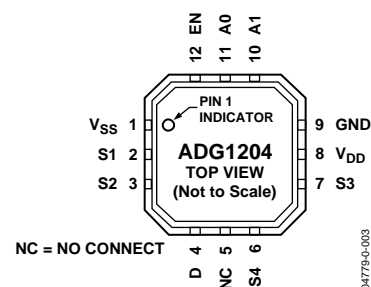


Figure 3. LFCSP Pin Configuration

Table 6. Pin Function Descriptions

Pin No.		Mnemonic	Function
TSSOP	LFCSP		
1	11	A0	Logic Control Input.
2	12	EN	Active High Digital Input. When low, the device is disabled and all switches are off. When high, Ax logic inputs determine on switches.
3	1	V _{SS}	Most Negative Power Supply Potential.
4	2	S1	Source Terminal. Can be an input or an output.
5	3	S2	Source Terminal. Can be an input or an output.
6	4	D	Drain Terminal. Can be an input or an output.
7–9	5	NC	No Connection.
10	6	S4	Source Terminal. Can be an input or an output.
11	7	S3	Source Terminal. Can be an input or an output.
12	8	V _{DD}	Most Positive Power Supply Potential.
13	9	GND	Ground (0 V) Reference.
14	10	A1	Logic Control Input.

TERMINOLOGY

I_{DD}

The positive supply current.

I_{SS}

The negative supply current.

V_D (V_S)

The analog voltage on Terminals D and S.

R_{ON}

The ohmic resistance between D and S.

R_{FLAT(ON)}

Flatness is defined as the difference between the maximum and minimum value of on resistance, as measured over the specified analog signal range.

I_S (Off)

The source leakage current with the switch off.

I_D (Off)

The drain leakage current with the switch off.

I_D, I_S (On)

The channel leakage current with the switch on.

V_{INL}

The maximum input voltage for Logic 0.

V_{INH}

The minimum input voltage for Logic 1.

I_{INL} (I_{INH})

The input current of the digital input.

C_S (Off)

The off switch source capacitance, which is measured with reference to ground.

C_D (Off)

The off switch drain capacitance, which is measured with reference to ground.

C_D, C_S (On)

The on switch capacitance, which is measured with reference to ground.

C_{IN}

The digital input capacitance.

t_{ON} (EN)

The delay between applying the digital control input and the output switching on. See Figure 24, Test Circuit 4.

t_{OFF} (EN)

The delay between applying the digital control input and the output switching off.

Charge Injection

A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Off Isolation

A measure of unwanted signal coupling through an off switch.

Crosstalk

A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Bandwidth

The frequency at which the output is attenuated by 3 dB.

On Response

The frequency response of the on switch.

Insertion Loss

The loss due to the on resistance of the switch.

THD + N

The ratio of the harmonic amplitude plus noise of the signal to the fundamental.

t_{TRANS}

The delay time between the 50% and 90% points of the digital input and switch on condition when switching from one address state to another.

TYPICAL PERFORMANCE CHARACTERISTICS



Figure 4. On Resistance as a Function of V_D (V_S) for Single Supply



Figure 7. On Resistance as a Function of V_D (V_S) for Different Temperatures, Single Supply



Figure 5. On Resistance as a Function of V_D (V_S) for Dual Supply

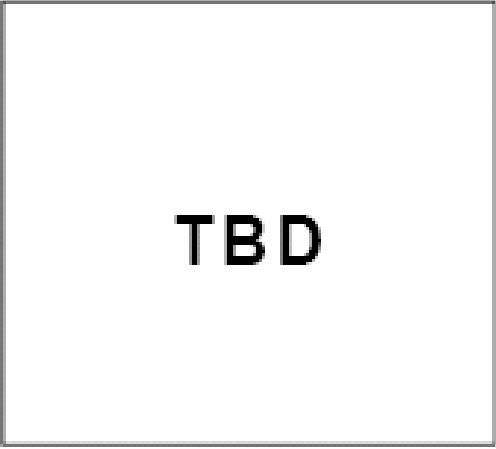


Figure 8. On Resistance as a Function of V_D (V_S) for Different Temperatures, Dual Supply



Figure 6. On Resistance as a Function of V_D (V_S) for Different Temperatures, Single Supply

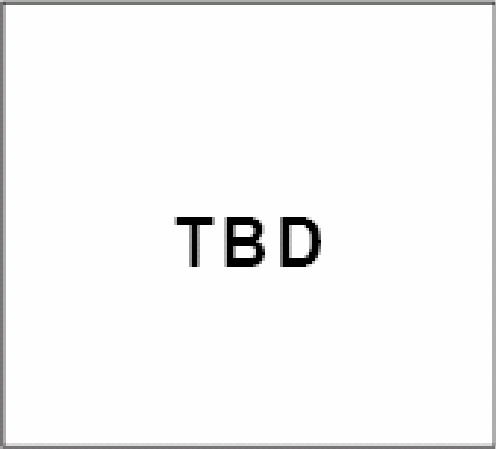


Figure 9. Leakage Currents as a Function of V_D (V_S)



TBD

Figure 10. Leakage Currents as a Function of V_O (V_S)



TBD

Figure 13. Leakage Currents as a Function of Temperature



TBD

Figure 11. Leakage Currents as a Function of V_O (V_S)



TBD

Figure 14. Supply Currents vs. Input Switching Frequency



TBD

Figure 12. Leakage Currents as a Function of Temperature



TBD

Figure 15. Charge Injection vs. Source Voltage



TBD

Figure 16. t_{ON}/t_{OFF} Times vs. Temperature



TBD

Figure 19. On Response vs. Frequency



TBD

Figure 17. Off Isolation vs. Frequency



TBD

Figure 20. THD + N vs. Frequency



TBD

Figure 18. Crosstalk vs. Frequency

TEST CIRCUITS

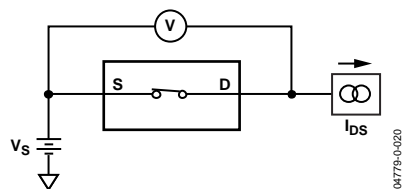


Figure 21. Test Circuit 1—On Resistance

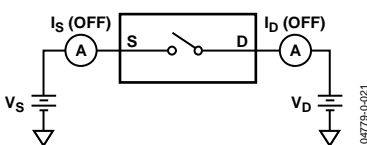


Figure 22. Test Circuit 2—Off Leakage

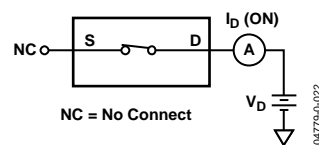


Figure 23. Test Circuit 3—On Leakage

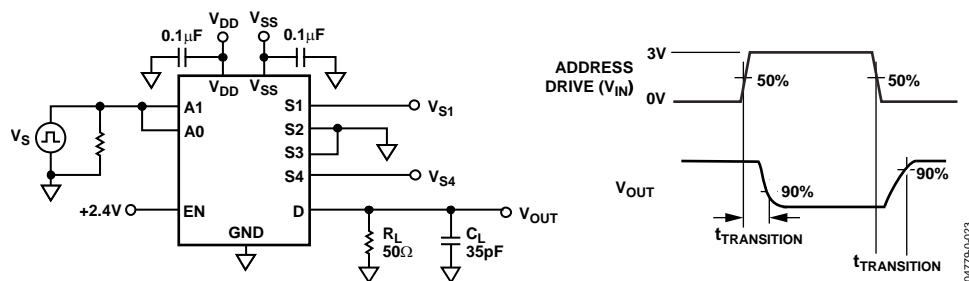


Figure 24. Test Circuit 4—Address to Output Switching Times

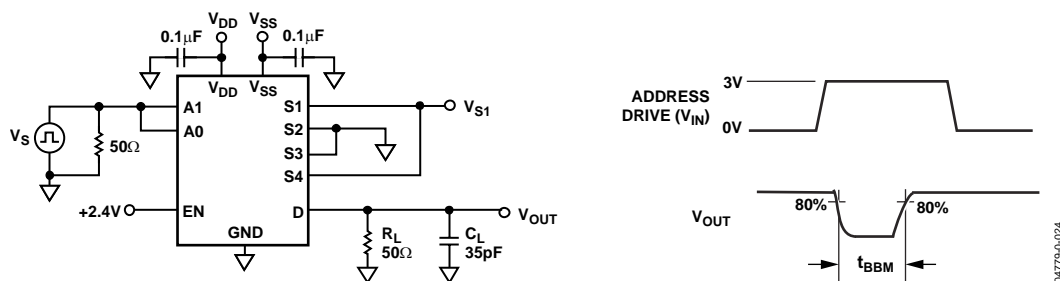


Figure 25. Test Circuit 5—Break-before-Make Time

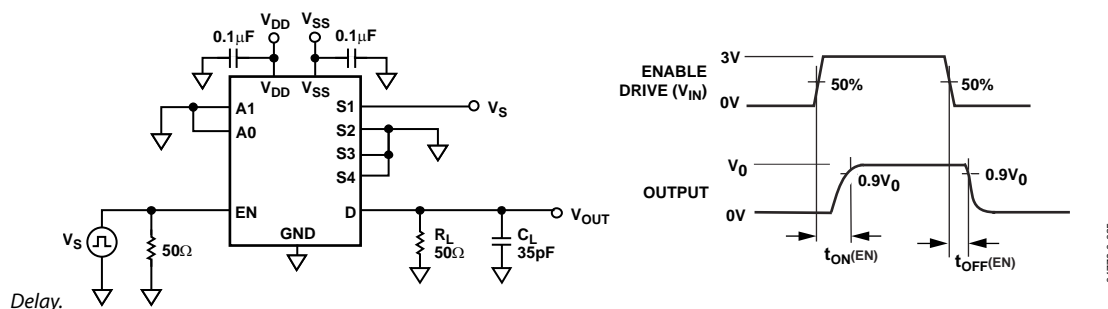


Figure 26. Test Circuit 6—Enable to Output Switching Delay

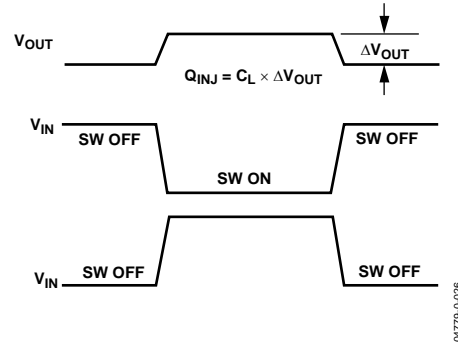
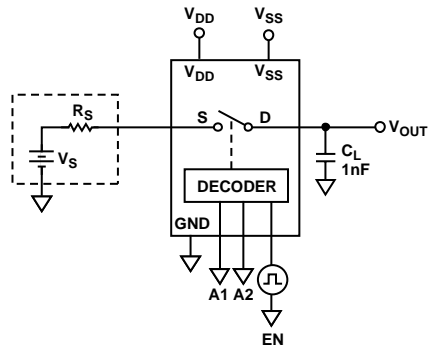


Figure 27. Test Circuit 7—Charge Injection

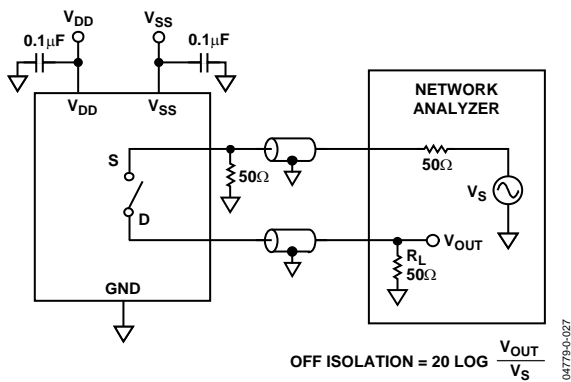


Figure 28. Test Circuit 8—Off Isolation

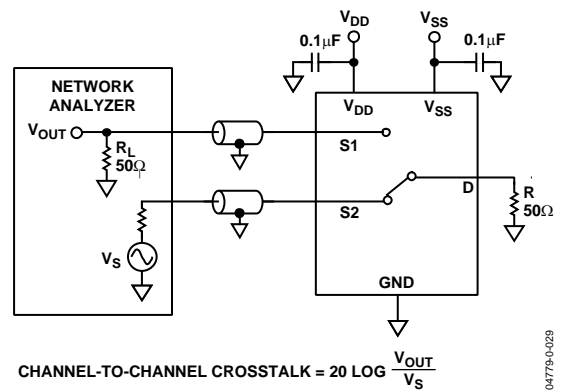


Figure 30. Test Circuit 10—Channel-to-Channel Crosstalk

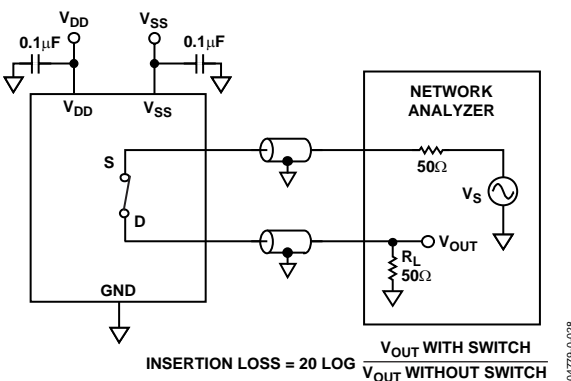


Figure 29. Test Circuit 9—Bandwidth

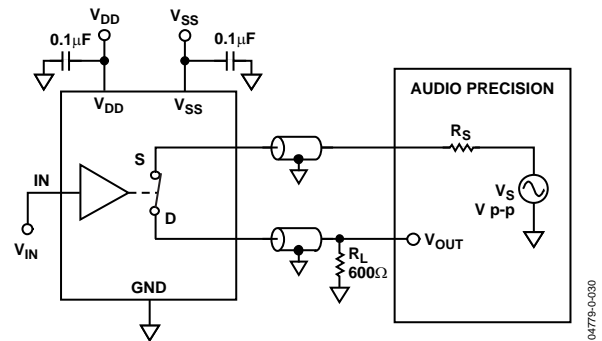
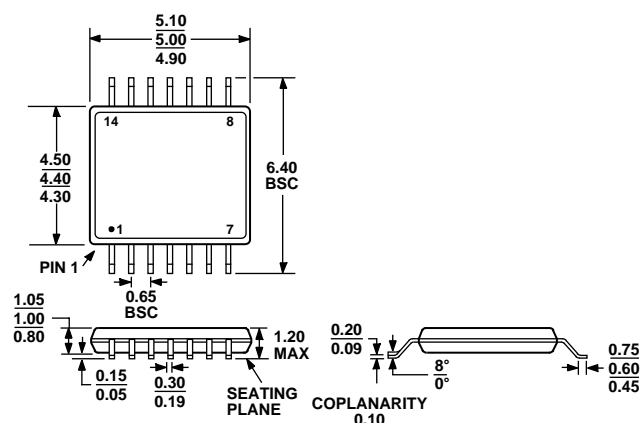


Figure 31. Test Circuit 11—THD + Noise

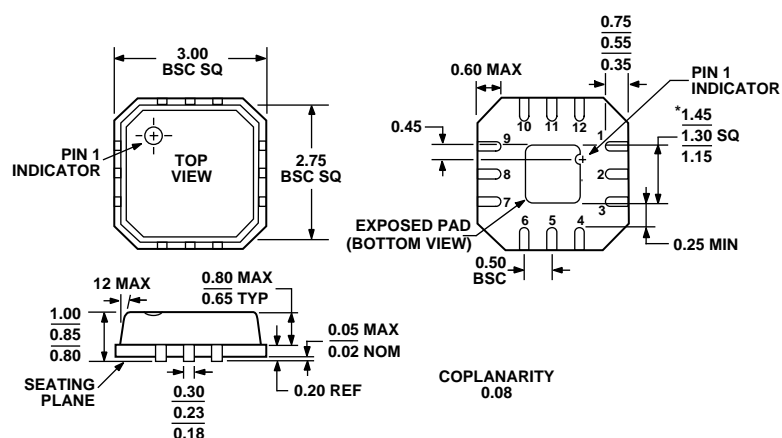
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153AB-1

Figure 32. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)

Dimension shown in millimeters



*COMPLIANT TO JEDEC STANDARDS MO-220-VEED-1
EXCEPT FOR EXPOSED PAD DIMENSION.

Figure 33. 12-Lead Lead Frame Chip Scale Package [VQ_LFCSP]
3 mm x 3 mm Body, Very Thin Quad
(CP-12-1)

Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG1204YRU	−40°C to +125°C	Thin Shrink Small Outline Package (TSSOP)	RU-14
ADG1204YCP	−40°C to +125°C	Lead Frame Chip Scale Package (LFCSP)	CP-12-1

NOTES