PA241

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FEATURES

- MONOLITHIC MOS TECHNOLOGY
- LOW COST
- HIGH VOLTAGE OPERATION—350V
- LOW QUIESCENT CURRENT TYP.—2.2mA
- NO SECOND BREAKDOWN
- HIGH OUTPUT CURRENT—120mA PEAK
- AVAILABLE IN DIE FORM—CPA241

8-PIN TO-3
PACKAGE STYLE CE

24-PIN PSOP
PACKAGE STYLE DF

10-PIN SIP
PACKAGE STYLE DW

APPLICATIONS

- PIEZO ELECTRIC POSITIONING
- ELECTROSTATIC TRANSDUCER & DEFLECTION
- DEFORMABLE MIRROR FOCUSING
- BIOCHEMISTRY STIMULATORS
- COMPUTER TO VACUUM TUBE INTERFACE

DESCRIPTION

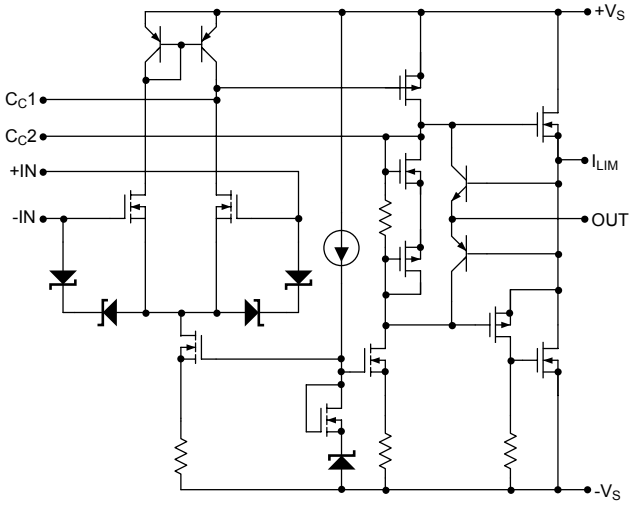
The PA241 is a high voltage monolithic MOSFET operational amplifier which achieves performance features previously found only in hybrid designs while increasing reliability. Inputs are protected from excessive common mode and differential mode voltages. The safe operating area (SOA) has no second breakdown limitation and can be observed with all type loads by choosing an appropriate current limiting resistor. External compensation provides the user flexibility in choosing optimum gain and bandwidth for the application.

The PA241CE is packaged in a hermetically sealed 8-pin TO-3 package. The metal case of the PA241CE is isolated in excess of full supply voltage.

The PA241DF is packaged in a 24 pin PSOP (JEDEC MO-166) package. The metal heat slug of the PA241DF is isolated in excess of full supply voltage.

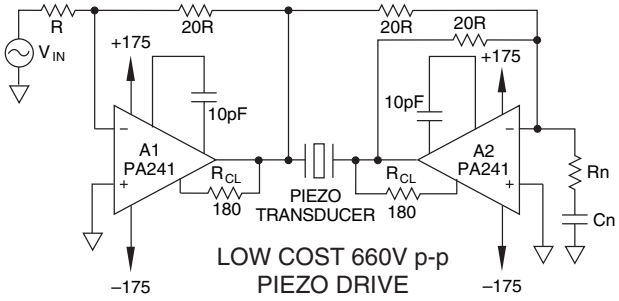
The PA241DW is packaged in Apex's hermetic ceramic SIP package. The alumina ceramic isolates the die in excess of full supply voltage.

EQUIVALENT SCHEMATIC



TYPICAL APPLICATION

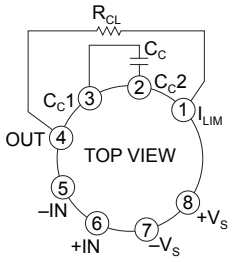
Ref: APPLICATION NOTE 20: "Bridge Mode Operation of Power Amplifiers"



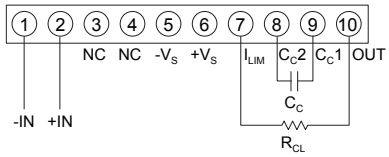
Two PA241 amplifiers operated as a bridge driver for a piezo transducer provides a low cost 660 volt total drive capability. The R_N C_N network serves to raise the apparent gain of A2 at high frequencies. If R_N is set equal to R the amplifiers can be compensated identically and will have matching bandwidths.

EXTERNAL CONNECTIONS

PA241CE

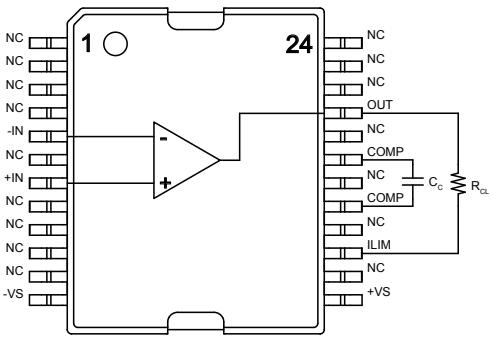


PA241DW



For CC values, see graph on page 4.
Note: CC must be rated for full supply voltage.

PA241DF



NOTE: PA241CE Recommended mounting torque is 4-7 in•lbs (.45 -.79 N•m)

CAUTION: The use of compressible, thermally conductive insulators may void warranty.

ABSOLUTE MAXIMUM RATINGS

	PA241CE PA241CEA	PA241DF PA241DFA
SUPPLY VOLTAGE, $+V_S$ to $-V_S$	350V	350V
OUTPUT CURRENT, continuous within SOA	60 mA	60 mA
OUTPUT CURRENT, peak	120 mA	120 mA
POWER DISSIPATION, continuous @ T_C = 25°C	12W	12W
INPUT VOLTAGE, differential	±16 V	±16 V
INPUT VOLTAGE, common mode	$\pm V_S$	$\pm V_S$
TEMPERATURE, pin solder – 10 sec	300°C	220°C
TEMPERATURE, junction[2]	150°C	150°C
TEMPERATURE, storage	–65 to +150°C	–65 to +150°C
TEMPERATURE RANGE, powered (case)	–40 to +125°C	–40 to +125°C

SPECIFICATIONS

PARAMETER	TEST CONDITIONS[1]	PA241CE, PA241DF MIN	PA241CE, PA241DF TYP	PA241CE, PA241DF MAX	PA241CEA MIN	PA241CEA TYP	PA241CEA MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial			25	40		15	30	mV
OFFSET VOLTAGE, vs. temperature[3]	Full temperature range		100	500		*	*	µV/°C
OFFSET VOLTAGE, vs supply			3			*		µV/V
OFFSET VOLTAGE, vs time			70	130		*	*	µV/kh
BIAS CURRENT, initial[6]			5/50	50/200		*	*	pA
BIAS CURRENT, vs supply			0.2/2			*		pA/V
OFFSET CURRENT, initial[6]			2.5/50	50/200		*	*	pA
INPUT IMPEDANCE, DC			10^{11}			*		
INPUT CAPACITANCE			6			*		pF
COMMON MODE, voltage range		$+V_S$–14			*			V
COMMON MODE, voltage range		$-V_S$+12			*			V
COMMON MODE REJECTION, DC	V_{CM} = ±90V DC	84	94		*	*		dB
NOISE, broad band	10kHz BW, R_S = 1K		50			*		µV RMS
NOISE, low frequency	1-10 Hz		125			*		µV p-p
GAIN								
OPEN LOOP at 15Hz	R_L = 5K	90	96		*	*		dB
BANDWIDTH, gain bandwidth product			3			*		MHz
POWER BANDWIDTH	280V p-p		30			*		kHz
OUTPUT								
VOLTAGE SWING	I_O = 40mA	$\pm V_S$–12	$\pm V_S$–10		$\pm V_S$–10	$\pm V_S$–8.5		V
CURRENT, peak[4]		120			*			mA
CURRENT, continuous		60			*			mA
SETTLING TIME to .1%	10V step, A_V = –10		2			*		µs
SLEW RATE	C_C = 3.3pF		30			*		V/µs
RESISTANCE[5], 1mA	R_{CL} = 0		150			*		Ω
RESISTANCE[5], 40 mA	R_{CL} = 0		5			*		Ω
POWER SUPPLY								
VOLTAGE		±50	±150	±175	*	*	*	V
CURRENT, quiescent			2.2	2.5		*	2.3	mA
THERMAL								
PA241CE RESISTANCE, AC junction to case	F > 60Hz		5.4	6.5		*	*	°C/W
PA241DF RESISTANCE, AC junction to case	F > 60Hz		6	7		*	*	°C/W
PA241CE RESISTANCE, DC junction to case	F < 60Hz		9	10.4		*	*	°C/W
PA241DF RESISTANCE, DC junction to case	F < 60Hz		9	11		*	*	°C/W
PA241CE RESISTANCE, junction to air	Full temperature range		30			*		°C/W
PA241DF RESISTANCE, junction to air[7]	Full temperature range		25			*		°C/W
TEMPERATURE RANGE, case	Meets full range spec's	–25		+85	*		*	°C

NOTES: * "A" specification is the same as the non "A" specification.

1. Unless otherwise noted T_C = 25°C, C_C = 6.8pF. DC input specifications are ± value given. Power supply voltage is typical rating.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to heatsink data sheet.
3. Sample tested by wafer to 95%.
4. Guaranteed but not tested.
5. The selected value of R_{CL} must be added to the values given for total output resistance.
6. Specifications separated by / indicate values for the PA241CE and PA241DF respectively.
7. Rating applies with solder connection of heatslug to a minimum 1 square inch foil area of the printed circuit board.

CAUTION The PA241 is constructed from MOSFET transistors. ESD handling procedures must be observed.

ABSOLUTE MAXIMUM RATINGS

	PA241DW PA241DWA
SUPPLY VOLTAGE, $+V_S$ to $-V_S$	350V
OUTPUT CURRENT, continuous within SOA	60 mA
OUTPUT CURRENT, peak	120 mA
POWER DISSIPATION, continuous @ T_C = 25°C	9W
INPUT VOLTAGE, differential	±16 V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder – 10 sec	220°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE, storage	–65 to +150°C
TEMPERATURE RANGE, powered (case)	–40 to +125°C

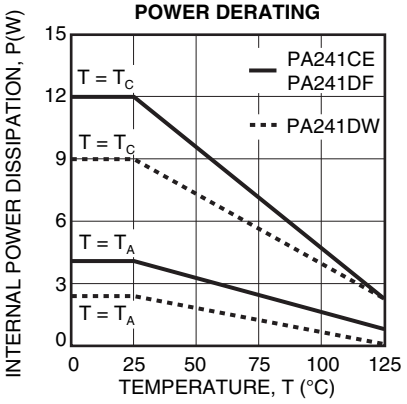
SPECIFICATIONS

		PA241DW			PA241DWA			
PARAMETER	**TEST CONDITIONS[1]**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT								
OFFSET VOLTAGE, initial			25	40		15	30	mV
OFFSET VOLTAGE, vs. temperature[3]	Full temperature range		100	500		*	*	µV/°C
OFFSET VOLTAGE, vs supply			3			*		µV/V
OFFSET VOLTAGE, vs time			70	130		*		µV/kh
BIAS CURRENT, initial			100	2000		*	*	pA
BIAS CURRENT, vs supply			15	50		*	*	pA/V
OFFSET CURRENT, initial			100	400		*	*	pA
INPUT IMPEDANCE, DC			10^{11}			*		
INPUT CAPACITANCE			6			*		pF
COMMON MODE, voltage range		$+V_S$–14			*			V
COMMON MODE, voltage range		$-V_S$+12			*			V
COMMON MODE REJECTION, DC	V_{CM} = ±90V DC	84	94		*	*		dB
NOISE, broad band	10kHz BW, R_S = 1K		50			*		µV RMS
NOISE, low frequency	1-10 Hz		125			*		µV p-p
GAIN								
OPEN LOOP at 15Hz	R_L = 5K	90	96		*	*		dB
BANDWIDTH, gain bandwidth product			3			*		MHz
POWER BANDWIDTH	280V p-p		30			*		kHz
OUTPUT								
VOLTAGE SWING	I_O = 40mA	$\pm V_S$–12	$\pm V_S$–10		$\pm V_S$–10	$\pm V_S$–8.5		V
CURRENT, peak[4]		120			*			mA
CURRENT, continuous		60			*			mA
SETTLING TIME to .1%	10V step, A_V = –10		2			*		µs
SLEW RATE	C_C = 3.3pF		30			*		V/µs
RESISTANCE[5], 1mA	R_{CL} = 0		150			*		Ω
RESISTANCE[5], 40 mA	R_{CL} = 0		5			*		Ω
POWER SUPPLY								
VOLTAGE		±50	±150	±175	*	*	*	V
CURRENT, quiescent			2.2	2.5		*	2.3	mA
THERMAL								
PA241DW RESISTANCE, AC junction to case	F > 60Hz		7	10		*	*	°C/W
PA241DW RESISTANCE, DC junction to case	F < 60Hz		12	14		*	*	°C/W
PA241DW RESISTANCE, junction to air	Full temperature range		55			*		°C/W
TEMPERATURE RANGE, case	Meets full range spec's	–25		+85	*		*	°C

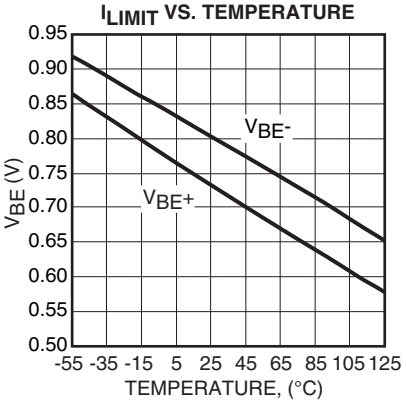
NOTES: * "A" specification is the same as the non "A" specification.
1. Unless otherwise noted T_C = 25°C, C_C = 6.8pF. DC input specifications are ± value given. Power supply voltage is typical rating.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to heatsink data sheet.
3. Sample tested by wafer to 95%.
4. Guaranteed but not tested.
5. The selected value of R_{CL} must be added to the values given for total output resistance.

CAUTION The PA241 is constructed from MOSFET transistors. ESD handling procedures must be observed.

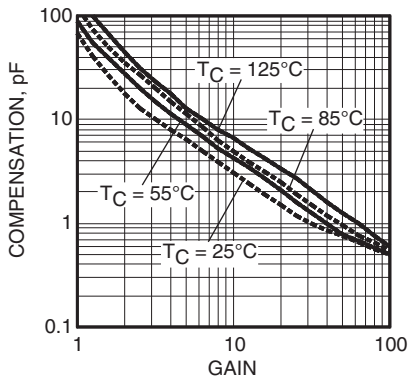
POWER DERATING



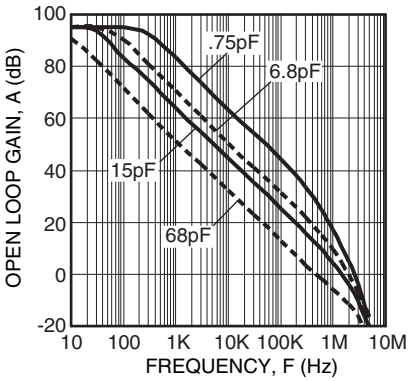
I_{LIMIT} VS. TEMPERATURE



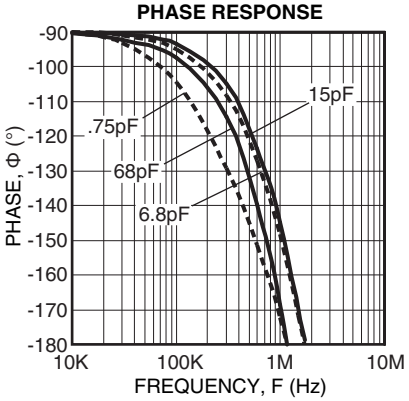
GAIN AND COMPENSATION



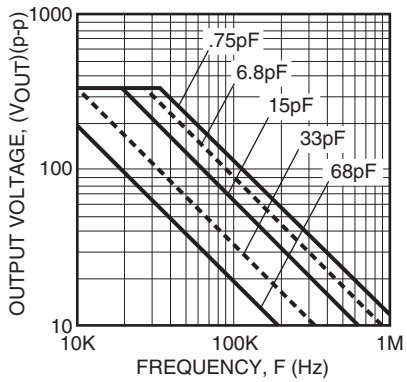
SMALL SIGNAL RESPONSE



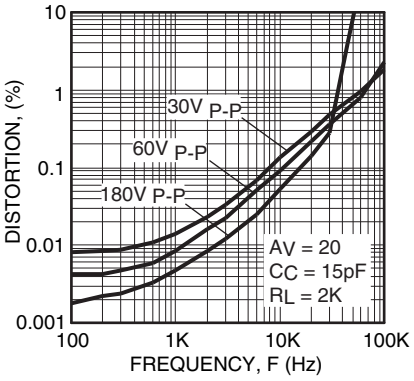
PHASE RESPONSE



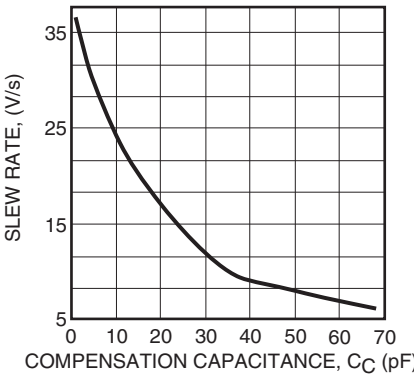
POWER RESPONSE



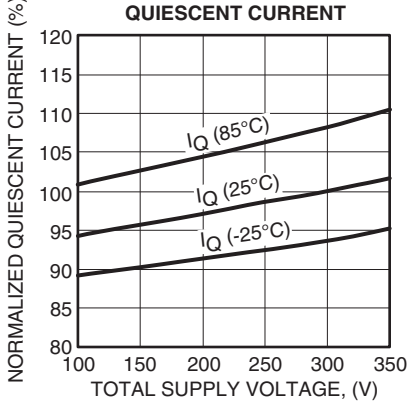
HARMONIC DISTORTION



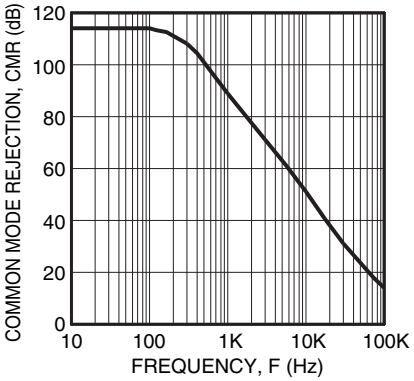
SLEW RATE



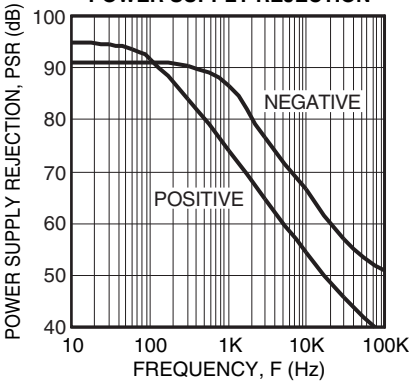
QUIESCENT CURRENT



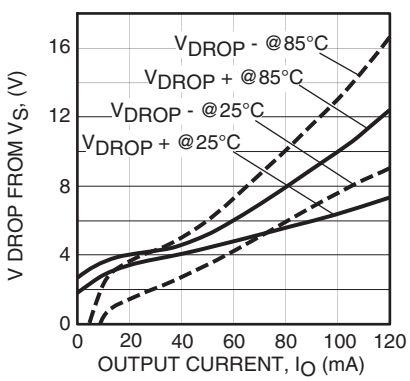
COMMON MODE REJECTION



POWER SUPPLY REJECTION



OUTPUT VOLTAGE SWING



GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, power supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexmicrotech.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit, heat sink selection, Apex's complete Application Notes library, Technical Seminar Workbook and Evaluation Kits.

PHASE COMPENSATION

Open loop gain and phase shift both increase with increasing temperature. The PHASE COMPENSATION typical graph shows closed loop gain and phase compensation capacitor value relationships for four case temperatures. The curves are based on achieving a phase margin of 50°. Calculate the highest case temperature for the application (maximum ambient temperature and highest internal power dissipation) before choosing the compensation. Keep in mind that when working with small values of compensation, parasitics may play a large role in performance of the finished circuit. The compensation capacitor must be rated for at least the total voltage applied to the amplifier and should be a temperature stable type such as NPO or COG.

OTHER STABILITY CONCERNS

There are two important concepts about closed loop gain when choosing compensation. They stem from the fact that while "gain" is the most commonly used term, β (the feedback factor) is really what counts when designing for stability.

1. Gain must be calculated as a non-inverting circuit (equal input and feedback resistors can provide a signal gain of -1, but for calculating offset errors, noise, and stability, this is a gain of 2).
2. Including a feedback capacitor changes the feedback factor or gain of the circuit. Consider Rin=4.7k, Rf=47k for a gain of 11. Compensation of 4.7 to 6.8pF would be reasonable. Adding 33pF parallel to the 47k rolls off the circuit at 103kHz, and at 2MHz has reduced gain from 11 to roughly 1.5 and the circuit is likely to oscillate.

As a general rule the DC summing junction impedance (parallel combination of the feedback resistor and all input resistors) should be limited to 5k ohms or less. The amplifier input capacitance of about 6pF, plus capacitance of connecting traces or wires and (if used) a socket will cause undesirable circuit performance and even oscillation if these resistances are too high. In circuits requiring high resistances, measure or estimate the total sum point capacitance, multiply by Rin/Rf, and parallel Rf with this value. Capacitors included for this purpose are usually in the single digit pF range. This technique results in equal feedback factor calculations for AC and DC cases. It does not produce a roll off, but merely keeps β constant over a wide frequency range. Paragraph 6 of Application Note 19 details suitable stability tests for the finished circuit.

CURRENT LIMIT

For proper operation, the current limit resistor, Rcl, must be connected as shown in the external connection diagram. The minimum value is 3.9 ohms, however for optimum reliability, the resistor should be set as high as possible. The maximum practical value is 110 ohms. Current limit values can be predicted as follows:

$$Ilimit = \frac{Vbe}{Rcl}$$

Where Vbe is shown in the CURRENT LIMIT typical graph.

Note that +Vbe should be used to predict current through the +Vs pin, -Vbe for current through the -Vs pin, and that they vary with case temperature. Value of the current limit resistor at a case temperature of 25° can be estimated as follows:

$$Rcl = \frac{0.7}{Ilimit}$$

When the amplifier is current limiting, there may be spurious oscillation present during the current limited portion of the negative half cycle. The frequency of the oscillation is not predictable and depends on the compensation, gain of the amplifier, value of the current limit resistor, and the load. The oscillation will cease as the amplifier comes out of current limit.

SAFE OPERATING AREA

The MOSFET output stage of the PA241 is not limited by second breakdown considerations as in bipolar output stages. However there are still three distinct limitations:

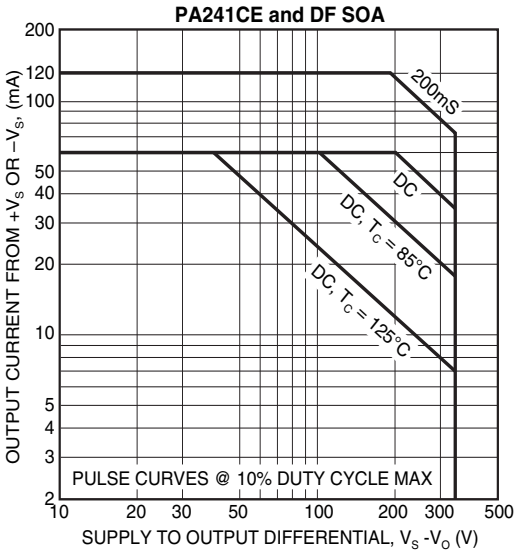
1. Voltage withstand capability of the transistors.
2. Current handling capability of the die metalization.
3. Temperature of the output MOSFETS.

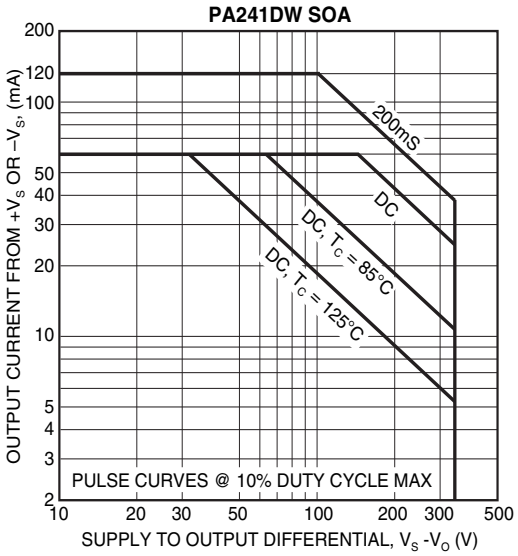
These limitations can be seen in the SOA (see Safe Operating Area graphs). Note that each pulse capability line shows a constant power level (unlike second breakdown limitations where power varies with voltage stress). These lines are shown for a case temperature of 25°C and correspond to thermal resistances of 5.2°C/W for the PA241CE and DF and 10.4°C/W for the PA241DW respectively. Pulse stress levels for other case temperatures can be calculated in the same manner as DC power levels at different temperatures. The output stage is protected against transient flyback by the parasitic diodes of the output stage MOSFET structure. However, for protection against sustained high energy flyback external fast-recovery diodes must be used.

HEATSINKING

The PA241DF package has a large exposed integrated copper heatslug to which the monolithic amplifier is directly attached. The solder connection of the heatslug to a minimum of 1 square inch foil area on the printed circuit board will result in thermal performance of 25°C/W junction to air rating of the PA241DF. Solder connection to an area of 1 to 2 square

inches is recommended. This may be adequate heatsinking but the large number of variables involved suggest temperature measurements be made on the top of the package. Do not allow the temperature to exceed 85°C.





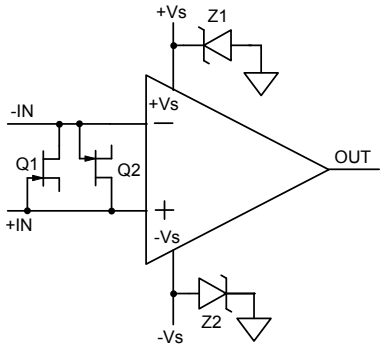


FIGURE 1

OVERVOLTAGE PROTECTION

Although the PA241 can withstand differential input voltages up to 16V, in some applications additional external protection may be needed. Differential inputs exceeding 16V will be clipped by the protection circuitry. However, if more than a few milliamps of current is available from the overload source, the protection circuitry could be destroyed. For differential sources above 16V, adding series resistance limiting input current to 1mA will prevent damage. Alternatively, 1N4148 signal diodes connected anti-parallel across the input pins is usually sufficient. In more demanding applications where bias current is important, diode connected JFETs such as 2N4416 will be required. See Q1 and Q2 in Figure 1. In either case the differential input voltage will be clamped to 0.7V. This is sufficient overdrive to produce the maximum power bandwidth.

In the case of inverting circuits where the +IN pin is grounded, the diodes mentioned above will also afford protection from excessive common mode voltage. In the case of non-inverting circuits, clamp diodes from each input to each supply will provide protection. Note that these diodes will have substantial reverse bias voltage under normal operation and diode leakage will produce errors.

Some applications will also need over-voltage protection devices connected to the power supply rails. Unidirectional zener diode transient suppressors are recommended. The zeners clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether the zeners are used or not the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversals as well as line regulation. See Z1 and Z2 in Figure 1.

APPLICATION REFERENCES:

For additional technical information please refer to the following Application Notes:
AN1: General Operating Considerations
AN3: Bridge Circuit Drives
AN25: Driving Capacitive Loads
AN38: Loop Stability with Reactive Loads

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