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XC1718 Serial Configuration PROM

Preliminary, August 1992 — Product and Programming Specification

Features

- One-Time Programmable (OTP) 18,144 x 1 bit serial memory designed to store configuration programs for Programmable Gate Arrays
- Simple interface to Logic Cell™ Array (LCA™) requires only one user I/O pin
- Low-power CMOS EPROM process
- Available in the space-efficient 8-pin plastic DIP and 20-terminal surface-mount PLCC package

Description

The XC1718 Serial Configuration PROM (SCP) provides an easy-to-use, cost-effective configuration memory for Xilinx FPGAs.

The XC1718 uses a simple serial-access procedure to configure one or more LCA devices. The XC1718 organization (18,144 x 1) supplies enough memory to configure one XC2064, XC2018 or XC3020.

The XC1718 is packaged in the economical 8-pin plastic DIP and the popular surface-mount 20-terminal Plastic Leaded Chip Carrier.

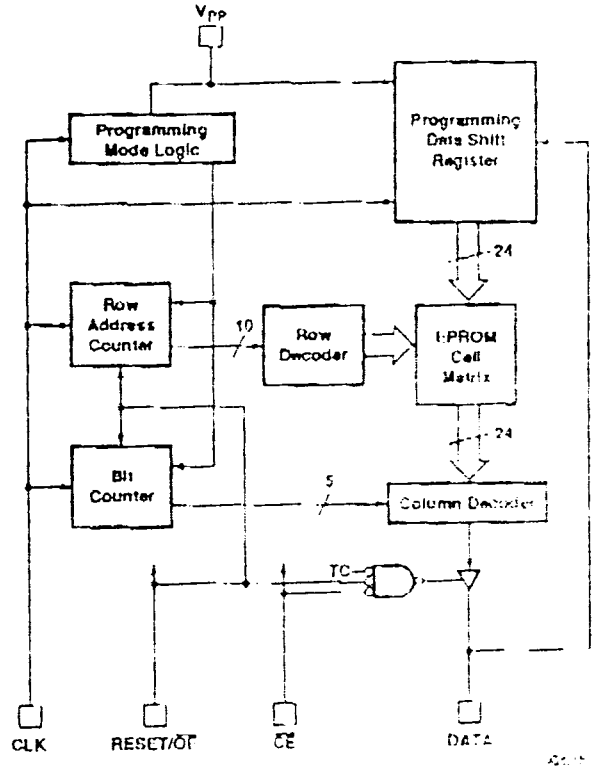
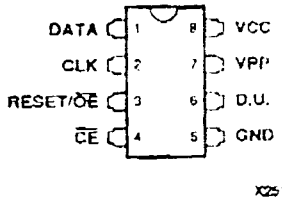
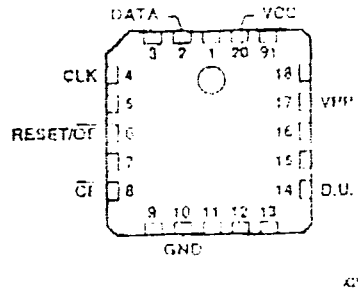


Figure 1. XC1718 Block Diagram



XC1718 8-Pin DIP Pin Assignments



XC1718 20-Pin PLCC Pin Assignments

Upon power-up or reconfiguration, an LCA device enters the Master Serial Mode whenever all three of the LCA mode-select pins are Low (M0=0, M1=0, M2=0). Data are read from the Serial Configuration PROM sequentially on a single data line. Synchronization is provided by the rising edge of the temporary signal CCLK, which is generated during configuration.

Master Serial Mode provides a simple configuration interface. Only a serial data line and two control lines are required to configure an LCA device. Data from the Serial Configuration PROM is read sequentially, accessed via the internal address and bit counters which are incremented on every valid rising edge of CCLK.

If the user-programmable, dual-function DIN pin on the LCA device is used only for configuration, it must still be held at a defined level during normal operation. The XC3000 and XC4000 families take care of this automatically with an on-chip default pull-up resistor. With XC2000 family devices, the user must either configure DIN as an active output, or provide a defined level, e.g., by using an external pull-up resistor, if DIN is configured as an input.

Standby Mode

The XC1718 enters a low-power standby mode whenever $\overline{CE}$ is asserted High. In this mode, the SCP consumes less than 0.5 mA of current. The output remains in a high-impedance state regardless of the state of the $\overline{OE}$ input.

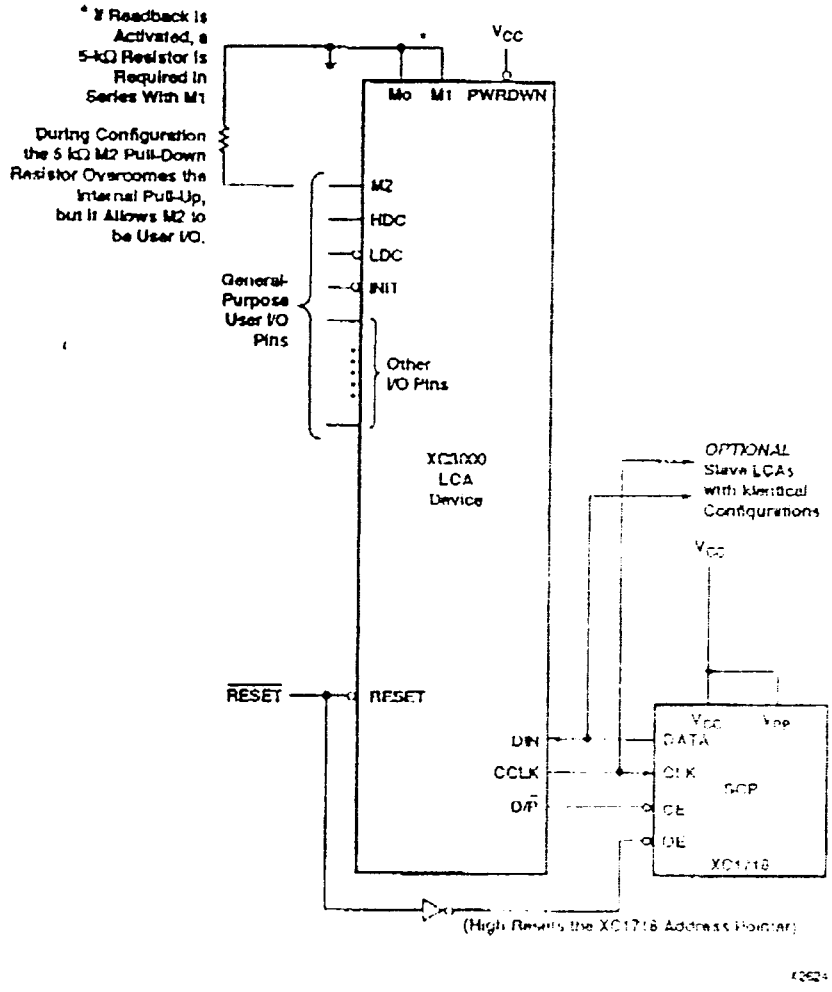


Figure 2. Master Serial Mode. The one-time-programmable XC1718 Serial Configuration PROM supports automatic loading of configuration programs up to 18K bits. An early O/P inhibits the PROM data output a CCLK cycle before the LCA I/Os become active.

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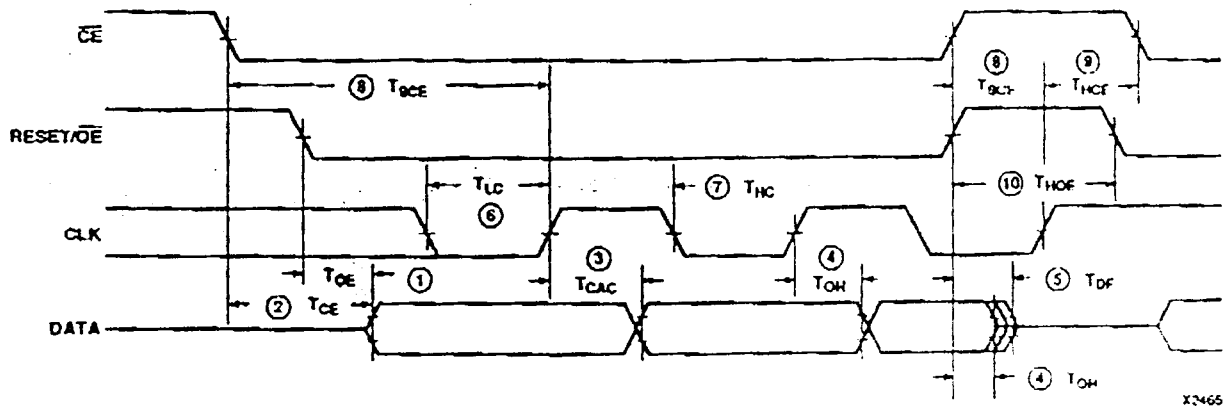
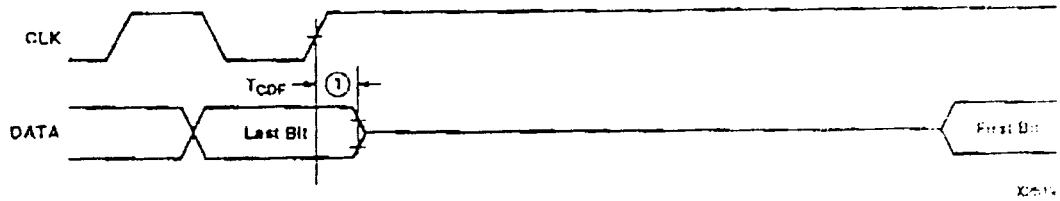
AC Characteristics Over Operating Conditions (V_{CC} = 5.0 V nominal)



Symbol		Description	Limits Min	Limits Max	Units
1	T_{OE}	$\overline{OE}$ to Data Delay		45	ns
2	T_{CE}	$\overline{CE}$ to Data Delay		60	ns
3	T_{CAC}	CLK to Data Delay		150	ns
4	T_{OH}	Data Hold From $\overline{CE}$, $\overline{OE}$, or CLK	0		ns
5	T_{DF}	$\overline{CE}$ or $\overline{OE}$ to Data Float Delay[2]		50	ns
6	T_{LC}	CLK Low Time[3]	100		ns
7	T_{HC}	CLK High Time	100		ns
8	T_{SCE}	$\overline{CE}$ Setup Time to CLK (to guarantee proper counting)	25		ns
9	T_{HCE}	$\overline{CE}$ Hold Time to CLK (to guarantee proper counting)[3]	0		ns
10	T_{HOE}	$\overline{OE}$ High Time (Guarantees Counters Are Reset)	100		ns

Notes: 1. AC test load = 50 pF
2. Float delays are measured with minimum tester ac load and maximum dc load
3. Guaranteed by design, not tested.



Symbol		Description	Min	Max	Units
1	T_{CDF}	CLK to Data Float Delay		50	ns

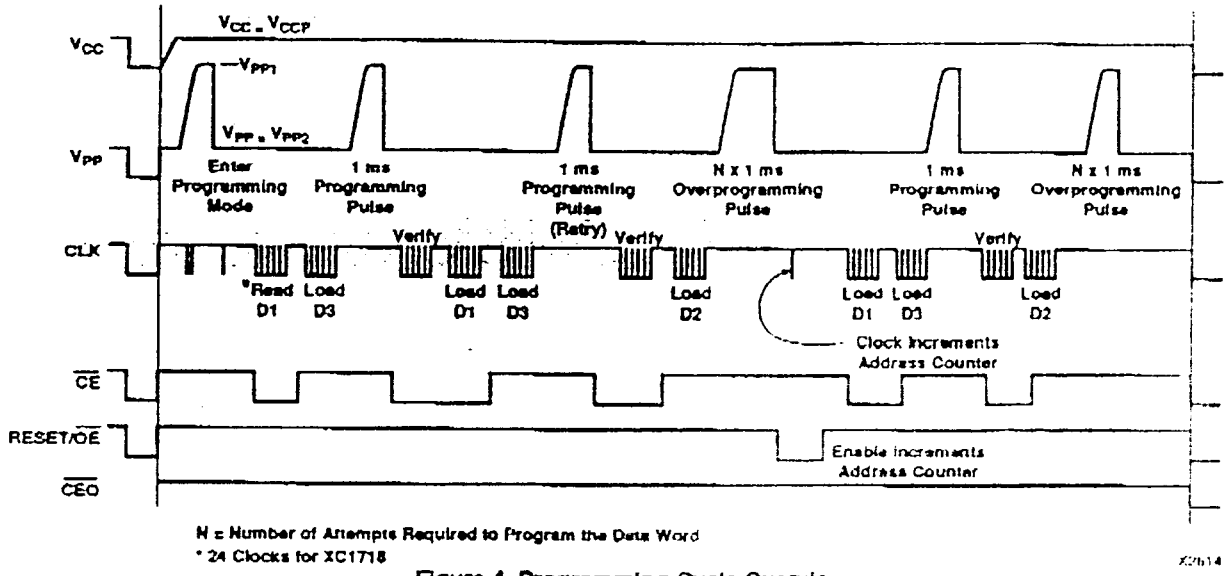


Figure 4. Programming Cycle Overview

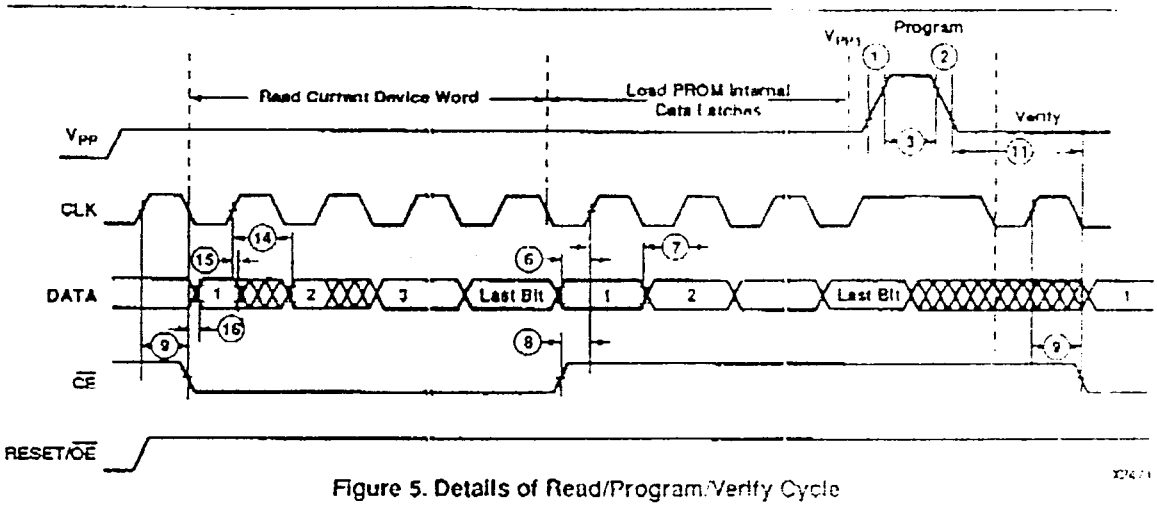


Figure 5. Details of Read/Program/Verify Cycle

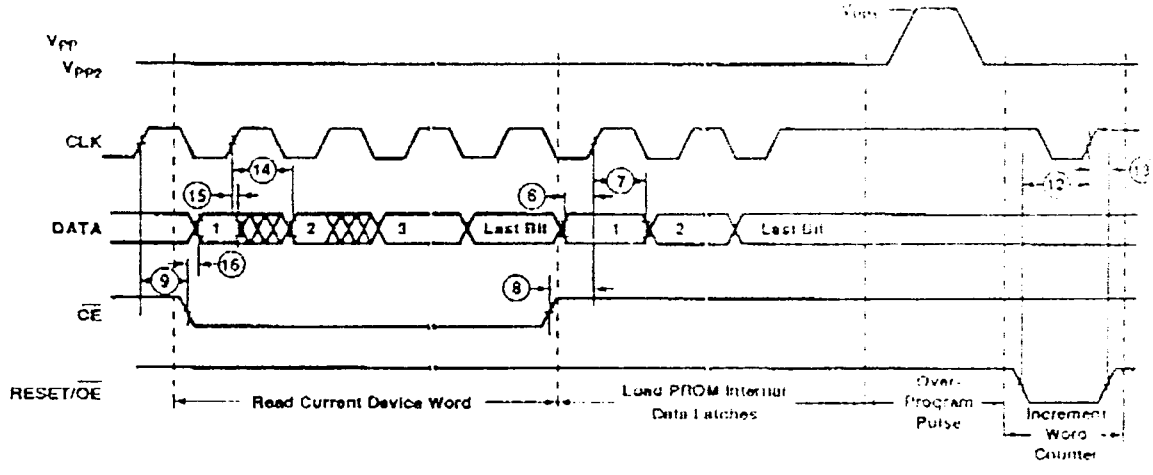


Figure 6. Overprogramming Detail

XC1718 Pin Assignments in the Programming Mode

DIP Pin	PLCC Pin	Name	I/O	Description
1	2	DATA	I/O	The rising edge of the clock shifts a data word in or out of the PROM one bit at a time.
2	4	CLK	I	Clock input. Used to increment the internal address/word counter for reading and programming.
3	6	RESET/ $\overline{OE}$	I	The rising edge of CLK shifts a data word into the PROM when $\overline{CE}$ and $\overline{OE}$ are High; it shifts a data word out of the PROM when $\overline{CE}$ is Low and $\overline{OE}$ is High. The address/word counter is incremented on the rising edge of CLK while $\overline{CE}$ is held High and $\overline{OE}$ is held Low
4	8	$\overline{CE}$	I	The rising edge of CLK shifts a data word into the PROM when $\overline{CE}$ and $\overline{OE}$ are High; it shifts a data word out of the PROM when $\overline{CE}$ is Low and $\overline{OE}$ is High. The address/word counter is incremented on the rising edge of CLK while $\overline{CE}$ is held High and $\overline{OE}$ is held Low.
5	10	GND		Ground pin.
6	14	D.U.		Don't Use. This pin is used for manufacturer test. During programming and normal operation, it is pulled High by internal logic.
7	17	V_{PP}		Programming Voltage Supply. Programming mode is entered by holding $\overline{CE}$ and $\overline{OE}$ High and V_{PP} at V_{PP1} for two rising clock edges and then lowering V_{PP} to V_{PP2} for one more rising clock edge. A word is programmed by strobing the device with V_{PP} for the duration T_{PGM}. V_{PP} must be tied to V_{CC} for normal operation.
8	20	V_{CC}		+5 V power supply input.

DC Programming Specifications

Symbol	Description	Min	Rec	Max	Units
V_{CCP}	Supply voltage during programming	5.25	5.5	5.75	V
V_{IL}	Low-level input voltage	0.0	0.0	0.4	V
V_{IH}	High-level input voltage	2.4	V_{CC}	V_{CC}	V
V_{OL}	Low-level output voltage			0.4	V
V_{OH}	High-level output voltage	3.7			V
V_{PP1}	Programming voltage*	14.5	15.0	15.5	V
V_{PP2}	Programming-mode access voltage	5.75	6.0	6.25	V
I_{PPP}	Supply current in programming mode			60	mA
I_L	Input or output leakage current	-10		10	µA
V_{CCL}	First pass verify supply voltage	4.4	4.5	4.5	V
V_{CCH}	Second pass verify supply voltage	5.5	5.5	5.6	V

*No overshoot is permitted on this signal. V_{PP} must not be allowed to exceed V_{CC} max.

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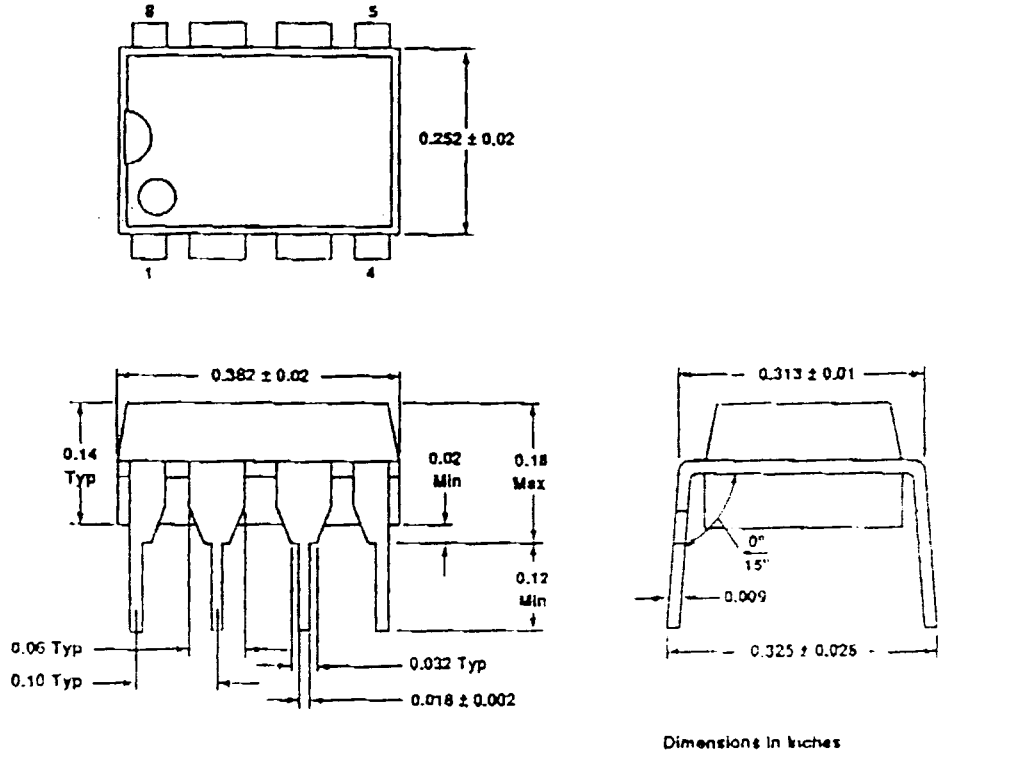
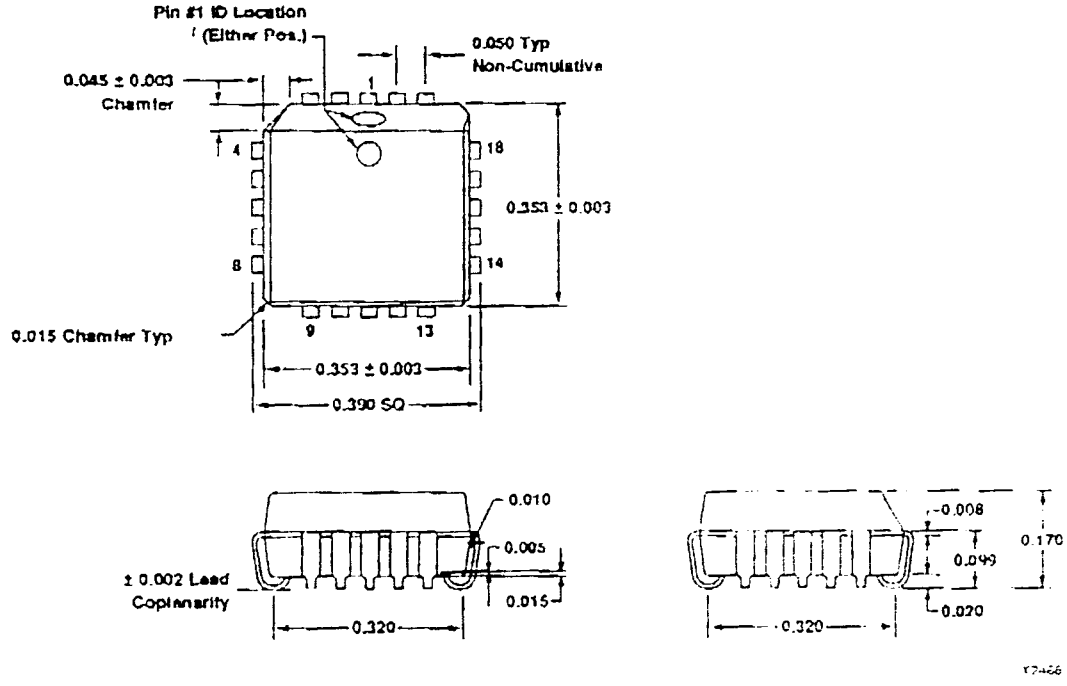
Physical Dimensions



8-Pin Plastic DIP (PD8)



20-Pin PLCC (PC20)